Ph.D.Dissertation

Design of Wide-Range Clock and Data Recovery with Multi-Phase Oversampling Frequency Detection

다중 위상 오버샘플링 주파수 검출 방식을 이용한 광대역 클럭 및 데이터 복원회로 설계

by

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August, 2019

Department of Electrical and Computer Engineering
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Design of Wide-Range Clock and Data Recovery with Multi-Phase Oversampling Frequency Detection

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Abstract

In this thesis, design techniques of a wide-range clock and data recovery (CDR) without a reference clock are proposed. For the referenceless operation, a frequency acquisition scheme using multi-phase oversampling is utilized. The analysis of the representative performances such as capture range and frequency acquisition time is provided and demonstrated by the measurement results. Furthermore, to achieve an unlimited frequency detection capability, an advanced referenceless CDR with a digital implementation is proposed.

At first, a single-loop referenceless CDR with a compact frequency acquisition scheme is presented. A bang-bang phase-frequency detector (BBPFD) is proposed that tracks the frequency difference by detecting the drift direction of the NRZ bit stream with respect to the multi-phase clock and generates UP/DN output signals accordingly. The UP/DN output signals from the BBPFD are connected directly to the loop filter, thereby reducing the acquisition time without any loss of cycles. When frequency lock is reached, the BBPFD is degenerated into the conventional bang-bang phase detector (BBPD). The effect of sampling phase mismatch is analyzed and the capture range is calculated. In addition, the frequency acquisition time is analytically derived and verified by simulation. The proposed CDR has been implemented in a 65 nm CMOS process and occupies an active area of 0.047 mm^2. The measured capture range is 6.7-to-11.2 Gb/s and the frequency acquisition time is less than 2.19 μs. The proposed CDR achieves error-free operation (BER < 10^{-12}) for PRBS31 pattern and consumes 22.5 mW at 10 Gb/s.

Advanced from the previous version, a referenceless digital CDR with an unlimited frequency detection capability is proposed. Based on the detailed capture-range analysis of the multi-phase oversampling scheme, a frequency detector with additional logic gates is proposed and its frequency detection curve shows an unlimited capability. Unlike the prior works, the proposed CDR achieves frequency acquisition regardless of the initial condition and its capture range is determined only by the operating range of the oscillator. The CDR fabricated in 65 nm CMOS consumes 37.3 mW at 20 Gb/s and occupies an active area of 0.045 mm^2. The measured capture range is from 4 Gb/s to 20 Gb/s and the worst-case acquisition time is 25 μs with a PRBS31 pattern.

Keywords : Acquisition time, bang-bang phase detector (BBPD), bang-bang phase-frequency detector (BBPFD), clock and data recovery (CDR), frequency acquisition, low power, multi-phase oversampling, phase-locked loop (PLL), referenceless, single loop, unlimited frequency detection.

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Chapter 1

Introduction

1.1 Motivation

In wireline communication systems, a clock and data recovery (CDR) plays a key role, such as recovering clock and retiming the incoming data. In general, the CDRs have a dual loop architecture for frequency locking and phase locking. Depending on whether frequency locking is achieved by using an external reference clock, the CDRs can be classified as a referenced CDR and a referenceless CDR. As shown in Figure 1.1, the wireline receiver without the reference clock does not utilize a phase-locked loop (PLL), but recovers the clock only through the input data stream. Although the referenceless CDR has a limited capture range and introduces several design issues, it is widely adopted in the wireline communications [1] - [41]. The main reason is the reduced cost of not using the external reference clock. Repeaters and

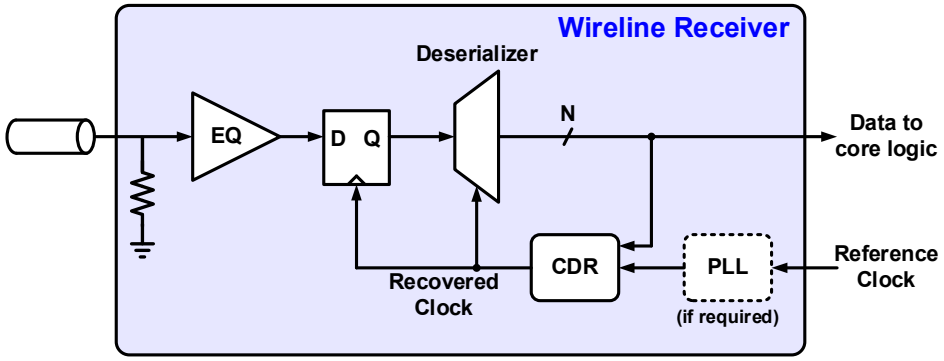


Fig. 1.1 Block diagram of wireline receiver.

active cables are representative examples since generating or distributing the reference clock is costly. It is much complicated to implement a low-noise, adjustable reference clock in such applications [1]. Furthermore, the CDR performance can be degraded due to the inaccuracy of the external reference clock frequency and the undesired coupling through the package.

To overcome the limited capture range and the design issues of the referenceless CDR, many works proposed frequency acquisition schemes for the referenceless operation. However, most of the previously proposed schemes have a trade-off between capture range, acquisition time, and power consumption. The detailed architectures and schemes of the referenceless CDRs will be discussed in Chapter 2.2.

To achieve a better trade-off, this thesis presents a single-loop referenceless CDR with a multi-phase oversampling bang-bang phase-frequency detector (BBPFD) [41]. The BBPFD using a direct UP/DN control not only improves the capture range but also reduces the acquisition time and prevents cycle slips which degrade the CDR performance [42]. Multi-phase sampling approaches were employed in prior works

[21] - [23]. However, the additional phases are used only for detecting frequency lock in [21] while the phase detector is vulnerable to long run length and thereby limits the loop bandwidth in [22], [23]. In this work, based on theoretical analyses, the frequency acquisition scheme using multi-phase oversampling is fully utilized and demonstrated in the prototype chip.

However, the first version still offer a limited capture range and the limitation is mainly determined by the capability of the frequency acquisition scheme. Also, the capture range depends on a specific initial frequency of the oscillator and it decides the upper and lower limits of the data rate. Furthermore, since the referenceless CDR is implemented by analog circuits, it is hard to implement additional functions such as a lock detector. Therefore, advanced from the first version, this thesis proposes a digital referenceless CDR with an unlimited frequency detection capability. As a result, the proposed CDR obtains frequency acquisition at any initial condition and its capture range is determined only by the operating range of the oscillator.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, backgrounds of the referenceless CDR are explained. The basic operation and building blocks of the general CDR are provided. And, the necessity and conventional architecture of the referenceless CDR are introduced. To show the motivation of this work, the comparison and limitation of the previously proposed frequency acquisition schemes are presented.

In Chapter 3, a single-loop referenceless CDR using a multi-phase oversampling phase-frequency detector (PFD) is presented. The proposed frequency acquisition scheme tracks the frequency difference by detecting the drift direction of the input data with respect to the multi-phase clock. The effect of sampling phase mismatch is analyzed and the capture range is calculated. Also, the frequency acquisition time is analytically derived and verified by the simulation results. Then, the circuit implementation is explained and the measurement results are shown.

In chapter 4, a digital referenceless CDR with an unlimited frequency detection capability is presented. Extended from the multi-phase oversampling scheme, additional logic gates for the unlimited capability are utilized and the simulated frequency detection curve demonstrates the capability. Then, the circuit implementation is explained and the measurement results are shown.

Chapter 5 summarizes the proposed works and concludes this thesis.

Chapter 2

Backgrounds

2.1 Clocking in Serial Link

Serial link is an interface where data is serialized for high-speed transmission. As shown in Figure 2.1, parallel data is serialized in the transmitter side and the serial data gets transferred to the receiver side through a channel. Then, the received data is deserialized for a parallel processing. These are known as SerDes components. The channel and interconnects could consist of cables, a printed circuit board (PCB), connectors, vias, and backplanes.

Recently, most of the wireline communication systems have adopted the serial links instead of the parallel links because of the less pin counts, increased through-put, and less issues of skew and crosstalk. The examples adopting the serial link are Ethernet, Fibre Channel, SONET, PCI Express, Serial ATA, and so forth [47]. Since

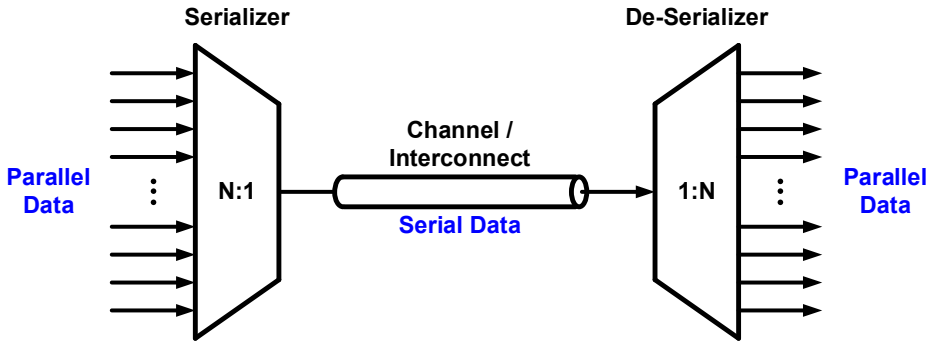


Fig. 2.1 Simplified architecture of serial link.

the required amount of data is exploding, the transfer rate of the serial link keeps increasing. Actually, most interface standards double the speeds with the next generation. For example, PCI Express Gen 3.0 which runs at 8 Gb/s, is moving to version 4.0 of the specification which run at 16 Gb/s [48]. As a result, the timing margin keeps decreasing and the design issues of timing circuits have been increased. To explore the timing circuits, we should review the clocking architectures of the serial link.

The design of timing circuits in the receiver side is different as the relationship between the received data and the sampling clock. Depending on the existence of the frequency difference and the phase relationship between the data and clock, the data-clock synchronization can be categorized by four levels such as synchronous, mesochronous, plesiochronous, and asynchronous [49]. These clocking architectures are closely related to the system performance such as a bit error rate (BER), a jitter tolerance, and amount of jitter. Thus, a proper clocking architecture should be selected for each application based on the required specification.

Figure 2.2 shows the example of the synchronous system. In the synchronous clocking, there is no frequency difference between the sampling clocks in the transmitter and the receiver. At the same time, the data is transmitted with a clock and the delays of two channels are matched. Therefore, there is no frequency difference or phase difference between the received data and the sampling clock in the receiver. These well matched frequency and phase guarantee a higher timing margin in the receiver compared to other clocking architectures resulting in a low BER. Though the synchronous clocking architecture is the best way to construct the serial link, it is almost impossible to implement the synchronous system in the real world because there are lots of uncertainties to interrupt the delay matching. While the timing margin for a safe sampling decreases as the data rate increases, the off-chip interconnection delays such as package, connectors, and PCB traces remains same. Therefore, the effect of the uncertainties keeps increasing as the operating speed increases.

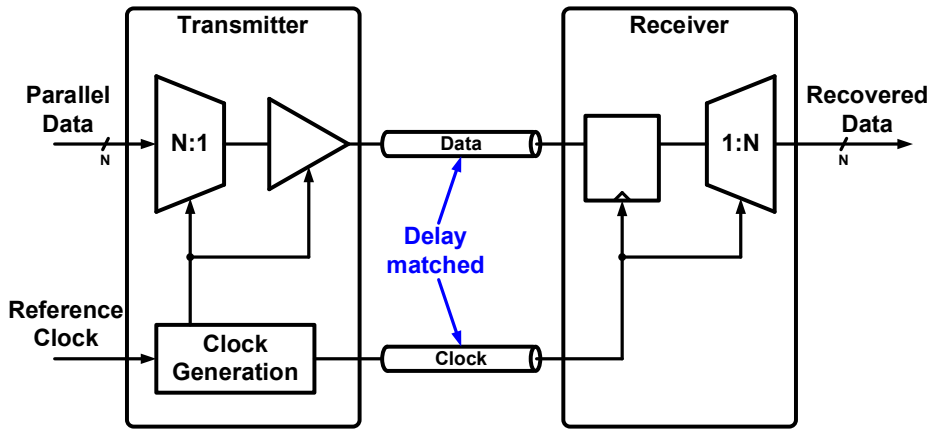


Fig. 2.2 Synchronous clocking architecture.

Figure 2.3 shows the example of the mesochronous clocking architecture [50]. While the clock frequency of the receiver is same as the transmitter clock in this clocking system, the data at the receiver is potentially out of phase with the clock. Therefore, in the receiver side, a clock recovery circuit is required to remove the timing skew between the data and the clock. Since the frequency offset does not exist, a simple de-skewing circuit such as a delay-locked loop (DLL) and a phase rotator can recover the clock. Most of the display interconnect adopts the mesochronous clocking because the receiver design is simpler than the plesiochronous clocking and asynchronous clock. However, the mesochronous clocking architecture requires an additional clock channel which is a big cost in several applications.

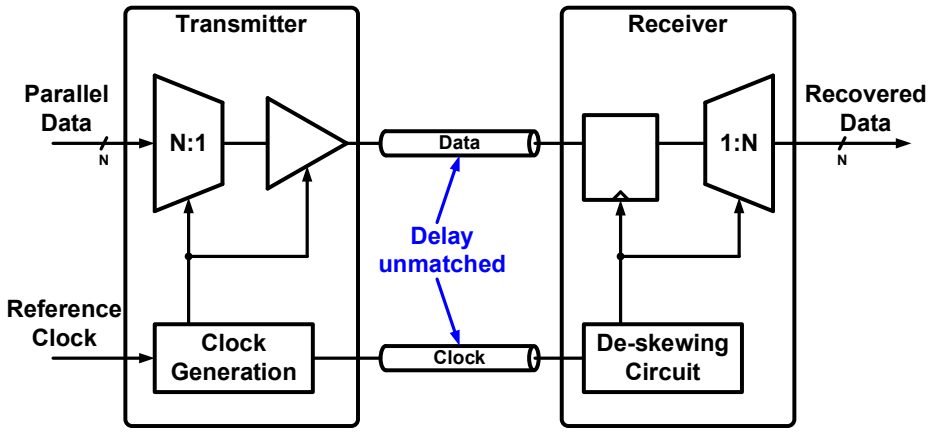


Fig. 2.3 Mesochronous clocking architecture.

Plesiochronous clocking architecture does not have a clock channel as shown in Figure 2.4. Instead of the clock forwarding, the receiver also has a reference clock for generating the sampling clock. Since the reference clocks in the transmitter and the receiver cannot be perfectly synchronized, a frequency difference between the

received data and the sampling clock of the receiver is caused. Due to the frequency offset, the phase relationship of the data and the clock rotates with the beat frequency. Therefore, the plesiochronous clocking architecture commonly requires a clock recovery circuit which includes both frequency detection logics and phase detection logics. So, compared with the previous architectures, the design of the receiver in the plesiochronous clocking is quite complicated. The clock recovery circuits are usually based on a PLL, a DLL, and an injection-locked oscillator (ILO). The most common example of the plesiochronous clocking architecture is optical interconnects such as SONET and SDH. In such applications, the distance between two systems is too long to use an additional clock channel, and thus the plesiochronous clocking is suitable.

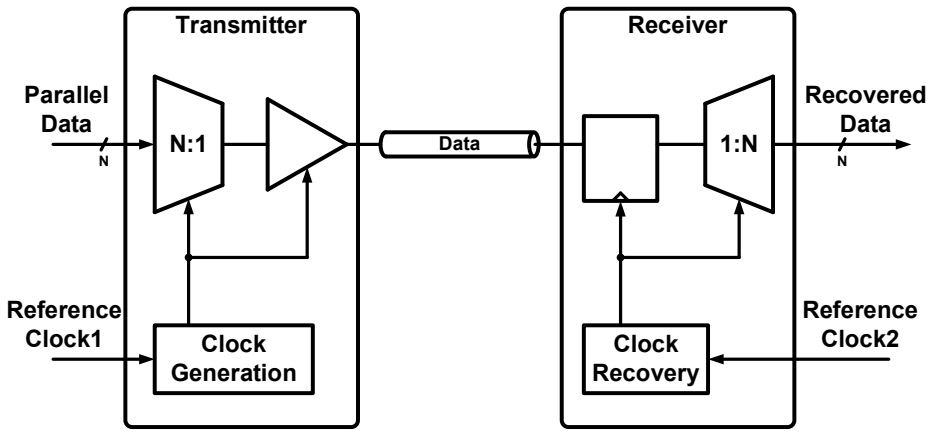


Fig. 2.4 Plesiochronous clocking architecture.

Figure 2.5 shows the example of the asynchronous clocking architecture. In the architecture, the transmitter clock and the receiver clock have no correlation. Therefore, a digital buffer such as an elastic buffer is used to eliminate the data loss. The

buffer solves the clock boundary problem with two pointers for the input and the output. If a greater frequency error exists between the transmitter and the receiver, a larger size of buffer is required to prevent a data overflow. Moreover, the data rate is limited by the low-speed digital buffer. Consequently, the asynchronous clocking is generally used in low-speed applications.

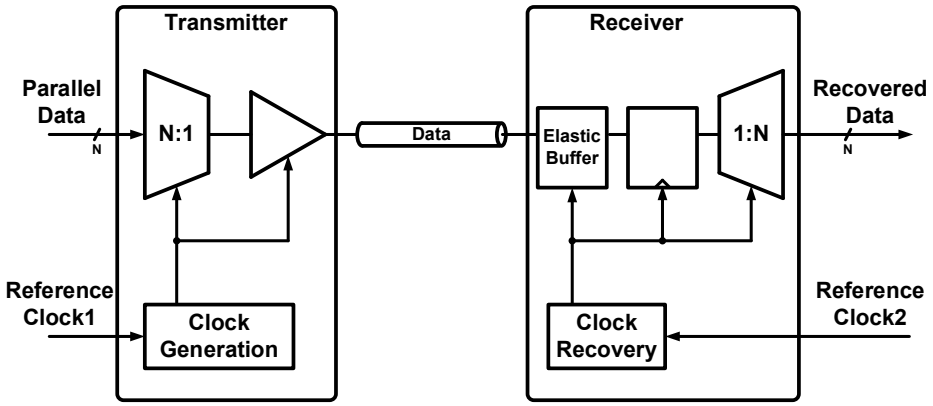


Fig. 2.5 Asynchronous clocking architecture.

2.2 Clock and Data Recovery

2.1.1 General Considerations

Clock and data recovery (CDR) is a critical block in high-speed transceivers serving in many applications such as backplane routing, optical communications, and chip-to-chip interconnects. The purpose of using CDR circuits in the receiver side is to perform synchronous operations such as retiming and demultiplexing on random data. As explained in Chapter 2.1, only the synchronous clocking architecture has a synchronized relationship between the received data and the sampling clock. However, in other architectures, the received data is not synchronize to the sampling clock. As the system speed increases, the synchronization is hard to achieve without the retiming circuits. Also, during the transmission, several noise sources degrades the signal-to-noise ratio (SNR) severely. Therefore, the CDR should recover a synchronized clock and retime the received data by the recovered clock.

Figure 2.6 shows the conceptual block diagram of the CDR circuit which is composed of a clock recovery circuit and a retimer to generate the recovered clock and the recovered data, respectively [51]. From the noisy received NRZ data stream, the clock recovery circuit recovers a periodic clock waveform. The retimer then receives this clock along with the received data, thus recovering the data. Due to several noise sources, the zero crossings of the received data are corrupted as shown in Figure 2.7. Therefore, the CDR circuit should aligns the rising edges of the recov-

ered clock to the optimum sampling points which secures the maximum SNR. The optimum sampling point is generally the middle of the data eye.

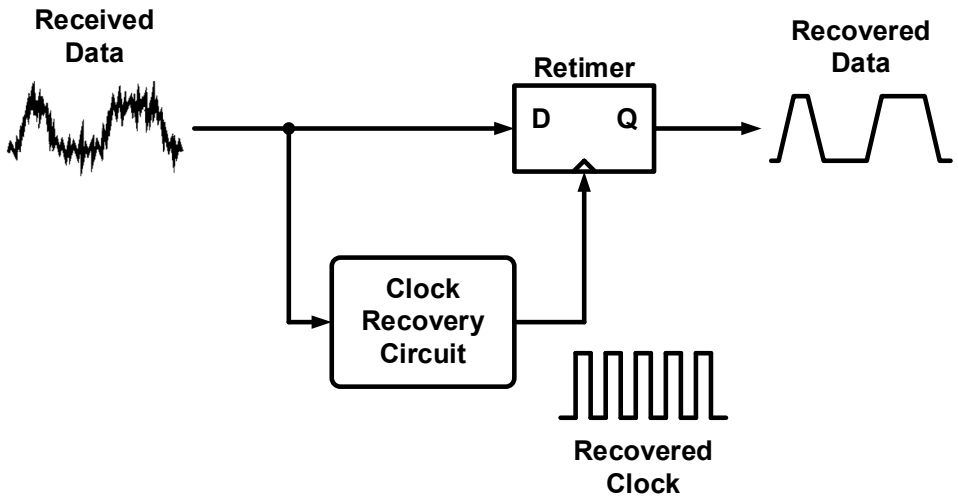


Fig. 2.6 Block diagram of conventional BBPD.

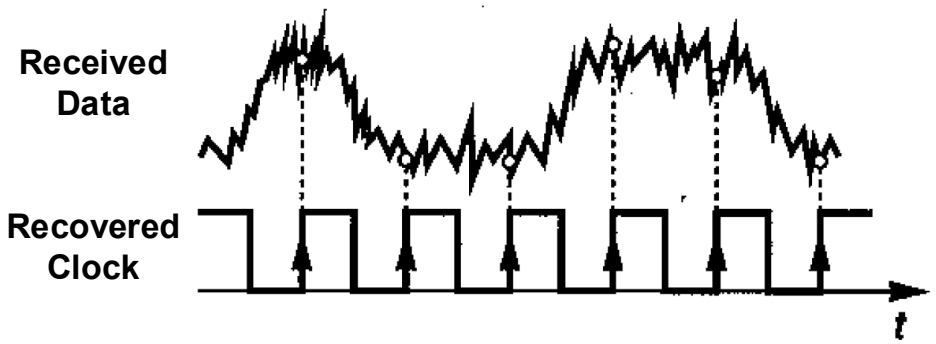


Fig. 2.7 Optimum sampling point of noisy received data.

2.1.2 CDR Architectures

CDR architectures can be classified by the existence of a feedback control. It is related to the phase relationship between the received data and the sampling clock explained in Chapter 2.1. Commonly used CDR topologies can be divided into three major categories: phase tracking CDR, open-loop CDR, and blind oversampling CDR [52]. The first category, the phase tracking CDR, can be implemented based on a PLL, a DLL, a phase interpolator (PI), and an ILO. In this chapter, we will discuss some types of CDRs included in the major categories.

2.1.2.1 PLL-based CDR

PLL-based CDRs can be classified according to the existence of a reference clock. The CDR without reference clock is handled in Chapter 2.2, so we will see the PLL-based CDR with a reference clock which conventional block diagram is shown in Figure 2.8 [53]. In the CDR architecture, the frequency tracking loop and the phase tracking loop drive the coarse control and fine control, respectively. Dual voltage-controlled oscillators (VCOs) are used for the two tracking loops. The frequency tracking loop with the PFD locks the phase and frequency of VCO2 output to that of the input reference clock. Utilizing the divider in the frequency tracking loop allows the reference clock to operate at a low frequency. Since VCO1 and VCO2 are identical, the control voltage of the frequency tracking loop can be used in the coarse control of the phase tracking loop. Then, the phase tracking loop with a phase detector (PD) locks the phase of VCO1 output to that of the input data through

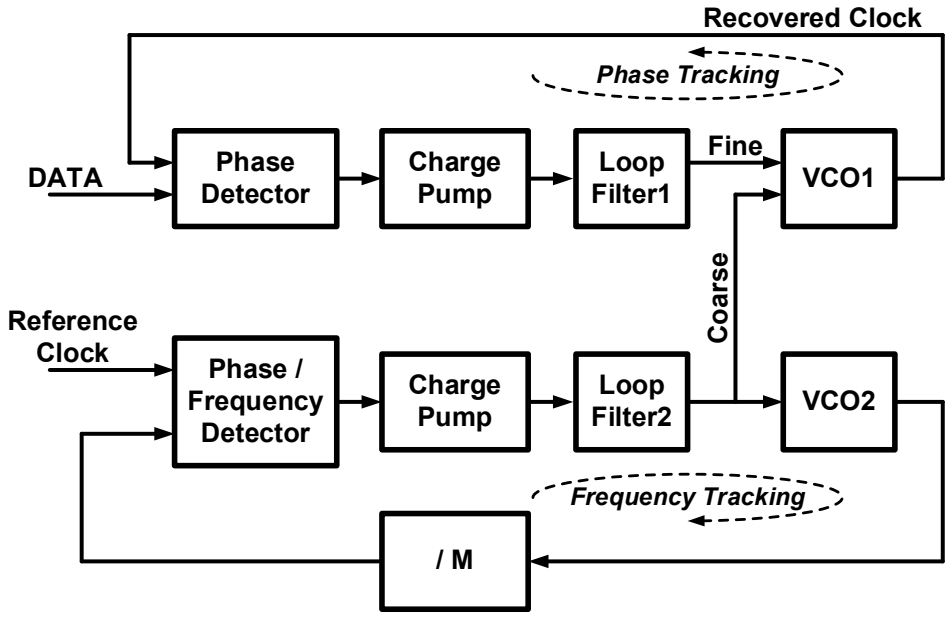


Fig. 2.8 PLL-based CDR architecture with dual VCO.

the fine control. The bandwidth of the phase tracking loop should be lower than that of the frequency tracking loop. There are several issues associated with the conventional PLL-based CDR architecture. First, although the control voltage is shared, a mismatch between the two VCOs causes a difference in the oscillator frequencies. Since the frequency of the sampling clock depends on that of the reference clock, a difference between the data rate and clock frequency can exist in this architecture. The mismatches degrade the CDR performance. In addition, the excessive area overhead is needed for the two VCO designs. The area issue becomes bigger if a LC oscillator is used to generate the clock.

Figure 2.9 shows one of the PLL-based CDR architecture reducing the area issue. This architecture utilizes a lock detector (LD) to sequentially enable the frequency

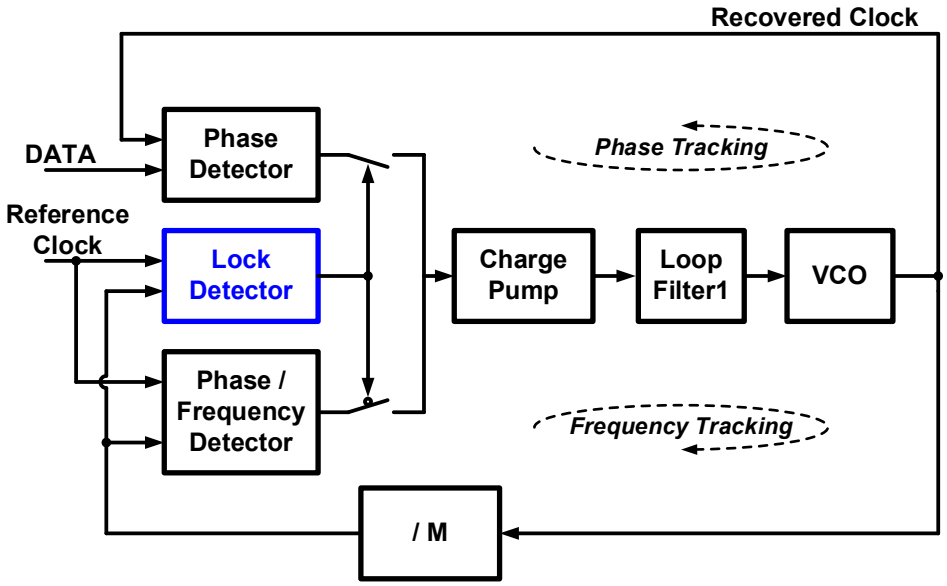


Fig. 2.9 PLL-based CDR architecture with lock detector.

tracking loop and the phase tracking loop. When the frequency lock is reached, the lock detection signal disables the path of the PFD but enables the path of the PD. If loss of phase locking occurs due to an unexpected noise, the LD re-activates the frequency tracking loop. However, this architecture has a problem of the mode transition. The transition may disturb the VCO control signal and cause a shift of the VCO frequency. It results in a failure of the phase locking.

2.1.2.2 ADPLL-based CDR

Unlike the PLL-based CDR using an analog loop filter in Figure 2.8 and Figure 2.9, an all-digital PLL (ADPLL)-based CDR with a digital loop filter (DLF) is

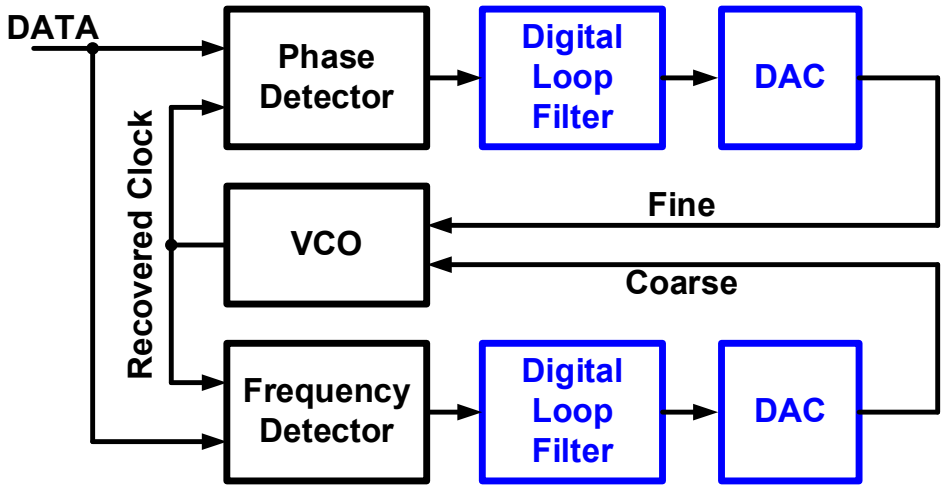


Fig. 2.10 ADPLL-based CDR architecture.

shown in Figure 2.10 [54], [55]. The ADPLL-based CDR includes digital-to-analog converters (DACs) in both the frequency and phase tracking loops. The DLF has several advantages compared with the analog loop filter. Using the digital logic rather than the analog components can minimize the required layout area and simplify the closed-loop stability analysis thanks to the reduced process, voltage and temperature (PVT) variations. Also, the analog loop filter has a large leakage in the deep submicron process. Another significant advantage of using the DLF is an easy programmability of the loop filter characteristics. However, the digital control has drawbacks. A long latency in the DLF and DAC can degrade the phase and frequency tracking capability. Also, the finite resolution of the DAC causes wondering of the VCO frequency leading to an increased jitter.

2.1.2.3 DLL-based CDR

An example of the DLL-based CDR architecture is shown in Figure 2.11 [56] - [58]. It looks similar with the PLL-based CDR shown in Figure 2.8. However, in this architecture, the frequency tracking loop provides a reference clock rather than a control voltage signal. Therefore, in a multi-channel system, the frequency tracking loop can be shared. As a result, the DLL-based CDR avoids the drawbacks of multi-VCO coupling, high power consumption, and large area. In addition, other advantage of using DLL is the stability of the system. The voltage-controlled delay line (VCDL) directly control the clock phase, so it does not introduce a pole in the loop transfer function. Also, the DLL-based CDR does not have a jitter accumulation issue of the PLL-based CDR.

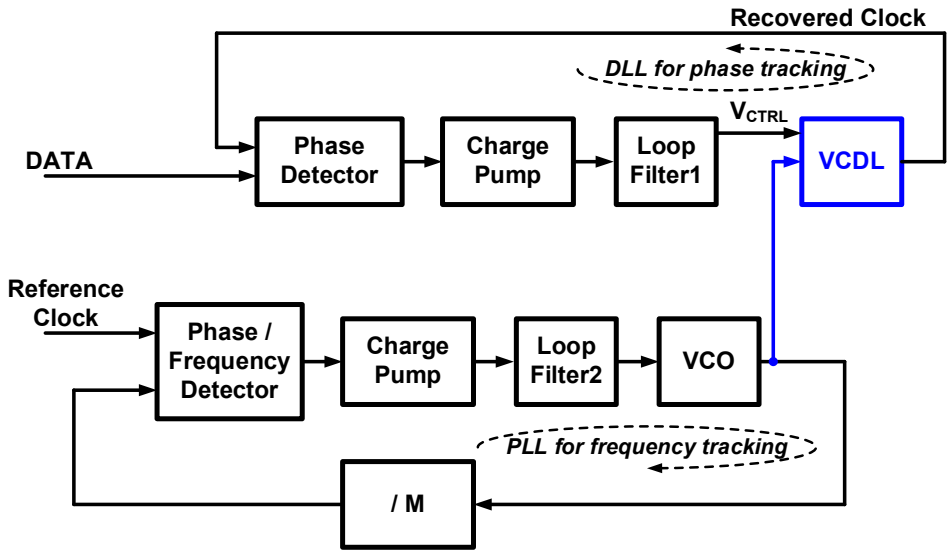


Fig. 2.11 DLL-based CDR architecture.

However, the primary drawback of the DLL-based CDR is a limited phase capturing range. For that reason, the CDR cannot track a frequency offset between the transmitter and the receiver and it is hard to achieve wide operating frequency range. In addition, due to the limited range, there are several locking issues such as a stuck locking and a harmonic locking [58].

2.1.2.4 Open-loop CDR

Figure 2.12 shows a simple open-loop CDR which uses an edge detector and a high-Q bandpass filter [59] - [62]. The edge detector operate as a pulse generator based on the received data transitions. The high-Q bandpass filter extracts the transition frequency, and thus it recovers a clock at the received data rate. The open-loop CDR is a very old technique of designing CDR and has several issues. Since it needs a high-Q filter, a monolithic integration is difficult. Also, a variable delay unit is necessary for the maximum sampling margin and it is typically PVT variant.

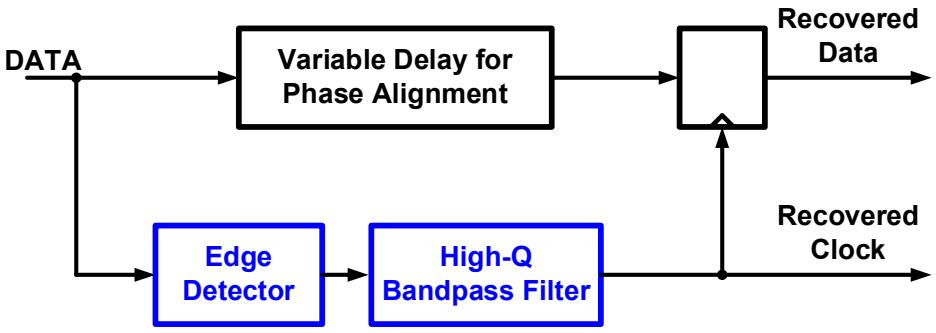


Fig. 2.12 Open-loop CDR architecture.

2.1.2.5 Blind Oversampling CDR

Figure 2.13 shows a blind oversampling CDR which is a feed-forward architecture [63], [64]. Unlike the phase tracking CDR, it has no feedback circuits and thus provides data recovery without any time delay. Other different point is that the oversampling-based CDR samples each received data bit at multiple points. A minimum of 3 samples per one bit are required for recovering the received data. So, a large data register is needed to store the sampled data. Then, by detecting the bit boundaries, a data selector recovers the received data. The primary advantages are fast acquisition and inherent stability. However, the drawbacks of the oversampling-based CDR are the need for high frequency data transitions and a large data register.

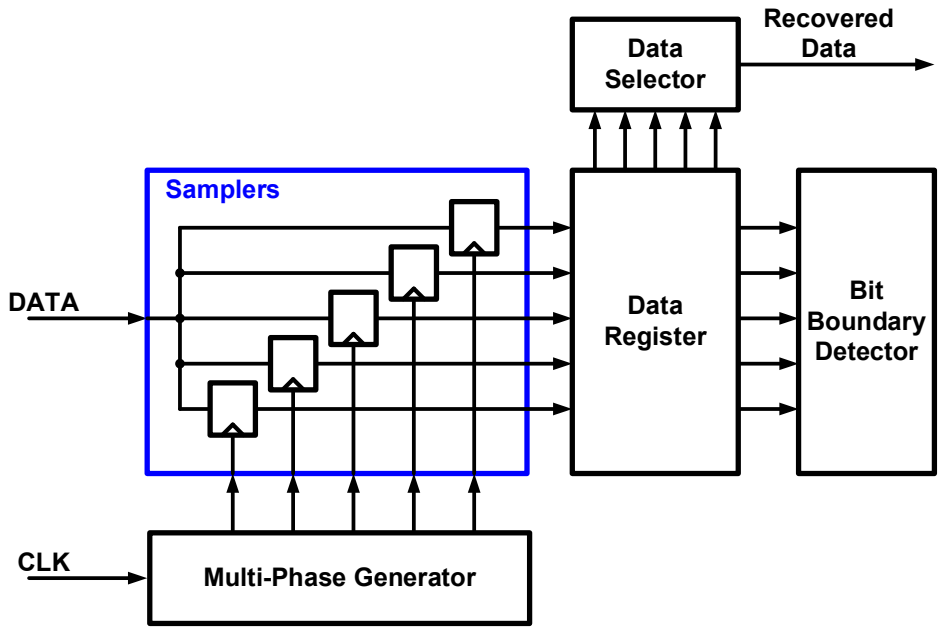


Fig. 2.13 Blind oversampling CDR architecture.

2.1.3 Types of Phase Detector

As shown in Chapter 2.1.2, the common components of the phase tracking CDR are a PD and an oscillator. Among the components, we will describe several types of the PD in this chapter. In the CDR architecture, the PD is a building block to measure the phase difference between the input data and the VCO clock. PDs can be categorized into a linear PD and a binary PD.

2.1.3.1 Linear Phase Detector

The linear PD generates the output voltage that is proportional to the amount of the phase error. Therefore, its transfer curve shows a constant slope as shown in Figure 2.14. The linearized gain curve makes that the CDR loop can be designed conveniently with constant loop parameters. Moreover, since the linear PD does not generate output when the phase error is close to zero, it can achieve relatively small jitter.

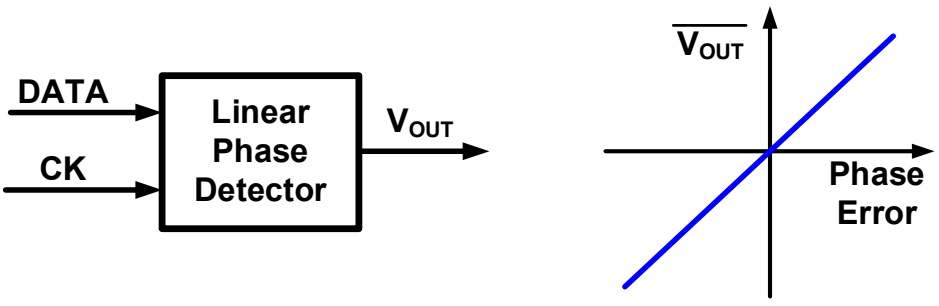


Fig. 2.14 Gain curve of linear PD.

A commonly-used linear PD is the Hogge PD as shown in Figure 2.15. [65]. The PD consists of two d-flip-flops and two XOR gates. First, the input data is sampled at the rising edge of the clock and the output is sampled at the falling edge of the clock. Then, the two sampled data and the input data are compared by the XOR gates generating an ERR signal and a REF signal. The REF signal is a reference pulse which has a constant pulse width. On the other hand, the pulse width of the ERR signal is proportional to the phase error. Therefore, when the clock is lagging (leading) the input data, the pulse width of the ERR signal is larger (smaller) than that of the REF signal. Using it, the phase detection can be achieved.

The drawback of the Hogge PD is that the input data should be amplified to drive the XOR gate. So, it requires a power-hungry block such as a limiting amplifier. Furthermore, it is hard to amplify the random data in a high-speed operation, so the Hogge PD is not suitable for the high-speed applications.

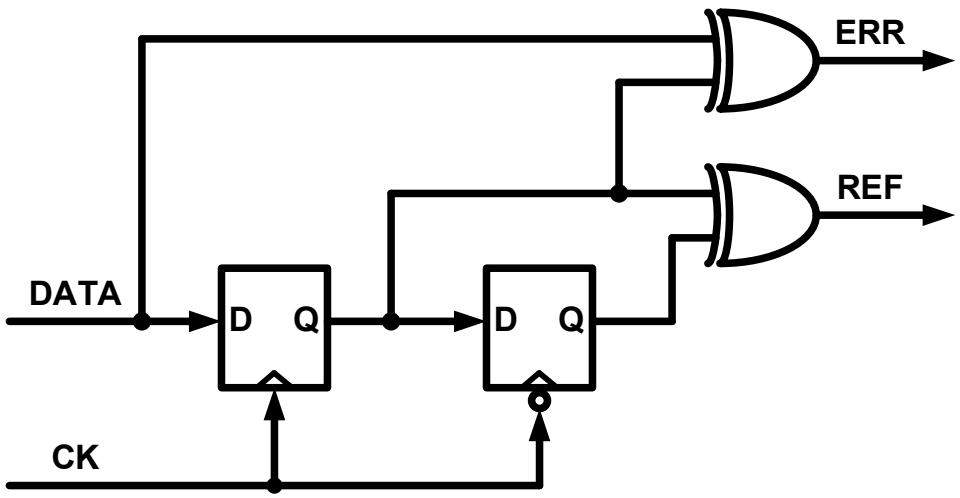


Fig. 2.15 Hogge phase detector.

2.1.3.2 Binary Phase Detector

Unlike the linear PD, the binary PD only indicates the polarity of the phase error. Thus, the gain curve of the binary PD has discontinuity at origin as shown in Figure 2.16. Since the PD basically adopts a sampling method without an analog amplifier, it can be implemented simply and enables high-speed operation. Also, its output inherently has a digital waveform which make it possible to design the system as a digitally-controlled architecture.

A typical binary PD is the Alexander PD as shown in Figure 2.17 [66]. Similar to the Hogge PD, the Alexander PD consists of four d-flip-flops and two XOR gates. First, the data is sampled twice at the rising edge and the falling edge of the sampling clock. That is, it uses 2x oversampling which uses two samples per 1-bit data. Then, the outputs are sampled by the rising edge of the clock for comparing the value of the samples at the same timing. The XOR gates find out where the transition exists between S1, S2, and S3 signals. Finally, the output of the Alexander PD de-

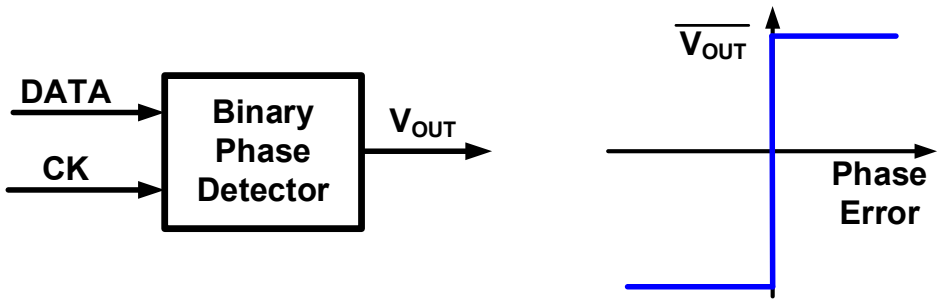


Fig. 2.16 Gain curve of binary PD.

tects the polarity of the phase error. The timing diagrams shown in Figure 2.18 shows the operation of the Alexander PD in two cases, clock lagging data and clock leading data.

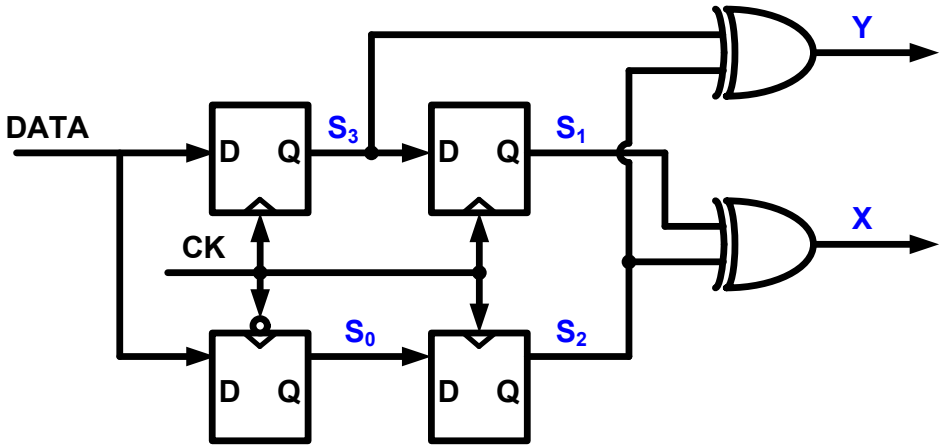
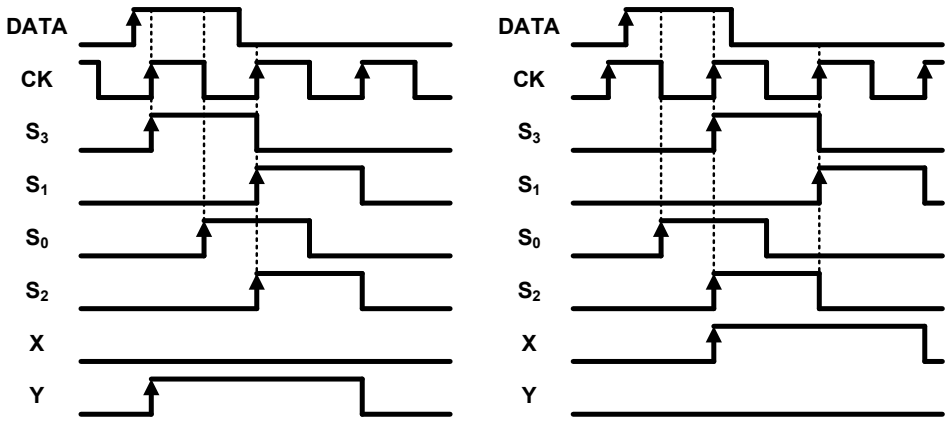


Fig. 2.17 Alexander phase detector.



(a) (b)

Fig. 2.18 Timing diagrams showing operation of Alexander PD.

2.2 Referenceless CDR

2.2.1 Overview

Figure 2.19(a) shows the PLL-based CDR architecture without a reference clock referred to as a referenceless PLL-based CDR. Unlike the CDR architecture shown

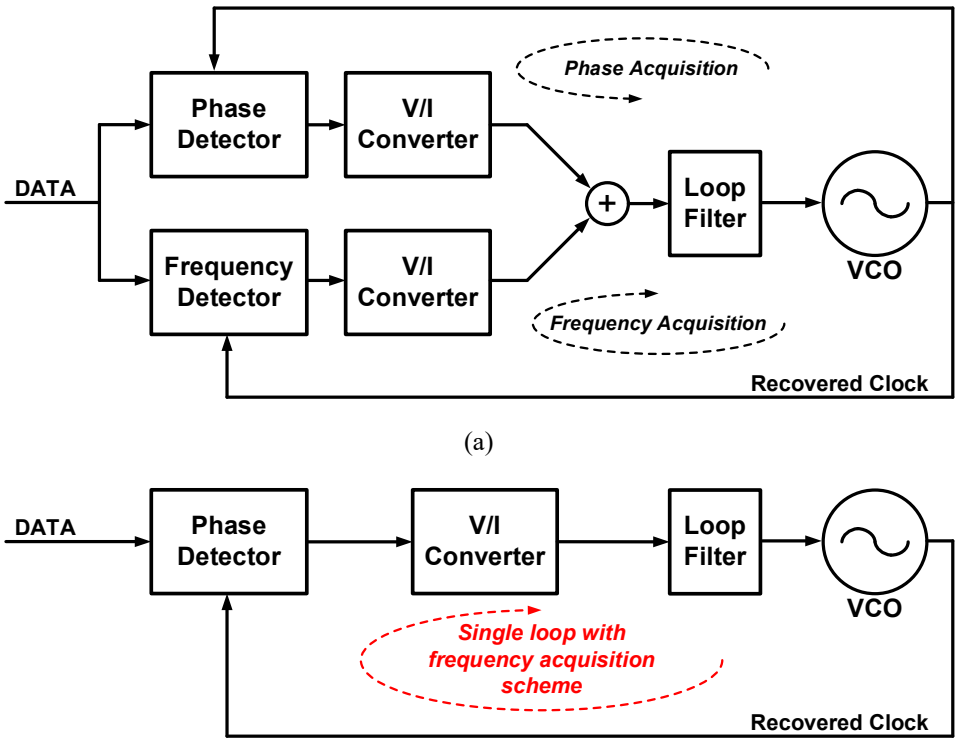


Fig. 2.19 Block diagram of (a) dual-loop referenceless CDR and (b) single-loop referenceless CDR.

in Figure 2.8, the frequency tracking loop provides a frequency comparison through a frequency detector (FD) which extracts the frequency information from the NRZ data stream. That is, the referenceless CDR does not rely on the reference clock, but it automatically adjusts the recovered clock frequency to the incoming data rate.

To achieve the frequency acquisition, a technique of extracting the frequency information from the input data is needed. The typical solution is a dual-loop architecture with a separate FD as shown in Figure 2.19(a) [1] - [11]. During either CDR startup or loss of phase lock, the FD is activated to produce a control voltage through the charge pump and the loop filter leading to move the VCO oscillation frequency toward the data rate. Once the frequency difference falls within the capture range of the phase tracking loop, the PD takes over and adjusts the clock phase to the data phase. The rotational FD and the Pottbacker FD are the most popular choice for the dual-loop referenceless CDR [43]. Detail operation of the FDs is provided in Chapter 2.2.2.

However, most of the separate FDs are sensitive to input jitters and the dual-loop architecture suffers from the increased hardware complexity and the inherent loop interference. Therefore, as shown in Figure 2.19(b), the design of the referenceless CDR with a single loop has been widely explored in recent works [12] - [20]. It has an advantage of simplicity in comparison to the dual-loop architecture. The main works proposed in this thesis also implement single-loop referenceless CDRs.

Besides the aforementioned structural aspects, a frequency acquisition scheme is the most challenge in the referenceless CDR. Several frequency acquisition schemes for the referenceless operation are introduced in Chapter 2.2.3.

2.2.2 Typical Frequency Detector

2.2.2.1 Pottbaker Frequency Detector

Figure 2.20 shows the circuit diagram of the Pottbaker FD proposed in 1992 [43]. The FD consists of two double-edged triggered flip-flops and a normal flip-flop. The NRZ data stream samples two-phase clock, an in-phase clock and a quadrature-phase clock. Then, the output of sampling Q2 by Q1 is the frequency detection signal indicating whether the clock frequency is higher or lower than the data rate.

The timing diagrams describing the operation principle of the Pottbaker FD is shown in Figure 2.21. First, when the clock frequency is higher than the data rate, the rising edge of Q1 is earlier than that of Q2. Therefore, the FD output keeps low. On the other hand, in the case of the lower clock frequency, opposite situation happens leading to the occurrence of the FD output as shown in Figure 2.21(b).

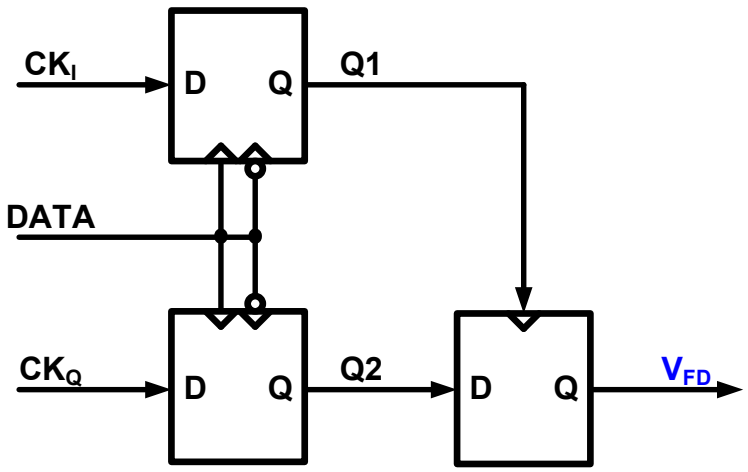


Fig. 2.20 Circuit diagram of Pottbaker FD.

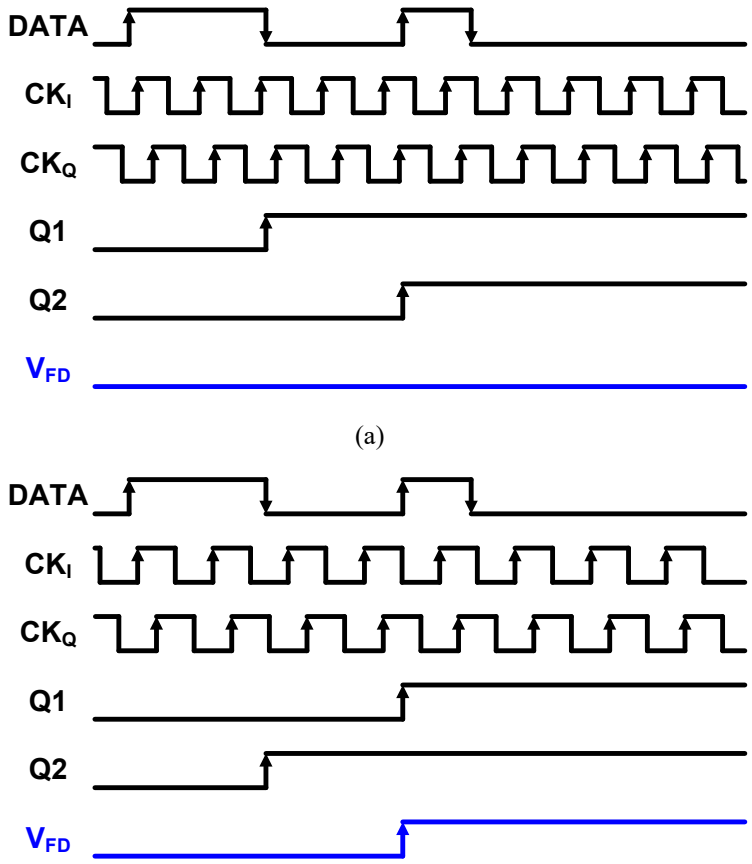
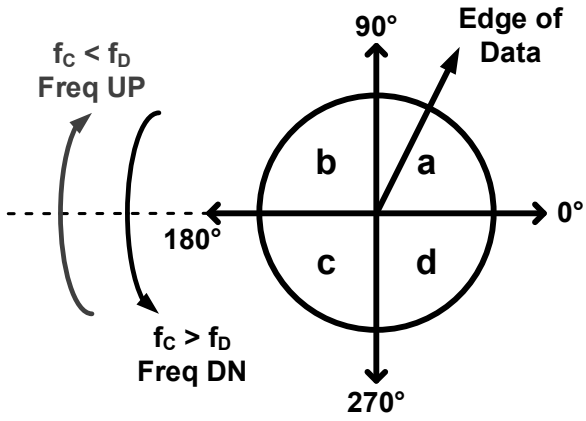


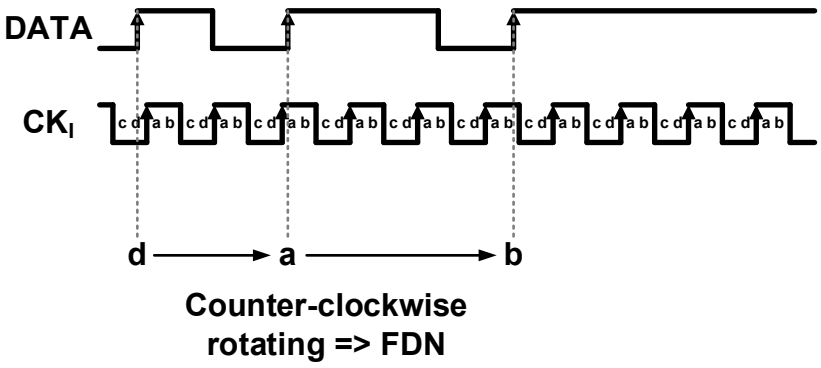
Fig. 2.21 Timing diagrams showing operation principle of Pottbaker FD when clock frequency is (a) higher and (b) lower than data rate.

2.2.2.2 Rotational Frequency Detector

Figure 2.22(a) shows the operation principle of a rotational FD proposed in [67]. The rotational FD detects the rotating direction of the data edge in the phasor dia-



(a)



(b)

Fig. 2.22 (a) Operation principle of rotational FD and (b) timing diagram example when clock frequency is higher than data rate.

gram. When the clock frequency is higher (lower) than the data rate, the edge of data rotates clockwise (counter-clockwise). Actually, in the timing diagram example shown in Figure 2.22(b), the data edge rotates counter-clockwise, and thus the clock frequency should be decreased.

The circuit diagram of the rotational FD is shown in Figure 2.23. Similar to the Pottbaker FD, the rotational FD also uses the quadrature-phase clock. However, it has two outputs, frequency UP signal (FUP) and frequency DN signal (FDN). Figure 2.24 shows the timing diagrams showing the operation of the rotational FD in two cases. As we explained, when the clock frequency is higher (lower) than the data rate, FDN (FUP) signal is generated, so the frequency detection is achieved.

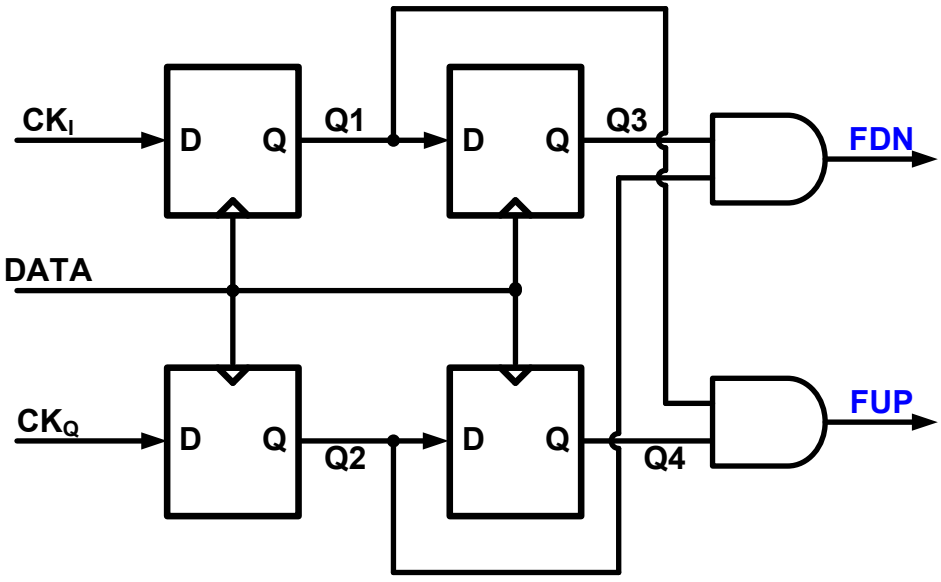
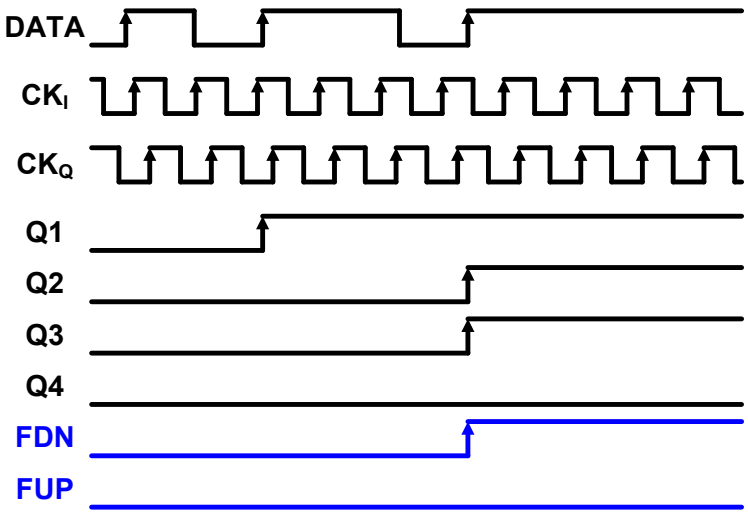
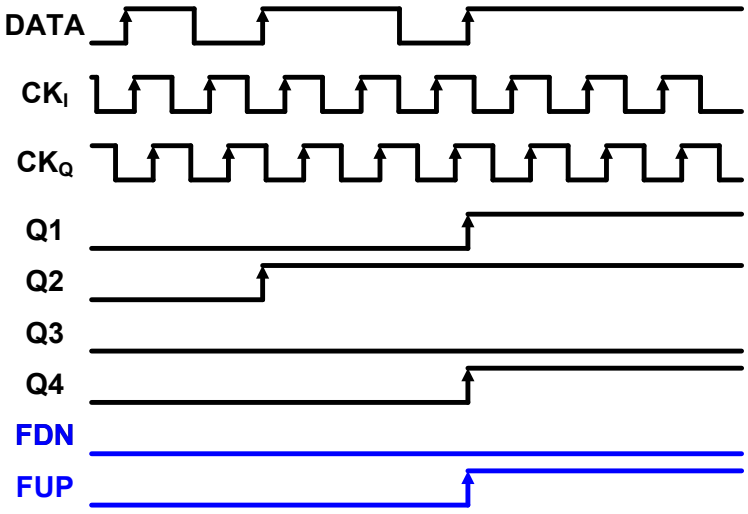


Fig. 2.23 Circuit diagram of rotational FD.



(a)



(b)

Fig. 2.24 Timing diagrams showing operation principle of rotational FD when clock frequency is (a) higher and (b) lower than data rate.

2.2.3 Frequency Acquisition Techniques

Frequency acquisition scheme is the most important challenge in the referenceless CDR. Most of the previously proposed schemes have a trade-off between capture range, acquisition time, and power consumption. In [12] and [13], referenceless digital CDRs are realized with a wide frequency acquisition range. However, in the frequency acquisition, they uses a clock pattern rather than a random data. That is, they rely on a training pattern which can only be applied in a few specific applications. In [5], the stochastic sub-harmonic frequency extraction is proposed as shown in Figure 2.25. Using a chain of frequency dividers, the proposed FD produces a known sub-harmonic tone from the incoming random data. A digital frequency-locked loop uses the extracted tone and drives the oscillator to any sub-rate of the input data frequency. Although the proposed CDR achieves the wide capture range, the scheme relies on the data transition density and it operates at low frequency which leads to a long frequency acquisition time.

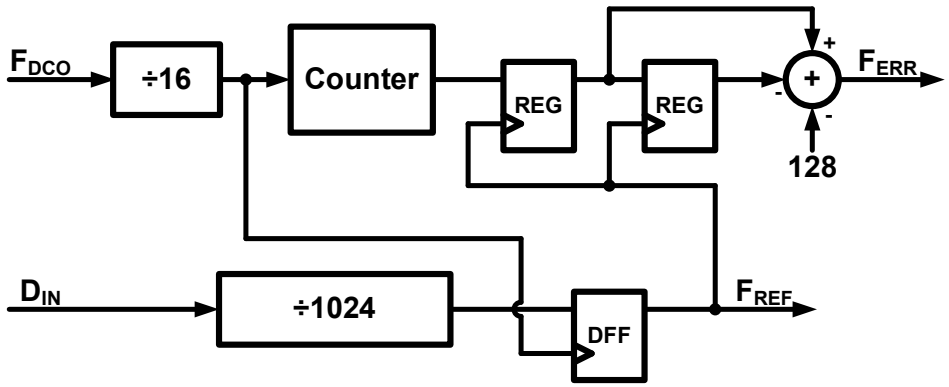


Fig. 2.25 Block diagram of FD proposed in [5].

Another approach presented in [9] counts the number of consecutive late or early signals from BBPD outputs to detect the frequency difference. It is immune to the input data transition density, but it also takes a long time to achieve frequency acquisition. In comparison to the counter-based scheme, fast acquisition is achieved in [14] and [15]. As shown in Figure 2.26 proposed in [14], the incoming data samples the high-speed clock. That means, the frequency acquisition schemes are sensitive to the intersymbol interference (ISI) of the input data, which becomes critical in the high-speed system. In [16], a phase-reset scheme is proposed which periodically resets the phase of the clock to limit the phase error. It is also sensitive to the data ISI and it requires a complicated delay calibration circuits which consume high power.

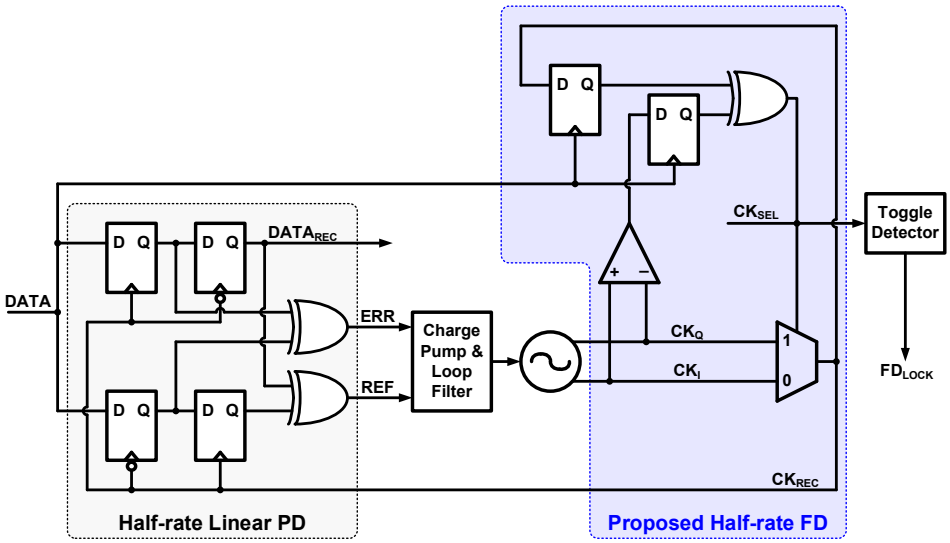


Fig. 2.26 Block diagram of FD proposed in [14].

Other recent approaches achieve the frequency acquisition by changing the characteristics of the PD. In [17], a non-zero strobe point is introduced in a linear PD as shown in Figure 2.27. Adding a flip-flop, a XOR gate, and buffers to the conventional linear PD, a strobe point detector is implemented. The strobe point detector controls the strobe voltage (V_{SP}) to tracks the frequency difference. It causes an offset in the PD transfer curve, and thus the PD has a frequency detection capability. Although the scheme leads to a wide capture range with a small hardware overhead, the frequency tracking is slow. Figure 2.28 shows the frequency acquisition scheme proposed in [18]. A phase roller which swaps the output of the BBPD depending on the phase difference window changes the characteristics of the BBPD to unilateral phase detection for capturing clock frequency. As a result, as shown in Figure 2.29, the PD gain curve demonstrates the unilateral phase detection. In the conventional

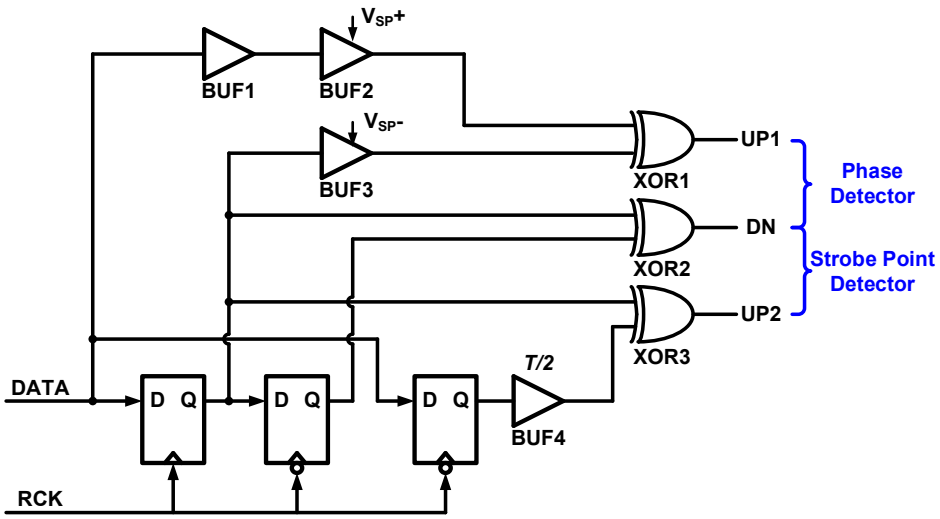


Fig. 2.27 Block diagram of linear phase detector combined with strobe point detector proposed in [17].

BBPD, the output polarity of the gray regions are opposite. However, delay buffers for the input data and a full-rate operation lead to high-power consumption.

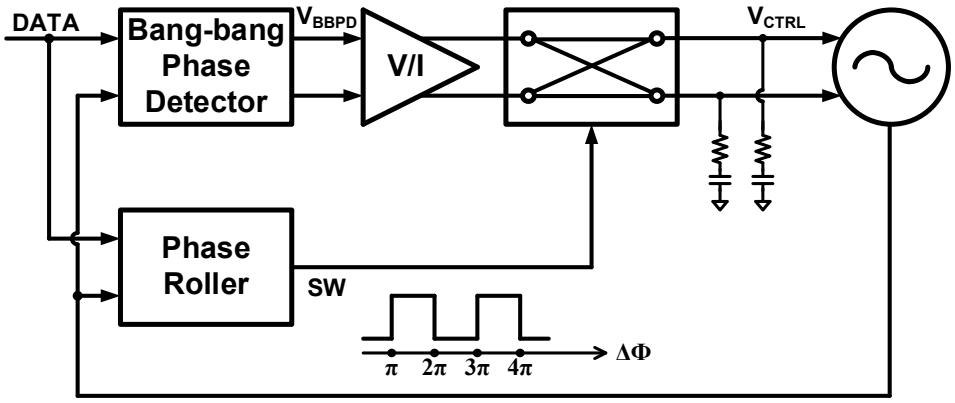


Fig. 2.28 Block diagram of BB-CDR with unilateral phase detection proposed in [18].

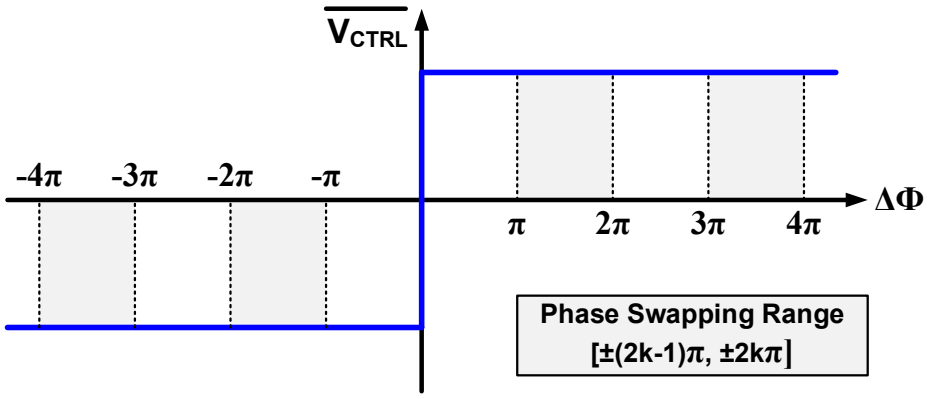


Fig. 2.29 PD gain curve proposed in [18].

Chapter 3

Referenceless CDR with Multi-Phase Oversampling PFD

3.1 Overview

Depending on whether the frequency locking is achieved by using an external reference clock, CDR circuits can be classified as a referenced CDR and a referenceless CDR. Although the referenceless CDR has a limited capture range and introduces several design issues, it is widely adopted in the wireline communications because of the reduced cost of not using the external reference clock. Repeaters and active cables are representative examples since generating or distributing the reference clock is costly. The referenceless CDR does not rely on the reference clock, but it automatically adjusts the recovered clock frequency to the incoming data rate.

Therefore, the referenceless CDR requires a technique of extracting the frequency information from the input data. As previously discussed, most of the previously proposed frequency acquisition schemes have a tradeoff between capture range, frequency acquisition time, and power consumption. To achieve a better tradeoff, we propose a single-loop referenceless CDR with a multi-phase oversampling bang-bang phase-frequency detector (BBPFD) which is based on the operation of the BBPD [41]. The BBPFD using a direct UP/DN control not only improves the capture range but also reduces the frequency acquisition time and prevents cycle slips which degrade the CDR performance [42]. Multi-phase sampling approaches were employed in the previous works [21] - [23]. However, in [21], the additional phases are used only for detecting frequency lock, which loses the advantages of the oversampling scheme. In [22] and [23], the BBPD is vulnerable to long run length and thereby limits the loop bandwidth. Therefore, in this work, the frequency acquisition scheme using the multi-phase oversampling is fully utilized and demonstrated in the prototype chip.

In this chapter, we present the analyses of the proposed frequency acquisition scheme with regard to the capture range, the effect of the phase mismatch, and the frequency acquisition time. Then, the detailed circuit implementation of the proposed referenceless CDR will be described. Finally, the measurement results of the prototype chip show the performance and demonstrate the theoretical analyses.

3.2 Proposed Frequency Acquisition

3.2.1 Operation of BBPD

Since the proposed frequency acquisition scheme is extended from the BBPD, we will start by reviewing the operating principle of the BBPD. Figure 3.1 shows the block diagram of the conventional BBPD. The input data is sampled by two different clock phases (CK0, CK180) and it results in the generation of data and edge samples (D1, E1, and E2). That is, the BBPD uses an oversampling factor of 2 because it takes two samples per data unit interval. The data and edge samples are compared by the XOR gates and the BBPD detects where the data transition occurs. The UP or DN signals are generated to align the in-phase clock (CK0) with the edges of the input data. In the locked state when the phase tracking is underway, the

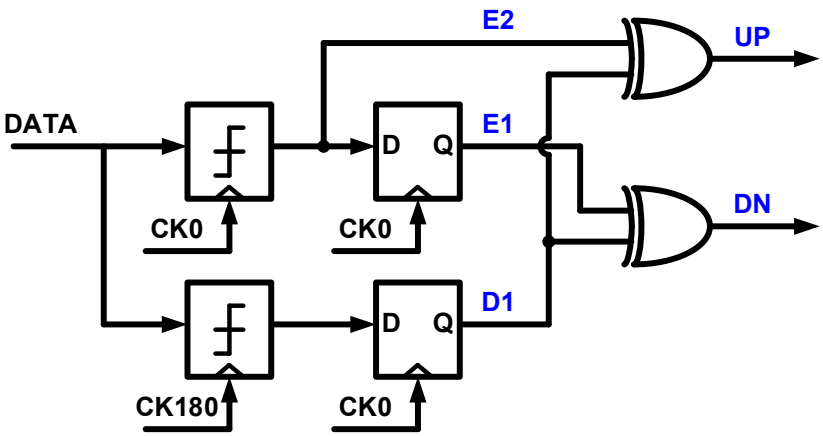
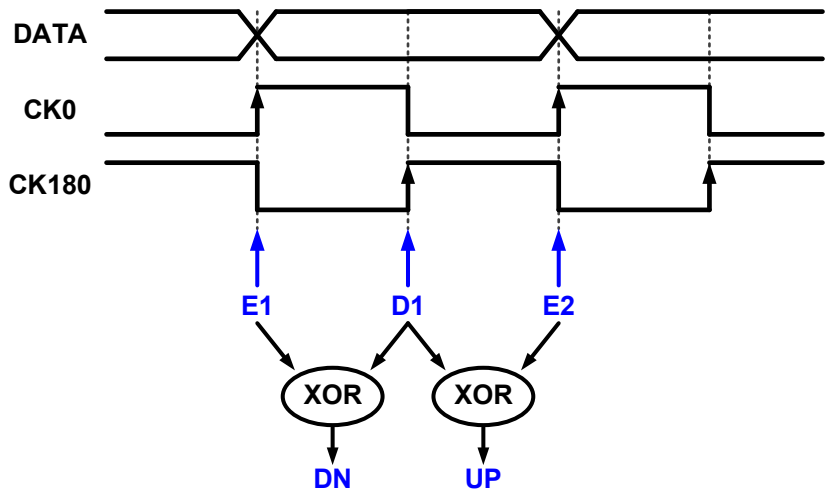


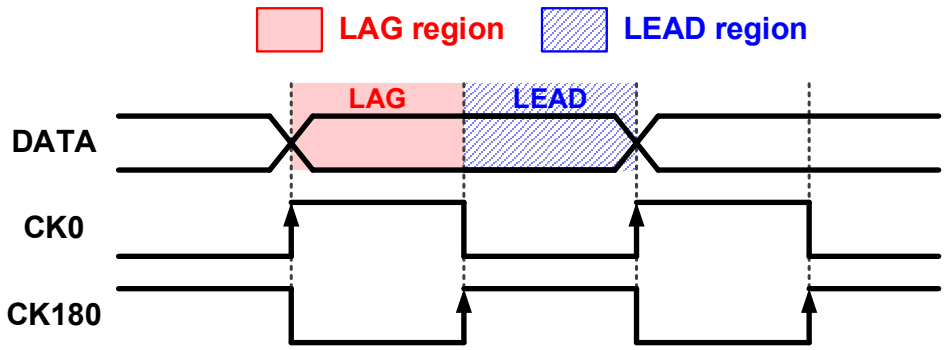
Fig. 3.1 Block diagram of conventional BBPD.

same number of the UP/DN signals are generated and the control voltage to the VCO is at the steady state.

The timing diagram in Figure 3.2(a) shows the operation principle of the conventional BBPD as explained in Figure 3.1. The situation corresponds to the phase-lock state which the rising edge of CK0 is aligned to the data edge. For simplicity, as



(a)



(b)

Fig. 3.2 (a) Operation principle of BBPD and (b) LAG region and LEAD region

shown in Figure 3.2(b), we define “LAG region” and “LEAD region” in the input data stream with respect to the rising edge of the in-phase clock. The LAG region and LEAD region mean that the in-phase clock is lagging and leading the data edge, respectively.

More specifically, if the rising edge of the in-phase clock is located in the front half of the data stream, corresponding to the LAG region, a data transition occurs between D1 and E2. As a result, UP signal is generated as shown in Figure 3.3. On the other hand, if the clock edge is located in the LEAD region, a data transition occurs between E1 and D1, generating DN signal. Note that such UP/DN signals are only meaningful when the frequency difference is within the frequency pull-in range of the BBPD. Otherwise UP/DN signals are randomly generated without any direction to locking.

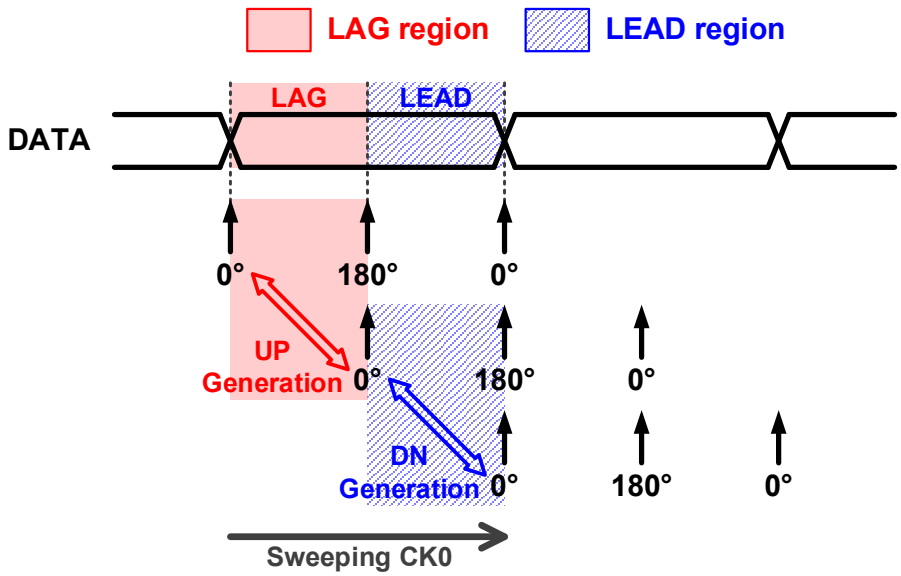
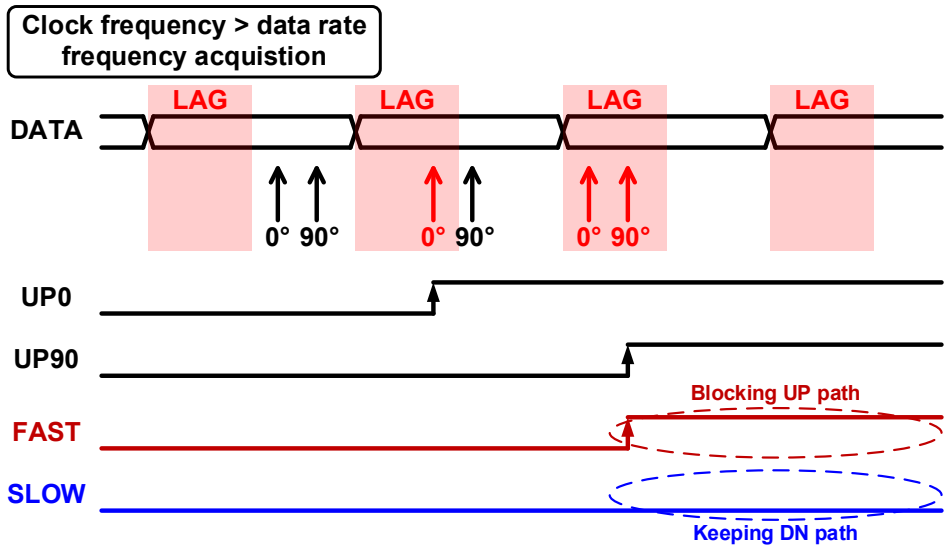


Fig. 3.3 Detailed timing relationship of LAG region and LEAD region

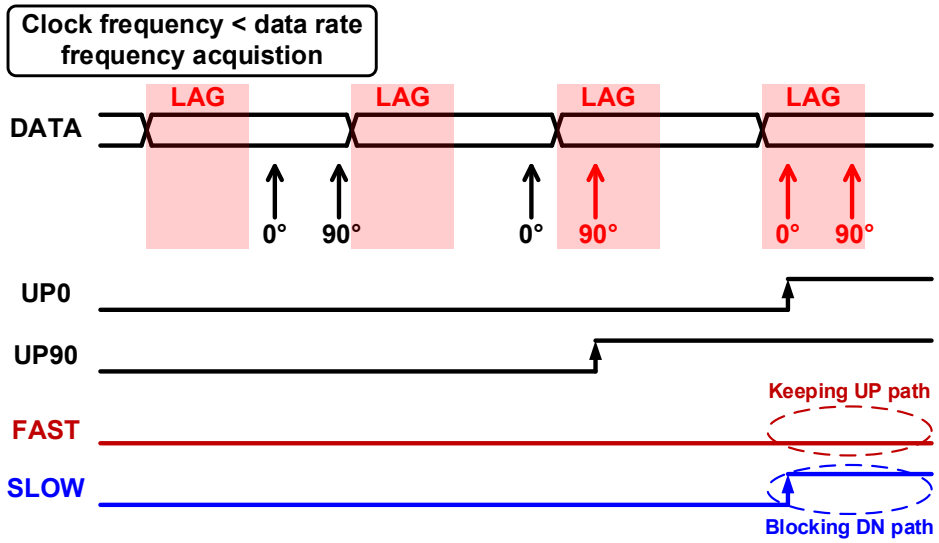
3.2.2 Proposed Bang-Bang Phase-Frequency Detector

The proposed BBPFD performs a central role in this work and offers the frequency acquisition capability as well as the phase detection capability of the BBPD by using double the number of clock phases. Figure 3.4 is a simplified timing diagram that shows how the proposed BBPFD can detect a frequency error. Although the timing diagram is made based on the result of the UP signal, the same principle can also be employed on the DN signal as shown in Figure 3.5. With two phases added for frequency acquisition, a total of four phases are utilized. UP0 (UP90) is the output of the BBPD clocked with CK0 (CK90). FAST and SLOW are the results of mutual sampling of UP0 and UP90.

First, when the clock frequency is higher than the data rate, the clock edges drift to the left (early) with respect to the data edge as shown in Figure 3.4(a). At the first sampling point, since both edges of CK0 and CK90 are located in the LEAD region, UP0 and UP90 are both low without any change. At the second sampling point, however, UP0 becomes high because CK0 enters the LAG region. At the third sampling point, CK90 also moves to the LAG region and leads the transition of UP90. That is, with the faster clock, the transition of UP0 comes earlier than that of UP90. That is, while SLOW remains at low, FAST becomes high. As a result, FAST disables the UP signal and only the DN signals appear at the output of the BBPFD.

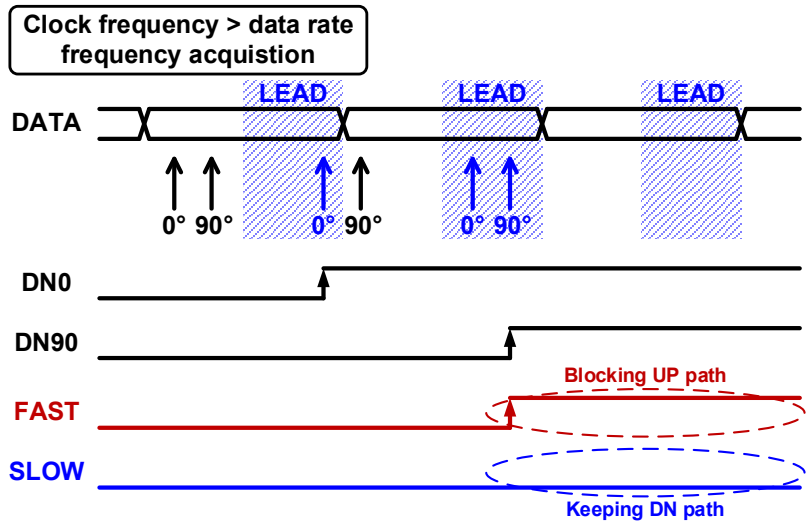


(a)

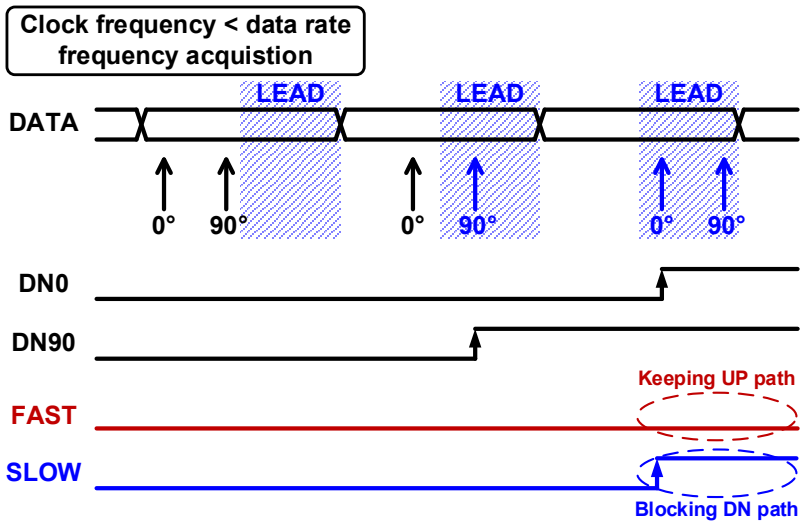


(b)

Fig. 3.4 Simplified timing diagram of proposed frequency acquisition with UP signals when clock frequency is (a) higher and (b) lower than data rate.



(a)



(b)

Fig. 3.5 Simplified timing diagram of proposed frequency acquisition with DN signals when clock frequency is (a) higher and (b) lower than data rate.

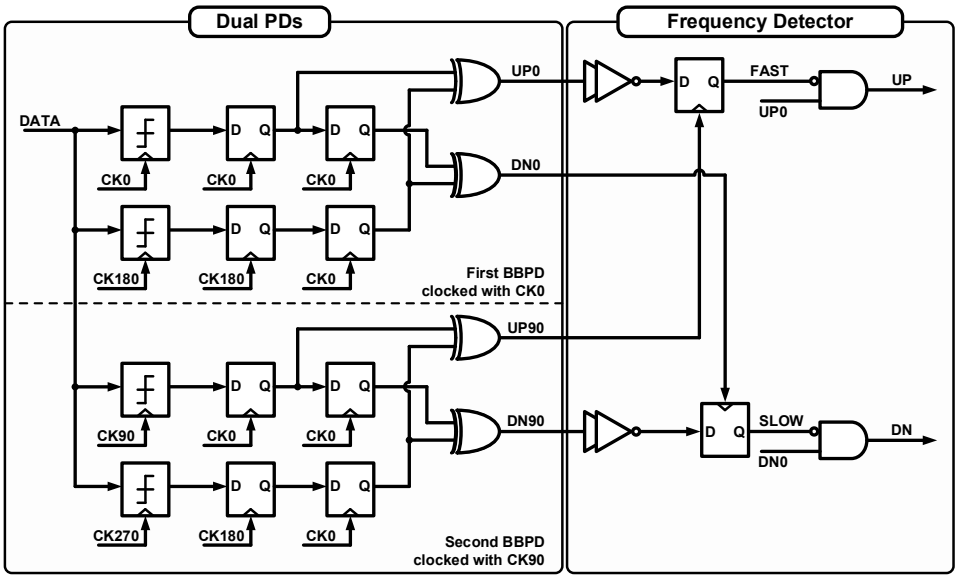


Fig. 3.6 Block diagram of proposed BBPFD

On the other hand, in the case of the slower clock, the opposite situation occurs as shown in Figure 3.4(b). Since the clock edges drift to the right (late) with respect to the data edge, the transition of UP0 is later than that of UP90, which asserts SLOW at high. As a result, SLOW blocks the DN path and only the UP signals are enabled. Consequently, in both cases, the frequency acquisition is achieved by detecting the drift direction of the clock edges and connecting/disconnecting the UP/DN path appropriately.

Based on the above operation principle, the proposed BBPFD can be implemented as shown in Figure 3.6. The BBPFD is divided into two blocks which are dual PDs and a frequency detector. The difference between the two BBPDs is which clocks are used to sample the input data. The first one is a typical BBPD where sampling clocks are CK0 and CK180. On the other hand, the second BBPD has the

same architecture as the first one, but the quadrature clocks, CK90 and CK270, sample the data. With the different sampling clocks, the dual PDs generate UP0, DN0, UP90, and DN90. Although the sampling clock phases are different, the outputs need to be synchronized for comparison at the next stage. Therefore, the final D-flip-flops (DFFs) of the dual PDs are retimed by the same clock, CK0. That is, the second BBPD compares the phases of the data and CK90 and then the outputs are synchronized by CK0. Using the UP and DN signals generated from the dual PDs, the frequency detector determines whether the recovered clock frequency is higher or lower than the data rate. As explained in Figure 3.4 and Figure 3.5, the result of sampling UP0(DN90) with UP90(DN0) indicates whether or not the clock frequency is higher (lower) than the data rate. The sampled outputs, FAST and SLOW, determine whether the UP and DN signals generated in the first BBPD will be transmitted to the final outputs or not. In the DFFs of the frequency detector, a race condition occurs because the UP/DN signals are synchronized for phase comparison. However, since sampling the previous value is correct according to the operation principle, it

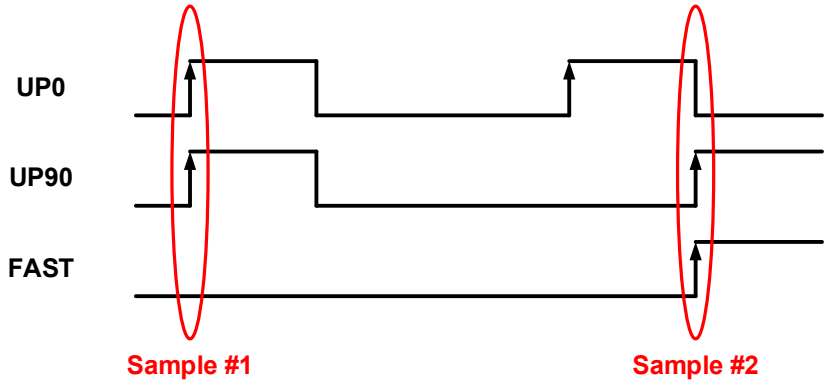


Fig. 3.7 Timing diagram showing ambiguous sampling points in FD.

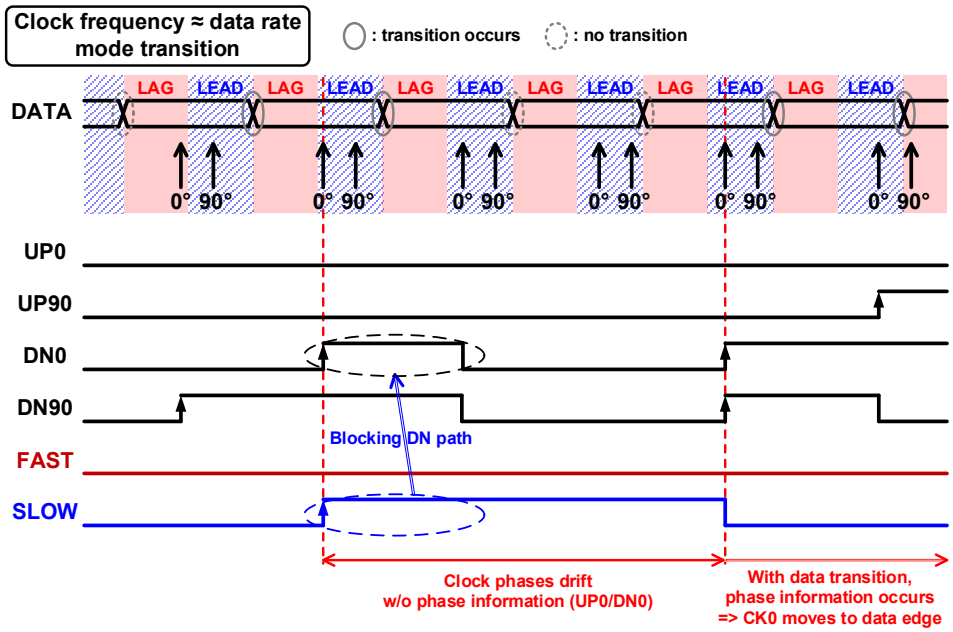


Fig. 3.8 Simplified timing diagram illustrating mode transition.

can be resolved by adding inverters to the input path of the DFF. The delay of the additional inverters is made larger than the hold time of the DFF. As a result, as shown in Figure 3.7, '0' is sampled at Sample #1 and '1' is sampled at Sample #2.

When frequency lock is reached, both FAST and SLOW are required to keep low and the normal BBPD operation is enabled. However, in the mode transition, a problem might occur if the direction of the first BBPD operation is opposite to that of the frequency detection signals. That is, CK0 is located in the LAG region (LEAD region), but FAST (SLOW) turns up. Figure 3.8 shows an example of the worst case that causes opposite signals. First, assume that the clock frequency is slightly lower than the data rate and CK0 is located in the LAG region without UP0. Then, CK0 goes into the LEAD region at the next sampling and SLOW occurs by the DN sig-

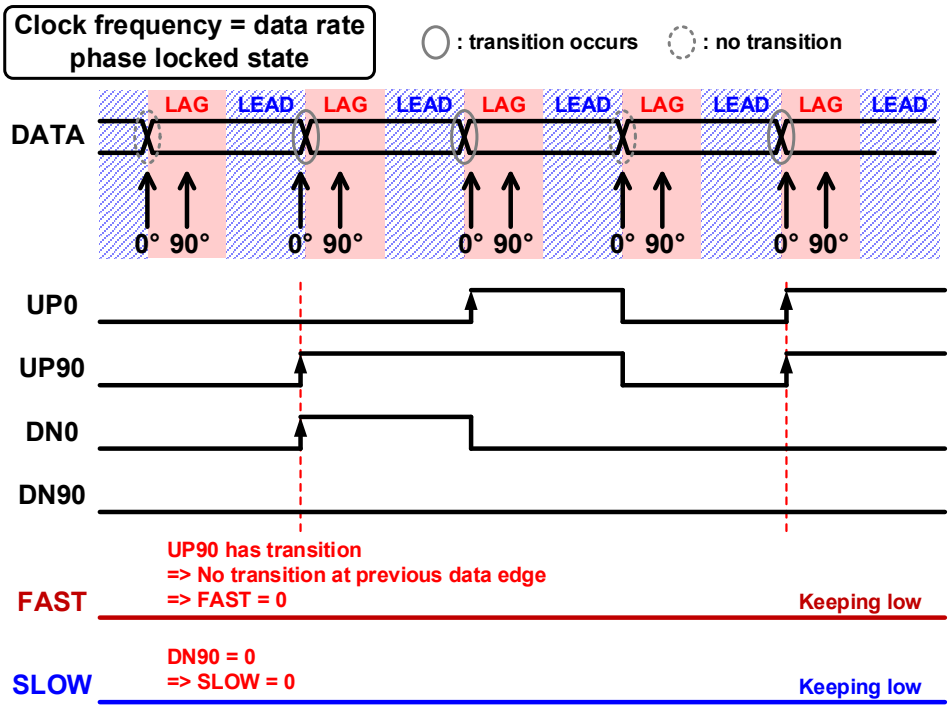


Fig. 3.9 Simplified timing diagram illustrating phase-locked state.

nals, inhibiting the DN path. After that, if there is no data transition, the clock phases drift without any direction due to lack of phase information. However, when the data transition occurs, the CDR updates the phase information and CK0 moves to the data edge. Therefore, after frequency lock, the edges of CK0 and the data are automatically aligned.

After the mode transition, the CDR goes into the phase locked state as shown in Figure 3.9. In the state, CK0 which is used as an edge clock dithers between the LAG region and the LEAD region, and thus either UP0 or DN0 appears if the data transition takes place. On the other hand, since CK90 is located in the LAG region,

UP90 depends on the data transition and DN90 keeps low which makes SLOW low. For the occurrence of FAST, the previous value of UP0 is high when UP90 has a transition, but it is not possible because there was no data transition at the previous sampling. Therefore, both FAST and SLOW keep low and the BBPFD is degenerated into the conventional BBPD.

3.2.3 Analysis of Capture Range

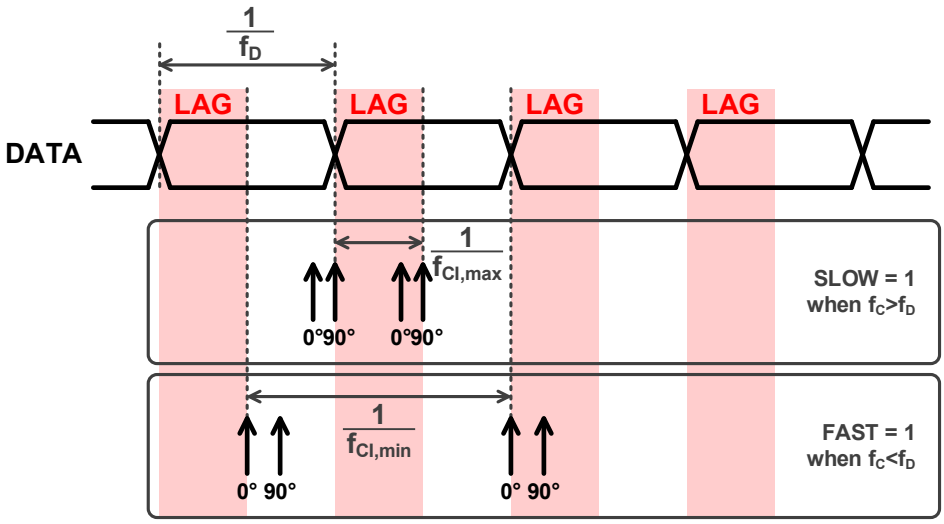
For the frequency acquisition, SLOW (FAST) should be kept low when the clock frequency is higher (lower) than the data rate. It means that the frequency acquisition will fail if the opposite case occurs. Figure 3.10(a) shows the timing diagrams in a full-rate system at the boundary cases where the opposite condition begins to occur. As a result, the two frequencies indicate the minimum and maximum bounds of the initial VCO frequency that the CDR can be safely locked when the data rate is fixed. The two frequencies, $f_{CI,min}$ and $f_{CI,max}$ are expressed as

$$f_{CI,min} = \frac{2}{3} f_D \text{ and } f_{CI,max} = 2f_D \tag{3.1}$$

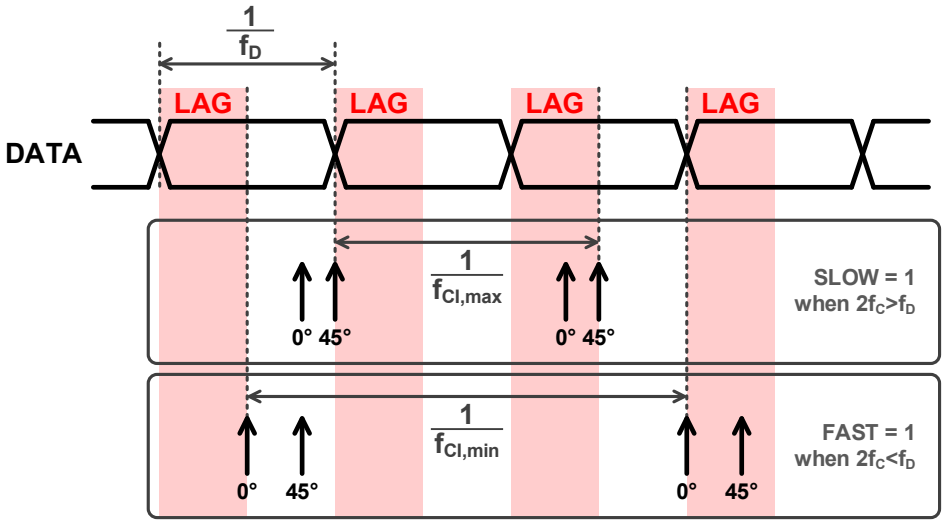
where f_D is the symbol rate of the input data. Therefore, the initial VCO frequency f_{CI} for the safe lock is determined as

$$\frac{2}{3} f_D \leq f_{CI} \leq 2f_D. \tag{3.2}$$

To guarantee frequency acquisition, the initial VCO frequency must be included in the range given in (3.2). On the other hand, when the initial VCO frequency is f_{CI}, the capture range of the input is from $0.5 \times f_{CI}$ to $1.5 \times f_{CI}$. Thus, the theoretical capture range of the proposed scheme is ±50 %. Although it is smaller than the capture range of the rotational FD (-37 % ~ +100 %) proposed in [2], the rotational FD produces a separate output from the phase detection output, necessitating the dual-loop architecture as explained in Chapter 2.



(a)



(b)

Fig. 3.10 Timing diagram for analysis of capture range in (a) full-rate system and (b) half-rate system.

If a half-rate 8-clock system with half-quadrature phases (CK0, CK45, CK90, CK135, CK180, CK225, CK270, and CK315) is used, as shown in Figure 3.10(b), the lower and upper bounds of initial frequencies are determined as

$$f_{CI,min} = \frac{2}{5} f_D \text{ and } f_{CI,max} = \frac{2}{3} f_D. \tag{3.3}$$

Therefore, the safe initial frequency f_{CI} for the correct frequency capturing is determined as

$$\frac{2}{5} f_D \leq f_{CI} \leq \frac{2}{3} f_D. \tag{3.4}$$

Thus, the capture range is from $1.5\times f_{CI}$ to $2.5\times f_{CI}$ with the center at $2\times f_{CI}$, which shows the reduced range of ±25 %.

In this work, due to the limited speed of the samplers, the half-rate 8-clock system is used rather than the full-rate 4-clock system. The following analyses are based on the half-rate system with the half-quadrature phases.

3.2.4 Effect of Phase Mismatch

Unlike the conventional half-rate CDR, the half-quadrature phases are required for the proposed frequency acquisition. However, in the clock buffering shown in Figure 3.11, the phase difference between the in-phase clock and the half-quadrature clock can vary and the phase mismatch can degrade the CDR capture range. Figure 3.12 shows post-layout simulation results of the CDR capture range with deliberate application of a phase difference between the paths of the in-phase clock (CK0/ CK90/ CK180/ CK270) and the half-quadrature clock (CK45/ CK135/ CK225/ CK315). Note that the half-quad phase means the phase difference between CK0 and CK45 and its nominal value at the frequency of 5 GHz is 25 ps. A total of five results are obtained and the results are normalized to the ideal point. The simulation shows that even if 30 % phase mismatch is present, the capture range is degraded by just 0.2 % from the nominal value. Even for the half-quad phases of 10 ps and 40 ps, the CDR capture range does not degrade by more than 7 %. Therefore, there is no

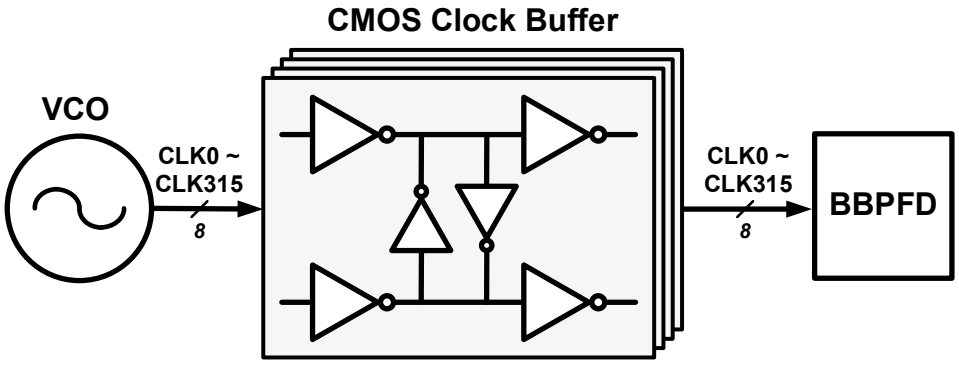


Fig. 3.11 Block diagram of clock path.

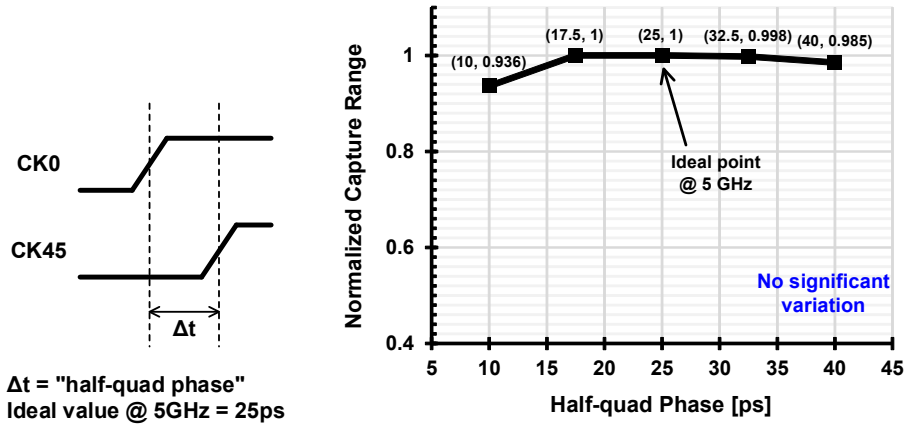


Fig. 3.12 Post-layout simulated capture range when half-quad phase deviates from nominal value of 25 ps.

significant variation in the capture range with respect to the half-quad phase. The reason is that the proposed frequency acquisition is achieved by using the phase sequence of CK0 and CK45, and the phase difference is not so critical unless it is too small or too large.

As demonstrated in the previous analysis, the exact phase difference is not important, so other phases can be used instead of the half-quadrature phases. However, the half-quadrature phases are selected for the following reasons. In the half-rate CDR, an even number of VCO stages is needed for generating I/Q phases. If the number of stages is larger than four, it is hard to design the ring oscillator operating above 5 GHz in the 65 nm CMOS technology. The I/Q mismatch of the two-stage ring oscillator is more severe than that of the four-stage ring oscillator [44]. Therefore, the four-stage ring oscillator is suitable and it means that no additional circuit is required to generate the half-quadrature phases.

3.2.5 Frequency Acquisition Time

In this chapter, an analysis of the frequency acquisition time is shown. Since the proposed scheme detects the transition of the input data, the acquisition time depends on the transition density. First, assume that the initial VCO clock frequency is higher than the data rate and that the frequency error is within the capture range. Among randomly generated UP and DN signals of the BBPD, one of the values is reset to low depending on the frequency error signal, FAST and SLOW, as shown in Table 3.1. Thus, the probability of generating only DN in the BBPFD is expressed as

$$P_{DN,\overline{UP},BBPFD} = P_{DN,BBPD} \cdot P(FAST = 1, SLOW = 0) + P_{DN,BBPD} \cdot \left(1 - P_{UP,BBPD}\right) \cdot P(FAST = 0, SLOW = 0) \quad (3.5)$$

where $P_{DN(UP),BBPD}$ means the probability of generating DN(UP) in the BBPD. In (3.5), if the input data is a clock pattern, the latter term equals zero because data

Table 3.1 Probability of UP/DN according to FAST/SLOW.

FAST	SLOW	Probability of generation	
		UP	DN
0	0	$P_{UP,BBPD}$	$P_{DN,BBPD}$
0	1	$P_{UP,BBPD}$	0
1	0	0	$P_{DN,BBPD}$
1	1	0	0

transition appears in every cycle, and thus FAST is kept high. However, with a random pattern, the transition density determines the occurrence of FAST and thus the probability that FAST is high equals the transition density. Therefore, the probabilities that FAST is high and low are expressed as

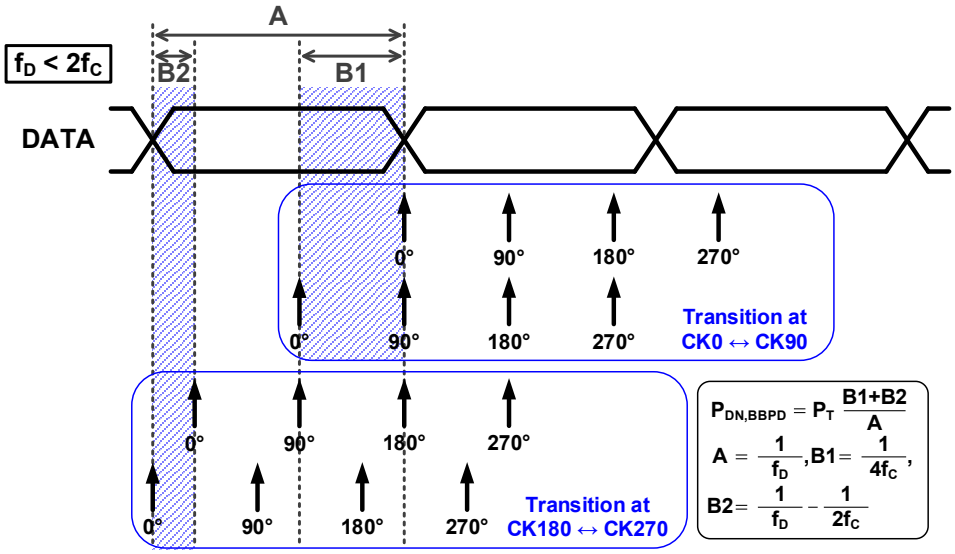
$$P(FAST = 1, SLOW = 0) = P_T \tag{3.6}$$

$$P(FAST = 0, SLOW = 1) = 1 - P_T \tag{3.7}$$

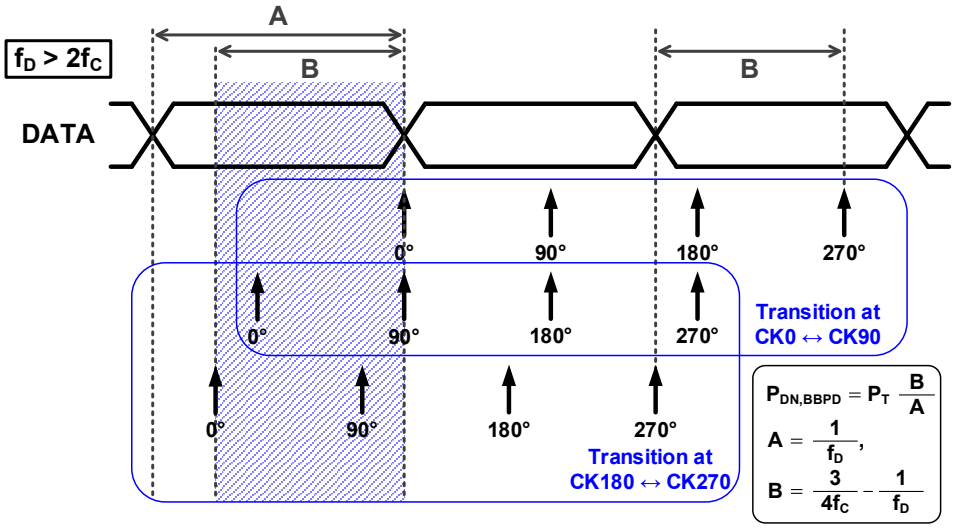
where P_T is the transition density of the input data. The probability of generating DN in the BBPD equals the probability that a data transition occurs after the edge clock and before the data clock as explained in Figure 3.2. In Figure 3.13, the probability is expressed as the ratio of the corresponding cases in one period and it is a function of the frequency difference and transition density. The probability of generating UP in the BBPD is similarly obtained. Figure 3.13(a) and (b) show two cases that the clock frequency is higher and lower than the data rate and the probabilities are expressed as

$$P_{DN,BBPD} = P_{UP,BBPD} = \begin{cases} P_T\left(\frac{1}{f_D} - \frac{1}{2f_C} + \frac{1}{4f_C}\right) / \left(\frac{1}{f_D}\right) = \frac{P_T}{2}(1 + \Delta F), & f_D < 2f_C \\ P_T\left(\frac{3}{4f_C} - \frac{1}{f_D}\right) / \left(\frac{1}{f_D}\right) = \frac{P_T}{2}(1 - 3\Delta F), & f_D > 2f_C \end{cases} \tag{3.8}$$

where the frequency difference is $\Delta F=(2f_C-f_D)/(2f_C)$ which corresponds to the half-rate system. Using (3.6), (3.7), and the first case in (3.8), (3.5) is calculated as follows.



(a)



(b)

Fig. 3.13 Timing diagram for calculating probability of generating DN when clock frequency is (a) higher and (b) lower than data rate.

$$P_{DN,\overline{UP},BBPFD} = \frac{P_T}{2}(1+\Delta F)\cdot P_T + \frac{P_T}{2}(1+\Delta F)\cdot\left[1-\frac{P_T}{2}(1+\Delta F)\right]\cdot(1-P_T). \quad (3.9)$$

Assuming the VCO gain is constant, the amount of the discharged current after the frequency acquisition started can be expressed as

$$C\frac{f_{CI}-f_C(t)}{K_{VCO}} = I_{CP}\int_0^t P_{DN,\overline{UP},BBPFD}\,dt$$

$$= I_{CP}\int_0^t (1+\Delta F)\cdot\left[\frac{P_T^2}{2}+\frac{P_T(1-P_T)}{2}\left[1-\frac{P_T}{2}(1+\Delta F)\right]\right]dt \quad (3.10)$$

where K_{VCO} is the VCO gain and I_{CP} is the pump current. By differentiating (3.10) with respect to time, a differential equation of $f_C(t)$ is obtained as follows.

$$-\frac{C}{K_{VCO}I_{CP}}\cdot\frac{df_C(t)}{dt} = \left(1+\frac{2f_C-f_D}{2f_C}\right)\cdot\left[\frac{P_T^2}{2}+\frac{P_T(1-P_T)}{2}\left[1-\frac{P_T}{2}\left(1+\frac{2f_C-f_D}{2f_C}\right)\right]\right]. \quad (3.11)$$

To calculate the frequency acquisition time using the integration by separation of variables, (3.11) is rearranged as

$$-\frac{C}{K_{VCO}I_{CP}}\cdot\frac{1}{P_T(1-P_T+P_T^2)}\cdot\int_{f_{CI}}^{f_D/2}\frac{f_C^2\,df_C}{\left(f_C-\frac{f_D}{4}\right)\left(f_C+\frac{f_DP_T(1-P_T)}{4(1-P_T+P_T^2)}\right)} = \int_0^{T_{ACQ}} dt. \quad (3.12)$$

Then, the frequency acquisition time T_{ACQ} is obtained as the first case in (3.13). Through the similar processes with the probability of generating only UP in the BBPFD and the second case in (3.8), the acquisition time when the initial VCO

clock frequency is lower than the data rate can be calculated. The result is described as the second case in (3.13) which has a similar form as the first case.

$$
T_{ACQ} = \begin{cases} \dfrac{C}{K_{VCO}I_{CP}} \cdot \dfrac{1}{P_T(1-P_T+P_T^2)} \cdot \left[f_{CI} - \dfrac{f_D}{2} - \dfrac{f_D}{4}(1-P_T+P_T^2)\ln\left(\dfrac{f_D}{4f_{CI}-f_D}\right) + \dfrac{f_D P_T^2(1-P_T)^2}{4(1-P_T+P_T^2)}\ln\left(\dfrac{\frac{f_D}{2}+\frac{f_D P_T(1-P_T)}{4(1-P_T+P_T^2)}}{f_{CI}+\frac{f_D P_T(1-P_T)}{4(1-P_T+P_T^2)}}\right)\right] \\ \qquad = \dfrac{C}{K_{VCO}I_{CP}} g_F(f_D, f_{CI}, P_T), \qquad f_D < 2f_C \\ \dfrac{C}{K_{VCO}I_{CP}} \cdot \dfrac{1}{P_T(1+P_T-P_T^2)} \cdot \left[f_{CI} - \dfrac{f_D}{2} - \dfrac{3f_D}{4}(1+P_T-P_T^2)\ln\left(\dfrac{-f_D}{4f_{CI}-3f_D}\right) + \dfrac{3f_D P_T^2(1-P_T)^2}{4(1+P_T-P_T^2)}\ln\left(\dfrac{\frac{f_D}{2}-\frac{3f_D P_T(1-P_T)}{4(1+P_T-P_T^2)}}{f_{CI}-\frac{3f_D P_T(1-P_T)}{4(1+P_T-P_T^2)}}\right)\right] \\ \qquad = \dfrac{C}{K_{VCO}I_{CP}} g_S(f_D, f_{CI}, P_T), \qquad f_D > 2f_C \end{cases} \tag{3.13}
$$

Therefore, the frequency acquisition time is determined by the data rate, the initial VCO frequency, and the transition density. When the initial VCO frequency is 4.5 GHz, the acquisition time with the various data rates and data patterns is shown in Table 3.2. K_{VCO} and I_{CP} are the simulated values of our CDR design.

The analysis is verified by the CDR simulation as shown in Figure 3.14. Clock pattern, PRBS7, and PRBS31 are used as the input data stream. As expected, the frequency acquisition time of the PRBS patterns is about 2.5 times than that of the clock pattern. The simulated acquisition time closely matches with the calculated value shown in Table 3.2. In addition, the simulation results show that the frequency

acquisition is achieved with few cycle slips. Generally, in the PLL-based CDR, the bidirectional phase detection causes cycle slips. In the proposed CDR, stochastically blocking of the incorrect UP/DN signals reduces the cycle slips.

Table 3.2 Calculated frequency acquisition time

f_D [Gb/s]	ΔF	Data pattern	P_T	$g_{F(S)}(f_D, f_{CI}, P_T)$	T_{ACQ} [ns]
8	0.11	Clock	1	0.946×10^9	94.6
		PRBS	~0.5	2.18×10^9	218
10	-0.11	Clock	1	0.867×10^9	86.7
		PRBS	~0.5	2.03×10^9	203

* f_{CI} = 4.5 GHz, K_{VCO} = 10 GHz/V, I_{CP} = 100 μA, C = 100 pF

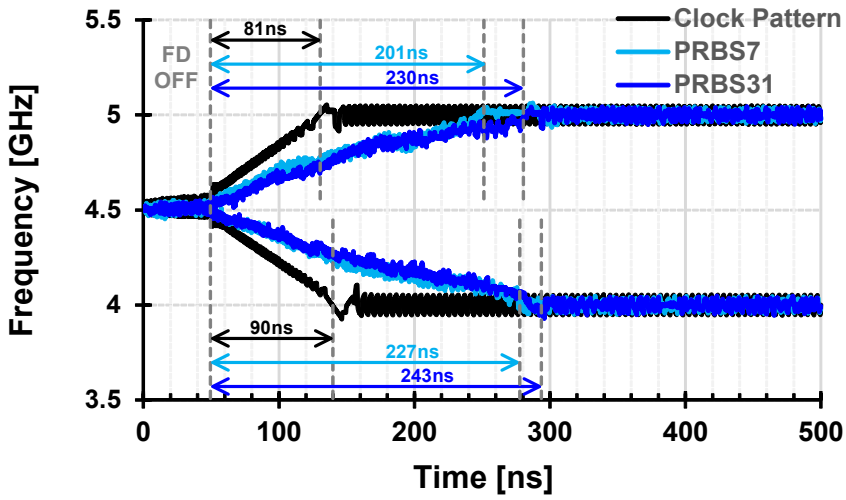


Fig. 3.14 Post-layout CDR simulation results with various input patterns.

3.3 Circuit Implementation

3.3.1 Referenceless CDR Architecture

The overall block diagram of the proposed referenceless CDR is shown in Figure 3.15. A half-rate architecture, rather than a full-rate, is used due to the timing constraint. The proposed CDR consists of a half-rate BBPFD, a charge pump, a loop filter, a 4-stage ring VCO, and a deserializer. To fully exploit the advantages of the single-loop structure described in Chapter 2, the CDR performs both frequency and phase acquisition in the single loop.

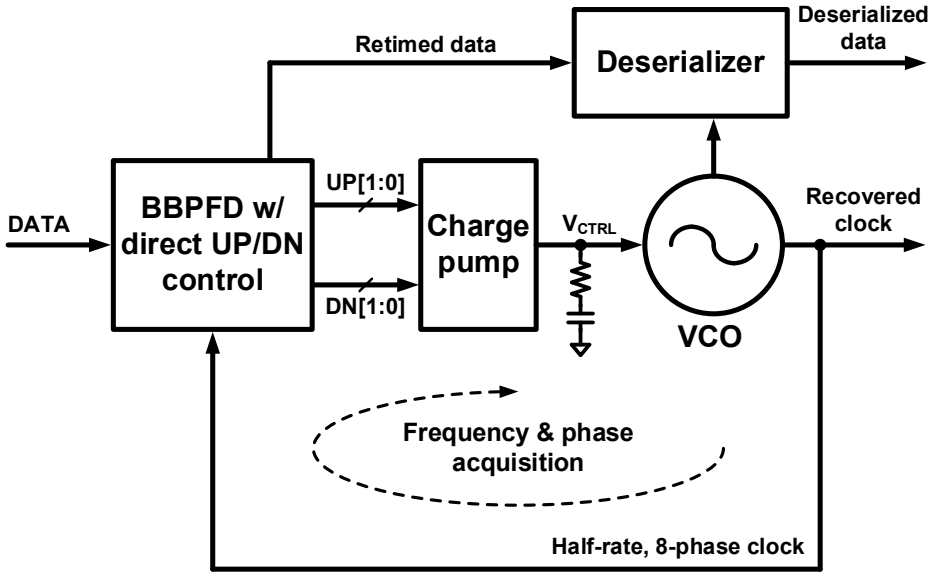


Fig. 3.15 Block diagram of proposed referenceless CDR.

3.3.2 Ring VCO and BBPD

The circuit diagram of the ring VCO is shown in Figure 3.16. A 4-stage ring oscillator is employed to generate the multi-phase, oversampling clock for the frequency acquisition. Each stage is implemented by current starved inverters and their delays are controlled by the control voltage from the loop filter.

Figure 3.17 and Figure 3.18 show the circuit diagrams of the dual PDs of the BBPFD described in Chapter 3.2.2. Based on the operating principle of Figure 3.2, a normal BBPD is implemented as shown in Figure 3.17. It corresponds to the first BBPD which is clocked with the in-phase clock. The samplers consist of a strong-arm comparator with an RS latch. Following the samplers, TSPC D-flip-flops are

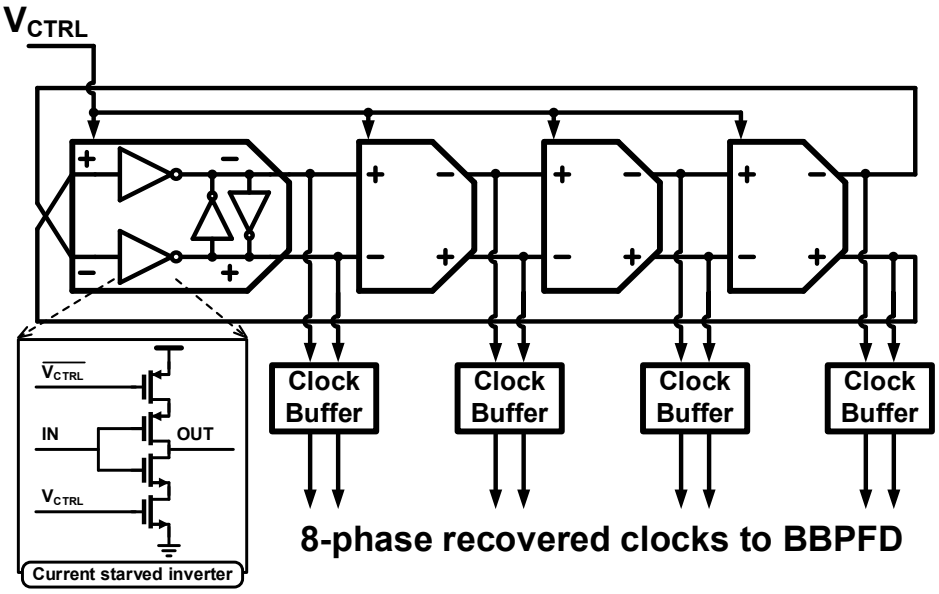


Fig. 3.16 Circuit diagram of proposed referenceless CDR.

implemented to synchronize the data and edge samples. Since the timing margin for synchronizing the data sampled by CK270 directly to CK0 is not large enough above 5 GHz operation, the second stage is added. As a result, the critical riming path is the bold line indicated in the figure. Its timing constraint is that the sum of the clock-to-q delay and the setup time of the TSPC D-flip-flop should be less than the half of the clock period. In the TSPC D-flip-flop, the post-layout simulated values of the clock-to-q delay and the setup time in the worst case are 55 ps and 30 ps, respectively. Therefore, the maximum frequency is about 5.88 GHz, which is beyond the target operation frequency.

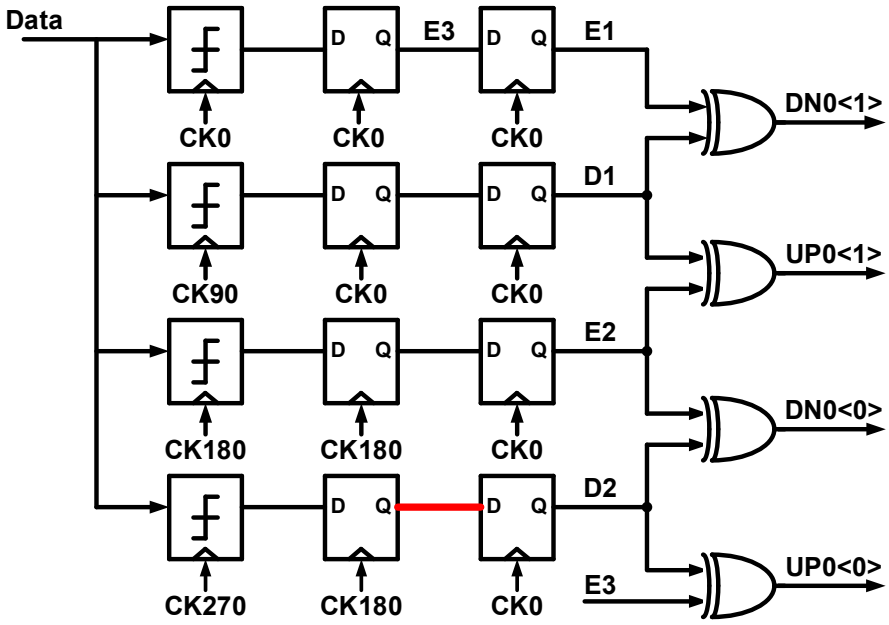


Fig. 3.17 Circuit diagram of first BBPD clocked with in-phase clock.

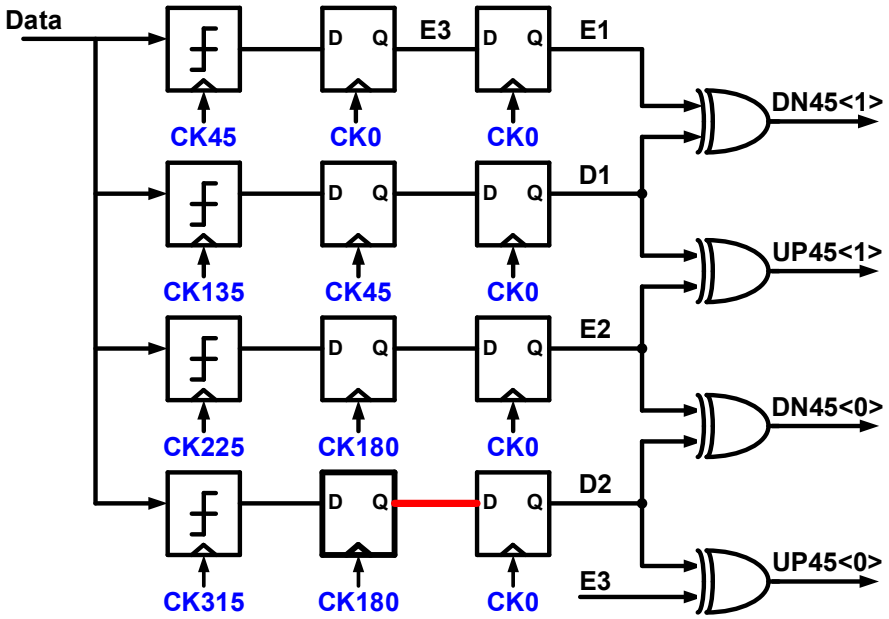


Fig. 3.18 Circuit diagram of second BBPD clocked with half-quadrature clock.

In the second BBPD, as shown in Figure 3.18, only the sampling clocks are different from the first BBPD. The retiming clocks of the comparators are the half-quadrature clocks and the clocks of the second stage are changed accordingly. The third stage is same with the first BBPD because all the UP/DN signals are needed to be synchronized for the phase comparison. The critical timing path is the bold line and its timing constraint is same as the first BBPD.

3.3.3 Charge Pump

As shown in Figure 3.19, the charge pump is implemented with dual compensation circuits based on replica-feedback biasing [45]. While a conventional charge pump shows a mismatch of the UP/DN currents which causes a reference spur, the charge pump can match the UP/DN currents over the wide range of V_{CTRL} thanks to the replica-feedback biasing. Simulation results in Figure 3.20 show the matched UP/DN currents. In addition to the compensation circuits, the pump current can be externally changed according to the operating stages of the CDR. The purpose of the controllable pump current is to increase the loop bandwidth for fast locking during

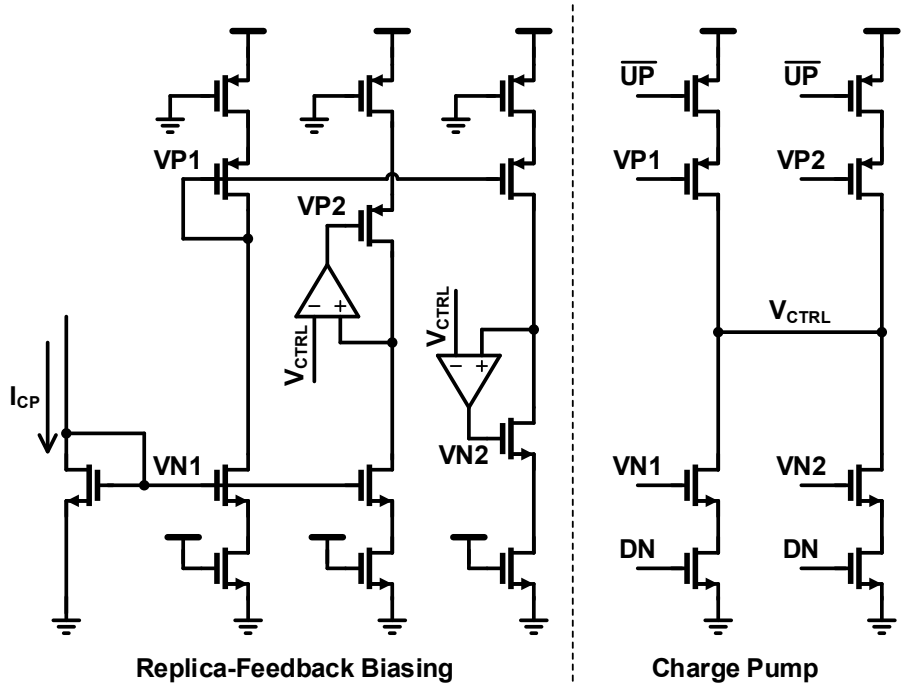


Fig. 3.19 Circuit diagram of charge pump.

the frequency acquisition when FAST or SLOW is asserted. Note that the VCO gain and the loop filter resistance also determine the loop bandwidth. To compare the effect of the three components, the loop characteristics of the charge-pump PLL should be considered and they are expressed as follows

$$\omega_c = \frac{K_{VCO} I_{CP} R}{2\pi} \tag{3.14}$$

$$\zeta = \frac{\sqrt{I_{CP} K_{VCO} C} R}{2\sqrt{2\pi}} \tag{3.15}$$

where w_c is the crossover frequency and ζ is the damping factor. While the three components are proportional to the loop bandwidth, only the resistance is directly

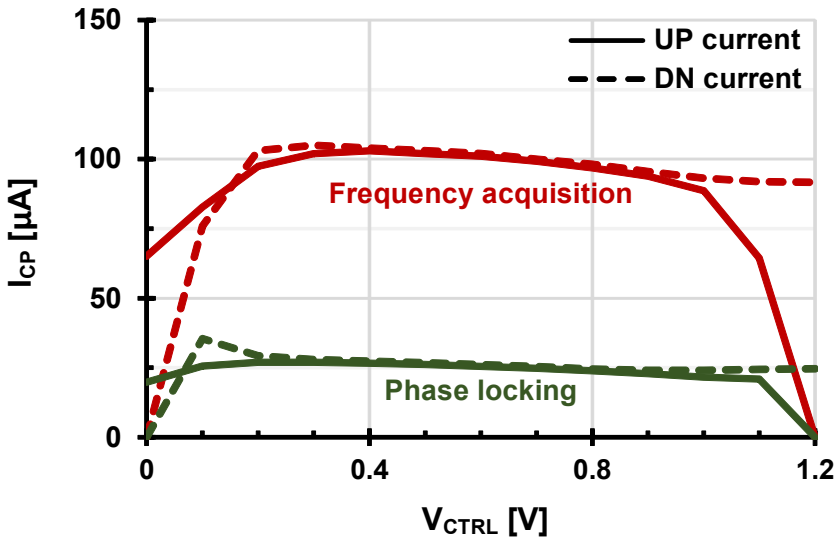


Fig. 3.20 Simulation results of UP/DN currents during frequency acquisition and phase locking.

proportional to the damping factor. Therefore, for the same loop bandwidth increase, a change in the resistor results in a larger damping factor change, which can cause a stability issue. In the case of K_{VCO}, it is not appropriate because it changes the operation range of the VCO. Consequently, in the PLL-based CDR, controlling the pump current is more effective for the purposes of manipulating the bandwidth. In this design, I_{CP} is 100 μA in the frequency acquisition mode and 25 μA in the phase locking mode as shown in Figure 3.20.

The pump current in the frequency acquisition mode cannot be increased arbitrarily because too large a gain causes failure during the mode transition. As explained

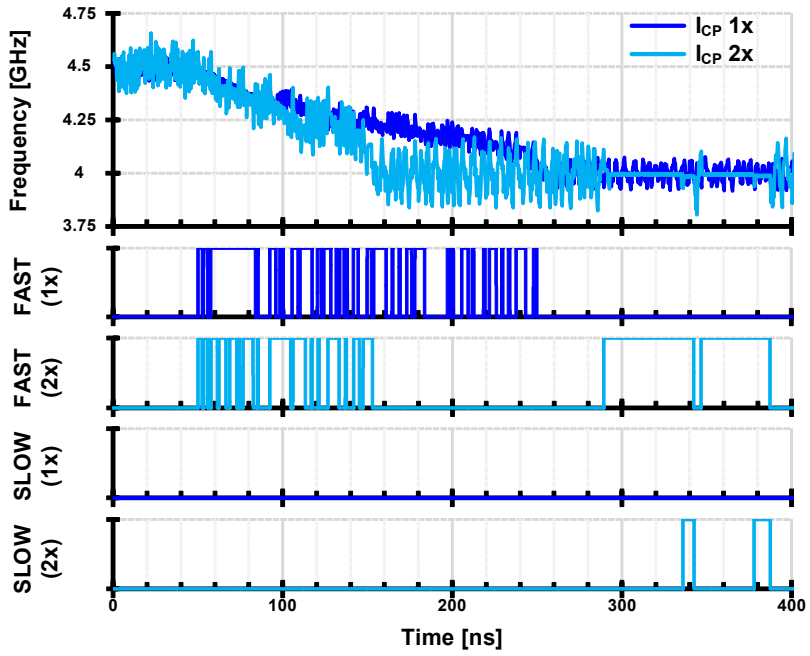


Fig. 3.21 Simulated frequency acquisition behaviors and FAST/SLOW transients for normal and doubled pump currents.

in Figure 3.9, to guarantee a seamless mode transition, CK90 has to be located in the LAG region. However, if the loop gain is too large, CK90 can deviate from the region and thus FAST and SLOW cannot keep low after frequency lock. Figure 3.21 shows the simulation results for doubling the pump current, indicating that a doubled pump current causes failure during the mode transition. In the locked mode, the simulated loop bandwidth is 90 MHz with K_{VCO} of 10 GHz/V, R of 40 Ω, and C of 100 pF, assuming VCO jitter is the dominant source of jitter [46]. The values of the loop filter components are fixed.

3.4 Measurement Results

The prototype chip has been designed and fabricated in a 65 nm CMOS technology. The chip photomicrograph is shown in Figure 3.22 with the active area of 0.047 mm^2 including the filter capacitance. All the blocks use a 1.3-V supply. In the measurement setup shown in Figure 3.23, the J-BERT (Agilent N4903A) generates a PRBS31 pattern for the input data and its swing is 300 mV. The data channel contains the 1-m RG-58 coaxial cable and the 2.3-cm on-board Rogers PCB trace. For the jitter tolerance measurement, the recovered data is fed back to the error detector of the J-BERT. The recovered clock is monitored by the oscilloscope (Tektronix MSO 73304DX).

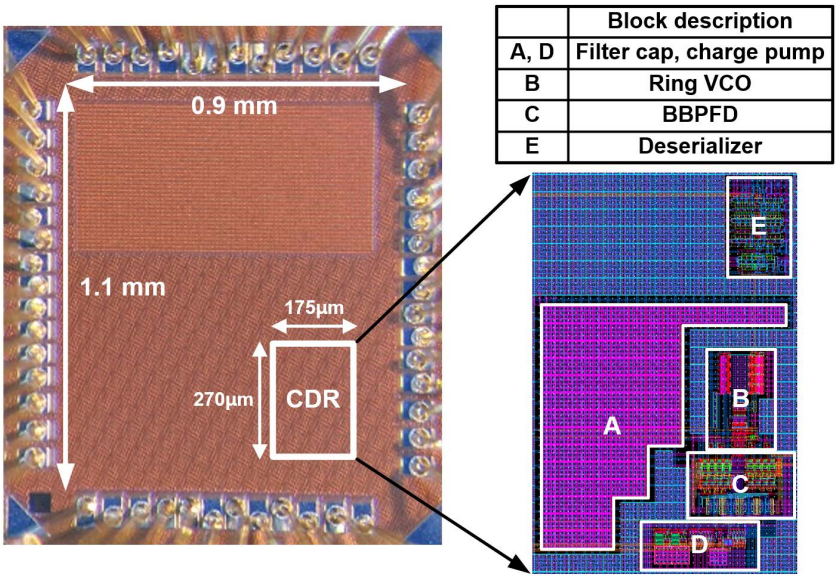


Fig. 3.22 Chip photomicrograph and block description.

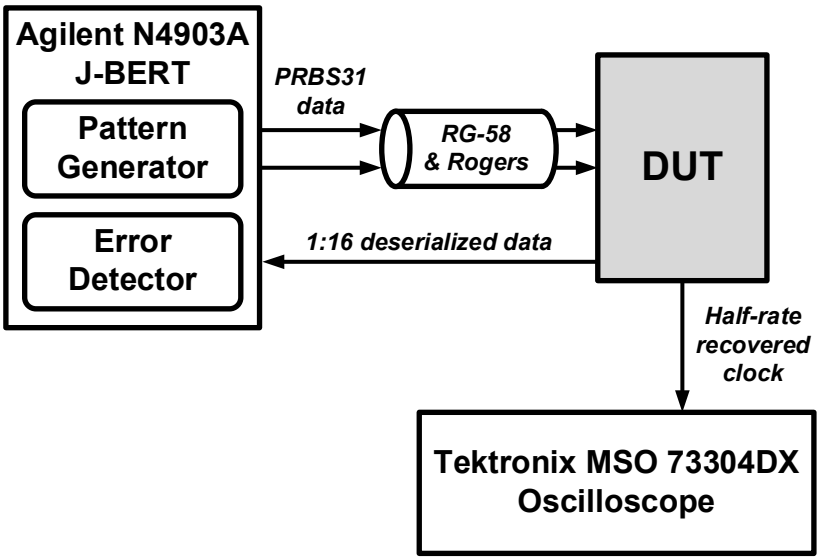


Fig. 3.23 Measurement setup.

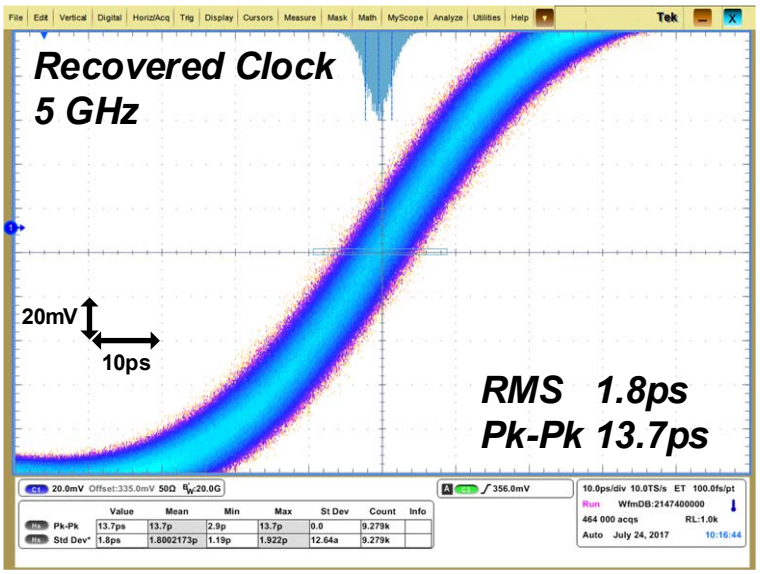
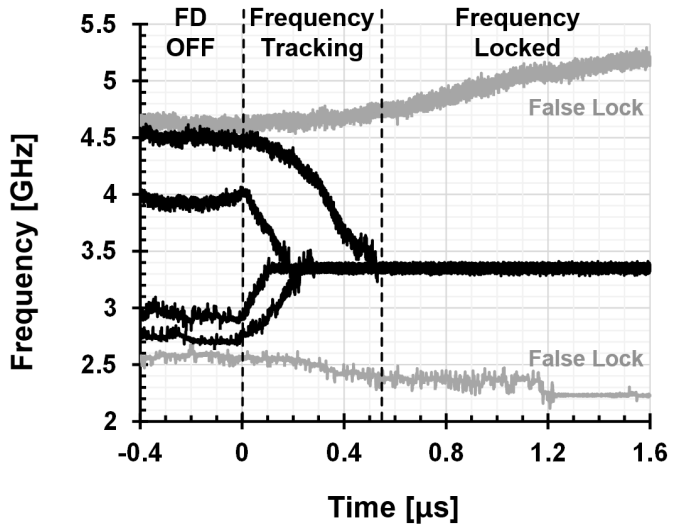


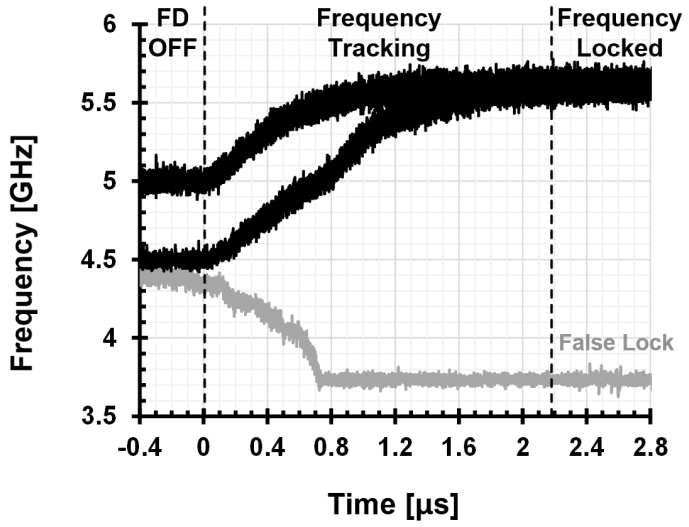
Fig. 3.24 Measured jitter histogram of recovered clock at 10 Gb/s.

The capture range is measured by initializing the VCO frequency to 4.5 GHz and measuring the data rate that the CDR can be locked. The result shows that the capture range of the proposed CDR is from 6.7 to 11.2 Gb/s which validates the analysis in Chapter 3.2.3. Figure 3.24 shows the measured jitter histogram of the recovered clock with the external jitter source disabled. At the data rate of 10 Gb/s, the RMS and peak-to-peak jitters of the recovered clock are measured to be 1.8 ps_{RMS} and 13.7 $ps_{PK\text{-}PK}$, respectively.

The measured frequency acquisition behaviors are shown in Figure 3.25. For the data rate of 6.7 Gb/s which corresponds to the lower bound of the capture range when the VCO is initialized at 4.5 GHz, the bifurcation is clearly seen at 4.5 GHz – slightly larger initial VCO frequency causes lock failure. In Figure 3.25(a), the range of the initial VCO frequency that the frequency acquisition is safely obtained is from 2.7 GHz to 4.5 GHz. The range matches well with the calculated range expressed as (3.4). If the initial VCO frequency is out of the range, the CDR goes to a false lock state (gray line). The false lock state shows that the proposed CDR is not immune to harmonic locking. However, within the range, the frequency detection circuits are enabled and the frequency is monotonically decreased or increased until the CDR goes to the frequency lock state. As can be seen from the frequency behaviors, phase locking is immediately reached right after frequency locking is done without any over/undershoot thanks to the direct UP/DN control with combined frequency and phase detection. The measured maximum acquisition times for data rates of 6.7 Gb/s and 11.2 Gb/s are 0.54 μs and 2.19 μs, respectively.



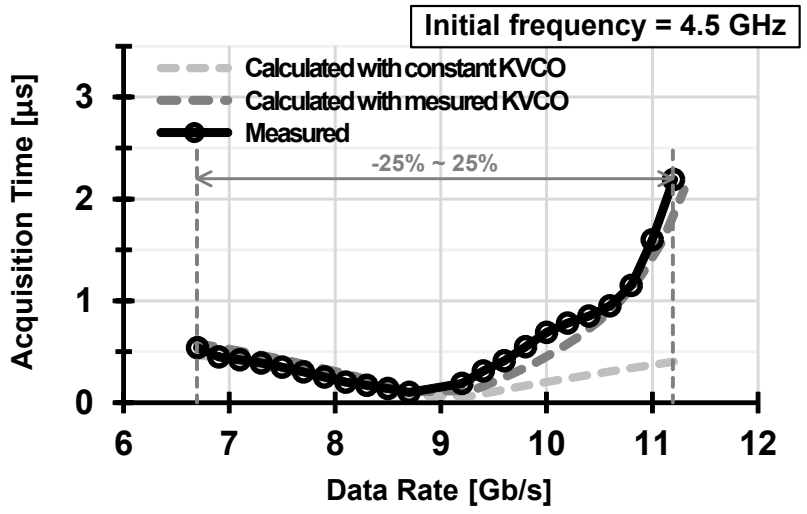
(a)



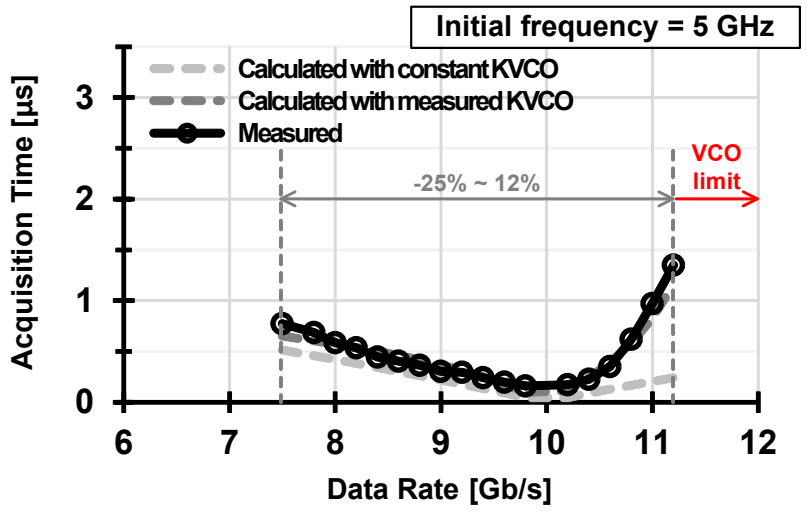
(b)

Fig. 3.25 Measured frequency acquisition behaviors for data rate of

(a) 6.7 Gb/s and (b) 11.2 Gb/s.



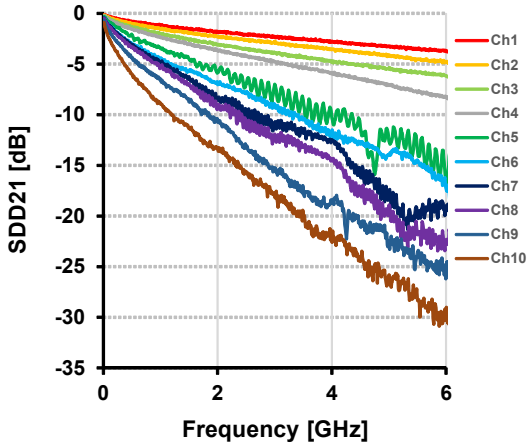
(a)



(b)

Fig. 3.26 Calculated and measured frequency acquisition time versus data rate in a half-rate CDR at initial VCO frequency of (a) 4.5 GHz and (b) 5 GHz.

In the same way, the frequency acquisition time is measured by varying the data rate as shown in Figure 3.26. In Figure 19(a), when the initial VCO frequency is 4.5 GHz, the frequency acquisition time is measured to be less than 2.19 μs for the frequency error of -25 % to +25 %. As analyzed in Chapter 3.2.5, the calculated acquisition time with a constant VCO gain is almost symmetric with respect to the center data rate (light-gray dotted line). However, the measured result is asymmetric, which is due to the reduced VCO gain. In the current-controlled ring VCO, the VCO gain is dramatically reduced at high operating frequency. The reduced gain makes the frequency acquisition slow as shown in (3.13) and Figure 3.25(b). Therefore, a positive initial frequency error exhibits a slower acquisition time than the negative case. It is verified by the calculated acquisition time with the measured VCO gain as shown in the dark-gray dotted line of the figure. In addition, if the operating frequency is higher than 5.6 GHz, the VCO gain becomes too small to keep the CDR

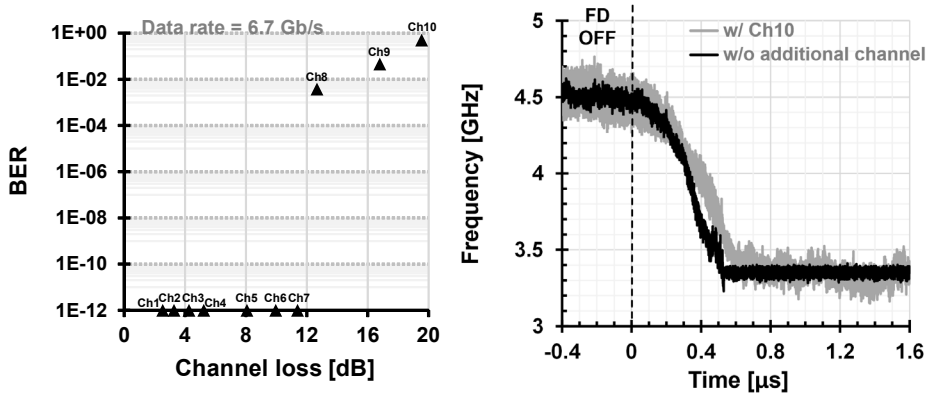


Channel	Loss [dB]	
	@ 3.35GHz	@ 5.6GHz
Ch1	2.53	3.59
Ch2	3.27	4.6
Ch3	4.26	5.9
Ch4	5.23	7.78
Ch5	8.07	13.8
Ch6	9.96	14.9
Ch7	11.39	19.3
Ch8	12.67	22.1
Ch9	16.8	23.7
Ch10	19.5	28.9

Fig. 3.27 Measured SDD21 of various channels and their insertion losses at 3.35 GHz and 5.6 GHz.

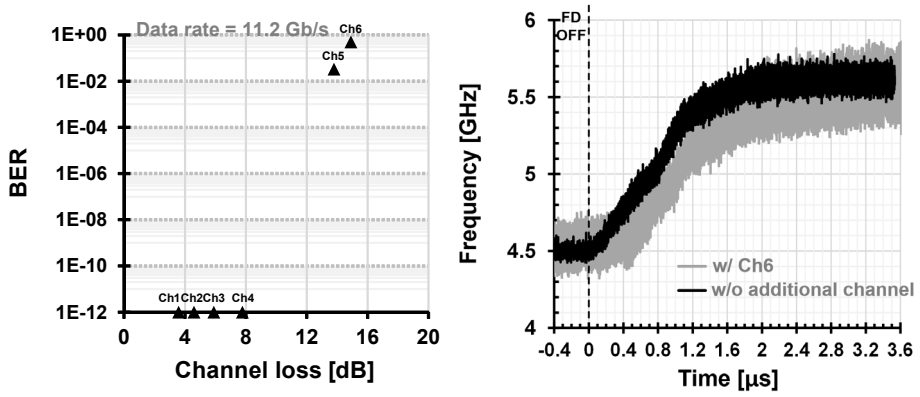
operation in the locked state. Thus, when the initial VCO frequency is 5 GHz, it cannot offer the calculated capture range of 50 % as shown in Figure 3.26(b).

As mentioned in Chapter 2, the schemes presented in [14] - [15] are directly influenced by ISI because they use the data as a clock signal. In this work, since the data is sampled by the recovered clock in a regular fashion and a sequence of clock phases is used to stochastically detect the frequency difference, the sensitivity is relatively small. To demonstrate the effects, measurements on BER and frequency acquisition behavior with various channels are performed. Figure 3.27 shows the measured SDD21 of the channels and their insertion losses. Ch1-4 and Ch5-10 are from SMA cables and DisplayPort cables, respectively. In Figure 3.28(a), BER is measured with Ch1-10 at the lower bound of the capture range, 6.7 Gb/s. The result shows that BER begins to degrade abruptly above 12 dB loss on the three worst channels. However, as shown in Figure 3.28(b), the frequency tracking is attained



(a) (b)

Fig. 3.28 (a) Measured BER with various channels and (b) frequency tracking behavior with and without Ch10 at 6.7 Gb/s.



(a) (b)

Fig. 3.29 (a) Measured BER with various channels and (b) frequency tracking behavior with and without Ch6 at 11.2 Gb/s.

although the CDR fails to lock. In Figure 3.29, similar results are obtained at the upper bound of the capture range, 11.2 Gb/s.

Figure 3.30 shows the measured jitter tolerance of the proposed referenceless CDR. The jitter tolerance is measured with a 10 Gb/s PRBS31 input data at 10^{-12} BER. At the jitter frequency lower than 6 MHz, the CDR exceeds the maximum jitter limit of the test equipment. The jitter tracking bandwidth is 14 MHz and the jitter tolerance at high frequency is 0.505 UI. At the data rate of 10 Gb/s, the measured power consumption is 22.5 mW and the power breakdown is shown in Figure 3.31(a). The power consumption is linearly scaled down along with the data rate as shown in Figure 3.31(b).

Table 3.3 shows the performance comparison with the state-of-the-art referenceless CDRs. It shows that the proposed referenceless CDR achieves the wide capture range while occupying a small area, since the frequency acquisition is realized with

small hardware overhead. Moreover, it offers the energy efficiency of 2.25 pJ/bit and exhibits the fastest acquisition time due to direct control.

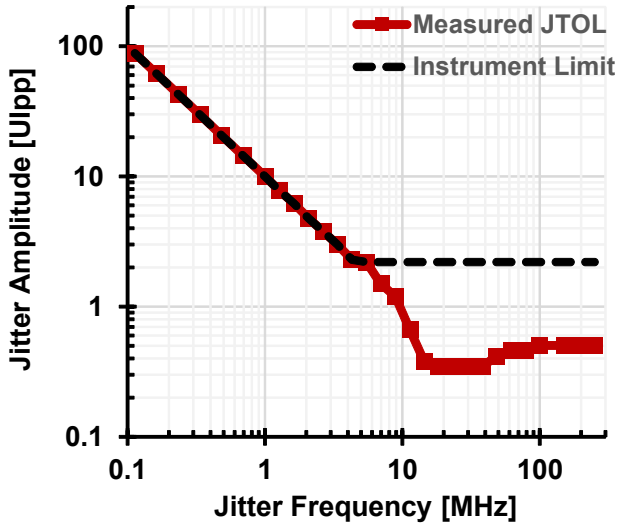
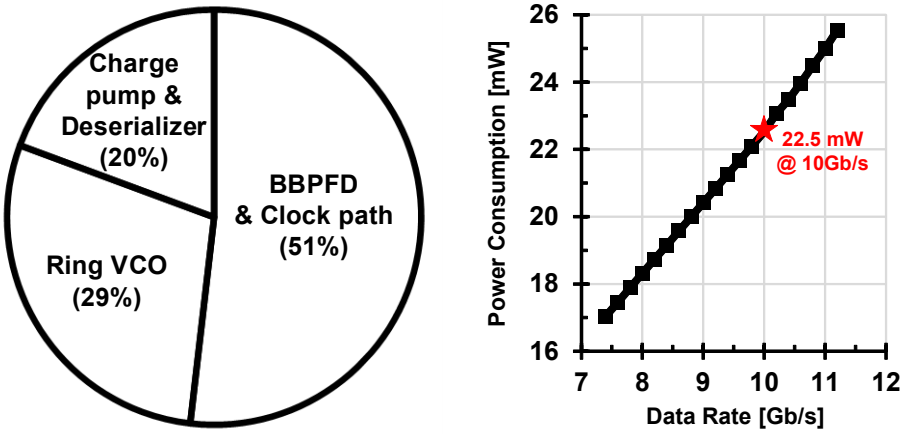


Fig. 3.30 Measured jitter tolerance with 10 Gb/s PRBS31 data at 10^{-12} BER.



(a) (b)

Fig. 3.31 (a) Measured power breakdown and (b) power consumption according to data rate.

Table 3.3 Performance comparison with previous works

	JSSC '13 [1]	TCAS-I '14 [18]	JSSC '15 [15]	JSSC '15 [17]	JSSC '16 [9]	ISSCC '16 [10]	ISSCC '17 [19]	This work
Technology	65 nm	90 nm	65 nm	180 nm	65 nm	28 nm	28 nm	**65 nm**
Supply Voltage [V]	1.0	1.0	-	1.8	1.2/1.0	0.9	0.9	**1.3**
Architecture	Full-rate	Full-rate	Half-rate	Full-rate	Half-rate	Half-rate	Baud-rate	**Half-rate**
Oversampling Ratio	2	2	2	2	2	2	1	**4**
PD Type	Linear PD	BBPD	BBPD	Linear PD	BBPD	BBPD	Baud-rate PD	**BBPD**
Loop Type	Dual	Single	Single	Single	Dual	Dual	Single	**Single**
Using data as clock signal	Yes	No	Yes	No	No	No	No	**No**
Data Pattern	PRBS31	PRBS31	PRBS7	PRBS31	PRBS7	PRBS9 8b10b	PRBS31	**PRBS31**
Data Rate [Gb/s]	8.5–11.5	9.28–12.46	8.5–12.1	8.2–10.3	4–10.5	7.4–11.5	22.5–32	**6.7–11.2**
Capture Range [%]	30	31.8	36	21	65	41	33.9	**50**
Acquisition Time [µs]	< 400	< 48	< 4	< 200	< 600	< 18.5	< 10100	**< 2.19**
JTOL @ High Frequency [UIpp]	0.58	0.22	0.18	0.34	0.3	0.56	0.2	**0.505**
Area [mm^2]	0.35	0.38 *	0.053	0.54	1.63	0.21 *	0.213	**0.047**
Power [mW]	60	92	43	174	22.5	22.9	102	**22.5**
Energy Efficiency [pJ/bit]	5.22	9.2	3.55	16.89	2.25	1.91	3.19	**2.25**

* Estimated from chip photomicrograph

Chapter 4

Digital CDR with Unlimited Frequency Detection Capability

4.1 Overview

Wide-range continuous-rate CDR circuits are becoming increasingly necessary for multi-standard applications. For the continuous-rate operation, referenceless CDRs are suitable because there is no need for an external reference clock determining the data rate in advance. However, since the referenceless CDRs extract the frequency information only from the input data stream, it is hard to obtain a wide capture range. To enhance the capture range, several frequency acquisition schemes have been presented in prior works [9], [10], [19], and [41]. However, they offer a limited capture range and the limitation is determined by the capability of the fre-

quency acquisition schemes. Furthermore, the capture range of the prior works depends on a specific initial frequency and decides the upper and lower limits of the data rate. Figure 4.1 shows the measured FD response in [38]. It is measured with a fixed initial frequency and the possible detection range of the frequency error is determined by the capability of the frequency acquisition scheme. Our previous work also has the same limitation which is clearly shown in Figure 3.25. That is, to gain frequency acquisition at the maximum data rate in the capture range, the initial frequency of the oscillator must be within a fixed range, otherwise frequency lock will fail.

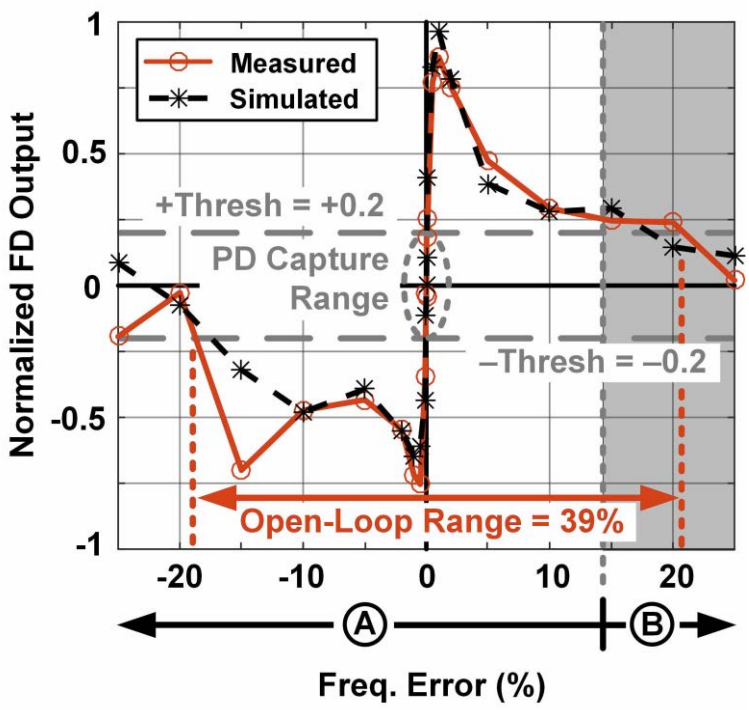


Fig. 4.1 Measured FD response of prior work [38].

In this paper, we present a referenceless digital CDR with an unlimited frequency detection capability that is extended from a multi-phase oversampling scheme. As a result, the proposed CDR obtains frequency acquisition at any initial condition and its capture range is determined only by the operating range of the oscillator.

4.2 Multi-Phase Oversampling FD

In this chapter, we briefly review the operation principle of the multi-phase oversampling frequency detector which is proposed in Chapter 3.2.2. The reason is that the frequency detector used in the proposed digital CDR is based on the multi-phase oversampling scheme. Subsequently, an accurate analysis of the capture range is described because the analysis in Chapter 3.2.3 is simplified. Actually, the relative widths of the LAG/LEAD regions change with a frequency offset, and thus the analysis becomes more complicated. Therefore, we will analyze the relationship between the relative widths of the regions and the frequency offset. Based on the relationship, we can investigate the causes of the capture-range limitation of the multi-phase oversampling scheme and calculate the range boundaries.

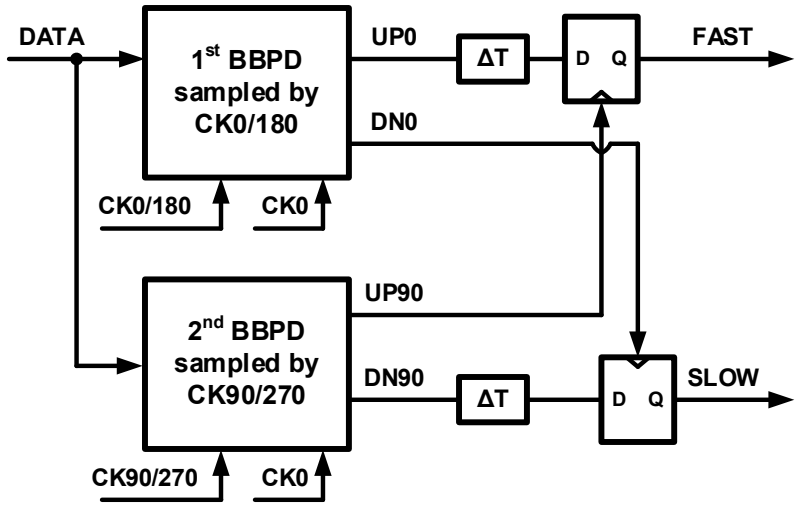


Fig. 4.2 Block diagram of multi-phase oversampling FD.

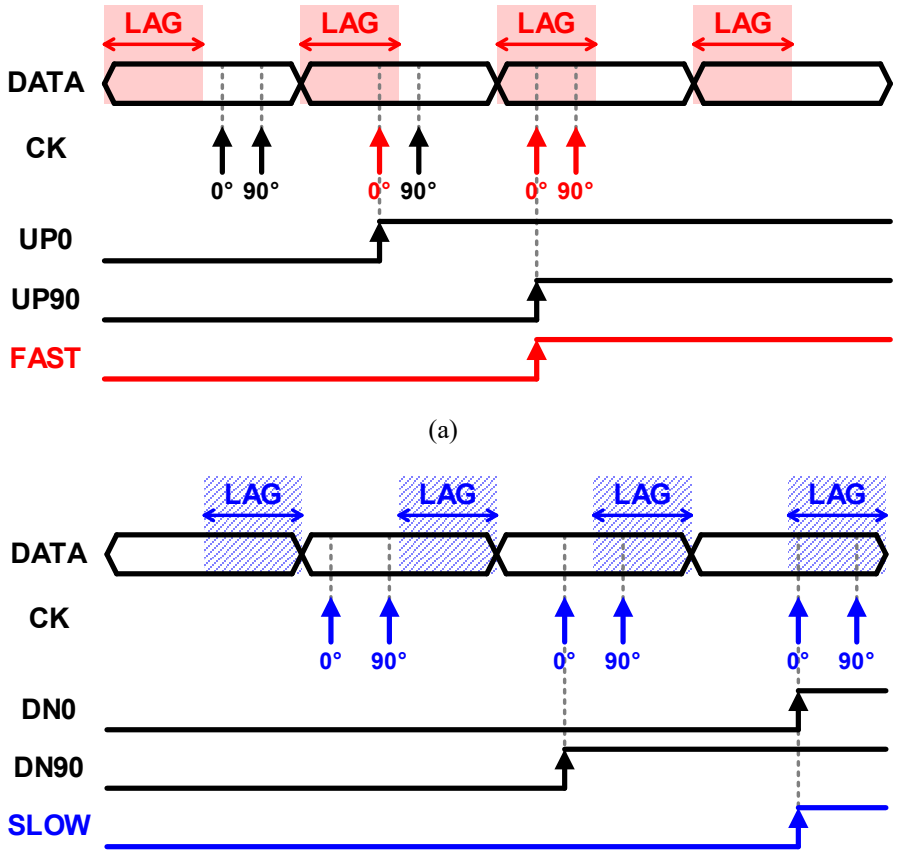


Fig. 4.3 Operation principle of multi-phase oversampling FD with (a) negative frequency offset and (b) positive frequency offset.

4.2.1 Operation Principle

The multi-phase oversampling FD uses 4x oversampling to obtain the frequency detection and composed of two BBPDs as shown in Figure 4.2. One BBPD is sampled by the in-phaes clocks and the other one is sampled by the quadrature-phase clocks. Then, mutual sampling of the outputs generate the frequency detection signals, FAST and SLOW. That is, it detects the drift direction of the multi-phase clock and finds the frequency information. Figure 4.3 summaries the operation principle through timing diagrams. First, when the clock frequency is higher than the data rate, the clock edges drift to the left direction relative to the data edge. As a result, the rising edge of UP0 is earlier than that of UP90, resulting in generation of FAST. In the opposite case, the clock edges move to the right direction and SLOW signal is generated.

However, if the clock frequency becomes too higher or too lower, the frequency detection would be failed. The limitation was analyzed in Chapter 3.2.3 assuming that the LAG/LEAD regions are constant as the frequency offset. In fact, the relative width of the regions vary with the offset and it will be discussed in the next chapter.

4.2.2 Effect of Frequency Offset on LAG/LEAD Regions

When the clock frequency is equal to the data rate, the LAG/LEAD regions are divided at the center of the data stream as explained in Figure 3.3. However, if a frequency offset ($f_D - f_C$) exists, the relative width of the LAG/LEAD regions with respect to the data stream varies with the amount of the offset. First, Figure 4.4 shows a timing diagram when the clock frequency is higher than the data rate corre-

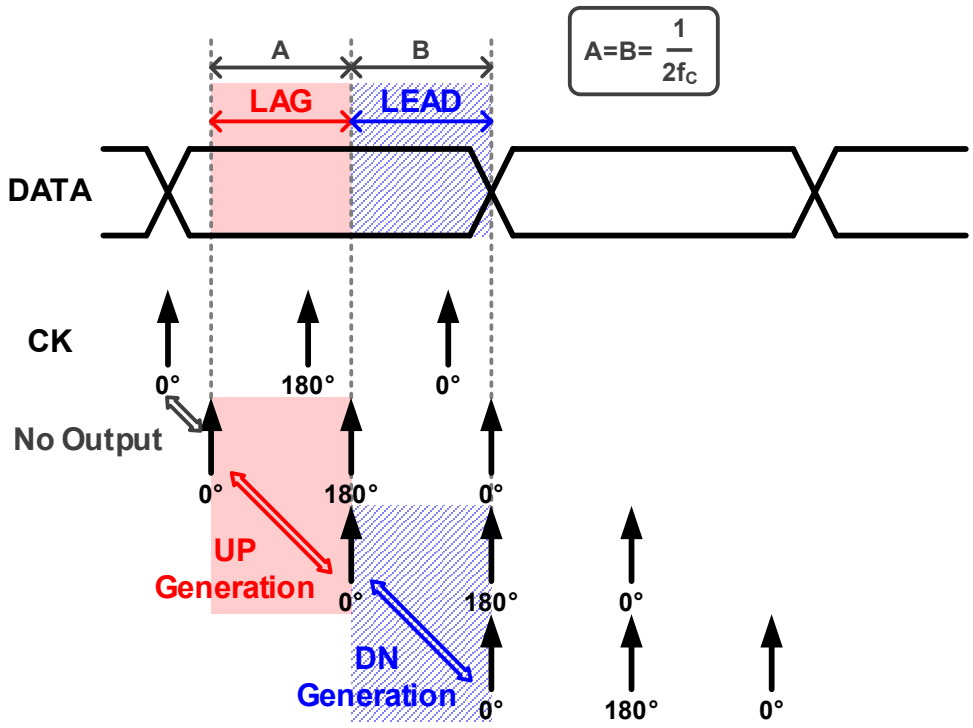


Fig. 4.4 Variation of LAG/LEAD regions with negative frequency offset.

sponding to a negative frequency offset. In this case, since the clock period is shorter than the unit interval, the relative width of the regions becomes smaller. As the clock frequency increases, the relative width decreases. On the other hand, in the case of a positive frequency offset, the opposite situation is caused as shown in Figure 4.5. Because the clock period is wider than the data unit interval, the relative width of the regions increases as the clock frequency decreases.

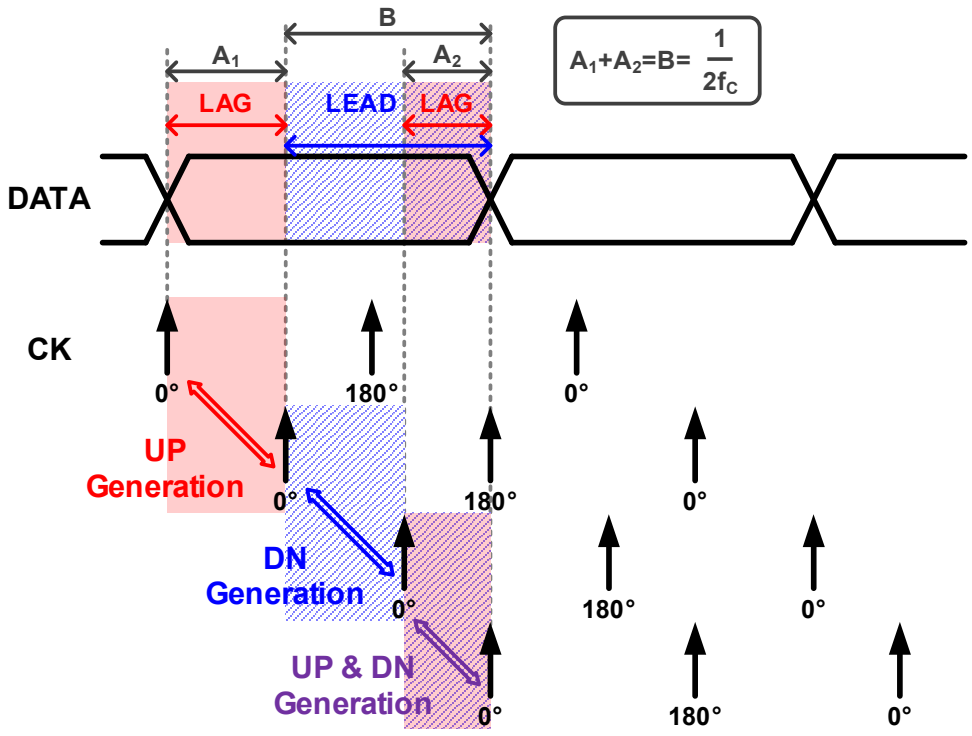


Fig. 4.5 Variation of LAG/LEAD regions with positive frequency offset.

4.2.3 Capture-Range Limitation of Multi-Phase Oversampling FD

Based on the perspectives in Chapter 4.2.2, we can investigate the exact causes of the capture-range limitation and the range boundaries of the multi-phase oversampling FD. First, we will describe the case that the clock frequency is higher than the data rate. Figure 4.4 shows that the relative width of the two regions decreases as the clock frequency increases. Due to that, no matter how the clock frequency becomes higher, a SLOW signal cannot occur in this case. As shown in the timing diagram in Figure 4.6, to generate SLOW, both CK90 of the first sampling point and CK0 of the next sampling point locate in the same LEAD region. However, the

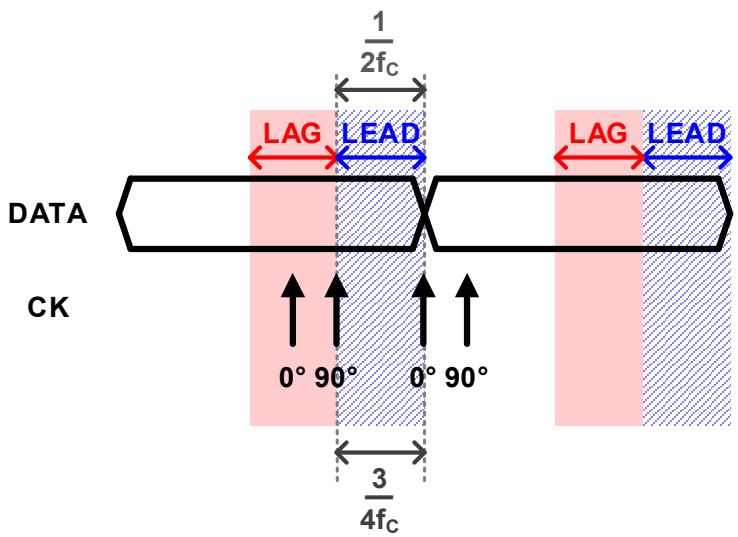


Fig. 4.6 Timing diagram showing that SLOW signal cannot occur with negative frequency offset.

equation in (4.1) is contradiction, and thus a SLOW signal cannot be generated.

$$\frac{1}{2f_C} = \frac{3}{4f_C} \tag{4.1}$$

Since the SLOW signal moves the loop in the opposite direction of the frequency lock, the result of Figure 4.6 is helpful to the frequency detection. However, a FAST signal also cannot be generated if the clock frequency is higher than a specific frequency. As shown in Figure 4.7, FAST signal is not generated when CK0 of the first sampling point is located in the first LAG region but CK90 of the next sampling point is out of the next LAG region. It is the boundary point and the condition of the clock frequency is expressed as

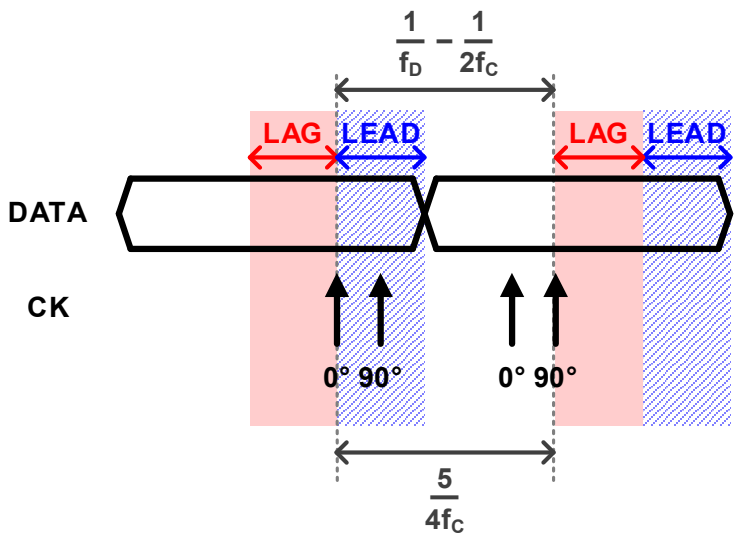


Fig. 4.7 Timing diagram showing that FAST signal cannot occur when clock frequency is higher than 1.75 times data rate.

$$\frac{1}{f_D} - \frac{1}{2f_C} > \frac{5}{4f_C} \tag{4.2}$$

$$f_C > \frac{7}{4} f_D \tag{4.3}$$

$$f_D - f_C < -\frac{3}{7} f_C \tag{4.4}$$

Therefore, the boundary frequency equals to 1.75 times the data rate. That is, if the clock frequency is higher than the boundary frequency, the multi-phase over-sampling FD would fail to detect the frequency error. In actual, due to the effect of

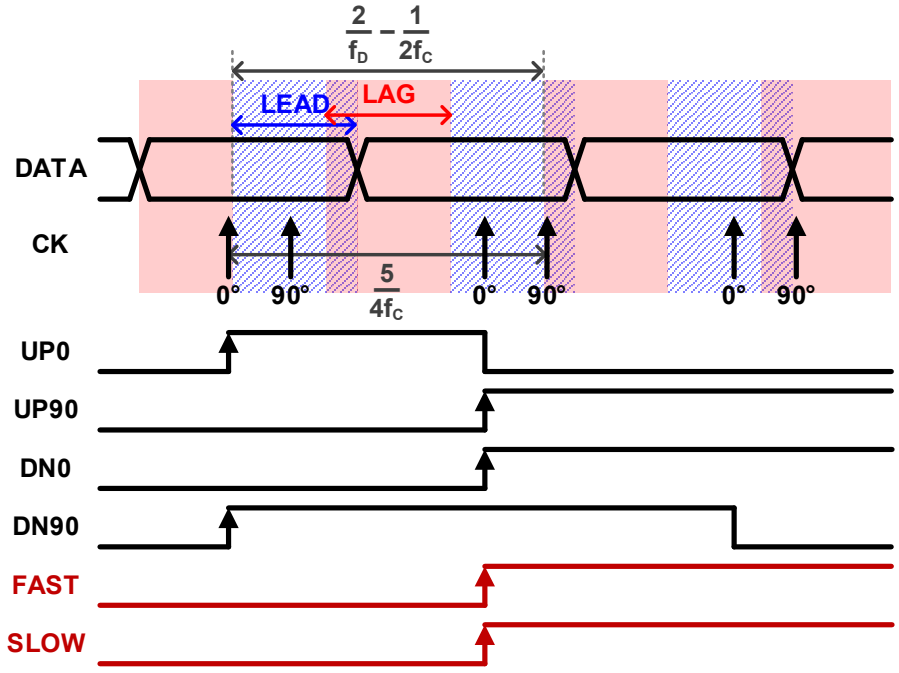


Fig. 4.8 Timing diagram showing capture-range limitation in the case of positive frequency offset.

various noise sources, the boundary point becomes different.

Next, we will discuss the cause of the capture-range limitation in the case of the positive frequency offset. As the clock frequency decreases, SLOW signal can be detected, but FAST signal is also generated as shown in Figure 4.8. The condition of the boundary frequency is expressed as

$$\frac{2}{f_D} - \frac{1}{2f_C} < \frac{5}{4f_C} \tag{4.5}$$

$$f_C < \frac{7}{8} f_D \tag{4.6}$$

$$f_D - f_C > +\frac{1}{7} f_C \tag{4.7}$$

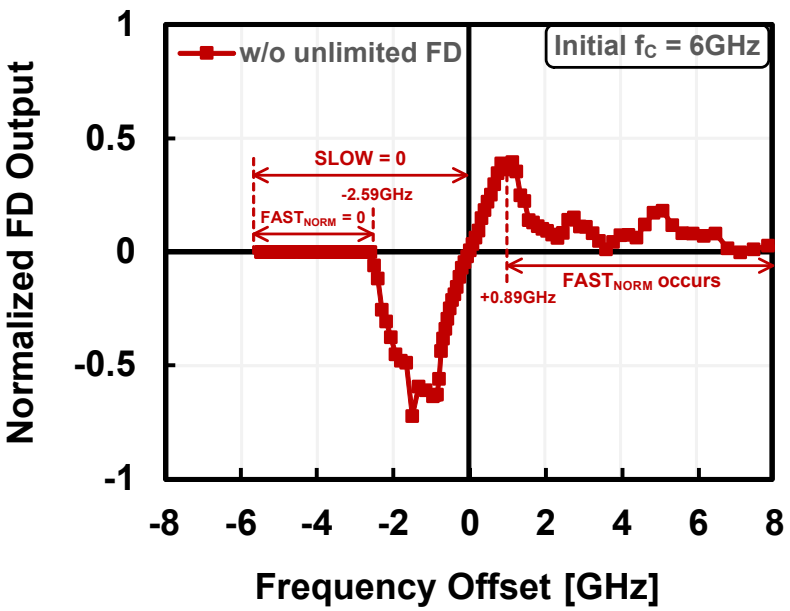


Fig. 4.9 Simulated open-loop response of multi-phase oversampling FD.

Therefore, the boundary frequency equals to 0.875 times the data rate. That is, if the clock frequency is lower than the boundary frequency, both FAST and SLOW occur and they move the loop in opposite directions. Then, frequency detection would be failed when the probability of generating FAST is comparable to that of generating SLOW.

To demonstrate the range boundaries we analyzed above, we simulated the open-loop FD response of the multi-phase oversampling FD as shown in Figure 4.9. The normalized FD output represents the difference between the probabilities of occurrence of SLOW and FAST. The initial DCO frequency is fixed to 6 GHz. With a negative offset, the FD output keeps a negative value until the frequency offset reaches −2.69 GHz. The boundary point is exactly same as the value that we derived in (4.4). When the frequency offset is a positive value, the FD gain increases until the offset reaches +0.89 GHz which is same as the value calculated using (4.7). After the point, FAST signal start to disturb the frequency detection. Finally, the frequency detection is failed if the frequency offset becomes larger.

4.3 Proposed Frequency Detector

4.3.1 Capture-Range Extension

In the previous section, we analyzed the causes of the capture-range limitation. Based on the causes, we can extend the capture range with some additional functions. We also explain the extension techniques divided into two cases of the negative offset and the positive offset.

First, when the clock frequency is higher than the data rate, the cause of the limitation is that the frequency detection signals are not detected, and it is because the LAG region becomes smaller as the clock frequency increases. Therefore, to overcome the limitation, we need to find other region which widens as the clock frequency increases. The suitable region is an inverse LAG (iLAG) region which detects the inverted UP signal as shown in Figure 4.10. It can be realized simply by adding inverters to the UP paths which will be explained in the next chapter.

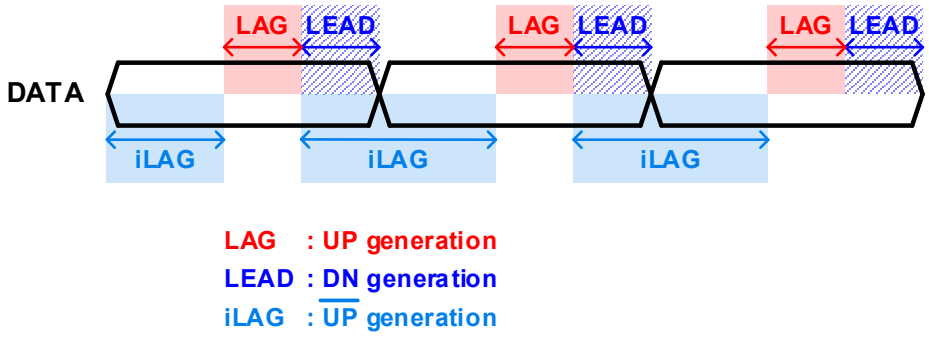


Fig. 4.10 Description of inverse LAG region.

On the other hand, in the case of the positive frequency offset, the cause of the limitation is that the both FAST and SLOW occur when the clock frequency is lower than 0.875 times the data rate. So, blocking FAST by SLOW can resolve the limitation. Figure 4.11 shows the same situation with Figure 4.10. By using FAST blocked by SLOW, only SLOW is generated and frequency detection is achieved. Since SLOW signal cannot be generated in the case of the negative frequency offset, this extension technique does not influence the opposite case.

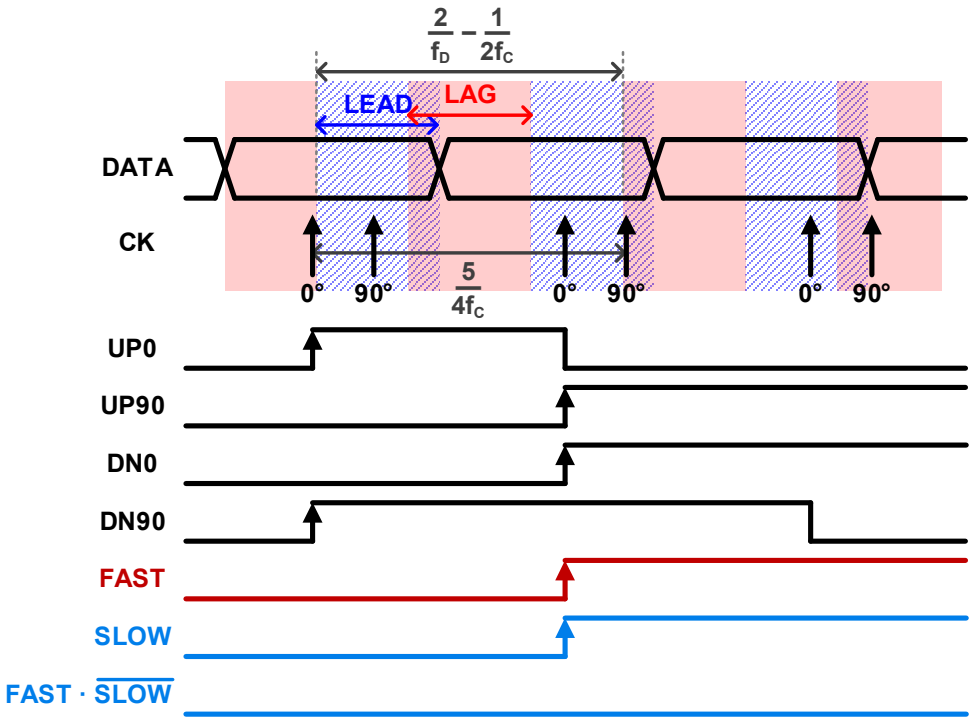


Fig. 4.11 Timing diagram showing capture-range extension in the case of positive frequency offset.

4.3.2 Frequency Detector with Unlimited Frequency Detection Capability

Figure 4.12 shows the block diagram of the proposed frequency detector which is realized based on the overcome techniques in Chapter 4.3.1. To achieve the unlimited frequency detection capability, additional blocks are added above the basic implementation of the multi-phase oversampling FD which is same as Figure 4.2. As shown in the right side of Figure 4.12, only two inverters, one flip-flop, and one AND gate are added. First, two inverters and one flip-flop are added to realize the extension technique with the negative frequency offset. Sampling the inverted UP0 by falling edges of UP90 generates the $FAST_{INV}$ signal.

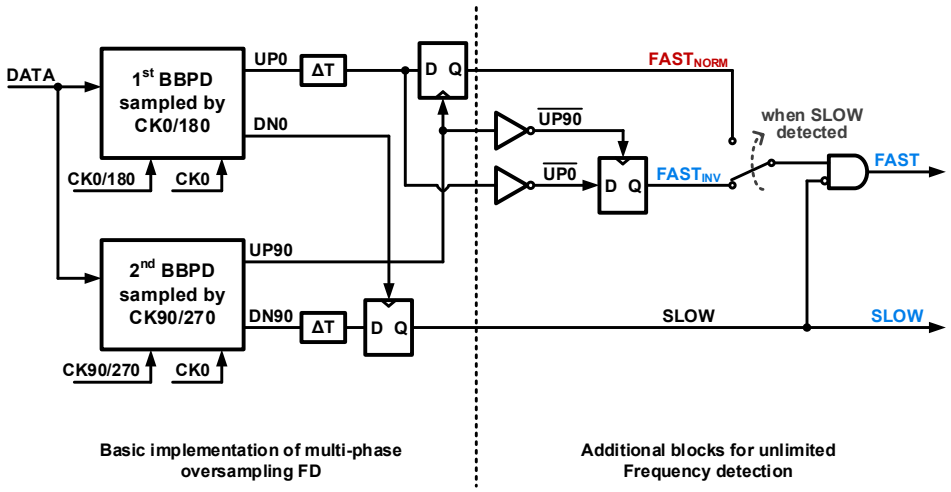


Fig. 4.12 Block diagram of proposed frequency detector with unlimited frequency detection capability.

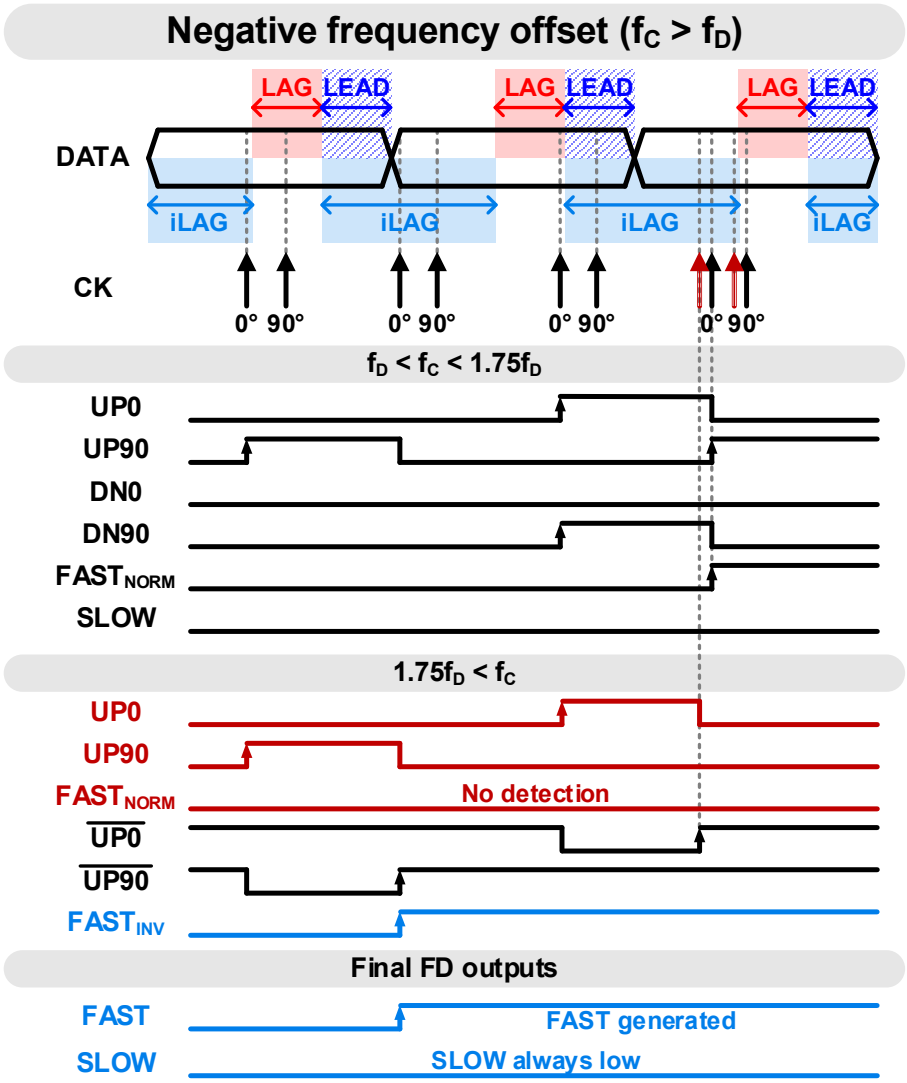


Fig. 4.13 Timing diagram showing FD operation with respect to range of negative frequency offset.

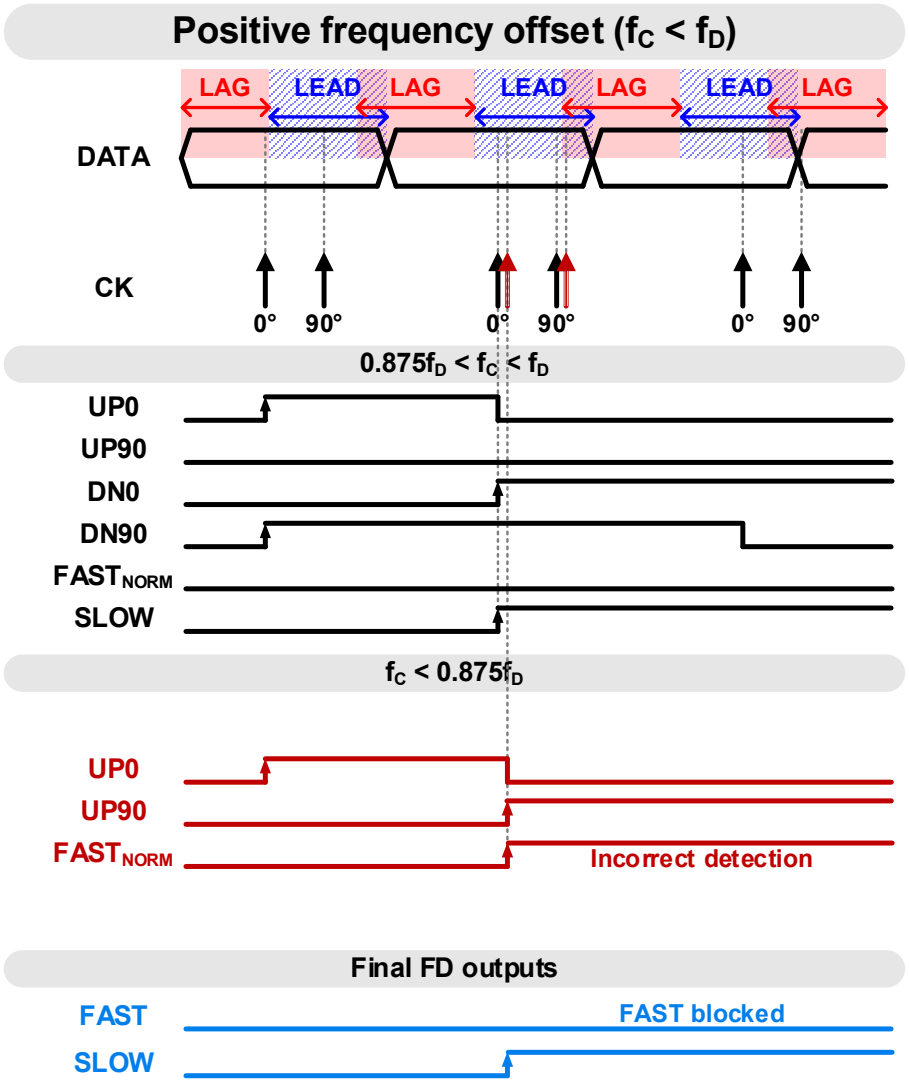


Fig. 4.14 Timing diagram showing FD operation with respect to range of positive frequency offset.

Unlike the generation of $FAST_{NORM}$, it uses the iLAG region, and thus the $FAST_{INV}$ signal can be detected even if the clock frequency is higher than 1.75 times the data rate. However, we should check the solution influences the opposite case. Using the $FAST_{INV}$ signal as the final FD signal will break the balance of the FD signals at the locking point. So, when the frequency lock is reached, it is required to switch the generation of FAST to the normal way. It can be realized by detecting the point that SLOW begins to occur. Therefore, we added a switching block into the FAST path. Next, one AND gate is added to realize the extension technique with the positive frequency offset. As we previously mentioned, the second solution does not influence the opposite case because SLOW cannot occur in the case of the negative frequency offset.

Figure 4.13 and Figure 4.14 summaries the capture-range limitation and extension of the proposed FD. They describes the FD operation with respect to the range of the frequency offset. As we discussed, the capture-range limitation is caused when the clock frequency is higher than 1.75 times the data rate and lower than 0.875 times the data rate. Utilizing the additional logic gates, the proposed FD can perform the frequency detection regardless the range of the frequency offset. Therefore, it achieves the unlimited frequency acquisition detection capability.

To demonstrate the capability, we simulated the gain curve of the proposed FD and compared with the result of the previous FD as shown in Figure 4.15. Unlike the FD without the additional functions, the proposed FD exhibits no capture-range limitation on a whole range of the frequency offset.

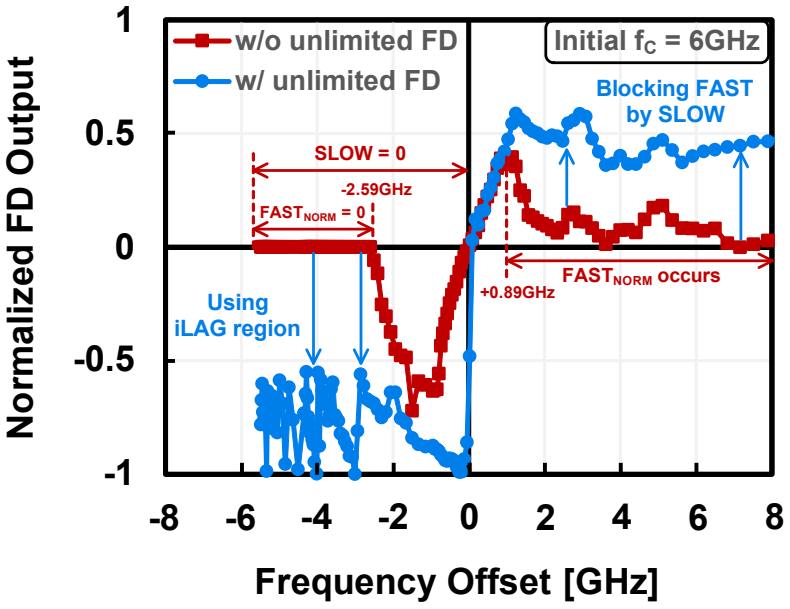


Fig. 4.15 Simulated open-loop response of proposed FD.

4.4 Circuit Implementation

4.4.1 Implementation of Digital CDR

Figure 4.16 illustrates the schematic of the proposed referenceless digital CDR. To alleviate the speed limit of the samplers, a half-rate architecture is adopted and, accordingly, an 8-phase clock is used for frequency acquisition. The CDR is composed of eight data/edge samplers, 2:16 deserializers, a digitally controlled oscillator

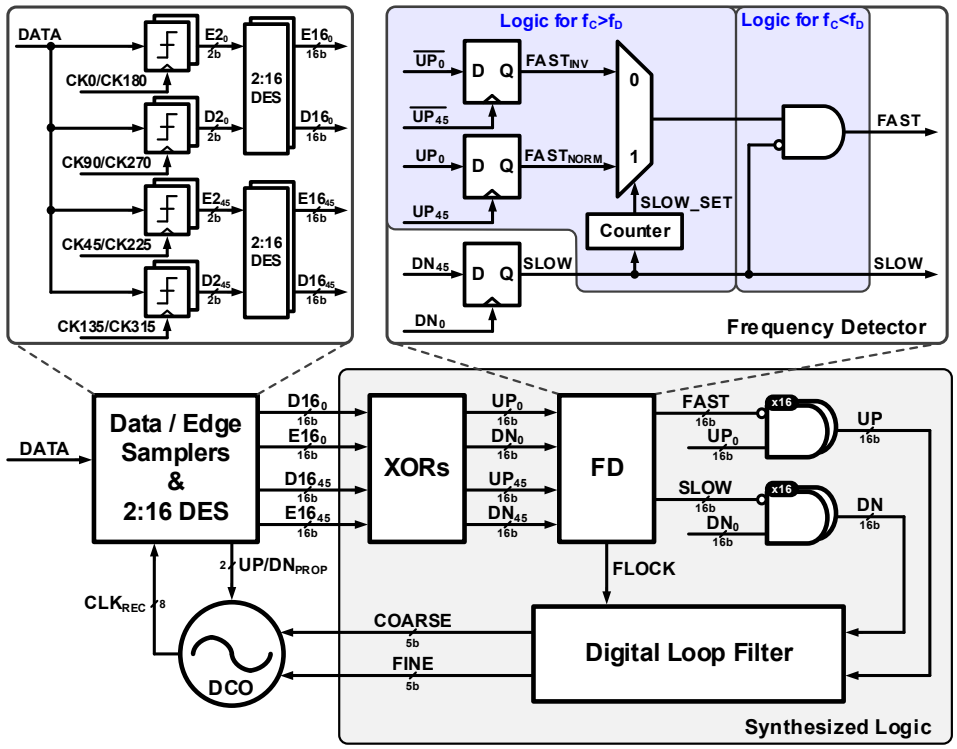


Fig. 4.16 Schematic of proposed referenceless CDR with unlimited FD.

(DCO), and synthesized logic gates for both frequency and phase acquisitions. In the synthesized logic gates, UP_0, DN_0, UP_{45}, and DN_{45} are generated by XORing the deserialized data/edge samples, and mutual samplings of the UP/DN signals generate the frequency detection signals. The additional logic gates for the unlimited capture range are implemented in the FD. A flip-flop, a multiplexer (MUX), and a counter of SLOW are added to detect the negative frequency offset. Depending on whether the counted value exceeds a threshold or not, the MUX selects between $FAST_{INV}$ and $FAST_{NORM}$. Blocking FAST by SLOW for detecting the positive frequency offset is realized by an AND gate. As a result, the final FAST and SLOW directly constrain the UP/DN paths to a digital loop filter (DLF), and frequency acquisition is achieved. When frequency lock is reached, neither FAST nor SLOW is generated and the normal UP/DN signals control the loop. To control the loop gain, a lock detection signal, FLOCK, is generated by counting the consecutive 0's of UP0 and DN0. The DCO frequency is controlled by an integral path from the DLF and a direct proportional path from the samplers. A segmented thermometer code is employed to control the integral path [68].

4.4.2 Digitally-Controlled Oscillator

As shown in Figure 4.17, the DCO consists of a digitally-controlled resistor (DCR), delay elements with varactor loads, and level shifters for full-swing outputs. A pseudo-differential inverter-based ring oscillator is used and it has a four-stage structure to generate multi-phase clocks for the proposed FD. The DCO frequency is controlled by the integral path and the direct proportional path. In the integral path, a segmented thermometer control alters the row and column cells of the DCR. The phase errors from the BBPD and the proportional gain are fed to the varactors to change the DCO frequency instantly.

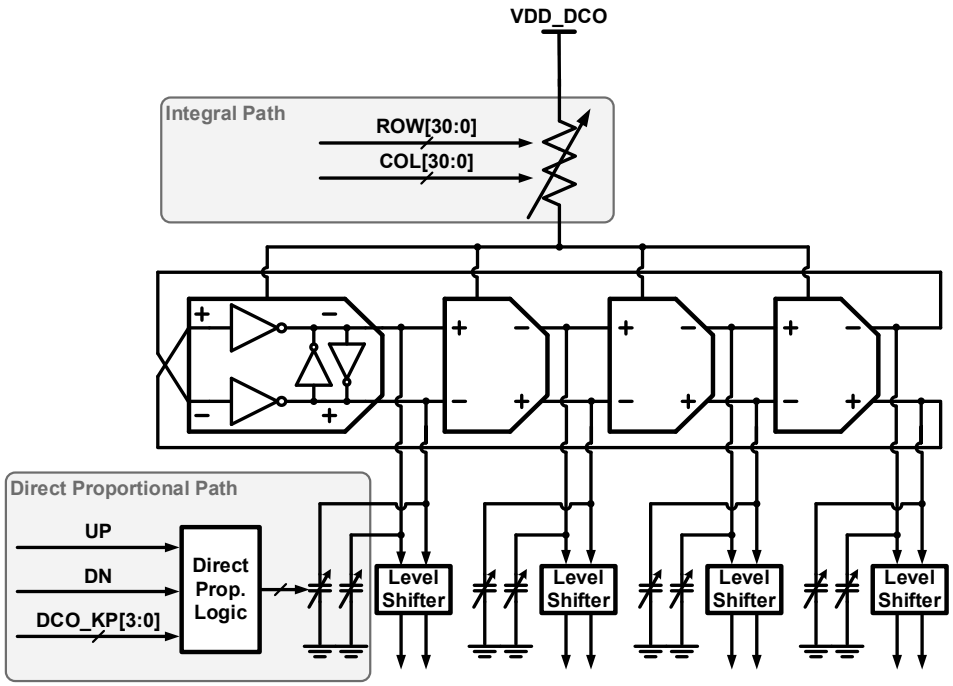


Fig. 4.17 Block diagram of DCO.

4.4.3 Frequency Lock Detector

Figure 4.18 shows the digital implementation of the frequency lock detector which is included in the DLF. The purpose of the lock detector is controlling the loop gain in the two states, frequency locking state and phase-locked state. When the frequency lock is reached, the clock phase drifts near the locking point and CK0 is located in either LAG region of LEAD region during several cycles. That means, either UP signal or DN signal keeps low in the cycles. Therefore, we can detect the frequency-locked state by counting the consecutive 0's of UP signal and DN signal. Thanks to the gain control, the proposed CDR can achieve fast frequency acquisition. However, too large gain in frequency locking state can lead to lock-detection failure, which is similar to the issue of the pump current size explained in Chapter 3.3.3.

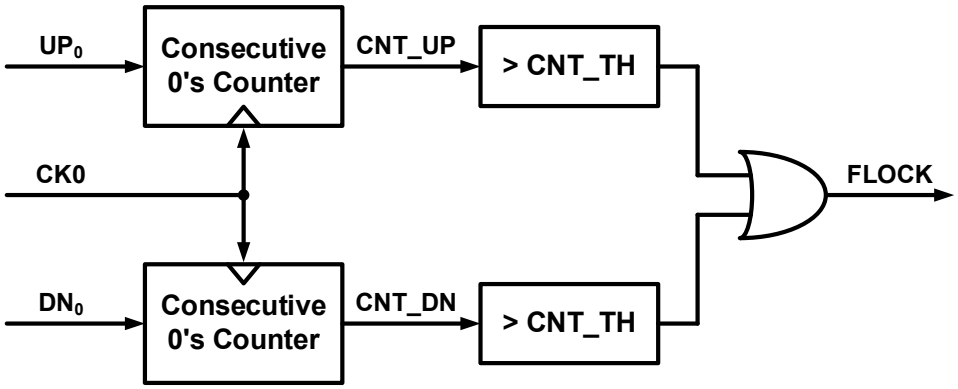


Fig. 4.18 Block diagram of frequency lock detector.

4.5 Measurement Results

The prototype CDR has been designed and fabricated in a 65 nm CMOS technology. The chip photomicrograph is shown in Figure 4.19 with the active area of 0.045 mm^2 excluding output buffers. All the blocks use a 1.2-V supply. In the measurement setup shown in Figure 4.20, the Signal Quality Analyzers (Anritsu MP1800A) generates a PRBS31 pattern for the input data and its swing is 300 mV. For the jitter tolerance measurement, the recovered data is fed back to the error detector of the Signal Quality Analyzers. The recovered clock is monitored by the oscilloscope

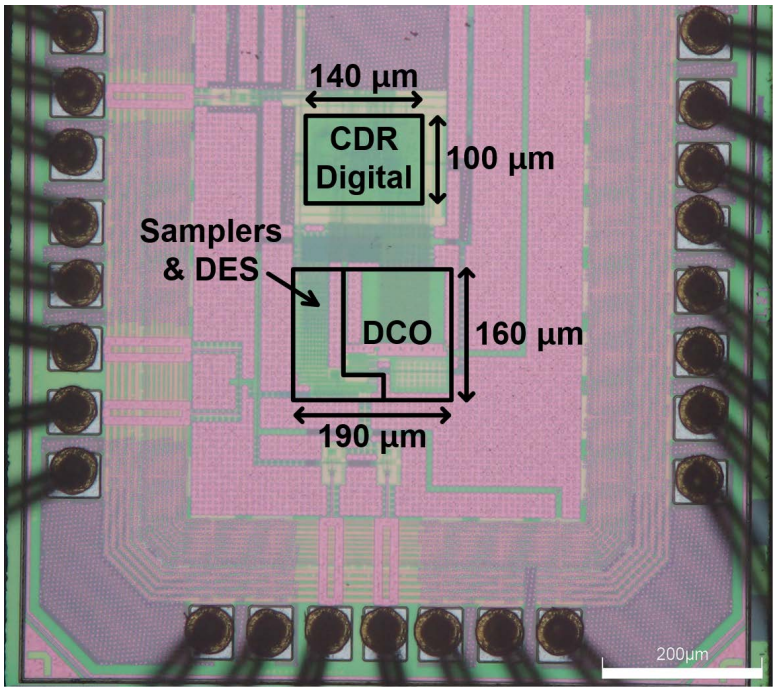


Fig. 4.19 Chip photomicrograph and block description.

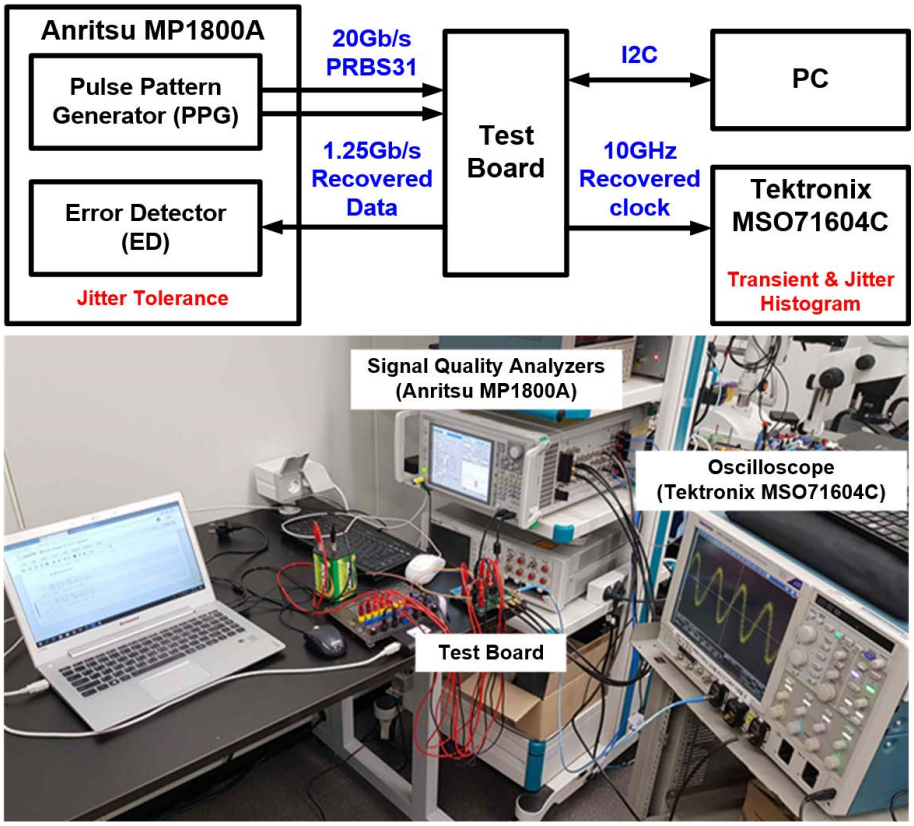
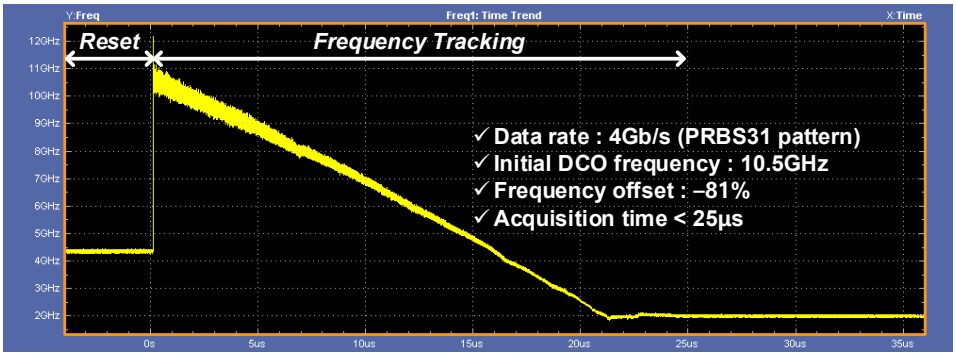


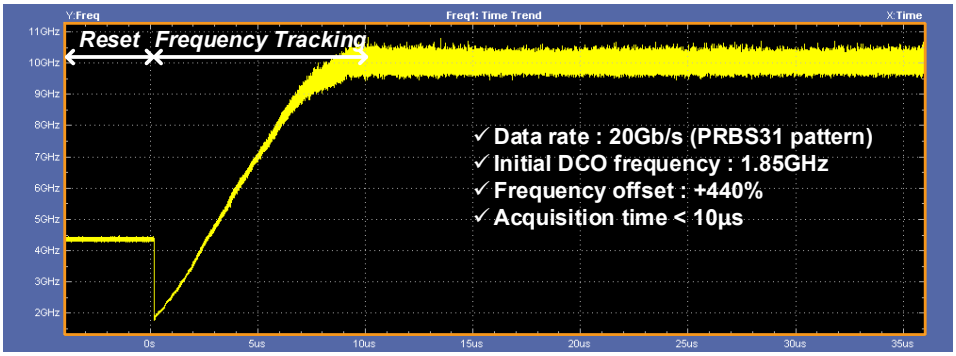
Fig. 4.20 Measurement setup.

(Tektronix MSO71604C). Using the oscilloscope, we can measure the frequency tracking behaviors and the jitter histograms of the recovered clock.

First, we will see the measurement results showing the performance of the proposed frequency acquisition scheme. As shown in the simulated FD curve in Chapter 4.3.2, the proposed FD has an unlimited frequency detection capability. To demonstrate it, we measured frequency tracking behaviors with various data rates and initial DCO frequencies. Figure 4.21 shows the transient results before post-processing for two cases corresponding to maximum negative and positive frequen-



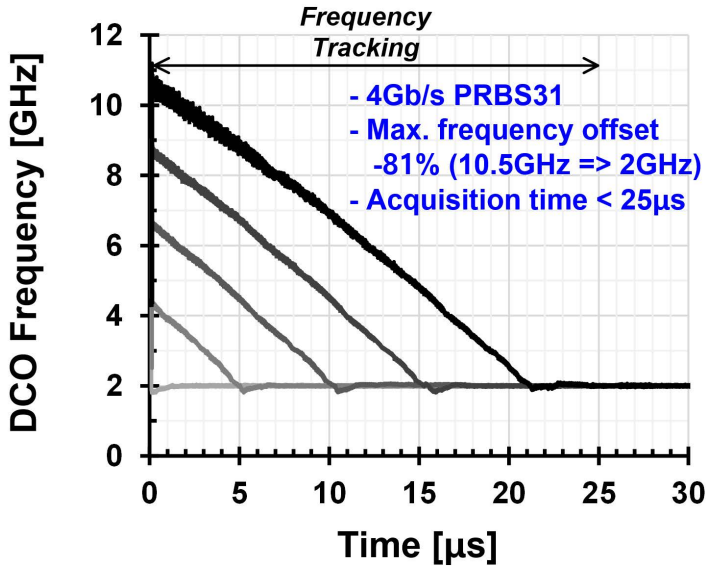
(a)



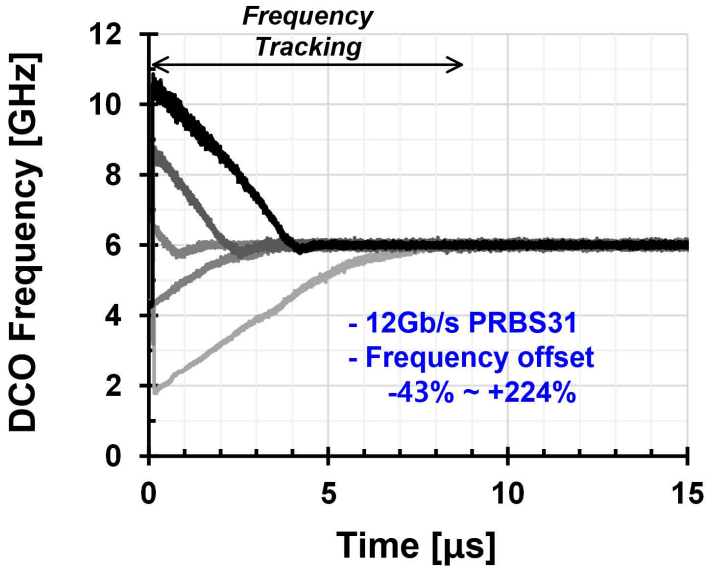
(b)

Fig. 4.21 Measured frequency acquisition behaviors before post-processing for two cases corresponding to (a) maximum negative frequency offset and (b) positive frequency offset.

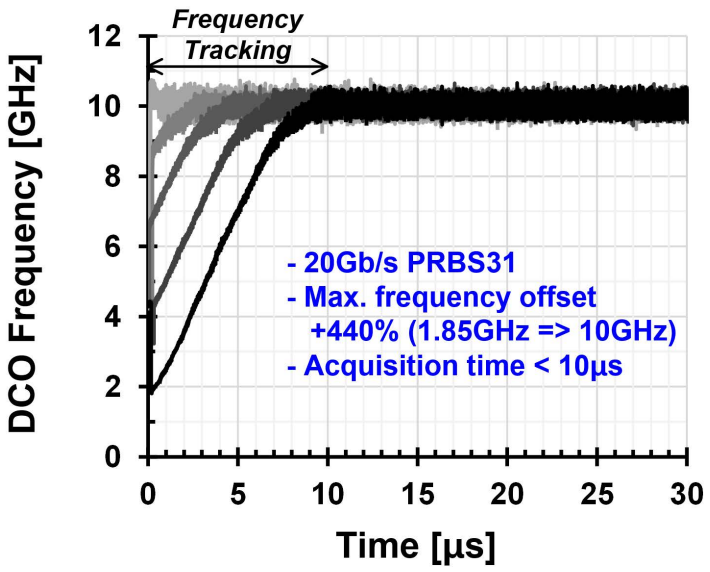
cy offset. In Figure 4.21(a), the data rate is 4 Gb/s, the initial DCO frequency is 10.5 GHz, and the frequency offset is −81 %. In Figure 4.21(b), the data rate is 20 Gb/s, the initial DCO frequency is 1.85 GHz, and the frequency offset is +440 %. As we designed, if there is a frequency offset, the DCO frequency moves to the direction of reducing the offset, and when approaching the data rate, the phase detection is performed. In order to show various results at once, we post-processed the measured transient results as shown in Figure 4.22.


Frequency
Tracking
- 4Gb/s PRBS31
- Max. frequency offset
-81% (10.5GHz => 2GHz)
- Acquisition time < 25µs
DCO Frequency [GHz]
Time [µs]
0
2
4
6
8
10
12
0
5
10
15
20
25
30

(a)


Frequency
Tracking
- 12Gb/s PRBS31
- Frequency offset
-43% ~ +224%
DCO Frequency [GHz]
Time [µs]
0
2
4
6
8
10
12
0
5
10
15

(b)



(c)

Fig. 4.22 Measured frequency acquisition behaviors with varying initial DCO frequency for data rate of (a) 4 Gb/s, (b) 12 Gb/s, and (c) 20 Gb/s.

The results in Figure 4.22 are measured with any initial frequency in the DCO operating range for three data rates. Unlike the results of the previous works shown in Chapter 4.1, the proposed FD achieves the frequency detection regardless of the initial DCO frequency. Therefore, the startup procedure to set the initial frequency within the capture range is not required and there is no problem if the frequency lock is released by an external factor. Based on the frequency acquisition behaviors, the measured acquisition time versus the frequency offset is shown in Figure 4.23. The worst-case acquisition times for the data rates of 4 Gb/s, 12 Gb/s, and 20 Gb/s are 25 µs, 9 µs, and 10 µs, respectively.

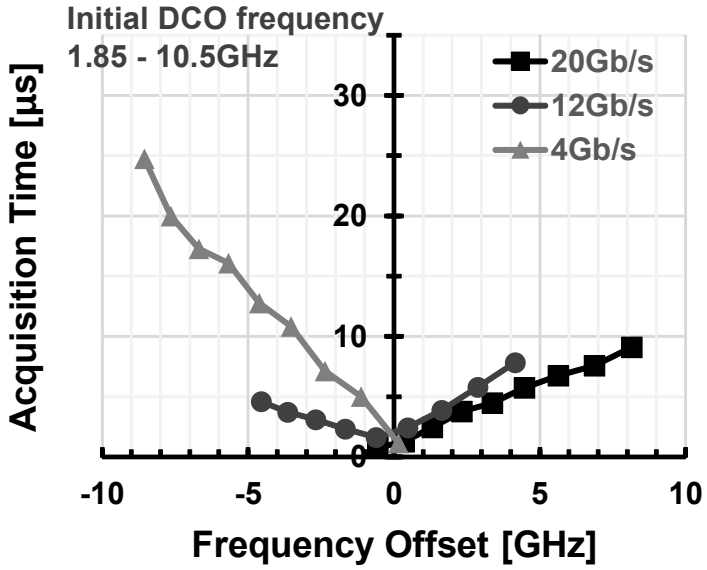


Fig. 4.23 Measured acquisition time versus frequency offset at data rate of 4 Gb/s, 12Gb/s, and 20Gb/s.

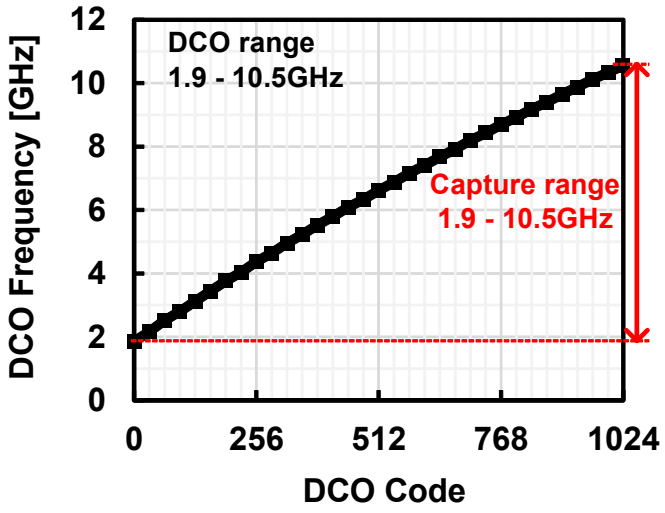
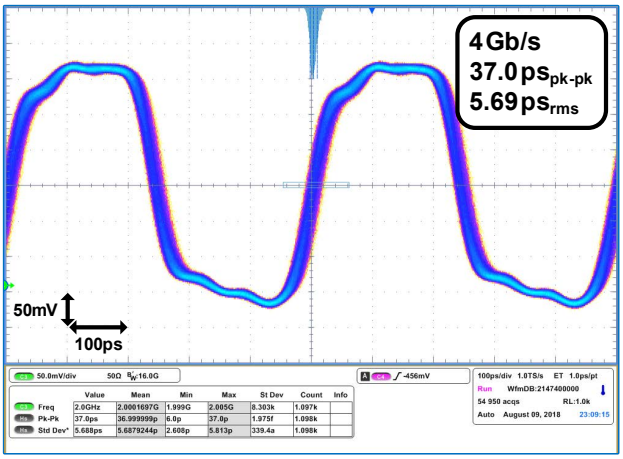
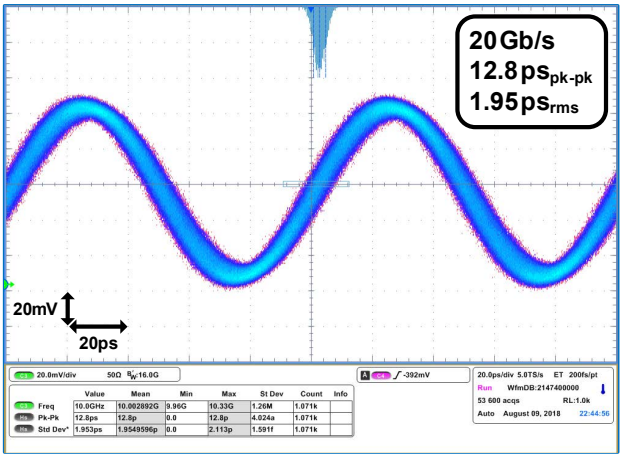


Fig. 4.24 Measured DCO gain curve.

Next, we will exhibit the measurement results showing the performance of the proposed CDR. The CDR consumes 37.3 mW at 20 Gb/s and the measured capture range is from 4 Gb/s to 20 Gb/s which is limited by the operating frequency of the DCO, neither by the frequency detection capability nor the initial DCO frequency.



(a)



(b)

Fig. 4.25 Measured jitter histogram of recovered clock at (a) 4 Gb/s (b) 20 Gb/s.

Figure 4.24 shows the measured DCO gain curve and the operating range of the DCO is from 1.9 GHz to 10.5 GHz which limits the capture range. The DCO gain curve shows a great linearity thanks to the size optimization of the DCR cells. The constant DCO gain is critical because the proposed CDR operates in a wide range.

Figure 4.25 shows the measured jitter histogram of the recovered clock at the boundary points of the capture range. The clock jitters are measured with the external jitter source disabled. At the data rate of 20 Gb/s, the measured RMS and peak-to-peak jitters are 1.95 ps and 12.8 ps, respectively. Figure 4.26 shows the measured jitter tolerance of the proposed referenceless CDR. The jitter tolerance is measured with a 20 Gb/s input data at 10^{-12} BER. At the jitter frequency lower than 30 MHz, the CDR exceeds the maximum jitter limit of the test equipment. The jitter tracking bandwidth is about 100 MHz and the jitter tolerance at high frequency is 0.42 UI.

Table 4.1 compares the performance of the proposed referenceless CDR with the state-of-the-art designs. This design offers the widest capture range and the lowest FOM. Furthermore, even with a large frequency offset, the CDR achieves fast frequency acquisition.

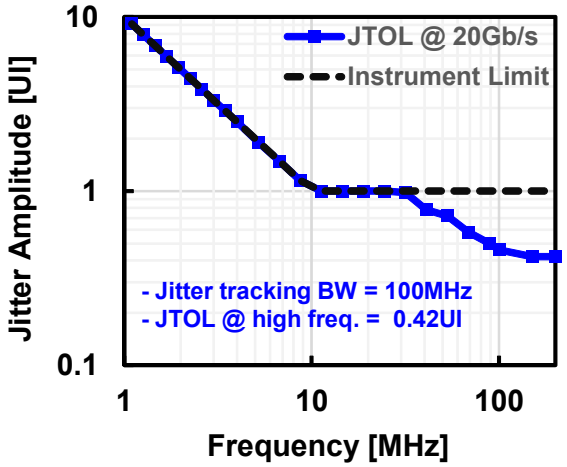


Fig. 4.26 Measured jitter tolerance at 20 Gb/s (BER < 10^{-12}).

Table 4.1 Performance summary and comparison

	JSSC 16 [9]	ISSCC 16 [10]	ISSCC 17 [19]	JSSC 18 [41]	This work
Technology	65nm	28nm	28nm	65nm	65nm
Supply [V]	1.2/1.0	0.9	0.9	1.3	1.2
Architecture	Half-rate	Half-rate	Baud-rate	Half-rate	Half-rate
Data Pattern	PRBS7	PRBS9	PRBS31	PRBS31	PRBS31
Data Rate [Gb/s]	4–10.5	7.4–11.5	22.5–32	6.7–11.2	4–20
Capture Range [%]	65	41	34	50	**133**
Initial Frequency Calibration	Required	Required	Required	Required	**Not Required**
Acquisition Time [µs]	<600 (+58% offset)	<18 (+29.5% offset)	<5500 (-19.6% offset)	<0.54 (-25% offset)	<25 (-81% offset)
			<10100 (+14.3% offset)	<2.19 (+25% offset)	<10 (+440% offset)
Area [mm^2]	1.63	0.21	0.213	0.047	0.045
Power [mW]	22.5 @10Gb/s	22.9 @11.5Gb/s	102 @32Gb/s	22.5 @10Gb/s	37.3 @20Gb/s
FOM [pJ/b]	2.25	1.91	3.19	2.25	**1.87**

Chapter 5

Conclusion

In this thesis, design techniques of wide-range CDR with a referenceless operation are proposed. To utilize the advantage of a single-loop architecture, the first version employs a compact frequency acquisition scheme using a multi-phase oversampling PFD which detects the drift direction of the multi-phase clock. The proposed scheme achieves the wide capture range and the fast acquisition time with a small hardware overhead. The capture range and the phase mismatch effect of the proposed scheme are analyzed, and the acquisition time is calculated. Through the measurement results of the frequency behaviors, the analysis of the range of the safe initial frequency is verified, and the capture range is measured to be 50%. The proposed CDR shows the fastest acquisition time of 2.19 μs compared with other referenceless CDRs, while achieving an energy efficiency of 2.25 pJ/bit.

Advanced from the first version, the second version achieves an unlimited frequency detection capability regardless of the initial oscillator frequency. Based on

the detailed capture-range analysis of the multi-phase oversampling scheme, a frequency detector with additional logic gates is proposed and its frequency detection curve shows the unlimited capability. Due to the digital implementation, a lock detector is easily added to control the loop gain for fast locking. The prototype chip has been fabricated in a 65-nm CMOS process. The proposed CDR achieves the widest capture range of 4-to-20 Gb/s and the lowest FOM of 1.87 pJ/b compared with the state-of-the-art designs.

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초 록

본 논문에서는 다중 위상 오버샘플링 주파수 검출 방식 (multi-phase oversampling frequency detection)을 이용하여 기준 클락이 없는 시스템 (referenceless system)에서 사용될 클럭 및 데이터 복원회로 (clock and data recovery)를 설계하는 방법을 제안한다. 기존 방식들과 비교하여 포획범위, 파워, 추적시간 세가지 성능에서 이점을 가지는 새로운 방식을 제안한다. 제안한 뱅뱅 위상-주파수 검출기 (bang-bang phase-frequency detector)는 다중 위상 클럭과 데이터와의 상대적인 위상 이동방향을 감지하여 주파수 차이를 검출한다. 제안하는 방식의 포획범위, 추적시간에 대한 이론적인 분석을 통해 나온 결과를 시뮬레이션과 측정을 통해 검증하였다. 65nm CMOS 공정을 이용하여 만들어진 칩은 10 Gb/s 에서 22.5 mW 의 파워를 소모하고 0.047 mm^2의 면적을 차지한다. PRBS31 패턴을 이용하여 측정되었고 포획범위는 6.7 Gb/s 에서 11.2 Gb/s 까지이고 추적시간은 2.19 μs 보다 작다. 제안하는 클럭 및 데이터 복원회로는 비트에러율 10^{-12} 이하 기준에서 문제없는 동작을 보여주었다.

앞선 버전에서 발전하여, 제한 없는 주파수 검출 능력을 가지는 클럭 및 데이터 복원회로를 제안한다. 동일하게 다중 위상 오버샘플링 주파수 검출 방식을 기반으로 하였고 추가적인 기능을 통해 포획범위 제한을 없애게 되었다. 또한, 초기 주파수 조건에 상관없이 주파수 검출이 가능하다. 65nm CMOS 공정을 이용하여 만들어진 칩은 20 Gb/s 에서 37.3 mW 의 파워를 소모하고 0.045 mm2 의 면적을 차지한다. PRBS31 패턴을 이용하여 측정되었고 포획범위는 4 Gb/s 에서 20 Gb/s 까지이고 이는 단지 발진기의

동작범위에 의해 제한되었다. 그 범위에서의 추적시간은 25 μs 보다 작다.

주요어 : 다중 위상 오버샘플링, 뱅뱅 위상-주파수 검출기, 클럭 및 데이터 복원회로, 주파수 검출기, 위상동기루프, 기준 클락 없는 시스템, 제한 없는 주파수 검출.

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