Ph.D. Dissertation

A Study on Combined Equalization and Timing Recovery for High Speed Links

고속 데이터 전송을 위한 결합된 방식의 이퀄라이제이션과 타이밍 복구 방법에 관한 연구

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A Study on Combined Equalization and Timing Recovery for High Speed Links

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Abstract

A rapid growth of data rates in high speed links application makes it difficult to maintain low bit-error rates (BERs) while communicating data across channels with limited bandwidths. The key enabler for high bandwidth input/output (I/O) links is improving both equalization and timing recovery ability. However, the undesired interaction between equalization and timing recovery which are accomplished through two different control loops results in degradation in performance and power efficiency. To avoid this negative phenomenon, this thesis presents combined equalization and timing recovery for high speed links. First, a receiver with a combined adaptation for separated equalization and timing recovery loops is designed. To find and maintain both an optimal set of coefficients for the equalizers and timing for CDR that minimizes the BER, a two-step adaptation algorithm employing single-bit response (SBR) measurements and stochastic hill climbing algorithm are presented. Second, this thesis presents an effective way to combine adaptive equalization and timing recovery in a single control loop using fractionally spaced equalizer (FSE). To additionally support plesiochronous clocking, the presented work realizes an infinite-range timing recovery using a set of two FSEs to cover different half-UI periods and the selection is seamlessly switched between the two. The timing recovery ability of fractionally spaced equalizer is analyzed and its equivalent timing-recovery loop model is derived as first order bang-bang controlled delay locked loop (DLL). A current-integrating summer

and multi-input regenerative latch help the 4-tap FSEs and 3-tap decision feedback equalizers (DFEs) achieve low power dissipation, respectively. A prototype receiver fabricated in a 28-nm CMOS consumes 3.5pJ/bit and 0.10mm^2 at 9Gb/s, while compensating for a 22-dB channel loss and 100ppm frequency offset between the transmitted data and blind sampling clocks.

Keywords : adaptive equalizer, clock and data recovery (CDR), decision-feedback-equalizer, fractionally spaced equalizer, receiver, wireline, high speed links

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Chapter 1.

Introduction

1.1. Motivation

Advances in CMOS process technology have led to a rapid growth of data rates in high speed links application (Figure 1.1), which makes it difficult to maintain low bit-error rates (BERs) while communicating data across channels with limited bandwidths (Figure 1.2, 1.3). Frequency dependent channel loss results in significant inter-symbol interference (ISI), which lowers the BER and degrades power efficiency. The channel loss also makes it difficult to recover timing owing to large data-dependent jitter (DDJ). Therefore, the key enabler for high bandwidth for high speed links is improving both equalization and timing recovery ability.

Also, the low power dissipation of a high-speed I/O transceiver is a key requirement in enabling large-scale integration of high-speed I/O links on a single chip and supporting a high off-chip I/O bandwidth. Because the data rate per pin also has to increase in order to meet this level of bandwidth demand, various channel equalization techniques are employed to compensate for the

presence of inter-symbol interference (ISI). However, many circuit elements, including continuous-time linear equalizers (CTLEs) and decision-feedback equalizers (DFEs), incur power losses. Therefore, system designers have to find a compromise between the total I/O bandwidth and system power dissipation.

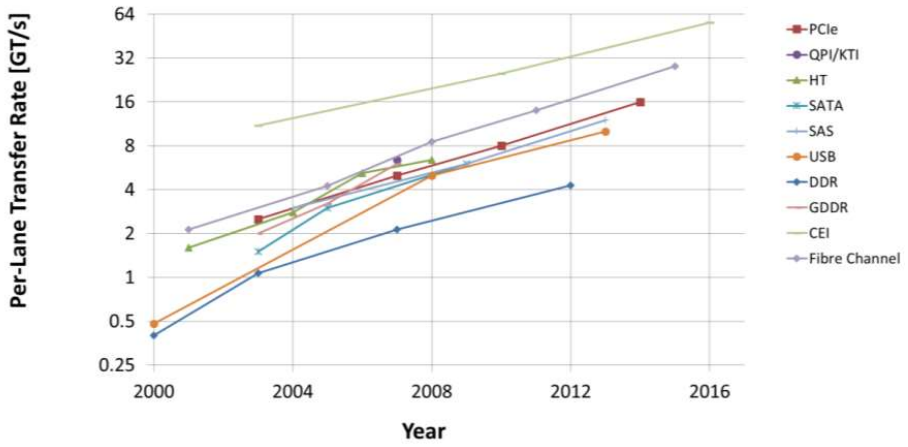


Figure 1.1: Per-pin data rate vs. Year for a variety of common I/O standards which is reported in ISSCC 2017 trends.

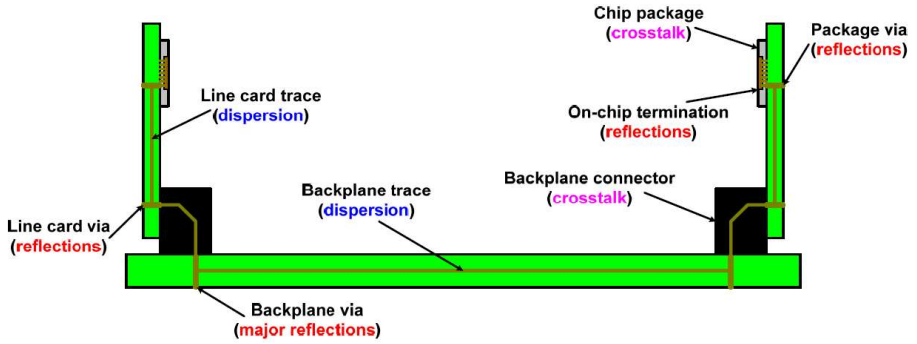
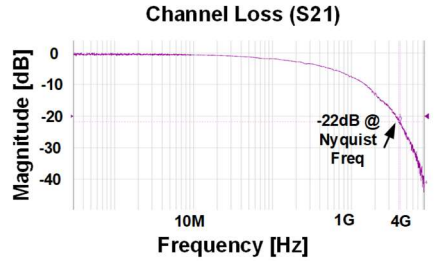
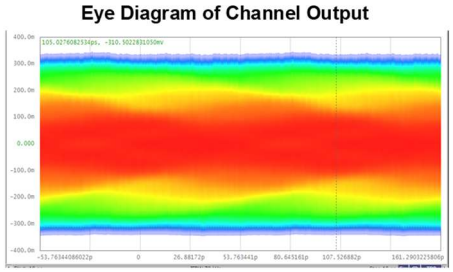


Figure 1.2: Backplane channel configuration.



(a)



(b)

Figure 1.3: (a) 25-inch FR4 channel loss and (b) its eye diagram.

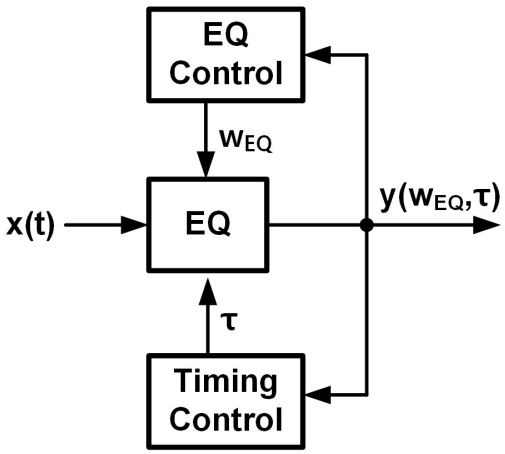


Figure 1.4: Conventional separated equalization and timing recovery.

In general, equalization and timing recovery are accomplished through two different control loops [1–3], as shown in Figure 1.4, which makes it necessary to consider possible interaction between the two. In these architectures, equalization and timing recovery are usually controlled to improve the voltage and timing margins, respectively. This separate feedback loops which uses different error metric may have undesired interaction and results in performance degradation. Previous works [4-6] reported that there can exist a situation where a timing adjustment made by the timing control loop results in sup-optimal equalizer tap coefficients (w_{EQ}), while an adjustment of the equalizer tap coefficients (w_{EQ}) by the equalization control loop results in a sup-optimal sampling timing (τ). Therefore, this undesired interaction between the equalization and timing

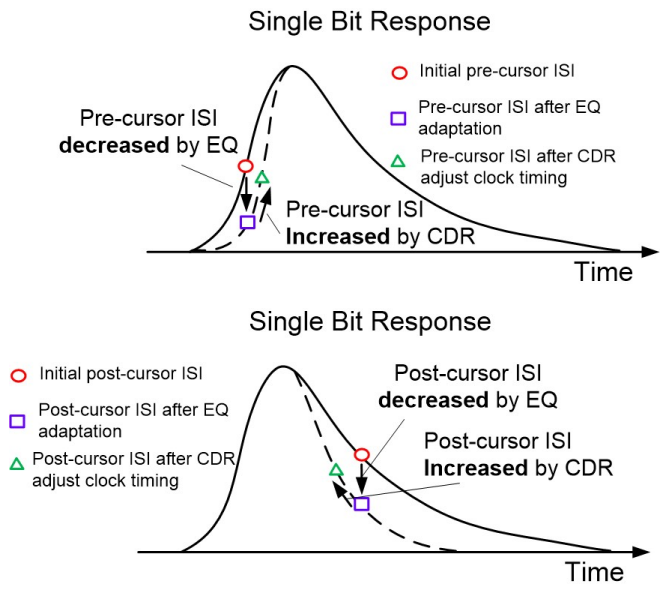


Figure 1.5: The undesirable interaction between the CDR and equalizer which changes the ISI in the opposite direction.

recovery results in degradation in performance and power efficiency. In particular, it was reported that this negative phenomenon is more pronounced when the channel has asymmetric ISIs [4].

The CDR and adaptive equalizer are supposed to act on the orthogonal metrics, the timing error and voltage error, respectively. However, many practical receivers having feedforward equalizers (FFE) and/or decision-feedback equalizers (DFE) along with the clock-and-data recovery circuits (CDR) such as 2× oversampling or baud-rate sampling CDRs exhibit undesirable interactions between the two, resulting in sub-optimal performance. The reason is that the FFE/DFE usually uses voltage error to make ISI zero ($h[k] = 0$ for $k \neq 0$, where $h[k]$ is single bit response). On the other hand, CDR usually uses timing error and aims to make the timing error zero ($h[-0.5] = h[0.5]$ for 2x oversampled

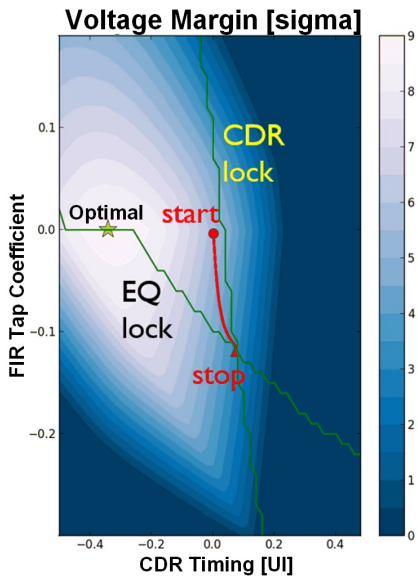


Figure 1.6: Contour plot of voltage margin with 1-tap FIR coefficient and CDR timing and its locking behavior (red line).

edge-equalized CDR and h [-1] = h [1] for Mueller-Muller CDR). Figure 1.5 illustrates the negative interaction between the CDR and the equalizer which makes ISI in opposite direction. Any timing adjustments made by the CDR change the ISI measured at each data sampling points, making the equalizer tap coefficients sub-optimal. On the other hand, any adjustments made by the adaptive equalizer change the timing of the equalized data, rendering the CDR's timing sub-optimal. Figure 1.6 shows contour plot of voltage margin when there are 1-tap FIR equalizer and 2x oversampled CDR. The locking behavior of equalizer coefficients and CDR timing shows they eventually locked in sub-optimal state.

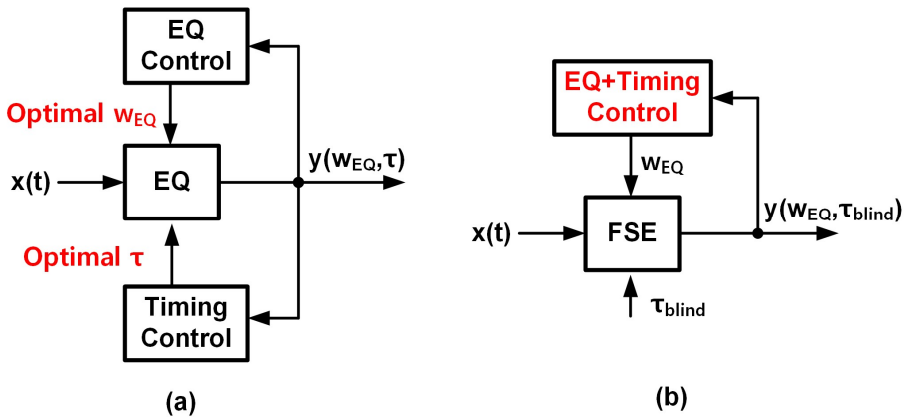


Figure 1.7: (a) A combined adaptation for separate equalization and timing recovery loops to maintain both the optimal CDR timing and the optimal EQ coefficients; (b) combined equalization and timing recovery using a fractionally spaced equalizer (FSE).

1.2. Thesis Contribution and Organization

This thesis presents receiver designs with combined equalization and timing recovery to avoid the undesired interaction between equalization and timing recovery. Also, the thesis presents various low power techniques for architecture and circuit implementation for lower power dissipation.

First, in Chapter 2, a combined adaptation algorithm for separate equalization and timing recovery loops is presented to maintain both the optimal timing for the CDR and the optimal tap coefficients for the adaptive equalizer (Figure 1.7(a)). A two-step adaptation algorithm that finds the equalizer coefficients and CDR timing which minimizes the BER is described. An extra data sampler with adjustable voltage and timing offsets measures the single-bit response (SBR) of the channel and coarsely tunes the initial coefficient values in the foreground. Next, the same circuit measures the eye-opening and bit-error rates and fine tunes the coefficients in background using a stochastic hill-climbing algorithm. The circuit designs for low-power dissipation are implemented and measurement result are demonstrated for prototype receiver chip design.

Second, in Chapter 3 and 4, a combined equalization and timing recovery using fractionally spaced equalizer (FSE) is presented. The FSE can combine equalization and timing recovery in a single control loop, as shown as shown in Figure 1.7(b). A 2× blind-oversampling FSE receiver is designed to support infinite-range timing recovery for plesiochronous systems. In Chapter 3, an analysis on combined equalization and timing recovery of FSE explains why

FSE has a timing recovery ability and derives its equivalent CDR model. In Chapter 4, the proposed FSE receiver is designed and the architecture and circuit implementation are explained. It uses a set of two FSEs having a 0.5-UI shifted timing relationship, one of which is selected to recover the data. While each FSE has a limited timing recovery range, an infinite range of timing recovery is enabled by using the two FSE alternately. Also, the measurement results is demonstrated.

The proposed FSE receiver for combined equalization and timing recovery was fabricated in a 28-nm CMOS and successfully operates at 8.3~9.1 Gb/s with a 100-ppm frequency offset between the data and blind sampling clocks. The receiver consumes 3.5pJ/bit of power and 0.10 mm^2 of area, and can compensate for up to 22-dB of channel loss at 4.5 GHz with a 0.2-UI_{pp} high-frequency jitter tolerance (JTOL) for a BER of less than 10^{-12}. The measurement results show that the proposed design achieves the goal of this dissertation, which is to adopt combined equalization and timing recovery for high speed links.

Chapter 2.

Design of Low Power Receiver with Combined Adaptation for Separated Equalization and Timing Recovery loops

This chapter presents a combined adaptation algorithm for separated equalization and timing recovery loops to maintain both the optimal timing for the CDR and the optimal tap coefficients for the adaptive equalizer (Figure 1.7(a)). A low-power equalizing receiver front-end is designed and it achieves a very low power efficiency of 0.46mW/Gbps. To achieve high energy efficiency, this receiver was enabled by judiciously combining multiple equalization techniques, in this case a one-tap FIR DFE, an IIR DFE, and a CDR timing offset adjustment, as presented in [6, 7]. Also, to find an optimal set of coefficients for such a heterogeneous equalizer and timing for CDR that minimizes the BER, a two-step adaptation algorithm employing single-bit response (SBR) measurements and eye-opening/BER measurements is presented.

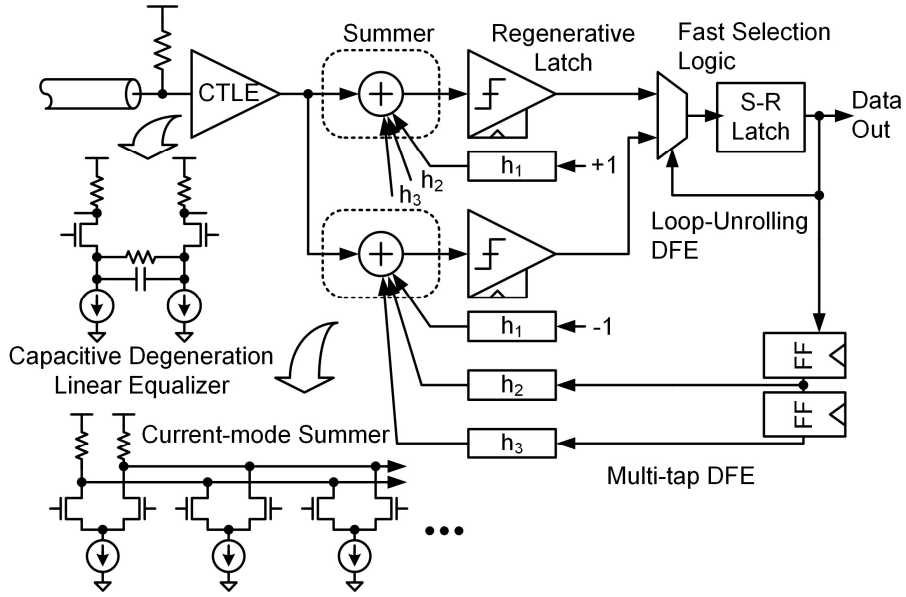


Figure 2.1: Common power-consuming circuit elements in backplane high-speed receivers (e.g., [8-10]): a current-mode summing circuit for multi-tap DFE, a fast digital logic for loop-unrolling DFE, and a continuous-time linear equalizer (CTLE).

2.1. Receiver Architecture

Figure 2.1 identifies the circuit blocks which have a tendency to consume a large amount of power in the existing backplane equalizing receiver designs [8-10]. First, the fast digital logic used in the loop-unrolling DFE receivers is one such block. A loop-unrolling DFE alleviates the stringent timing requirement in the DFE feedback path by moving the feedback loop entirely into the digital domain. That is, the DFE computes both the possible outcomes without the

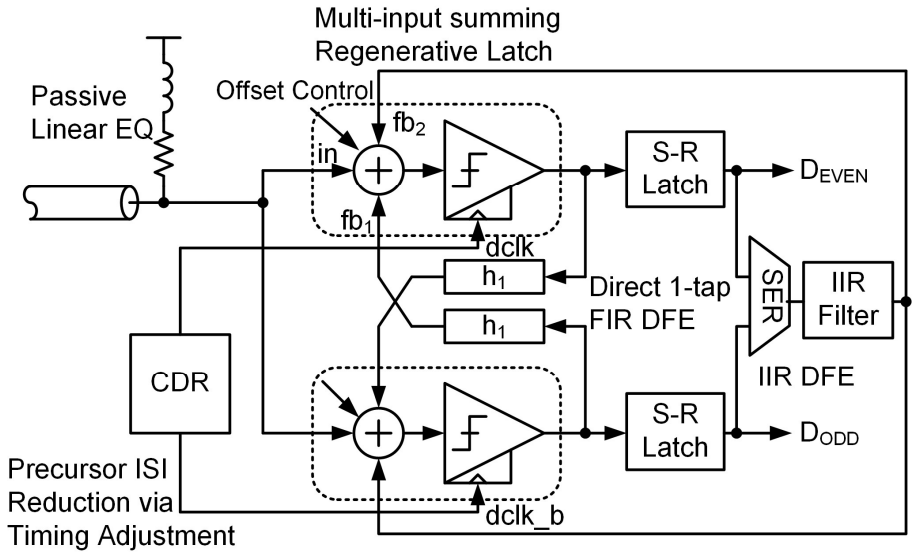


Figure 2.2: The proposed DFE receiver front-end with three ISI-reduction schemes: one-tap direct-feedback FIR DFE, IIR DFE, and CDR with adjustable timing offsets.

information on the previous bit and selects one of them later when the decision result becomes available. While this DFE architecture can typically achieve the higher bitrates than the previously-reported direct-feedback DFE, its additional sampling stages and fast selection logic cause overhead in terms of hardware and power dissipation. Second, a multi-tap FIR DFE used in order to cancel the long-trailing post-cursor ISIs may also consume large power. This is especially true when a current-mode summing circuit is used and/or when the equivalent circuit must satisfy the required linearity and bandwidth. Third, yet another power-consuming circuit is the high-bandwidth CML differential stages placed on the input signal path, such as the limiting amplifiers (LA; not shown) and continuous-time linear equalizers (CTLE). In many existing equalizing receiver designs, a CTLE is combined with a DFE to compensate the pre-cursor as well

as post-cursor ISIs. The power efficiency of the LA or CTLE stages is particularly poor when they are implemented in multiple stages in order to provide both high gain and high bandwidth.

Our primary objective in this work is to realize a power-efficient equalizing receiver front-end by combining multiple equalization techniques as sourced from the literature [5, 11-13]. It will be shown that doing so not only can eliminate all of the four power-hungry circuit blocks stated previously but also can compensate for the pre-cursor and post-cursor ISIs effectively. For instance, the timing-critical first post-cursor ISI tap is cancelled by a direct-feedback finite-impulse-response (FIR) DFE which exploits the overlaps between the two half-rate comparators' evaluation periods [12], eliminating the fast digital logic required for loop-unrolling DFEs. Second, an infinite-impulse-response (IIR) filter is utilized to subtract the remaining post-cursor ISIs [13], this time eliminating the multi-tap DFE. Third, DFE signal summation is performed by the comparator circuit without consuming static power. Lastly, the pre-cursor ISIs are suppressed by passive inductors added in series with the termination resistors [11] and by shifting the data sampling phase from its nominal position [5], removing the CTLE and limiting amplifier stages.

In addition to the equalizer implementation, a combined adaptation algorithm is presented to find the optimal coefficients that minimize the BER of such a heterogeneous equalizer and optimal sampling timing for CDR. Many prior adaptation algorithms [14-17] assumed a homogeneous equalizer architecture (e.g., FIR DFE), which may adversely interact with other equalizer adaptation loops (e.g., CTLE) or clock-and-data recovery (CDR) loops [5].

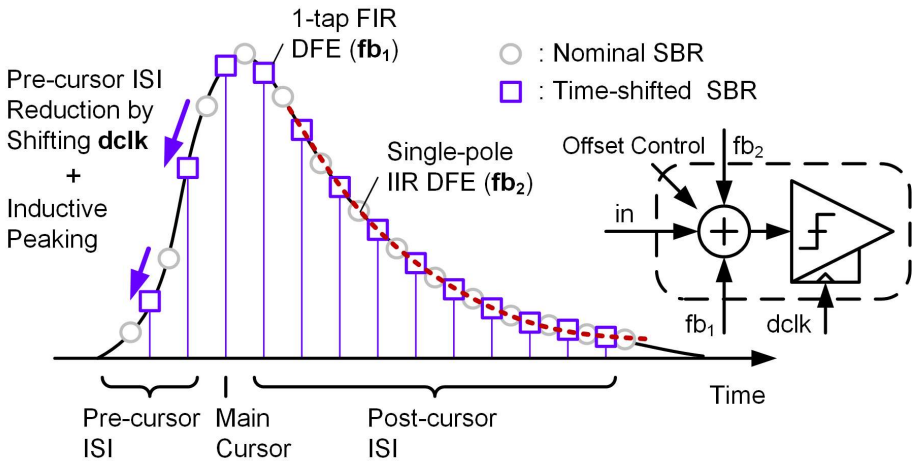


Figure 2.3: The channel loss compensation schemes of the proposed equalizing receiver.

In Figure 2.2, the proposed receiver compensates for the channel-induced ISIs largely by three means. First, the first post-cursor ISI is removed by a one-tap FIR DFE. Second, the trailing post-cursor ISIs after the first one are canceled by an IIR DFE with a single-pole continuous-time low-pass filter. Third, the pre-cursor ISIs are mitigated by shifting the recovered clock phase in the CDR to an earlier timing position instead of using a CTLE. Interestingly, the input signals to our multiple-input clocked comparator in Figure 2.3 correspond to these three ISI compensation schemes. For example, the one-tap direct-feedback FIR DFE signal is fed to the fb_1 input, the IIR DFE feedback signal is fed to fb_2 input, and the time-shifted recovered clock of the CDR is fed to *dclk*. Therefore, this multi-input clocked comparator design is essential in our equalizing receiver, of which the circuit details are described in the next

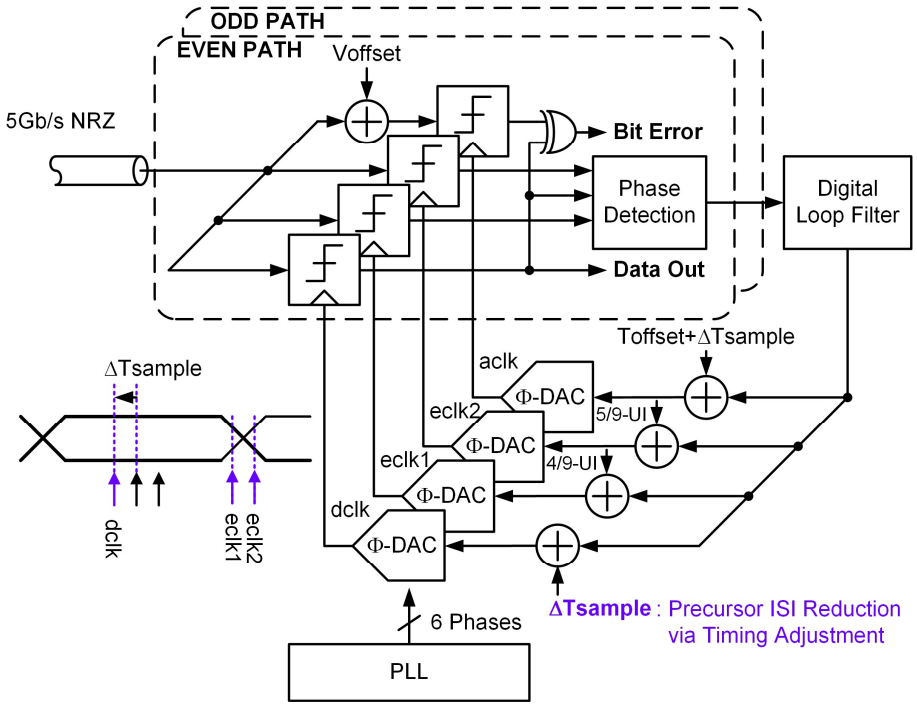


Figure 2.4: The overall architecture of the receiver front-end, illustrating the timing offset adjustments using the digital phase interpolators (ϕ-DACs) in the clock-and-data recovery (CDR) loop.

section.

As illustrated in Figure 2.2, the proposed DFE receiver front-end basically has a half-rate architecture in which two parallel data samplers (called *even* and *odd*), each triggered by a different polarities of the half-rate clocks (*dclk* and *dclk_b*) deserialize the incoming 5-Gb/s data stream into two 2.5-Gb/s streams. This half-rate architecture is widely adopted and can double the data rate for a given clock frequency. When implementing a one-tap direct-feedback DFE, the half-rate architecture allows the direct connection of one sampler output's to the other sampler's feedback input without an explicit delay stage. However, such an implementation is associated with potential timing issues

because the equalization loop and CDR loop is separated. The proposed solutions to these are discussed in section 2.3.

A judicious combination of the one-tap direct-feedback DFE and IIR DFE can eliminate most of the power-hungry circuits previously needed to cancel the post-cursor ISIs, as shown in Figure 2.2. The direct-feedback DFE architecture eliminates the short-latency digital logic required in a loop-unrolling DFE [10]. The IIR DFE [13] replaces the multi-tap FIR DFE and eliminates the need for a large fan-in summation circuit. Furthermore, the IIR DFE replaces the digital-to-analog converter (DAC) required to generate the feedback signal in a multi-tap DFE with a single-stage, continuous-time low-pass filter.

In mitigating the pre-cursor ISIs, the proposed receiver adopts a technique that shifts the data sampling timing in the CDR [5] instead of relying on a power-consuming CTLE stage. The data sampling timing is shifted by adjusting the time-spacing between the data sampling clock (***dclk***) and the edge sampling clocks (***eclk*$_1$**, ***eclk*$_2$**) in the CDR, whose architecture is shown in Figure 2.4. The CDR essentially contains a dual-loop architecture of which the individual phases of ***dclk***, ***eclk*$_1$**, and ***eclk*$_2$** can be digitally controlled via a set of phase interpolating stages or phase-domain DACs [18]. The ***dclk***-to-***eclk*$_1$** and ***dclk***-to-***eclk*$_2$** spacings can be digitally adjusted by adding a digital offset (ΔT_{sample}) to the phase-domain DAC input which controls the data sampling phase. Because the only additional hardware required is a single digital adder, this is an attractive means of reducing the pre-cursor ISIs with very little overhead in terms of hardware and power dissipation.

2.2. Circuit Implementation

2.2.1. Multiple-Input Summing Regenerative Latch

Figure 2.5 shows the circuit schematic of the regenerative latch, which also performs signal summation without dissipating static current. The circuit is basically a StrongARM latch with multiple input pairs connected in parallel. There are four input pairs. First, the main input pair (*in+*, *in-*) samples the incoming data signal. Second, the first feedback input pair (fb_1+, fb_1-) receives the data output of the alternative-phase regenerative latch and subtracts it from the incoming signal to cancel the first post-cursor ISI, realizing a one-tap direct-feedback FIR DFE. The DFE tap coefficient is controlled by a 4-bit digital code

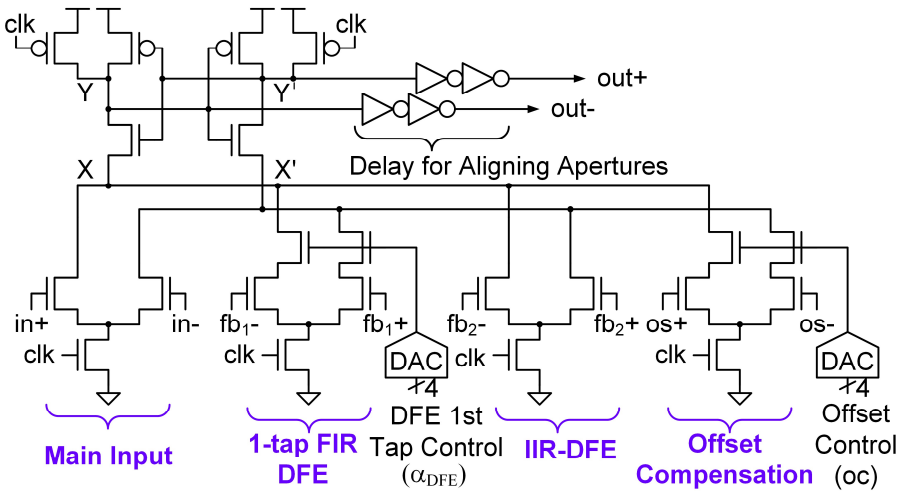


Figure 2.5: The multi-input regenerative latch with static-current-free signal summation.

(α_{DFE}[3:0]) via a 4-bit resistor-ladder digital-to-analog converter (DAC). Third, the second feedback input pair (fb_2+, fb_2-) receives the output of the shared single-pole IIR DFE filter and subtracts it to cancel the trailing post-cursor ISIs. Lastly, the final input pair (os+, os-) receives a binary signal that determines the polarity of the offset voltage to be counter-balanced. Again, the offset magnitude is controlled by an external 4-bit digital code (oc[3:0]) via a DAC.

Among the input signals, note that the (fb_1+, fb_1-) and (os+, os-) inputs are binary-valued determining only the polarity of the corresponding signals, while their analog weights are set by the external digital codes, α_{DFE} and oc. For both cases, the digital code is first converted to an analog voltage, which then drives the gate terminal of the common-gate devices, connected in series with the input pair devices. These devices modulate the drain voltages of the input pair devices that operate in triode regions and hence their currents. Figure 2.6 plots the resulting change in the simulated comparator offset magnitude (i.e. the slicing threshold) as the DAC input code varies.

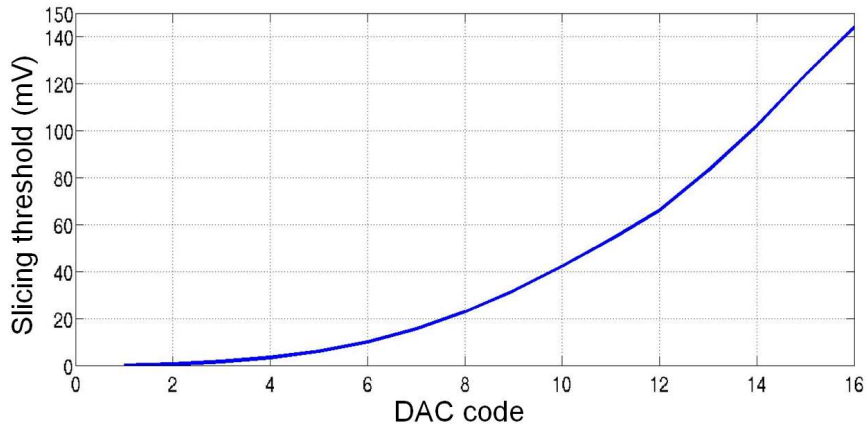


Figure 2.6: The simulated result of the slicing threshold magnitude versus the DAC input code.

The basic operation of the comparator is as follows. When the clock (clk) rises, the current steered by each of the input pairs according to its respective differential input discharges the internal nodes (X and X') of the comparator. The individual currents from the input pairs are linearly added and hence the comparator makes the final decision based on the sum of the input differences. Therefore, the signal summation process can be accomplished at a much lower cost in terms of power and speed as compared to the current-mode summation stage in Figure 2.1.

It is noteworthy that while the parallel input pairs increase the capacitance (C) on the internal nodes X/X', the total discharging current (I) also increases, keeping the sampling aperture of the comparator roughly the same, which is set by the ratio C/I [19]. In addition, the regeneration bandwidth and power dissipation are largely determined by the capacitance on the large-swing nodes Y/Y', which is weakly dependent on the number of input pairs [19].

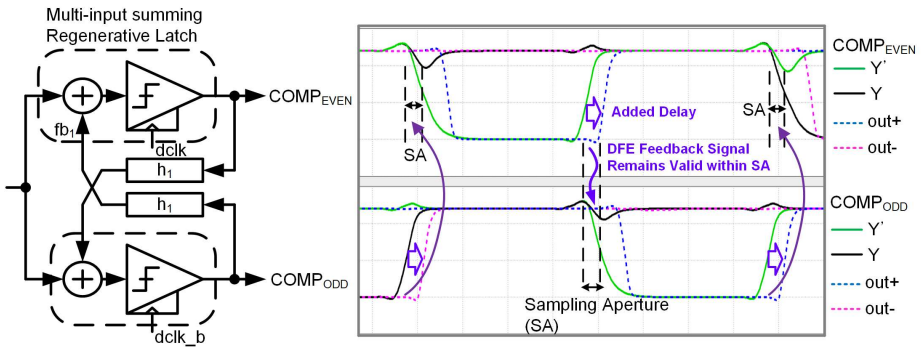


Figure 2.7: The one-tap direct-feedback FIR DFE and its simulated waveforms illustrating the delayed reset operation.

2.2.2. One-tap FIR DFE via Direct Feedback

The proposed receiver adopts a direct-feedback DFE instead of a loop-unrolling DFE architecture in order to avoid the digital selection logic that typically consumes a large amount of power to meet the timing requirements [10]. On the other hand, the speed limitations in the existing direct-feedback DFE [20] can be overcome by creating deliberate overlaps between the evaluation periods of the two half-rate regenerative latch stages such that the settled output signal of one latch can be fed directly into the input of the other while the other is in the sampling phase, as illustrated in Figure 2.7.

The two inverters added at the outputs of the first-stage latch in Figure 2.5 serve to create these overlaps between the evaluation periods. Basically, they delay the reset of the signals fed to the other comparator's fb_1-input so that the previously settled data values can be held while the comparator remains in the sampling phase. Once the sampling phase is over, the signals can be reset without affecting the results. These inverters also serve as buffers that present smaller loads to the latch stage, improving the regeneration bandwidth and hence the latch's gain and sensitivity. This way, a one-tap direct-feedback FIR DFE can be realized with minimal impacts on the speed and area. Similar to the offset control circuit, the tap weight is digitally controlled by the coefficient α_{DFE}, which adjusts the bias voltage to the common-gate devices via a DAC.

2.2.3. Single-Pole IIR DFE

The trailing post-cursor ISIs after the first one are cancelled by an IIR DFE, assuming that the trailing trajectory of the single-bit response can be well

approximated as a single-pole, exponentially-decaying curve. The decision feedback signal is generated by feeding a serialized output data stream into a single-pole low-pass filter, adopting the circuits described in an earlier study [13]. These are shown in Figure 2.8. The gain and pole frequency of the filter are adjustable by tuning the difference between the two bias currents (I_{DC}, I_{EQ}) and switching the load capacitance (C_{EQ}), respectively. The filter stage consists

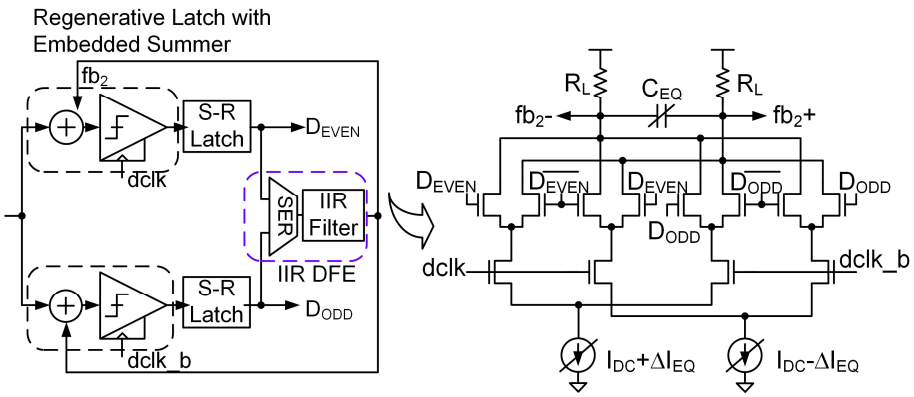


Figure 2.8: The single-pole IIR DFE filter circuit presented in earlier work [13].

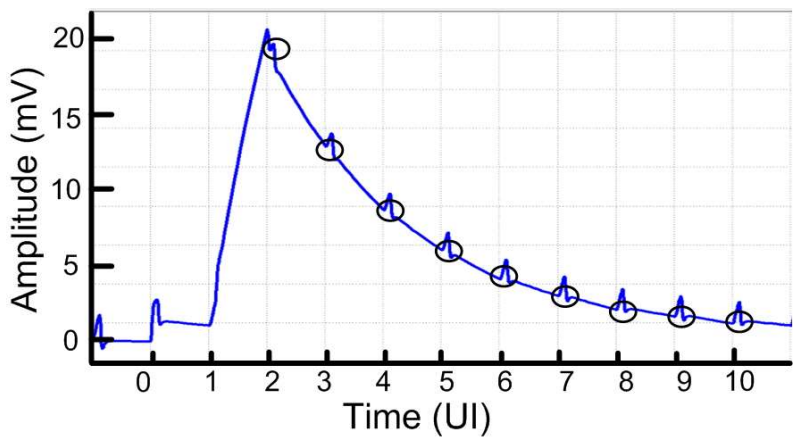


Figure 2.9: The simulated single-bit response of the IIR DFE filter.

of two levels of cascaded differential pairs. The bottom pairs connected to the data sampling clocks *dclk*, and *dclk_b* functions as a multiplexer that serializes the odd and even data streams from the samplers back to a single 5-Gb/s stream. The top pairs are composed of two sets of two input pairs that are connected to the different polarities of the even and odd data inputs (D_{EVEN} and D_{ODD}), respectively. The two pairs in each set are biased with different amounts of tail current, $I_{DC}+I_{EQ}$ and $I_{DC}-I_{EQ}$. The common-mode component of the bias current (I_{DC}) determines the output common-mode voltage of the filter stage while the differential component (I_{EQ}) sets the differential gain and hence the output swing of the filter. Figure 2.9 shows the simulated single-bit response of the IIR filter stage, exhibiting a single-pole exponentially decaying response. The time constant of this exponential decay is adjusted by varying the load capacitance (C_{EQ}).

Although this filter stage does consume static current, the current level can be low because the stage does not require a high bandwidth. This is especially the case here, as this IIR DFE is not responsible for compensating for the first post-cursor ISI and the filter stage is supposed to emulate the trailing post-cursor ISIs with a low-pass frequency response.

By combining the two aforementioned DFE implementations, the equalizing receiver can effectively compensate for the post-cursor ISIs without incurring a large amount of power dissipation. In addition, the IIR DFE has benefits equivalent to those of a multi-tap FIR DFE without requiring a large fan-in summation circuit. These factors further reduce the power dissipation and improve the operating speed of the equalizing receiver.

2.2.4. Pre-Cursor ISI Reduction via Inductive Peaking Termination and CDR Timing Adjustment

The pre-cursor ISIs are suppressed by passive inductors added in series with the termination resistors [11] and by shifting the data sampling phase from its nominal position [5], removing the CTLE and limiting amplifier stages. As for the termination with inductive peaking, its equivalent circuit model is shown in Figure 2.10(a). Figure 2.10(b) and (c) compare the simulated SBRs with and without the inductors, demonstrating that the inductive peaking does help reduce the pre-cursor ISI by 37% in this case. The pre-cursor ISI is also reduced by shifting the data sampling point to an earlier position as opposed to using a

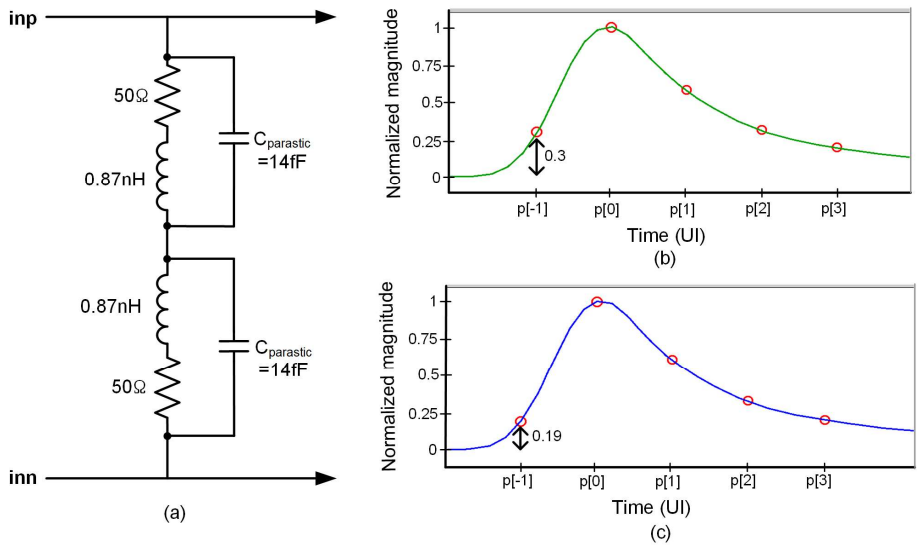


Figure 2.10: (a) The equivalent circuit model of the receiver input termination with passive inductive peaking and the simulated single-bit responses (b) without the inductors and (c) with the inductors.

CTLE. While this is not a generally applicable equalization scheme for all cases, most high-speed I/O channels indeed exhibit relatively short and sharp preceding edges in their single-bit responses, making this method effective in reducing the pre-cursor ISIs [5].

Shifting the data sampling timing to an earlier position has three effects on the channel SBR. First, the post-cursor ISIs become larger, but they can be compensated by the DFE. Second, the pre-cursor ISIs become smaller and this is the main benefit of using this technique. Third, the amplitude of the main cursor may become smaller or larger depending on the main cursor position relative to the peak of the SBR. If the main cursor is located before the peak, moving it to an earlier position will reduce its amplitude. In this case, the optimal shift amount is expected to be a compromise between pre-cursor ISI reduction and main-cursor amplitude degradation. On the other hand, if the main cursor is initially located after the peak, shifting it to an earlier position will increase its amplitude to some extent while reducing the pre-cursor ISIs. Because the eye-opening will always improve by shifting the main cursor in this case, it is reasonable to expect that the optimal main cursor position is always located before the peak.

The dual-loop, feed-forward-interpolating CDR shown in Figure 2.4 [21] is perhaps the most suitable architecture to apply this time-shifting technique, as it can individually adjust the data and edge sampling phases by adding digital offsets to the corresponding phase-domain DAC inputs. The implementation details of the CDR are described in the previous work [21]. The CDR uses a set of two edge sampling clocks (*eclk1*, *eclk2*) to find a phase interval that encloses

the desired lock point, instead of using only one edge clock to detect the phase error referenced to the lock point. This method, termed the optimal phase interval detection scheme, prevents the CDR phase from dithering when it is close to the lock point and allows a coarse resolution of the phase-domain DACs without impacting the BER. For instance, the CDR in [21] demonstrated a BER less than 10^{-9} even with a phase resolution as low as 1/9-UI. This low resolution requirement of the phase DACs helps reduce the power dissipation. The nominal *dclk*-to-*eclk1* and *dclk*-to-*eclk2* spacings are four and five steps (4/9- and 5/9-UI), respectively, and increasing the digital offset (ΔT_{sample}) added to the phase DAC input controlling the data sampling phase shifts the phase towards the earlier position. Each subset of the receiver data path consists of a total of four samplers, one to sample the data, two to detect timing errors, and one to monitor the in-situ eye-opening [22]. The timing and offset of the last sampler can be individually adjusted, which allows the measurements of the single-bit response (SBR) and bit-error rate (BER) in addition to the eye opening as will be explained in the next section.

2.3. Combined Adaptation Algorithm for Separated Equalization and Timing Recovery loops

This section presents a combined adaptation algorithm for separated equalization and timing recovery loops to maintain both the optimal timing for the CDR and the optimal tap coefficients for the adaptive equalizer.

Figure 2.11 illustrates the overall system configuration to realize the adaptation loop of the proposed equalizer. The equalizer has a total of five digitally controlled coefficients: the tap coefficient of the direct-feedback FIR DFE (α_{DFE}), the DC and differential bias currents (I_{DC} and I_{EQ}) and load

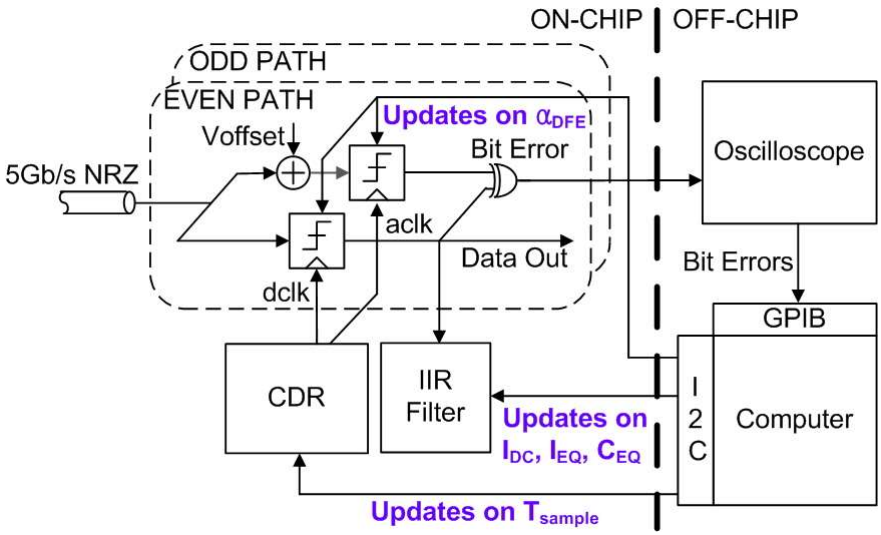


Figure 2.11: The system configuration for the two-step, minimum-BER equalizer adaptation process.

capacitance of the IIR DFE filter (C_{EQ}), and the shift applied to the data sampling timing of the CDR (T_{sample}). Our prototype equalizer chip includes a pair of adaptive samplers with adjustable voltage and timing offsets to measure the SBR, BER, and the eye opening as well as a digital control interface (i.e., the I^2C interface) to externally program the equalizer coefficients. The adaptation algorithm that updates the coefficients based on the measured SBR and eye-opening results is realized with a software program on a personal computer (PC). An oscilloscope is used as an ad-hoc data acquisition device to detect the existence of bit errors at the prescribed voltage/timing margins over a specified test period.

The additional pair of adaptive samplers measures the SBR and BER as well as the eye opening at the data sampler input. The adaptive samplers are triggered by a separate clock, denoted as *aclk*, which has a programmable timing offset to the data sampling clock (*dclk*), adjusted in units of 1/9-UI. Also, the adaptive samplers have their own offset calibration codes, with which one can apply deliberate voltage offsets in steps of 10-mV. As depicted in Figure 2.11, the data sampler output is compared to the corresponding adaptive sampler output, yielding a bit error signal if the two have different values. For instance, if the adaptive sampler with certain voltage and timing offsets always yields the same outputs with the data sampler, it implies that the receiver can tolerate such additional offsets, or equivalently, that the received signal has an eye opening at least as large as the applied offset distances.

The proposed adaptation algorithm is carried out in two steps, as shown in the flow diagram in Figure 2.12. First, the algorithm measures the SBR in the

foreground and determines the initial coefficient values by dead reckoning. This coarse tuning step ensures an adequate initial eye opening, with which, the fine-tuning search can converge to the correct optimum. Second, the algorithm measures the eye opening in the background and iteratively updates the coefficients to minimize the BER using a stochastic hill-climbing method. Essentially, a hill-climbing algorithm is a local search algorithm which updates the currently best-known solution in one incremental step at a time in a direction that improves the objective metric. In our case, the metric is the eye opening or the BER measured at a specific voltage/timing offset position. As will be

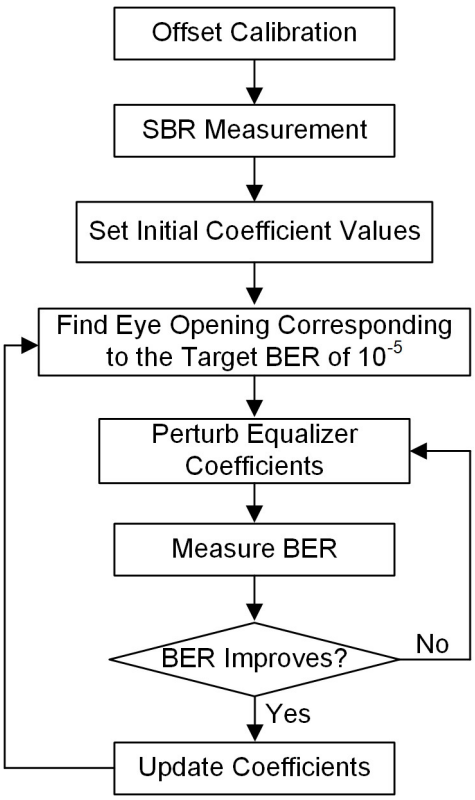


Figure 2.12: Flow diagram illustrating the two-step, minimum-BER equalizer adaptation algorithm.

explained later, the stochastic hill-climbing algorithm can alleviate the burden of trying all the neighboring sets of coefficients during the search while still guaranteeing the correct convergence to the optimum. Therefore, the optimum can be reached with the fewer iteration steps compared to the use of a basic hill-climbing algorithm, especially when the number of coefficients is large.

Unless noted explicitly, it is assumed that the described equalizer adaptation procedure is always preceded by a foreground offset calibration step in order to maximize the voltage margin of the receiver despite the presence of local device mismatch. Such an offset calibration step is necessary especially since the removal of the limiting amplifier and CTLE stages may enhance the impact of the comparator offsets on the overall receiver sensitivity. The offset of each comparator is calibrated by finding the offset adjustment code which results in a randomly alternating output stream when a zero differential input is applied.

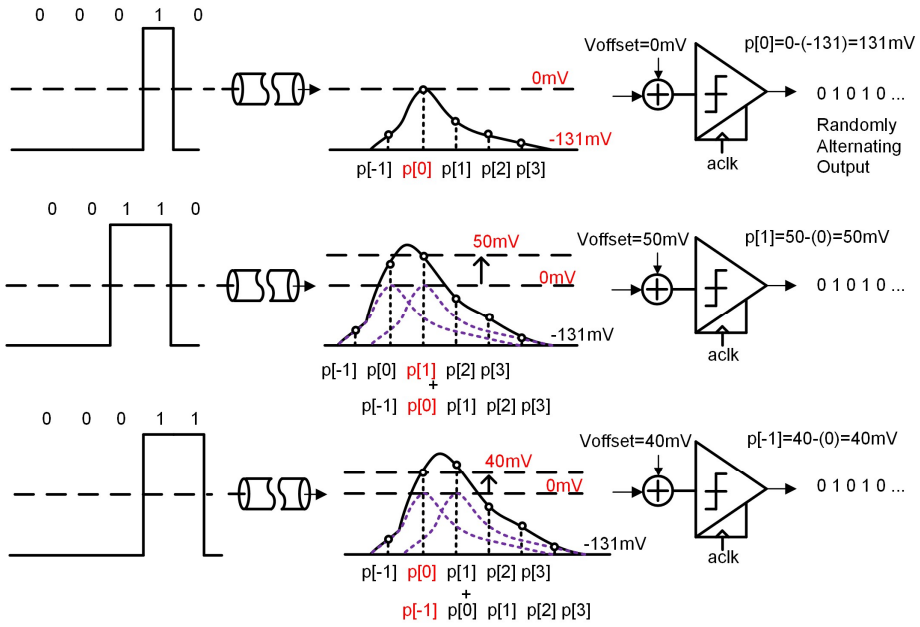


Figure 2.13: An illustration of the proposed single-bit response (SBR) measurement method.

2.3.1. Coarse Adaptation Based on Single-Bit Response Measurement

The proposed adaptation algorithm determines the proper initial coefficient values based on the channel SBR characterization results rather than using a fixed or randomly chosen set of initial values. This is to ensure that the subsequent fine adaptation process can start with an adequate amount of eye opening. Since the DFE subtracts the expected post-cursor ISI from the incoming signal assuming that all of the previously detected bits are correct, it is possible for the DFE to generate new bit errors when some of the previous bits are erroneous. Such error propagation may prevent the proper convergence of the fine adaptation process. Furthermore, the proposed equalizing receiver

can be more susceptible to such issues since it may receive initially much poorer-quality signal than other equalizing receivers that employ CTLEs or feed-forward equalizers. Blind adaptation techniques that do not require an initially open eye exist, but they typically call for sophisticated digital signal processing and incur substantial power and area costs [23, 24].

The process of estimating the channel SBR using the adaptive sampler is illustrated in Figure 2.13. It is carried out in the foreground, where the transmitter sends a set of training sequences to the receiver. When estimating a five-bit long SBR consisting of one pre-cursor ISI and three post-cursor ISI samples, the possible set of training sequences would be 00010, 00011, 00110, 01010, and 10010. The adaptive sampler is used to detect the signal amplitude sampled at the main cursor position (the fourth bit position in the training

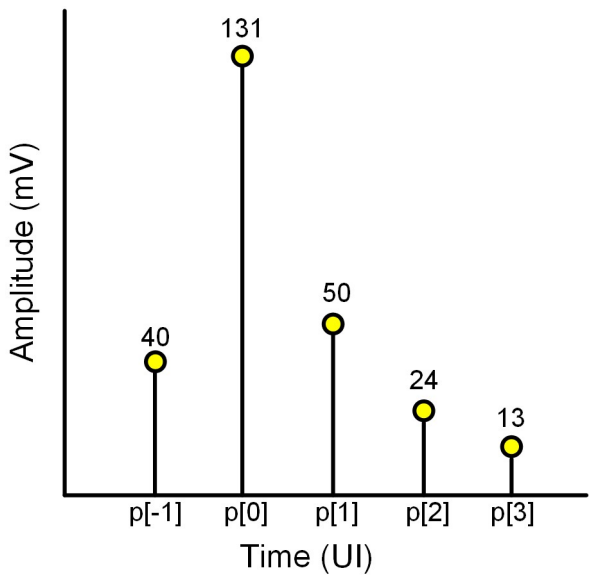


Figure 2.14: The measured 5-Gbps single-bit response (SBR) of a channel with a -15-dB loss at 2.5 GHz.

sequence) by varying its voltage offset until the point at which the sampler gives randomly alternating outputs due to noise is reached. As illustrated in Figure 2.13, once the amplitude of the main cursor is measured from the 00010 training sequence, the first pre-cursor and the first, second, and third post-cursor ISIs can be each estimated from the change in the signal amplitude when the training sequence changes from 00010 to 00011, 00110, 01010, and 10010, respectively.

Figure 2.14 plots the estimated 5-Gb/s SBR of the channel used in the experiment. The channel has a -15-dB loss at 2.5 GHz, and one pre-cursor and three post-cursor ISIs are determined as sufficient to model the SBR. While the accuracy of this SBR measurement is limited by the coarse resolution of the voltage offset adjustment (10-mV), the resulting SBR can nonetheless determine the initial coefficient values that yields an adequate initial eye opening.

2.3.2. Fine Adaptation using Stochastic Hill Climbing

Once the initial coefficient values are determined using the SBR information, the adaptation algorithm then incrementally updates the coefficient values using a stochastic hill-climbing algorithm [25] to minimize the BER measured at the specified voltage and timing offset positions.

Figure 2.15 illustrates the difference between the basic hill-climbing algorithm used in earlier work [22] and the stochastic hill-climbing algorithm proposed in this work. The basic hill-climbing algorithm considers all neighboring sets of coefficient values that can be reached by selectively changing each of the current coefficient values by at most one unit step. In our case with five equalizer coefficients, there would be 242 ($=3^5$-1) neighboring candidates to be considered. After measuring the BERs of all of these candidates, the current solution is updated to the one that yields the lowest BER and the search process continues. While this basic hill-climbing algorithm always follows the steepest gradient path and hence the shortest trajectory to the final solution, the number of BER measurements required can become

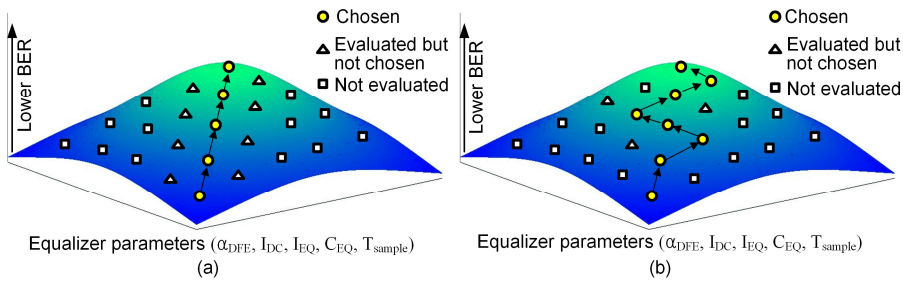


Figure 2.15: An illustration comparing (a) the basic hill-climbing algorithm and (b) the proposed stochastic hill-climbing algorithm.

exceedingly large, especially as the number of equalizer coefficients increases.

In comparison, the stochastic hill-climbing algorithm randomly selects one neighboring candidate out of 242 and updates the current solution as soon as the chosen candidate is found with the lower BER, even if it is not the lowest. Figure 2.16 shows a flow diagram of the proposed stochastic hill-climbing algorithm used for the fine adaptation process. First, the algorithm perturbs each of the equalizer coefficients randomly by at most one unit step and checks whether the BER increases or decreases after the perturbation. If the BER

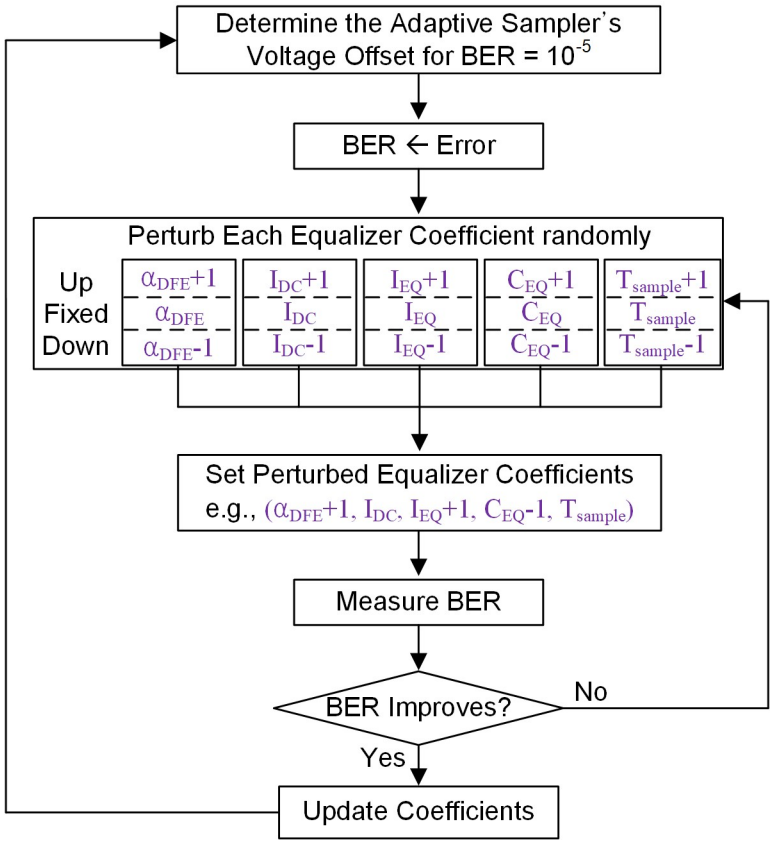


Figure 2.16: Detailed flow diagram of the coefficient fine-tuning process using the stochastic hill-climbing algorithm.

decreases, it adopts the perturbed coefficient values as a new solution. Otherwise, it keeps the original coefficient values and tries other perturbed values. Second, once the coefficients get updated, the voltage offset of the adaptive sampler is adjusted in order to track the point that corresponds to the BER of 10^{-5}. The BER value of 10^{-5} is chosen as an appropriate value that can track the eye opening boundary without requiring too many bit samples to measure. As illustrated in Figure 2.15(b), while this stochastic hill-climbing algorithm does not guarantee a solution trajectory that follows the steepest gradient path, it can reach the final optimum with the far fewer BER measurements than the basic hill-climbing algorithm. The convergence property can be easily proven based on the fact that the stopping criterion is identical to that of the basic hill-climbing algorithm.

It is important to note that perturbing only one coefficient at a time (that is, considering 10 neighboring candidates for the case with five coefficient variables) does not guarantee convergence to the correct optimum. For instance, simultaneously changing two coefficients may decrease the BER, whereas changing only one of them increases the BER. In the earlier work in [5], a possible false convergence due to the interaction between the DFE adaptation loop and CDR feedback loop was reported. To avoid such false convergence issues due to the inter-dependencies among the coefficients, it is necessary to consider all the 242 neighboring candidates.

2.4. Measurement Results

The prototype equalizing receiver and the supporting CDR are implemented in a 65nm LP/RF CMOS technology. A photograph of the chip is shown in Figure 2.20 and its performance characteristics are summarized in Table I. The receiver front-end, including the total of eight comparators and DFE units, consumes 2.3mW from a single 1.2V supply and is able to compensate for -15dB of channel loss while receiving a 5-Gb/s, 2^7-1 PRBS pattern. The power does not include the additional hardware power consumed by, for instance, the

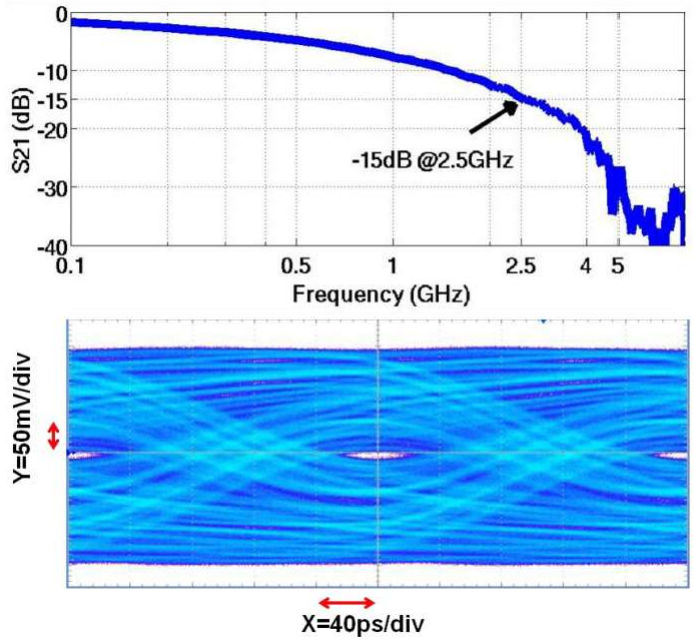


Figure 2.17: The frequency response of the channel with a -15dB loss at 2.5GHz (top) and the eye diagram of the 5-Gb/s, 27-1 PRBS NRZ data stream measured at the channel output (bottom).

PC, oscilloscope, and JBERT, and the foreground/background dynamic power used during the equalizer adaptation process. The remaining CDR circuits, including the multi-phase PLL, phase DACs, phase detection (PD) logic, and digital loop filter, consume 6.8mW in total. Figure 2.17 shows the frequency characteristics of the channel used during the test and the measured eye diagram at its output, which is nearly closed.

Figure 2.18 demonstrates the operation of the described equalizer adaptation algorithm. Figure 2.18(a) and (b) plot the time trajectories of the five equalizer coefficients as the iteration proceeds. Figure 2.18 (c) and (d) plot the changes in the vertical eye opening, confirming that the coefficients are indeed updated in the direction that improves the eye opening. Based on the measured SBR shown in Figure 2.14, the initial, coarsely tuned coefficient values are (α_{DFE},

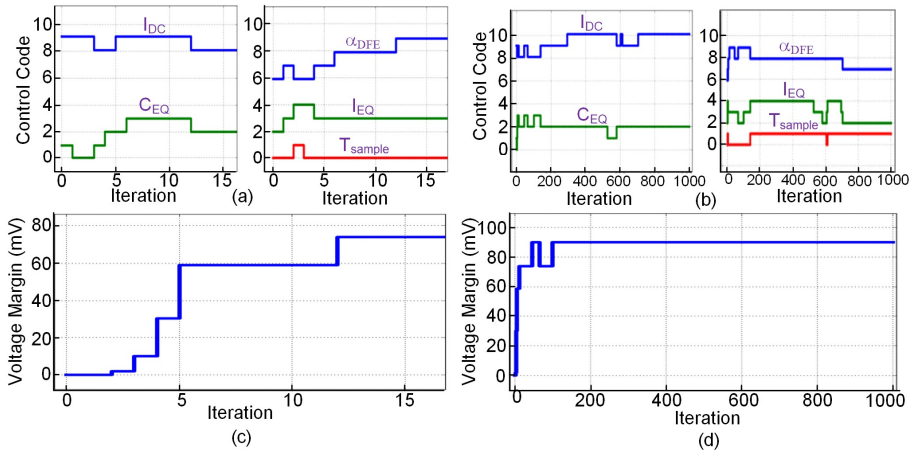


Figure 2.18: The measured trajectories of the equalizer coefficient (α_{DFE}, I_{DC}, I_{EQ}, C_{EQ}, T_{sample}) improvements in the voltage margin: (a) and (c) during the first 15 iterations showing the quick convergence, and (b) and (d) during the first 1000 iterations confirming the settlement.

I_{DC}, I_{EQ}, C_{EQ}, T_{sample}) = (6, 2, 9, 1, 0), which denote the settings for the FIR DFE tap coefficient (α_{DFE}), the IIR filter's common-mode and differential bias currents (I_{DC} and I_{EQ}), the IIR filter stage's capacitive load (C_{EQ}), and the CDR timing offset (T_{sample}), respectively. Figure 2.18 shows that the coefficients converge to their final values fairly quickly within 15~20 iteration cycles due to the initially set values based on the SBR and the stochastic hill-climbing algorithm. The final coefficient values found by the algorithm were (α_{DFE}, I_{DC}, I_{EQ}, C_{EQ}, T_{sample}) = (7, 10, 2, 2, 1), which correspond to the actual values of 55 mV, 28 μA, 7 μA, 18 fF, and 1/9 UI, respectively. The total of 1000 iterations took 1 hour and 25 minutes.

Figure 2.19 shows the effective eye diagram measured at the input of the

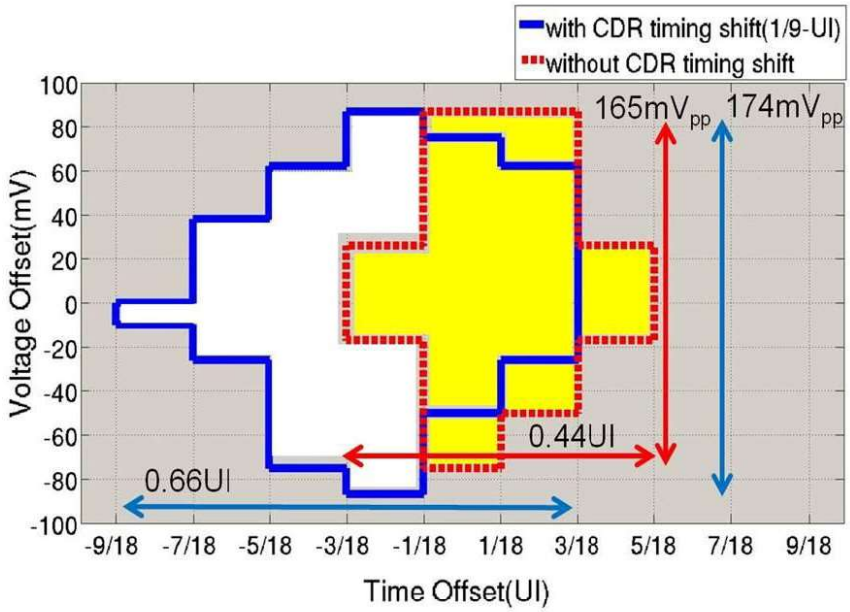


Figure 2.19: The effective eye diagram at the comparator input after the DFE subtraction, measured using an in-situ eye-opening monitor [22].

comparator after the DFE feedback signals, canceling the post-cursor ISIs, have been applied. This is measured by the same adaptive samplers that were used previously to measure the SBR and BER during the adaptation process. By comparing the output of the main data sampler with that of the adaptive sampler with different voltage and timing offsets, one can find the largest timing and voltage shifts that still recover the correct data with a target BER, and thus the eye opening. With the described equalization techniques applied, the worst-case eye-opening measured in this way with a BER of 10^{-9} was $174mV_{pp}$ and $0.66UI_{pp}$. In this case, the optimal shift in the data sampling positions was 1/9 UI. Figure 2.19 also shows the eye-opening without the timing shift, which has a much smaller eye-opening with values of $0.44UI_{pp}$ and $165mV_{pp}$, demonstrating the effectiveness of the CDR timing-shifting technique in reducing the pre-cursor ISI.

TABLE I

SUMMARY OF THE PROTOTYPE CHIP PERFORMANCE.

Technology	65nm CMOS
Data rate	5 Gbps
Power	2.3mW (front-end)
	6.8mW (CDR)
Supply	1.2V
Area	0.0036 mm^2
Channel loss	-15dB at 2.5GHz
Data pattern	2^7-1 PRBS
BER	$<10^{-9}$

Table 2.1: Performance Summary.

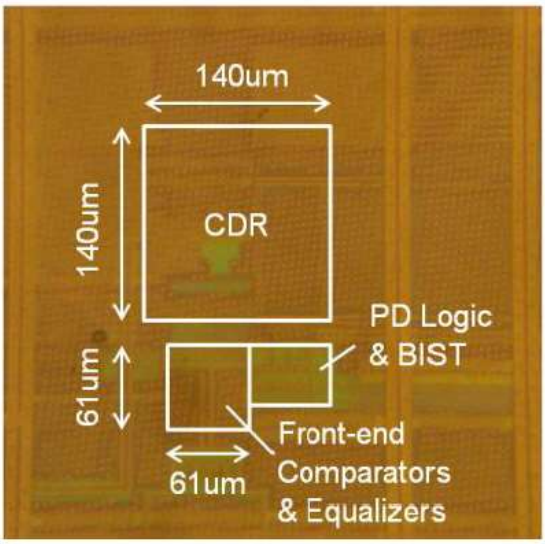


Figure 2.20: A die photograph of the prototype equalizing receiver fabricated in 65nm CMOS.

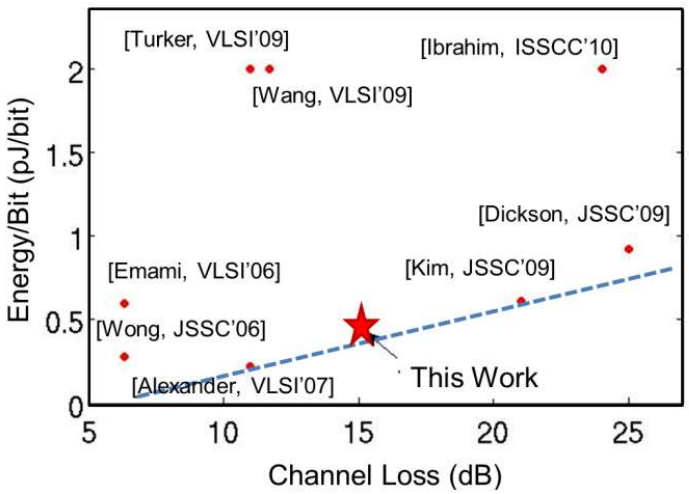


Figure 2.21: Comparison of the energy-efficiency values (pJ/bit = mW/Gbps) of recently published equalizing receiver front-ends.

Chapter 3.

Analysis on Combined Equalization and Timing Recovery of FSE

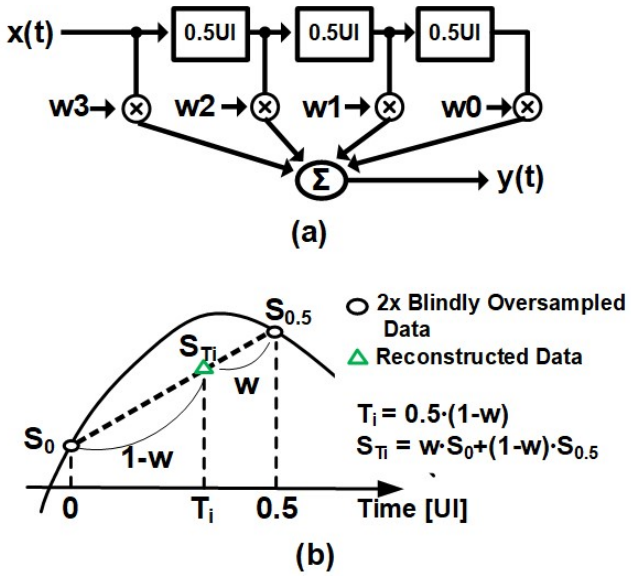


Figure 3.1: (a) Block diagram of 4-tap finite impulse response (FIR) filter with a 0.5-UI tap spacing; (b) timing recovery via data interpolation.

To avoid the undesired interaction between equalization and timing recovery, a previous work [4] demonstrated that fractionally spaced equalizers (FSE) can combine equalization and timing recovery in a single control loop, as shown in Figure 1.7(b). FSEs are FIR filters that have a tap spacing of less than 1-UI. Figure 3.1(a) shows a 4-tap FSE that uses a 0.5-UI tap spacing. The most interesting thing is that FSE can act as a clock and data recovery (CDR) because the 0.5-UI-spaced FIR filtering not only performs feedforward equalization but also timing recovery. This timing recovery is possible by interpolating the blindly oversampled data and reconstructing intermediate data points, as shown in Figure 3.1(b) [4, 27–29]. The reconstructed timing is adjusted by controlling the FIR tap coefficients. The simple architecture uses FSE as a unification of

the equalizer and CDR, which allows for reduced power dissipation and improved overall link performance.

The main reason why FSEs can recover timing is because it can avoid aliasing effects by sampling the input signal multiple times per symbol period. In contrast, a symbol spaced equalizer (SSE), which samples the input signal only once per symbol period, suffers from aliasing effects, which results in significant loss of information unless the sampling (τ) is maintained optimal.

3.1. Comparison of Aliasing Effects between FSE and SSE

The previous work [26] analyzed FSE and SSE in a frequency domain and compared their aliasing effects. In high-speed link systems, as shown in Figure 3.2, the equalized signal *u(t)* can be expressed as:

$$u(t) = \sum_{m} a_m h(t - mT) \qquad (1)$$

where $\{a_m\}$'s are transmitted data symbols, T is the symbol period, and $h(t)$ is the overall equalized pulse response.

For SSE, the output is sampled at instants of $t=nT+\tau$ and the transfer function $H_T(f)$ becomes a folded spectrum of $H(f)$, as shown in Figure 3.3(a) [26]:

$$H_T(f) = C(f) \sum_{k=-\infty}^{\infty} F(f - \frac{k}{T}) \exp\{2\pi j(f - \frac{k}{T})\tau\}$$

$$= C(f) F_T(f) \qquad (2)$$

where $C(f)$ is the transfer function of SSE, $F(f)$ is the Fourier transform of the pulse response. From equation (1), the aliasing happens near Nyquist frequency ($f_0/2=1/2T$).

On the other hand, for FSE, the output is sampled with sampling timing at $t=nT'+\tau$, where $T'<T$. The transfer function $H_{T'}(f)$ is also a folded spectrum of $H(f)$:

$$H_{T'}(f) = C(f)\sum_{k=-\infty}^{\infty} F(f - \frac{k}{T'})\exp\{2\pi j(f - \frac{k}{T'})\tau\} \qquad (3)$$

For instance, by choosing sampling rate twice higher than the highest frequency component of *F(f)*, as shown in Figure 3.3(b), the aliasing effect can be mitigated. In general, a 2× oversampling ratio is enough to avoid aliasing owing to the low-pass characteristics of the channel. In equation (2), only the $k = 0$ term survives [26].

$$H_{T'}(f) = C(f)F(f)\exp(2\pi jf\tau), \qquad |f| < \frac{1}{2T'} \qquad (4)$$

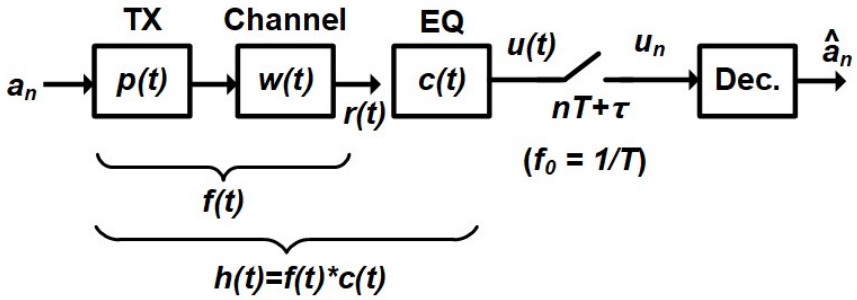


Figure 3.2: Block diagram of a high speed link system.

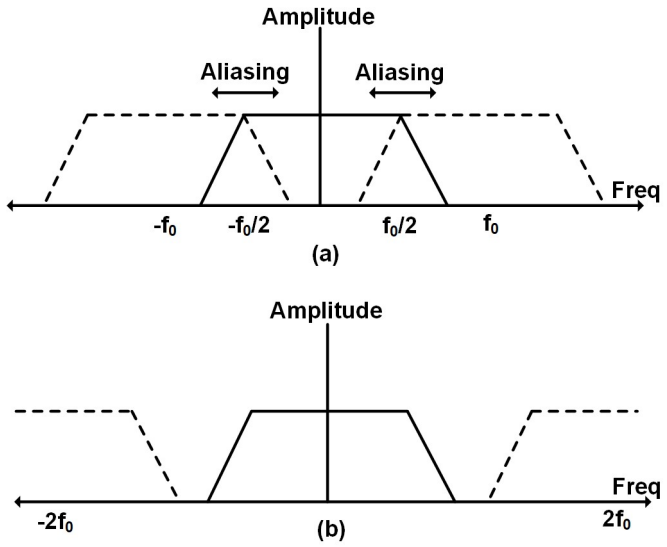


Figure 3.3: (a) Frequency response of a sampled impulse response when using a symbol spaced equalizer (SSE). (b) Frequency response of a sampled impulse response when using a fractionally spaced equalizer (FSE).

3.2. Timing Recovery Ability of FSE

From equation (1), an SSE can only act on the aliased spectrum of the folded spectrum $F_T(f)$, as shown in Figure 3.3(a). This can lead to a severe information loss when an aliased spectrum has the null with a poor choice of the sampling timing τ, as shown in Figure 3.4 [26]. A null near the Nyquist frequency ($f_0/2$) implies that the receiver is sampling at the transitioning edge rather than at the center of the data eye in the time domain. In this case, SSE cannot recover the correct data regardless of how many taps are used. This is why SSE needs an additional timing control loop that aligns sampling time to the middle of the data eye.

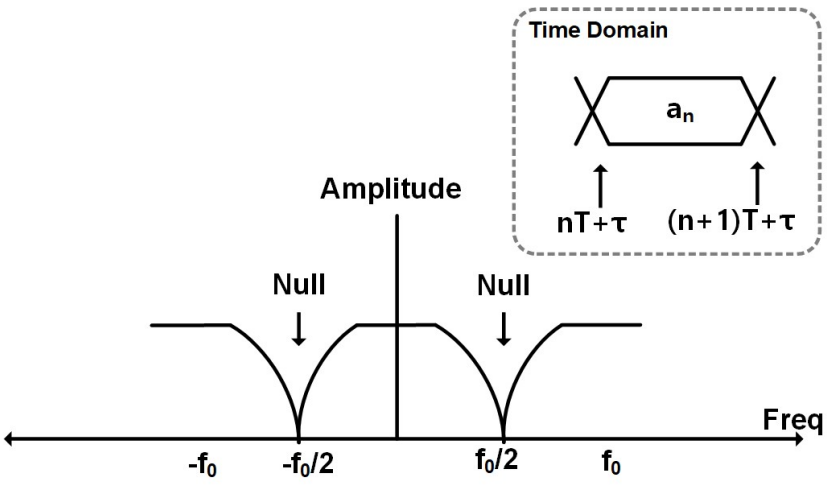


Figure 3.4: Aliased spectrum, which has null when the symbol spaced equalizer (SSE) samples data at the edge of the eye.

On the other hand, FSE does not need an additional timing control loop because FSE performs combined equalization and timing recovery. In the equation (3), the transfer function of FSE, $C(f)$, acts on both the $F(f)$ term and $\exp(2\pi jf\tau)$ term at the same time. By acting on the channel loss term, $F(f)$, FSE performs the equalization and by acting on the delay term, $\exp(2\pi jf\tau)$, FSE performs the timing recovery. Typically, timing recovery is performed by changing sampling timing of sampling clock while input data delay is fixed. In contrast, timing recovery using FSE is performed by changing the delay of input data while sampling timing is fixed because the delay of t_0 for data is equivalent to delay of $-t_0$ for sampling clock as shown in Figure 3.5.

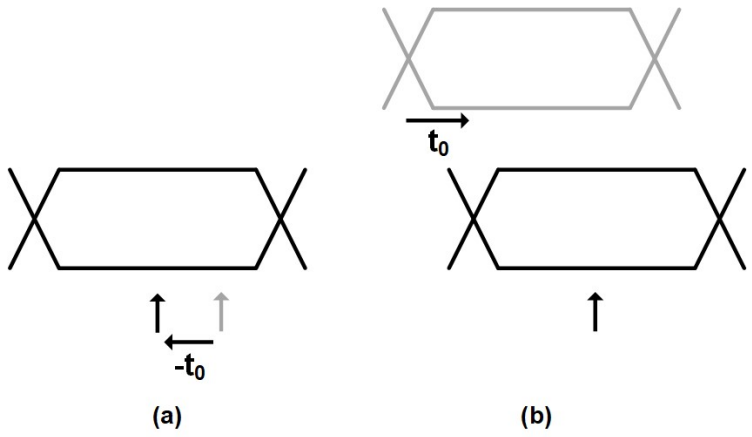


Figure 3.5: The delay of $-t_0$ for sampling clock timing, (b) the delay of t_0 for data.

3.3. Analysis on FSE CDR as a Bang-Bang Controlled Delay Locked Loop

On the other hand, the received signal $r(t)$ before the equalization in Figure 3.2 can be expressed as:

$$r(t) = \sum_m a_m f(t - mT) \qquad (5)$$

where $f(t)$ is the pulse response of the channel. For instance, an ideal pulse response of NRZ signaling through a lossless channel would be a trapezoidal wave as shown in Figure 3.6(a). With its sufficiently short transition times compared to the unit interval T, a 2× oversampling FSE receiver is guaranteed to have at least one sample hitting the position with the maximum eye opening

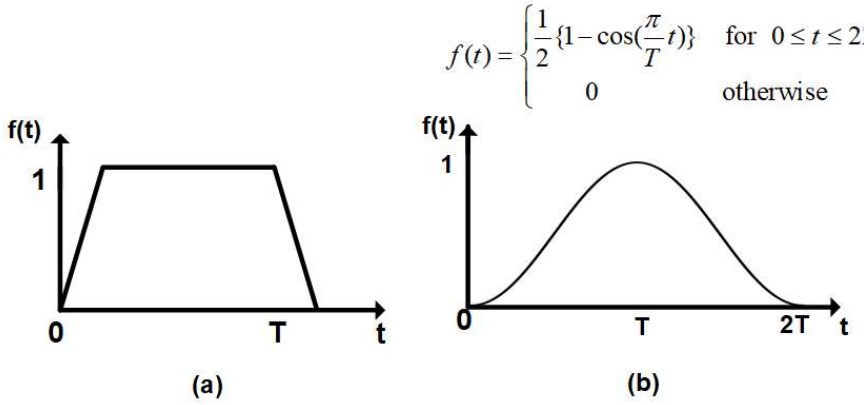


Figure 3.6 (a) An ideal NRZ pulse propagating through a lossless channel; (b) a raised cosine pulse which has $f_0/2$ frequency.

across all possible timing offsets between the incoming data and sampling clock. Hence, it is obvious that the FSE can always recover the correct data in this ideal case.

The more realistic pulse response would have its power spectrum concentrated within the Nyquist frequency ($f_0/2$), such as a raised-cosine pulse as shown in Figure 3.6(b). This pulse response still does not have any ISIs, which is suitable for analyzing the timing-tracking capability of the FSE receiver while setting its equalization capability aside.

Without the presence of ISI, it is expected that the only the first two taps (w_0, $w_{0.5}$) will be utilized to perform the timing interpolation. The (w_0, $w_{0.5}$)-values that interpolate the data samples at arbitrary timing positions can be derived by minimizing the mean squared error (MSE) of the equalized pulse response Y, which is a matrix multiplication of the pulse response F and the FSE's impulse response C, compared to the ideal equalized pulse response $\hat{Y}$:

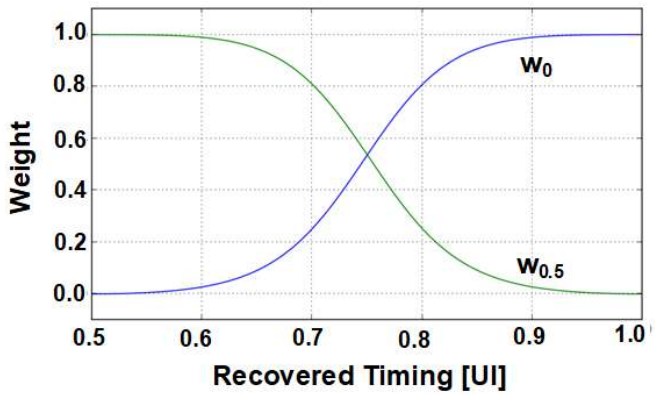


Figure 3.7: FSE tap coefficients, (w_0, $w_{0.5}$) which minimize mean square error (MSE) when the pulse response is a raised cosine as shown in Figure 3.6(b).

$$FC = Y$$

$$\begin{pmatrix} f_{-1} & f_{-1.5} \\ f_0 & f_{-0.5} \\ f_1 & f_{0.5} \end{pmatrix} \begin{pmatrix} w_0 \\ w_{0.5} \end{pmatrix} = \begin{pmatrix} y_{-1} \\ y_0 \\ y_1 \end{pmatrix} \qquad (6)$$

Figure 3.7 plots the calculated FSE weights (w_0, $w_{0.5}$) as a function of the recovered timing τ_r. If the sign-sign LMS algorithm updates each tap coefficient value by a fixed amount Δw, the change will cause an effective timing shift of $\Delta\tau$ in the recovered timing τ_r. Figure 3.8(a) shows the calculated $\Delta\tau$ with respect to recovered timing τ_r.

Based on this $\Delta\tau$, we can derive an equivalent timing recovery loop model of the adaptive FSE receiver as shown in Figure 3.9. It is basically a first-order bang-bang controlled DLL. In this model, the timing error (τ_e) introduces a residual ISI at the sampling point, which is detected by the error sampler as a voltage error, which is plotted in Figure 3.8(b). The voltage error then changes

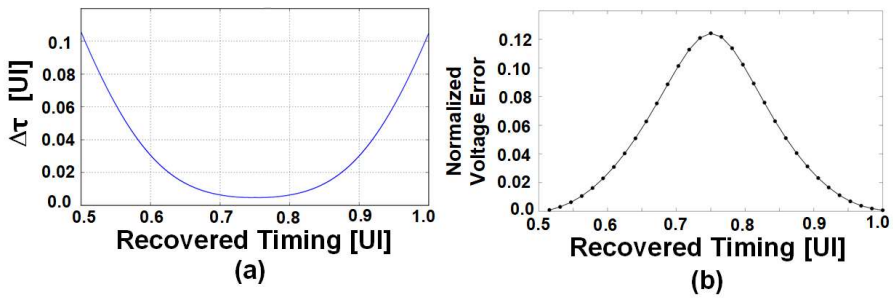


Figure 3.8: (a) The amount of recovered timing shift when the FSE tap coefficients change by Δw=1/32; (b) the normalized voltage error detected by the error sampler.

the FSE weight (Δw) by using the SS-LMS adaptation and Δw causes a timing change ($\Delta\tau$). The model applies a time-to-weight conversion gain ($1/K_{w\text{-}t}$) to scale the timing error (τ_e) between the blind-sampling clock (τ) and recovered timing (τ_r) to weight error (w_e), and applies a weight-to-time gain $K_{w\text{-}t}$ to convert the resulting weight change (Δw) to the timing change ($\Delta\tau$). The equivalent timing-recovery loop is bang-band controlled since the SSLMS algorithm updates the FSE weights by a fixed step Δw upon the error detection, which is modeled by a slicer producing ±1 value. While Figure 3.8(a) shows that the

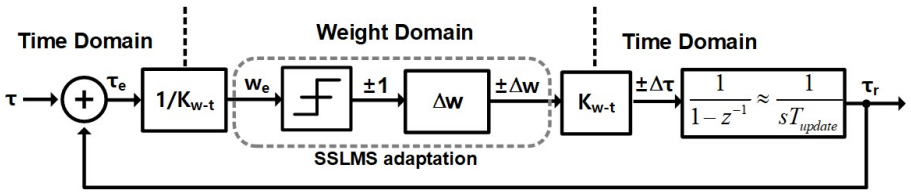


Figure 3.9: An equivalent timing recovery loop model of the adaptive FSE receiver.

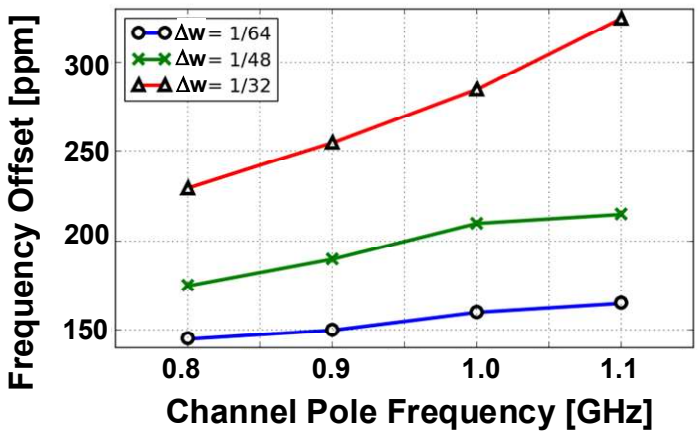


Figure 3.10: A simulated maximum amount of frequency offset with various update step Δw and channel pole frequency.

gain $K_{w\text{-}t}$ varies widely with the recovered timing (τ_r), the overall loop gain and hence the closed-loop bandwidth do not change as much since the inverse gain is applied at the time-to-weight conversion ($1/K_{w\text{-}t}$) , which also varies due to the different pulse response values at different positions.

When the nonlinear, dithering behavior caused by the slicer is sufficiently linearized by the random signal at its input, one can derive the equivalent tracking bandwidth and jitter tolerance characteristics using the pseudo-linear analysis presented in [30]. The paper [30] uses two different linearized gains for the deterministic signal component and random noise component, respectively, and predicts the jitter transfer and jitter tolerance characteristics of the bang-bang controlled CDR. It can be shown that the overall CDR loop transfer function $H(s)$ can be approximated as:

$$H(s) = \frac{1}{1 + s / p}, \qquad p \approx \frac{K_{slicer} \cdot \Delta w}{T_{update}} \tag{7}$$

where K_{slicer} is an approximation linearized gain of the slicer, Δw is the amount of change in the FSE weights per update and T_{update} is the update period of the SSLMS algorithm. The CDR's tracking bandwidth p improves with the larger Δw and shorter T_{update} with possible penalty in the steady-state performance such as the high-frequency jitter tolerance due to the dithering in the FSE weight values.

In presence of ISIs, the timing-tracking capability of the FSE degrades since the fixed weight change made by the SSLMS adaptation at each update period must address the timing error as well as the residual ISI error. Figure 3.10 and

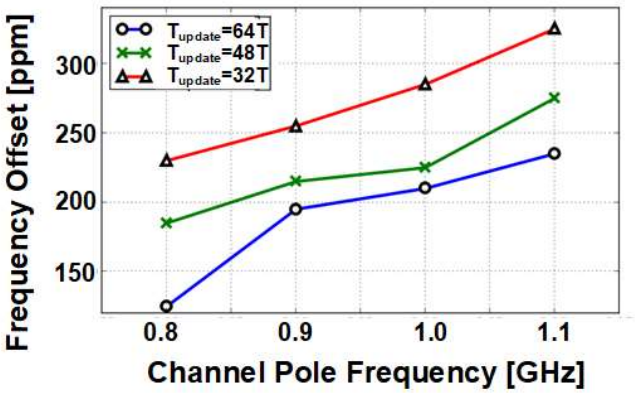


Figure 3.11: A simulated maximum amount of frequency offset with various update period T_{update} and channel pole frequency.

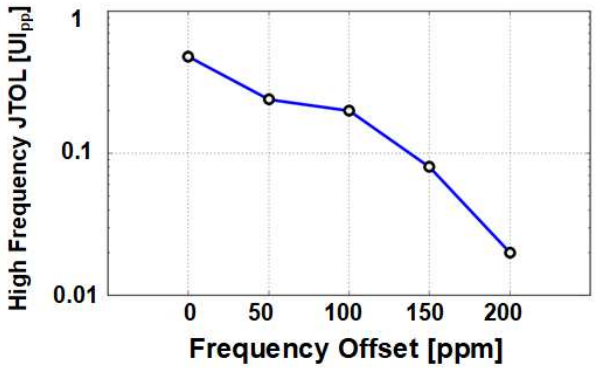


Figure 3.12: The simulated high-frequency jitter tolerance versus the frequency offsets between the blind-sampling clock and input data.

11 shows the simulated maximum frequency offset that the proposed infinite-range FSE receiver can track with no bit errors. The simulation shows that when the channel is modeled as a single-pole system and its bandwidth decreases, the maximum frequency offset that can be tracked by the FSE receiver decreases, implying that the increase in the ISI causes a decrease in the effective CDR

bandwidth. Figure 3.10 and 11 also shows that the CDR bandwidth increases with the larger update step Δw and shorted update period T_{update} as our analysis suggests. In addition, Figure 3.12 shows that the high-frequency jitter tolerance degrades as the frequency offset increases since the SS-LMS adaptation must also address the timing drift due to the frequency offset.

Chapter 4.

Design of FSE Receiver with Combined Adaptive Equalization and Infinite-Range Timing Recovery

The previous problem of using FSEs as a CDR [4] is that the timing recovery range is limited because the FSE adjusts the recovered timing via a set of weights that span a finite time window, as shown in Figure 4.1(b). This drawback limits the use of FSEs as a CDR to mesochronous systems (Figure 4.2 (a)), where the same data and clock frequencies are guaranteed. However, it renders the receiver not suitable for plesiochronous systems (Figure 4.2(b)) where the timing offset between the data and sampling clock would drift indefinitely owing to a small frequency offset. Since many high-speed link applications are implemented as a plesiochronous system, it is important to extend the limited timing recovery range of FSE to infinity.

This thesis present a 2× blind-oversampling FSE receiver that extends a previous FSE receiver [4] to support infinite-range timing recovery for plesiochronous systems. As shown in Figure 4.3, the proposed receiver uses a

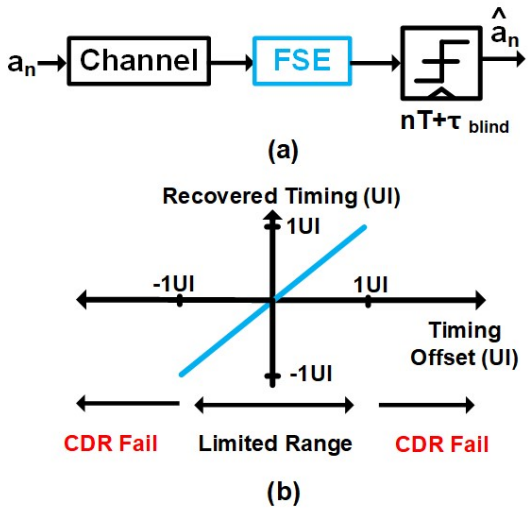


Figure 4.1: (a) Previous fractionally spaced equalizer (FSE) receiver [4], which only supports mesochronous systems, and (b) recovered timing of the FSE with a timing offset, which shows a limited timing recovery range.

set of two FSEs having a 0.5-UI shifted timing relationship, one of which is selected to recover the data. While each FSE has a limited timing recovery range, an infinite range of timing recovery is enabled by using the two FSE alternately, as presented in [37]. The thesis provides an in-depth explanation of

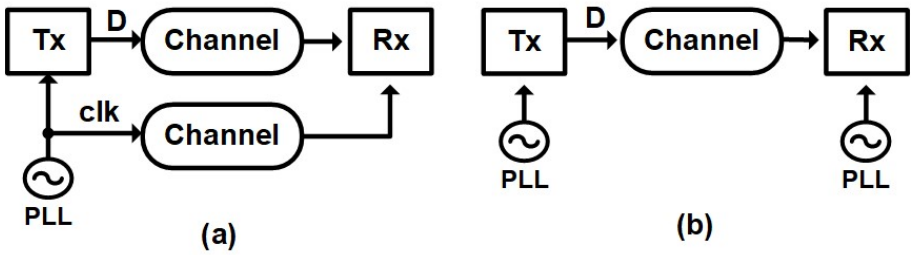


Figure 4.2: (a) Mesochronous system, which only needs phase offset calibration, and (b) a plesiochronous system, which needs both frequency and phase offset calibration.

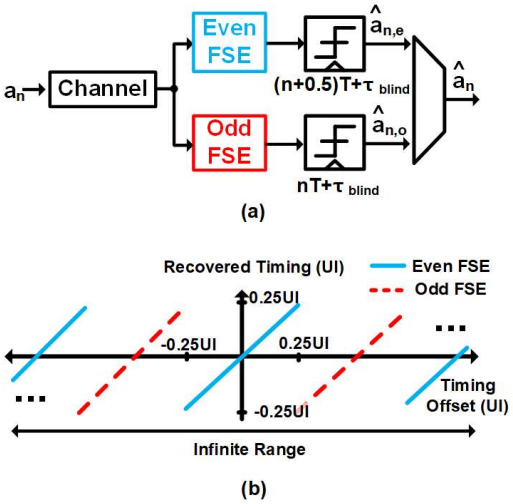


Figure 4.3: (a) Proposed 2× blind oversampling fractionally spaced equalizer (FSE) receiver, which supports plesiochronous systems; (b) recovered timing of the proposed FSE with a timing offset, which shows an infinite range of timing recovery.

the architecture, circuit implementation, and adaptation algorithm.

The proposed receiver was fabricated in a 28-nm CMOS and successfully operates at 8.3~9.1 Gb/s with a 100-ppm frequency offset between the data and blind sampling clocks. The receiver consumes 3.5pJ/bit of power and 0.10 mm^2 of area, and can compensate for up to 22-dB of channel loss at 4.5 GHz with a 0.2-UI_{pp} high-frequency jitter tolerance (JTOL) for a BER of less than 10^{-12}.

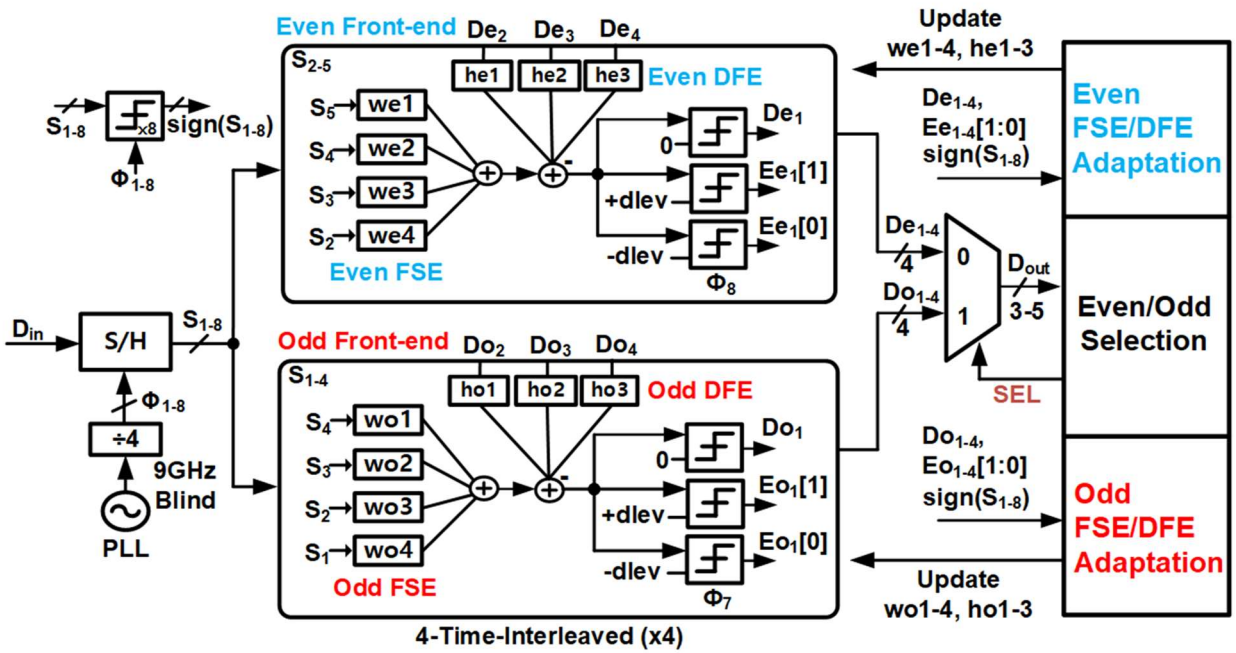


Figure 4.4: Overall architecture of the proposed fractionally spaced equalizer (FSE) receiver.

4.1. Receiver Architecture

The receiver architecture to support a plesiochronous system is illustrated in Figure 4.4. A four time-interleaved architecture is used to reduce the speed of each time-interleaved unit by a factor of 4. The reduced speed improves the comparator sensitivity and relaxes the bandwidth condition of key building blocks. Furthermore, the four time-interleaved architecture enables the use of a sample and hold (S/H) circuit [31, 32] for analog delay elements for each FSE tap. The 8-phase, quarter-rate blind clocks with 50% duty cycle ($\phi_{1\text{-}8}$) (Figure 4.5) are generated by frequency-dividing the 9-GHz differential full-rate clocks from a phase-locked loop (PLL). The receiver in this work demonstrates a full-rate architecture; however, an extension to a double-data-rate (DDR) architecture is also possible by using the half-rate quadrature clocks.

A quarter-rate S/H circuit is used to replace the analog delay line to reduce area and power dissipation. It samples and deserializes the incoming 9-Gb/s data stream into a set of eight, 0.5-UI spaced data samples ($S_{1\text{-}8}$) to establish a delayed version of input for each FSE tap, as shown in Figure 4.6. Using S/H as an analog delay element allows for lower power dissipation and smaller area than using an active delay cell or passive delay cell using inductors and capacitors [33]. The sampled value is quantized to a 1-bit digital signal $sign(S_{1\text{-}8})$ to give the polarity information of each FSE tap input to a sign-sign least-mean-square (SSLMS) adaptation engine.

To support an infinite range of timing recovery, the receiver employs two FSE/decision feedback equalizer (DFE) front-ends (the even and odd front-ends) that process the data samples from the S/H circuit. The even front-end and odd front-end have a 0.5-UI shifted timing relationship; the even front-end processes data samples (S_{i+1}-S_{i+4}) for which timings are 0.5-UI shifted from those of the odd front-end (S_i-S_{i+3}). Each front-end is composed of a 4-tap FSE and a 3-tap DFE with different sets of tap coefficients ($we_{1–4}$ and $wo_{1–4}$) that are independently adapted by the SSLMS algorithm. The FSE performs the 0.5-UI-spaced 4-tap FIR feedforward linear equalization as well as timing recovery. The DFE performs 1-UI-spaced, 3-tap additional ISI canceling by subtracting the post-cursor ISIs of the three previous data decisions from the FSE output. The data slicer generates the data signal (De_{1-4}, Do_{1-4}) to give the polarity information of each DFE tap input to the SSLMS adaptation engine. Two error slicers produce error signals (Ee_{1-4}[0], Ee_{1-4}[1]) that compare the equalized signal with the reference data levels (+*dlev* and −*dlev*). The error signals (Ee_{1-4}[1:0], Eo_{1-4}[1:0]) give the polarity information of the voltage errors to the SSLMS adaptation engine.

While each FSE has a limited timing recovery range, the alternate use of the two FSE enables an infinite range of timing recovery as shown in Figure 4.3. Before the amount of timing drift exceeds the limited timing recovery range of each FSE, the effective timing recovery range increases by 0.5-UI by changing the selection to the other FSE. The unselected FSE waits for the next selection and shifts the sampling position by 1-UI by resetting its coefficients. By repeating this process when every 0.5-UI of timing drift occurs, infinite timing recovery is achieved.

A multiplexer stage selects one 4-bit output (D_{out}) between those of the even front-end (D_{even}) and odd front-end (D_{odd}) as instructed by the adaptation engine via the selection signal (*SEL*). Each of the even/odd FSE/DFE front-ends recovers the data assuming that the optimal data timing is located in a different half-UI period and the overall receiver can recover data with an arbitrary

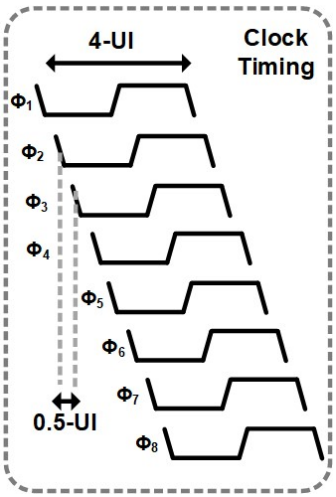


Figure 4.5: Timing diagram of clock signals.

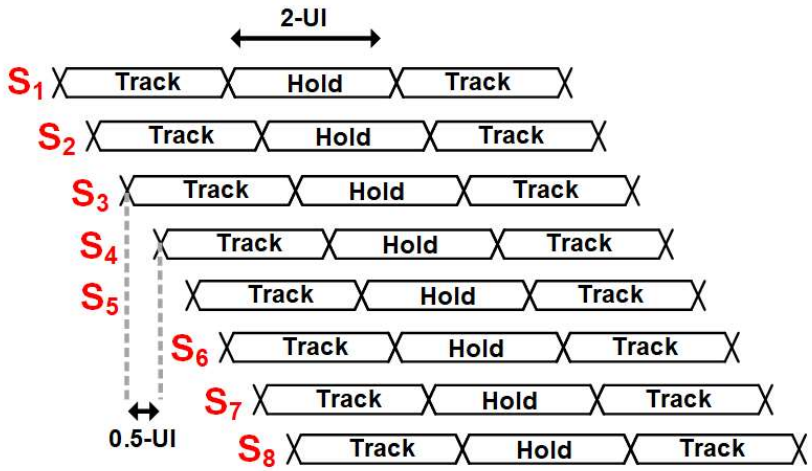


Figure 4.6: Timing diagram of sampled signals.

sampling timing by properly selecting one output. This multiplexer stage also inserts or deletes 1-bit data when a data underflow or overflow occurs owing to the frequency offset between the transmitted data and receiver sampling clock [34, 35].

We used several ways to reduce power consumption and improve the FoM. First, we tried to minimize the static current which causes a lot of power consumption. The most of the key building blocks of S/H, FSE and DFE consume dynamic powers only. Also, the receiver avoids using CTLE and current-mode summation which dissipate static currents. Second, S/H circuit helps implement FSE with low power. S/H is used to replace the analog delay line to reduce area and power dissipation. Using S/H as an analog delay element allows for lower power dissipation and smaller area than using an active delay cell or passive delay cell with inductors and capacitors. Third, the receiver does not use the loop-unrolling DFE architecture which increases the power

consumption and hardware complexity for DFE and decision operation. Instead, direct feedback DFE is used. It is enabled by using a multi-input regenerative latch circuit, which performs the 3-tap DFE operation. By performing the summation within the latch, the signal summation is accomplished with the lower power and higher speed than using the additional current-mode summation stage.

4.2. Circuit implementation

4.2.1. S/H Circuit

The S/H is composed of PMOS switches and storage capacitances, as shown in Figure 4.7 [31], which depicts a half circuit schematic of S/H for simplicity. There is one main sampling switch (M1) and three dummy transistors (M2–4) to cancel the charge injection. M2 and M3 cancel the clock feedthrough by

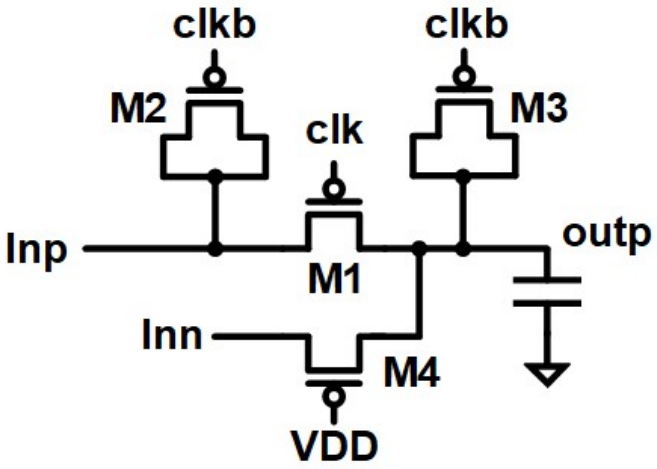


Figure 4.7: Half circuit schematic of the sample and hold (S/H) circuit.

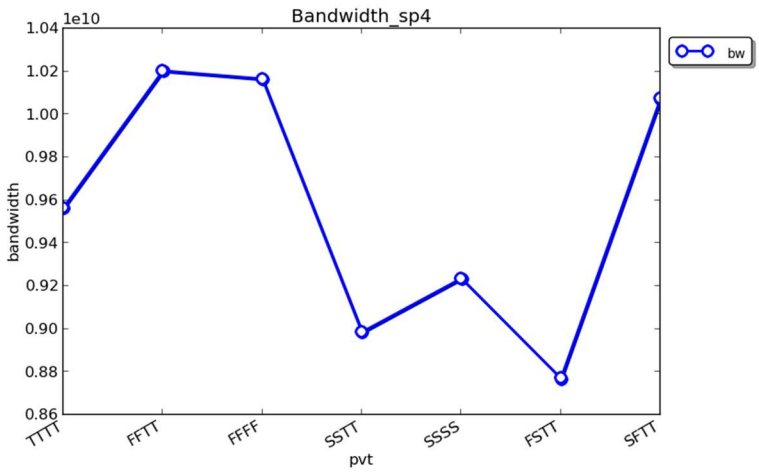


Figure 4.8: Bandwidth of S/H circuit with various PVT corner.

connecting the complementary clock (*clkb*) to their gates. M4 cancels the differential data feedthrough during the hold phase by connecting the complementary input to the drain. When the clock (*clk*) is low, the output tracks the input voltage by charging the output capacitor; when the clock is high the output holds the sampled input value. To mitigate the effect of charge injection from FSE and kT/C noise at the output, a large capacitance of 60fF is used as an output capacitor. The size of the pass gate (M1) is determined as W/L = 1.2um/0.06um to achieve a worst-case bandwidth across all PVT corners of more than 8 GHz as shown in Figure 4.8.

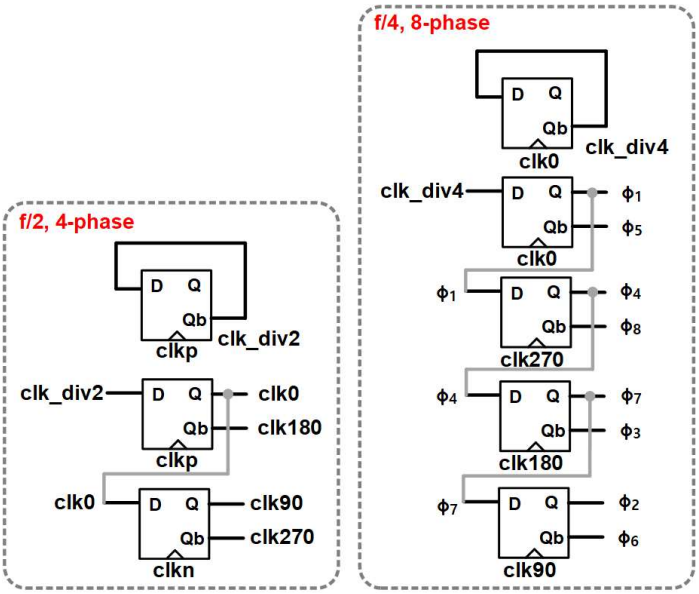


Figure 4.9: Eight-phase clock generator.

4.2.2. Eight-Phase Clock Generator

The 8-phase, quarter-rate blind clocks ($\phi_{1\text{-}8}$) are generated by frequency-dividing the 9-GHz differential full-rate clocks (*clkp*, *clkn*), as shown in Figure 4.9. The timing relationships of the 8-phase clocks ($\phi_{1\text{-}8}$) are shown in Figure 4.5. First, the differential full-rate clocks (*clkp* and *clkn*) are divided by 2 using a D flip flop. Then, the 4-phase clocks (*clk0, clk90, clk180*, *clk270*) are generated by retiming the divided clock (*clk_div2*) with the full-rate clocks (*clkp*, *clkn*). Then, the clk0 is used to generate divided-by-4 clocks (*clk_div4*). Finally, the 8-phase clocks ($\phi_{1\text{-}8}$) are generated by retiming the divided-by-4 clocks (*clk_div4*) with the 4-phase clock (*clk0, clk90, clk180* and *clk270*). To maximize setup timing margin, the retiming are sequenced in order of *clk0*, *clk270*, *clk180*, *clk90*.

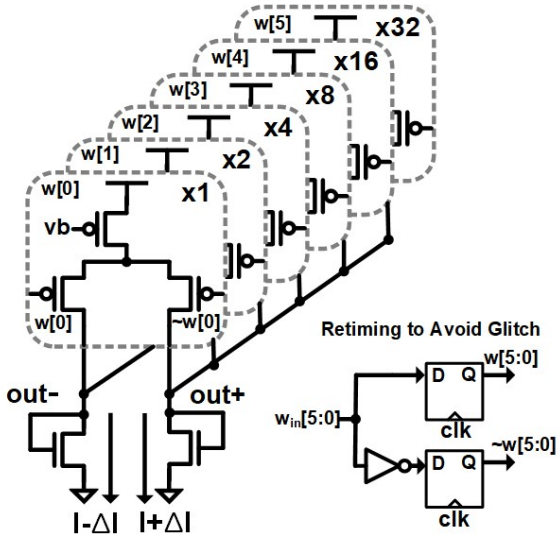


Figure 4.10: 6-bit current steering DAC.

4.2.3. 6-bit Current Steering DAC

The 6-bit current steering DAC is composed of 63 PMOS current sources, 63 differential pair switches and 2 diode-connected NMOS loads. Each unit current is steered either to the *out*+ or to the *out*- node by the differential pair switches. Hence, the differential currents ($I+\Delta I$, $I-\Delta I$) are binary-coded controlled by a 6-bit digital code (w[5:0]). Figure 4.10 shows the 6-bit current steering DAC. The binary-weighted current control may have undesirable performance degradation when the 6-bit control code has glitches. For example, when w[5:0] is changed from 100000 to 011111, the difference in the switching timings may result in a large fluctuation of the nodes *out*+ and *out*-. To make glitch-free switching of w[5:0], six retiming flip-flops are used.

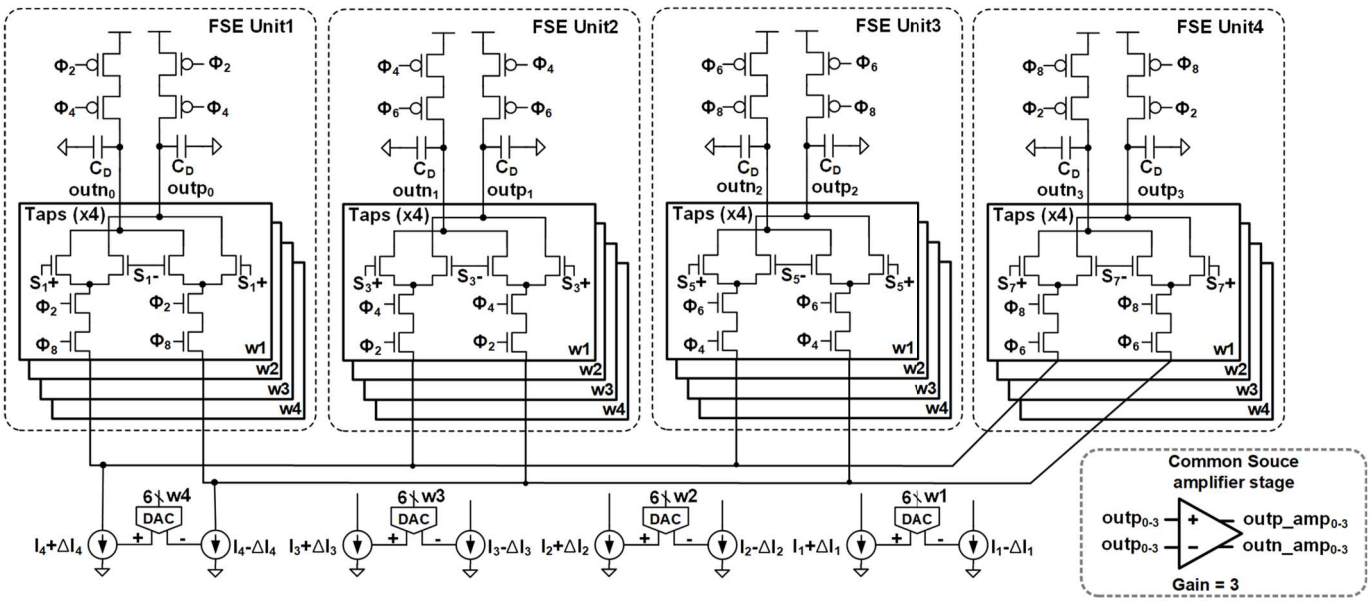


Figure 4.11: Diagram of a 4-tap fractionally spaced equalizer (FSE) front-end circuit.

4.2.4. 4-tap FSE Circuit

The weighted summation required by the 4-tap FSE is performed by a low-power, current-integrating summer circuit [31, 36]. Figure 4.11 illustrates the 4-tap FSE circuit and its timing diagram is shown in Figure 4.12. The FSE circuit is composed of four time-interleaved units that are triggered by different clocks ($\phi_{1\text{-}8}$). Each input (S_i–S_{i+3}) from S/H drives a set of two differential input pairs that differentially discharge the outputs ($outp_{1\text{-}4}$ and $outn_{1\text{-}4}$) depending on the difference between their bias currents. Since these bias currents ($I_{1\text{-}4}+\Delta I_{1\text{-}4}$)

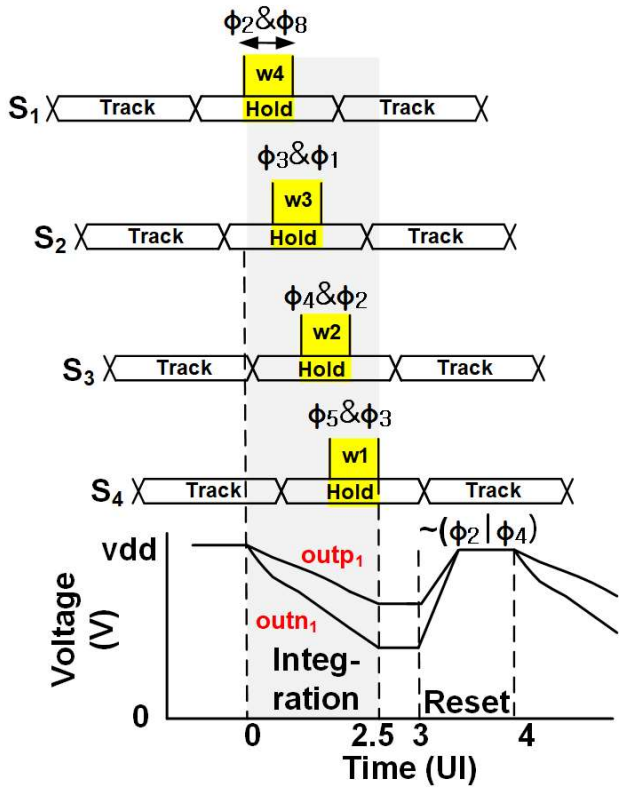


Figure 4.12: Timing diagram of 4-tap fractionally spaced equalizer (FSE) circuit.

are controlled differentially by a 6-bit weight code via a current-steering DAC, the overall circuit can compute the weighted sum of four inputs. The designed minimum common mode voltage of the outputs ($outp_{1\text{-}4}$ and $outn_{1\text{-}4}$) is 624mV and the opening voltage is 216mV as shown in Figure 4.15.

The operation is sequenced by the multi-phase clocks (ϕ_1–ϕ_8). First, in the reset phase, the output voltages are pre-charged to the supply voltage. Then in

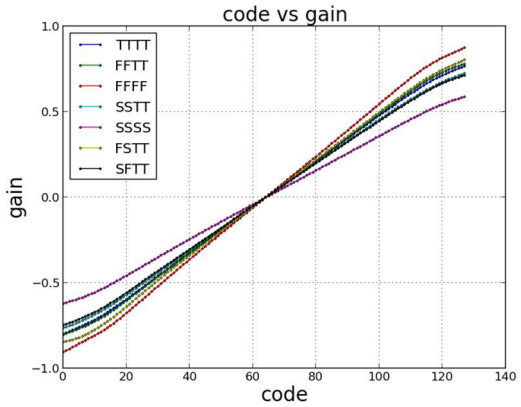


Figure 4.13: The weight of each tap controlled by a 6-bit weight code.

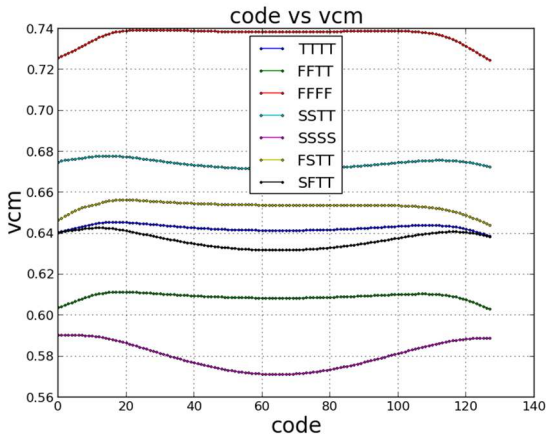


Figure 4.14: The common mode voltage of FSE with a 6-bit weight code.

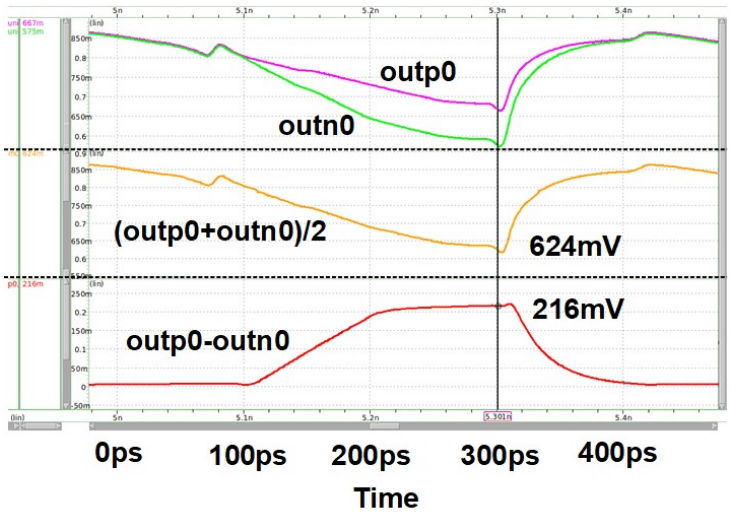


Figure 4.15: The simulated waveform of FSE outputs (outp0 and outn0)

the integration phase, each FSE input sequentially discharges the output weighted by each FSE tap coefficients (*w1-4*). The integration time for each tap is located in the middle of the hold period of S/H to ensure the largest timing margin. Since each FSE unit integrates a given input contribution at different intervals, the four FSE units in each even/odd front-end can share the same current source devices. This current sharing not only reduces the static current of the current source but also mitigates the mismatch caused by the 6-bit current steering DAC and the current source.

One important consideration for this current integrating summer is that the gain of each tap will decrease as the number of tap increases due to the fixed output voltage range allowed for discharge. To mitigate this lowered gain, a common-source amplifier stage is added to provide an additional gain of 3 to the output value. Figure 4.13 plots the overall amplified weight value as the DAC code varies

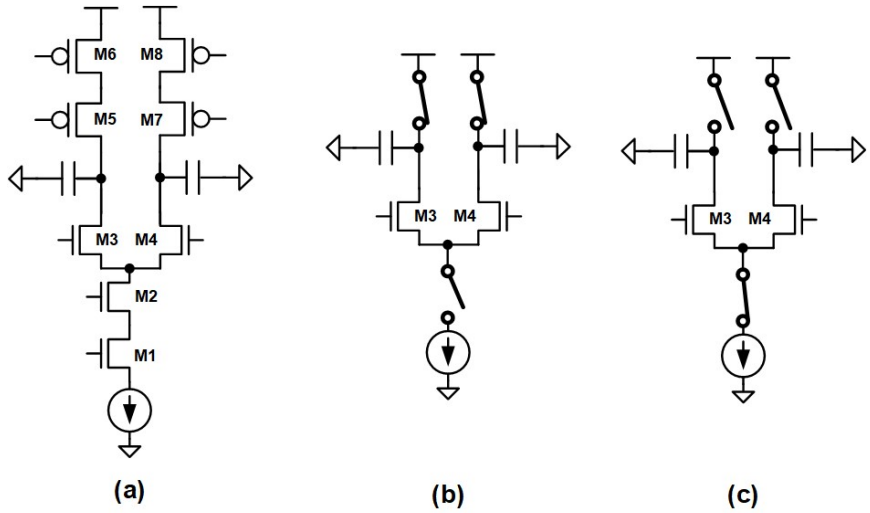


Figure 4.16: Diagram of FSE tap. (a) FSE circuit, (b) FSE circuit in reset phase, (c) FSE circuit in integration phase.

While the circuit of FSE is composed of more than 5 stacked MOSFETs as shown in Figure 4.16(a), the FSE can perform the fast operation and have enough voltage headroom with low VDD because most of stacked MOSFETs are used as switches that turn on or off depending on the operation phase. In the reset phase (Figure 4.16(b)), M5-8 are shorted and pre-charge the capacitor load and M1-2 are opened. In the integration phase (Figure 4.16(c)), M5-8 are opened and M1-2 are shorted to discharge the capacitor load. In this state, it is similar to operate as common source amplifier with capacitor load which is composed of only 2 stacked MOSFETs.

4.2.5. Multi-Input Regenerative Latch For 3-tap DFE

Figure 4.17 describes a multi-input regenerative latch circuit [6], which performs the 3-tap DFE operation. This circuit is a StrongARM latch that performs a static-current-free signal summation during the sampling aperture period.

The slicer has a total of six input pairs driven by one main input (*in*), three DFE feedback inputs (*h1–3*), one data-level reference input (*dlev*), and one offset input for calibration (*off*). The main input (*in*) samples the FSE output. The three DFE feedback inputs (*h1-h3*) receive the three previous data decision (D_{n-1}, D_{n-2}, D_{n-3}) from other regenerative latches. The three post-cursor ISIs are

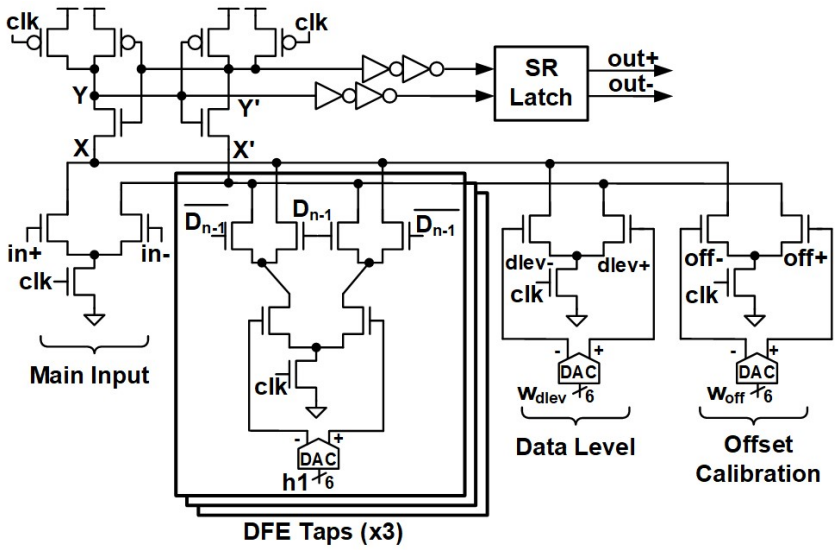


Figure 4.17: Multi-input regenerative latch circuit for a 3-tap decision feedback equalization.

subtracted, which realizes a 3-tap direct feedback FIR DFE. The data-level reference input (*dlev*) is only used for the error comparator, which generates the error signal for the SSLMS adaptation. The error comparator compares the equalized signal with the data-level reference (*dlev*). The offset input (*off*) compensates the offset caused by device mismatch.

The amount of DFE subtraction, data level reference, and offset calibration is weighted by a 6-bit digital code (*h1-3*, w_{dlev}, w_{off}) that controls the differential currents of the current-steering DAC. Figure 4.18 shows the simulated threshold of the comparator as the offset code varies. The control range of the offset calibration is determined to cover the whole range of the offset. The Monte-Carlo simulation shows the offset's standard deviation of 17mV (Figure 4.19).

The operation of the clocked regenerative latch is as follows. When the clock (*clk*) is low, the voltages of *X*, *X'*, *Y,* and *Y'* are pre-charged. When the clock (*clk*) rises, the current differences steered by the input pairs are linearly added

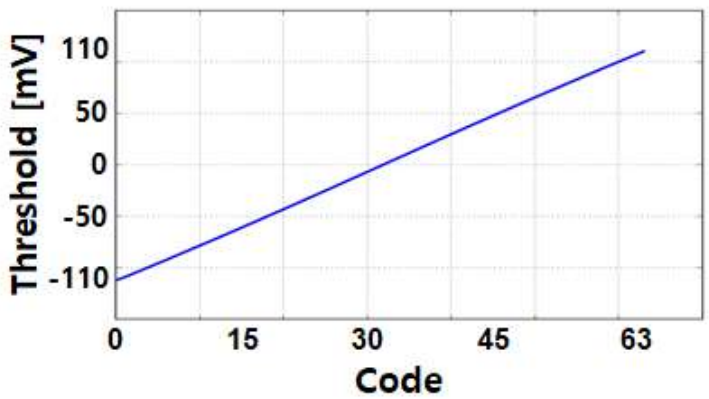


Figure 4.18: Simulated threshold of the comparator controlled by a 6-bit code.

and discharge the pre-charged nodes *X* and *X'*. Depending on the sum of the input differences, the discharging rates of the *X, X', Y*, and *Y'* nodes are determined. The final decision is made by the two cross- coupled inverters via

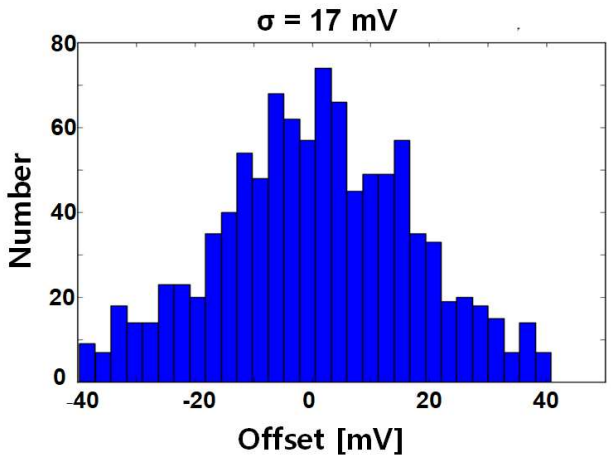


Figure 4.19: Monte-Carlo simulated histogram of the multi-input regenerative latch input-referred offset.

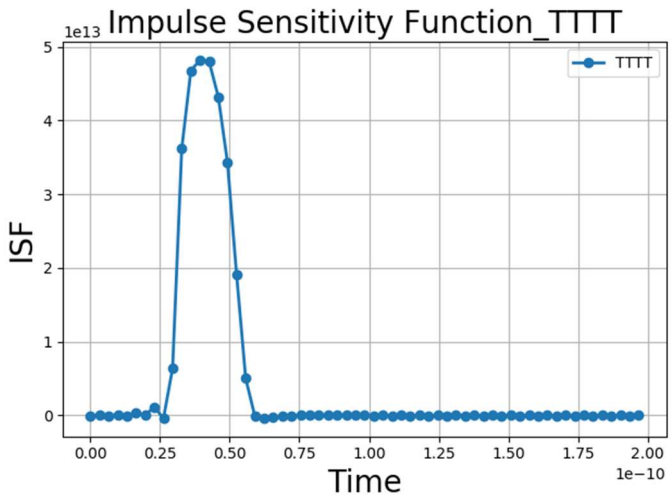


Figure 4.20: The simulated impulse sensitivity function of the regenerative latch.

regeneration based on the voltage difference between *Y* and *Y'* node. The bandwidth of the comparator is not deteriorated by the increased number of parallel input pairs [6]. The total capacitance (*C*) and discharging current (*I*) on the internal node *X* and *X'* increase together as the number of input pairs increases. The sampling aperture is almost unchanged because it is determined by the ratio between capacitance and current (*C*/*I*) [19]. Also, the regeneration bandwidth has little dependency on the number of input pairs because it is largely determined by the capacitance on *Y* and *Y*' [19].

By performing the summation within the latch, the signal summation is accomplished with lower power and higher speed as compared with using the additional current-mode summation stage. Also, the loop-unrolling architecture can be avoided owing to fast timing to close the DFE feedback, which further simplifies the hardware and reduces power.

As shown in Figure 4.17, the X and X ' nodes are totally discharged when the

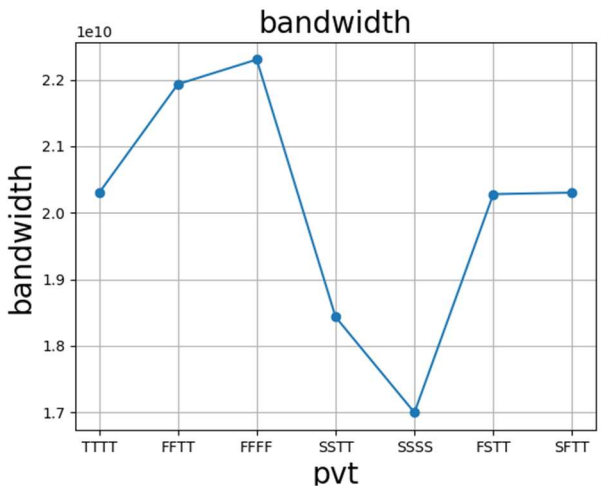


Figure 4.21: The simulated bandwidth of the regenerative latch.

clock rises, and the regeneration starts in the Y and Y' nodes depending on which node of X or X' is discharged faster. By this operation, the regenerative latch acts as a quantizer to quantize the input signal to decide whether the input signal is larger or smaller than the threshold of the latch. Therefore, even if un-equalized relatively large-swing data comes, the latch does not need large capacitance at node X because it does not need to produce linear output at node X and X'.

For DFE circuit shown in Figure 4.17, the circuit operates in three operation phases, which are reset phase, sampling phase and regeneration phase. In reset phase, X and X' is pre-charged. In sampling phase, each input pairs dis-charges X and X'. In this phase, the reset MOSFET and cross-coupled inverters for regeneration do not affect the voltage headroom of differential input pairs. Therefore, it is similar to operate as common source amplifier with capacitor load which is composed of only 2 stacked MOSFETs.

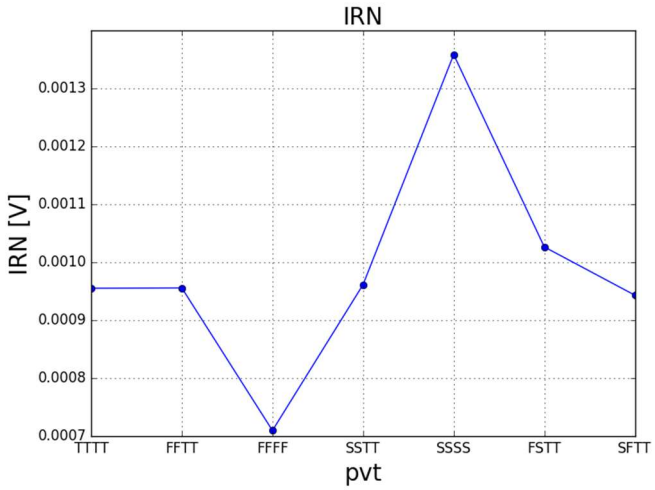


Figure 4.22: The simulated input referred noise of the regenerative latch.

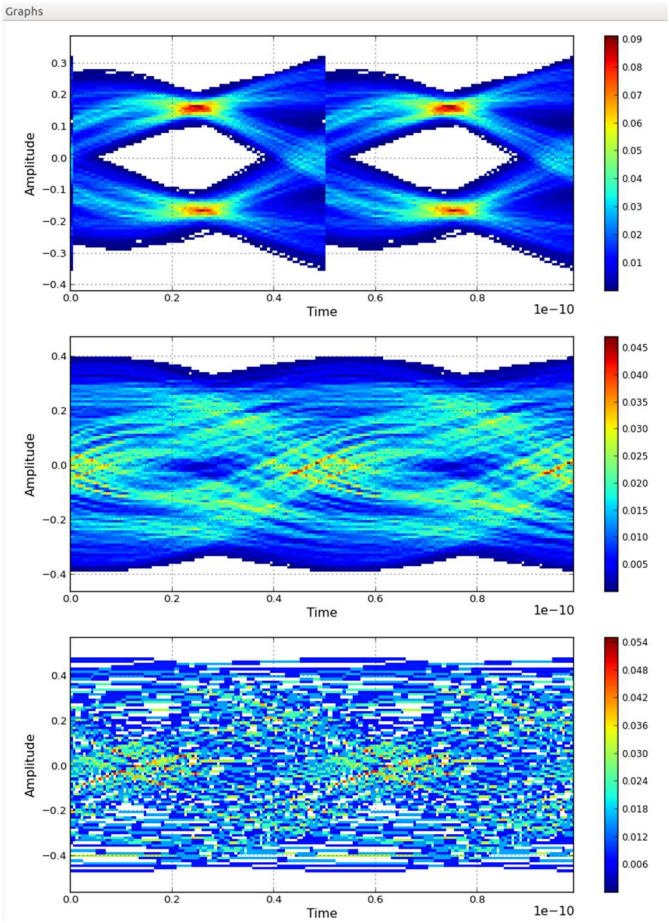


Figure 4.23: The simulated eye diagram of equalized signal after DFE (up), equalized signal after FSE (middle), un-equalized signal (bottom).

Figure 4.20 shows the simulated impulse sensitivity function of the regenerative latch. From the ISF, the bandwidth and input referred noise can be simulated as shown in Figure 4.21 and 4.22.

Figure 4.23 shows the simulated eye diagram of equalized signal after DFE and FSE. At first, the unequalized signal has entirely closed eye opening, but after the DFE and FSE, the signal is equalized and has wide eye opening.

4.3. FSE/DFE Adaptation and Even/Odd Selection Algorithm

4.3.1. FSE/DFE Adaptation Algorithm

The adaptation of FSE and DFE is performed via a SSLMS algorithm [38] to serve two purposes simultaneously: equalizer adaptation and timing calibration. The SSLMS algorithm reduces hardware complexity since it requires only the polarity information of the error signals ($Ee_{1\text{-}4}$ and $Eo_{1\text{-}4}$) and the input signals scaled by the FSE/DFE taps ($S_{1\text{-}8}$, $De_{1\text{-}4}$ and $Do_{1\text{-}4}$). Figure 4.24 shows a block diagram of the SSLMS adaptation engine. The first-stage multiplexers select the proper error signals according to the current data. If the datum is 1, the error signal is selected to $Ee_{1\text{-}4}[1]$, which is compared with $+dlev$. Otherwise, if the datum is 0, the error signal is selected to $Ee_{1\text{-}4}[0]$, which is compared with $-dlev$. The subsequent XNOR gates compute the update directions $up_w[3:0]$ and $up_h[3:0]$ for the FSE and DFE taps according to the following SSLMS formula:

$$w_{n+1} = w_n - sign(e)\cdot\mathrm{sign}(s), \qquad (8)$$

where w is the FSE/DFE tap coefficient, e is the error signal, and s is the input

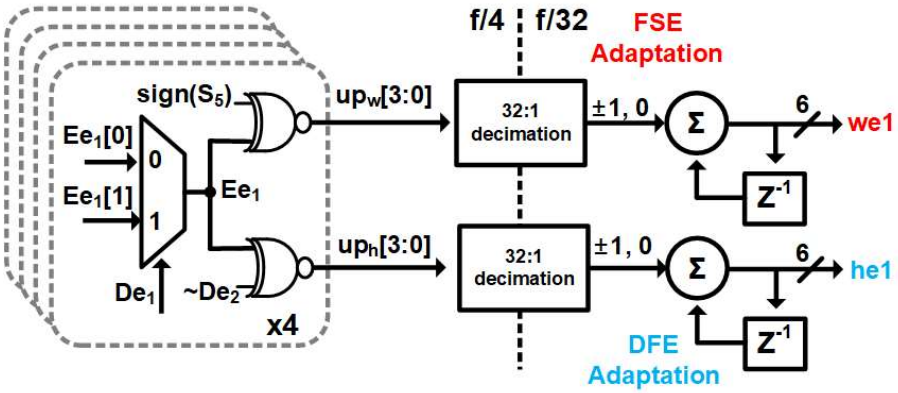


Figure 4.24: Block diagram of the sign-sign least-mean-square (SSLMS) adaptation engine.

signal scaled by w. To lower the operating frequency of the synthesized digital adaptation engine and reduce possible dithering of the tap coefficient values, a set of 32:1 decimation filters aggregate 32 update directions before updating each 6-bit FSE/DFE tap coefficient.

This 32:1 decimation makes the update period T_{update} equal to $32 \cdot T$ since the 32 of up and down signal is decimated to one of up or down signal. Also, the number of bits for the FSE/DFE tap coefficients makes Δw equal to 1/32, the amount of change in the FSE weights per update.

The maximum frequency offset that FSE receiver can track is determined by the bandwidth of the FSE receiver. The bandwidth is related to two design parameters, which are the update period (T_{update}) and the update step (Δw) ($H(s) = \frac{1}{1 + s/p}, \quad p \approx \frac{K_{slicer} \cdot \Delta w}{T_{update}}$) as shown in Figure 3.10 and 3.11. For faster tracking ability, a smaller update period (T_{update}) and larger update step (Δw) are necessary for higher bandwidth. However, the update period (T_{update}) has a lower limit due to the timing constraint of the synthesized digital block for the

adaptation logic. Also, the update step (Δw) has a upper limit because the larger update step increases dithering and quantization noise. The operation of the proposed FSE receiver is limited for frequency offsets about 100 ppm

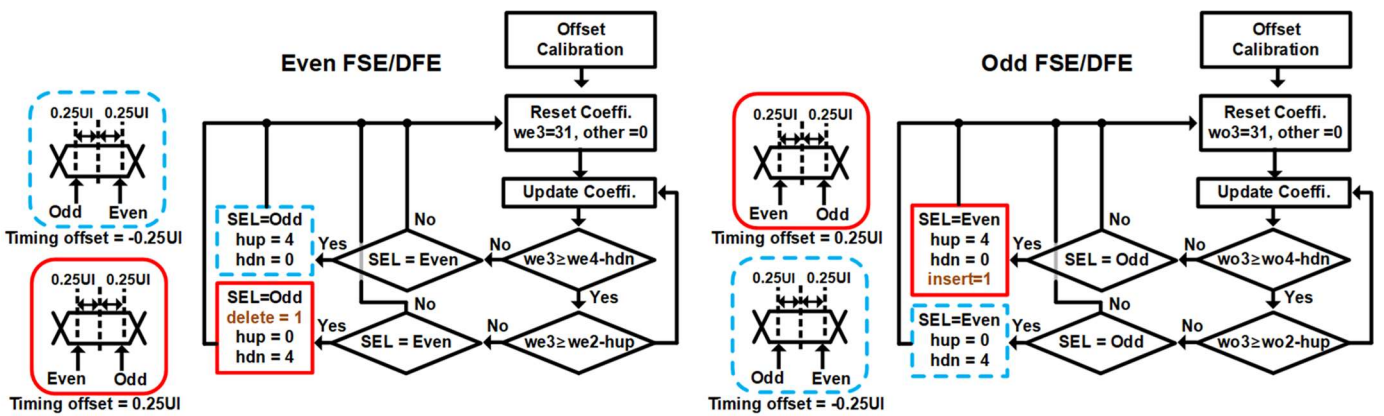


Figure 4.25: Flowchart illustrating the selection algorithm.

4.3.2. Even/Odd Selection Algorithm

In this architecture, the key decision is to decide whether the final output D_{out} should be selected from the even or odd front-end. To estimate which front-end is more appropriate, the decision is made based on the currently adapted values of the even/odd FSE tap coefficients. Figure 4.26(a) shows that each front-end is designed to cover a different half-UI range of the timing offset between the data and blind-sampling clock. To let the FSE suppress the pre-cursor ISI while the DFE cancels the post-cursor ISI, the FSE uses two pre-cursor taps and one post-cursor tap while the third tap is used as the main cursor tap. As the amount of timing drift increases, the adjacent tap value slightly increases and eventually the third tap coefficient of the currently-selected front-end no longer has the largest tap coefficient value. This is the time when the selection is switched; that is, when the timing offset is about ±0.25 UI, which is the ideal point to make a switch between the two front-ends while maximizing the overall timing margin. However, if the timing offset is near ±0.25-UI, the selection may have redundant switching due to noise or dithering. To avoid redundant switching at ±0.25-UI, a hysteresis of 1/32-UI is applied by adding or subtracting the offset of 4, as shown in Figure 4.26(b).

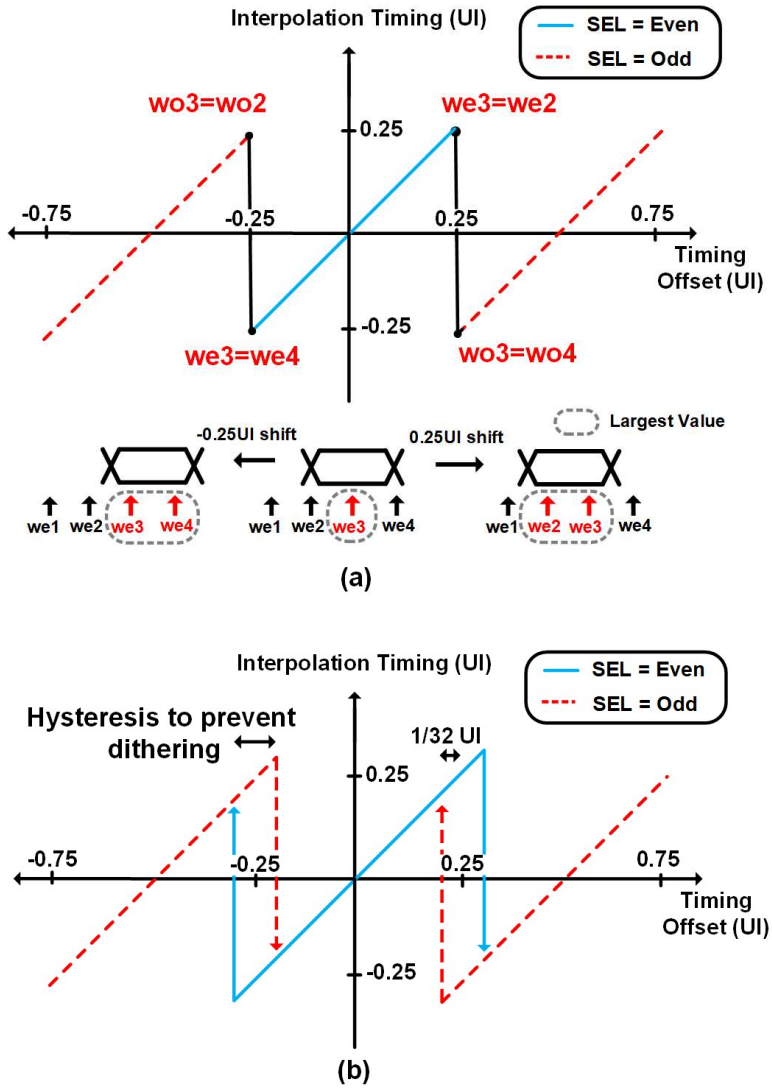


Figure 4.26: (a) Selection of even/odd front-ends versus the timing offset between data and blind sampling. (b) Selection of even/odd front-ends with hysteresis.

Figure 4.25 shows the flowchart of the proposed front-end selection algorithm. When an even or odd front-end is first selected, its third tap coefficient is initialized to the maximum value of 31 while all others are reset to 0, and the SSLMS adaptation begins. The algorithm keeps the current selection as long as the third tap coefficient has the largest value. When it becomes smaller than one of the other tap coefficients owing to the timing drift, the algorithm switches the selection. The unselected front-end prepares for the next selection by resetting its coefficients. As discussed, the algorithm also inserts or deletes 1-bit data as necessary to address data underflows or overflows. As illustrated in Figure 4.27, when the transmit frequency is higher than the receive frequency, a data overflow may occur while the multiplexer

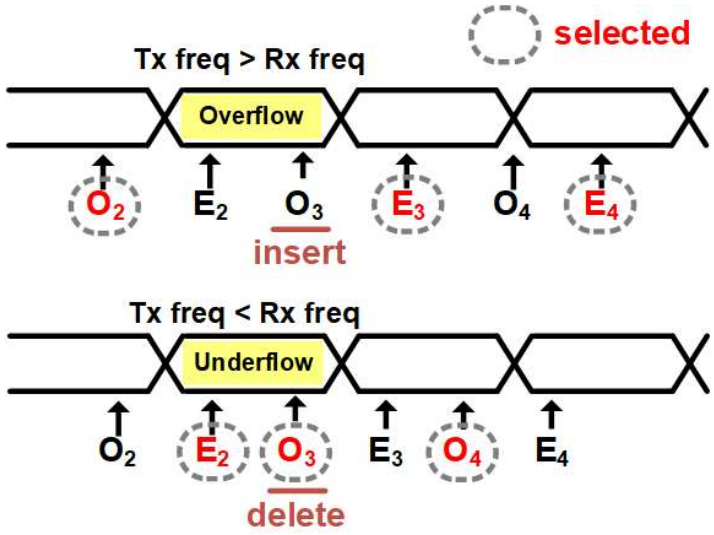


Figure 4.27: Illustration of data overflow/underflow cases when there is a frequency offset between the transmitted data and the receive clock.

selection is switched from odd to even. In this case, the multiplexer adds the lost bit (O_3) back to the output data stream. On the other hand, when the transmit frequency is lower, the same data bit can be selected twice while the selection is switched from even to odd. In this case, the multiplexer stage deletes the duplicate bit from the output data stream.

One overflow or underflow occurs for every 1-UI phase drift between the transmitted data and sampling clock as shown in Figure 4.28. On the other hand, a switch between the even and odd selections occurs every 0.5 UI phase drift. Therefore, one delete or insert operation is expected to occur for every two selection switching. Let's assume that the period of input data is 110ps and the

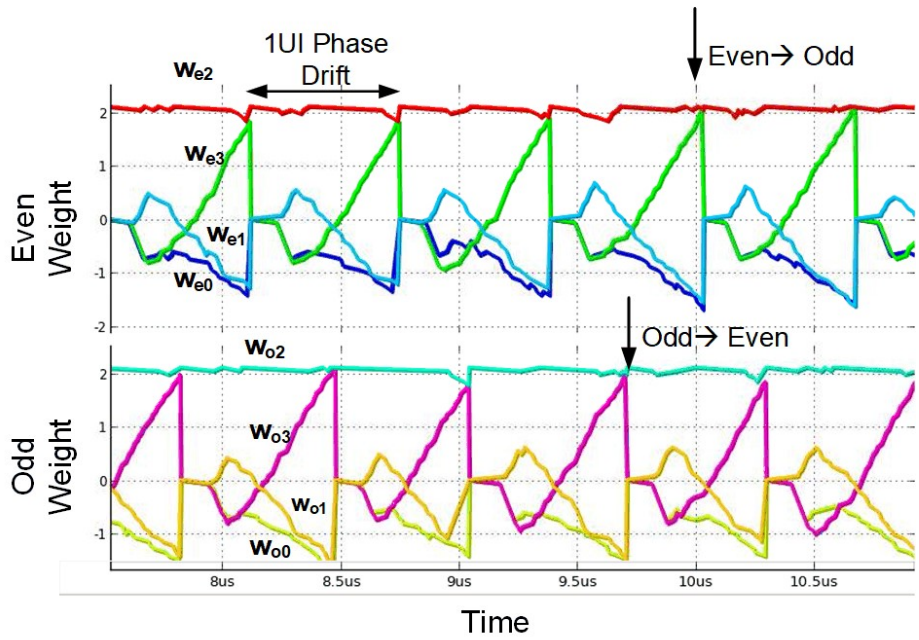


Figure 4.28: The simulation of transient locking transient for even/odd FSE when there is a 100ppm frequency offset between the transmitted data and the receive clock.

period of the RX sampling clock is 100ps. The first even-to-odd selection occurs when the first 0.5-UI drift happens at about 550ps. At this point, both the numbers of transmitted data bits and sampled data bits are 5, there is no overflow and the delete operation need not happen. Eventually, the 1-UI phase drift happens at 1100ps and the selection is changed from odd back to even.

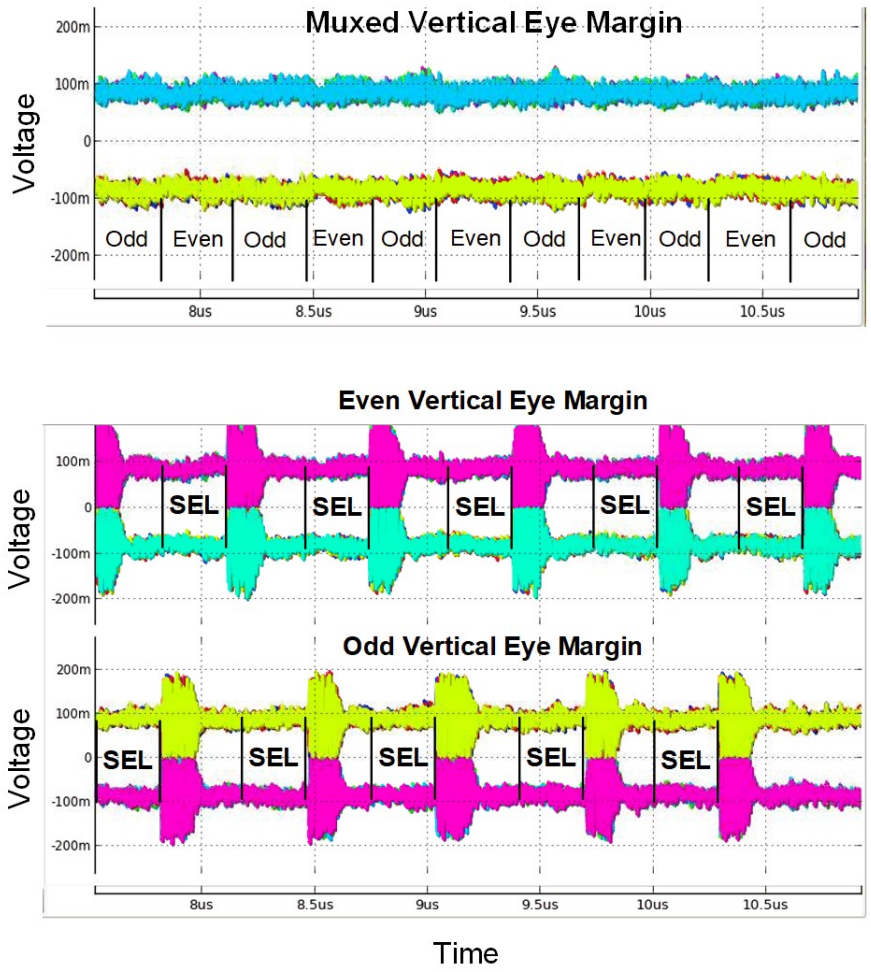


Figure 4.29: The simulated vertical eye margin of multiplexed data and even/odd FSE output when there is a 100ppm frequency offset between the transmitted data and the receive clock.

This time, one-bit overflow indeed happens and the delete operation needs to be performed. Figure 4.29 shows the simulated multiplexed eye has wide vertical eye margin while there is the 100ppm frequency offset between transmitted data and sampling clock.

4.4. Measurement Results

The prototype chip was fabricated using 28-nm CMOS technology, and its die photograph is shown in Figure 4.31(b). Figure 4.30 shows the measurement setup. The receiver was tested by feeding a 9 Gb/s, 2^{31}-1 PRBS pattern generated by a bit-error-rate tester (BERT). The receiver inputs were driven with 0.3-V_{PP} differential input signals with 0.55V common mode. The tested channels are 7.5-, 20- and 25-inch long FR4 microstrip PCB traces. The frequency response of the channels are shown in Figure 4.31(a). The channel loss at a Nyquist frequency of 4.5 GHz are 9.5, 15.1, and 22.3dB for 7.5-, 20- and 25-inch long FR4 channels, respectively. The BER is measured with an on-chip PRBS checker and an oscilloscope. The receiver including the S/H circuit, two FSE/DFE front-ends, and digitally synthesized adaptation engine consumes power of 31.5mW and has an active area of 0.10 mm^2, operating at a 0.85 V supply. The PLL supplying the blind-oversampling clocks consumes 17mW.

Figure 4.32 shows the measured FSE/DFE tap coefficient values while sweeping the timing offset between the blind sampling clock and input data when the 25-inch FR4 channel is used. Each front-end covers a different half

UI and the selection between the even an d odd frontend is switched when the third tap (*w3*) becomes smaller than the adjacent taps (*w2*, *w4*). Figure 4.33 shows the vertical eye opening of the equalized signal at the input of the regenerative latch for a BER of 10^{-12} while sweeping the timing offset. The

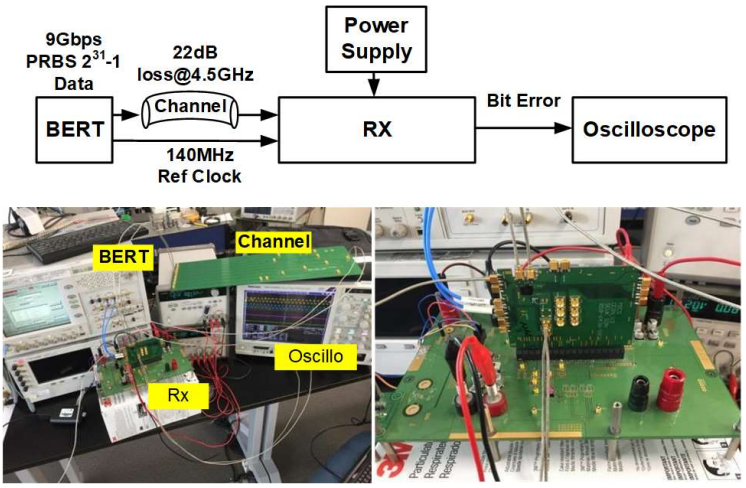


Figure 4.30: Measurement setup.

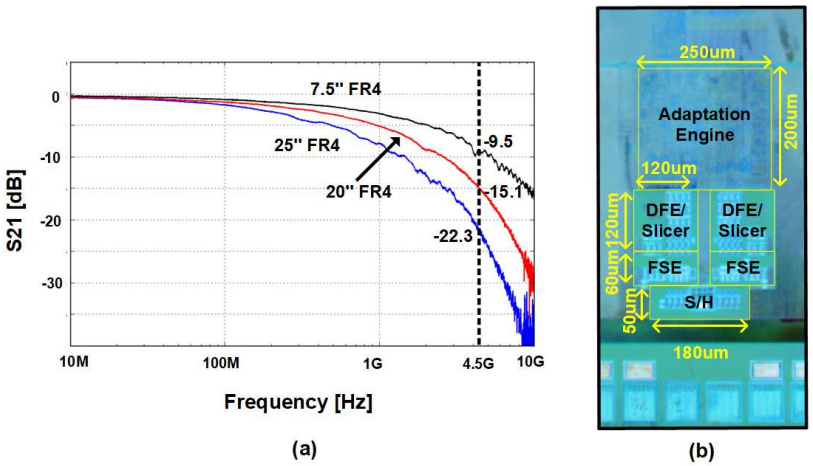


Figure 4.31: (a) Frequency response of 7.5-, 20-, and 25-inch FR4 micro strip PCB channels. (b)Die photograph.

voltage margin is measured by adjusting the input-referred offset of the regenerative latch and finding the minimum offset voltage that causes a bit-error. The input-referred offset is adjusted by using the offset code to find voltage margin of the regenerative latch. The input-referred offset value with the offset code is measured by finding DC input voltage value that make the regenerative latch generate toggling output. The worst-case voltage margin of

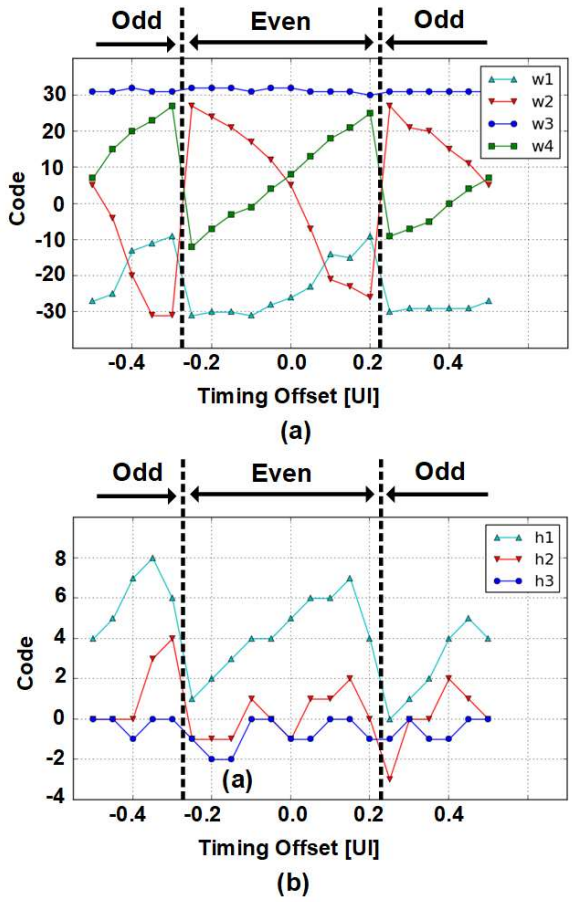


Figure 4.32: Measured trajectories of (a) the fractionally spaced equalizer (FSE) / (b) decision feedback equalizer (DFE) tap coefficients at each timing offset position.

$80mV_{pp}$ is achieved across all timing offsets. Figure 4.34 shows the measured BER bathtub curves; 7.5-, 20-, and 25-inch FR channels result in 0.2-UI, 0.24-UI, and 0.31-UI horizontal eye openings, respectively, with a BER of 10^{-12}.

Figure 4.35 shows the measured transient waveforms of the bit-error signals

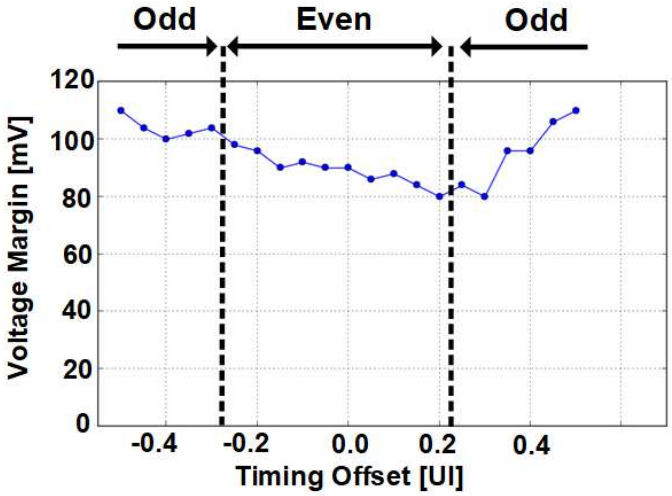


Figure 4.33: Voltage margin of the proposed receiver at each timing offset position.

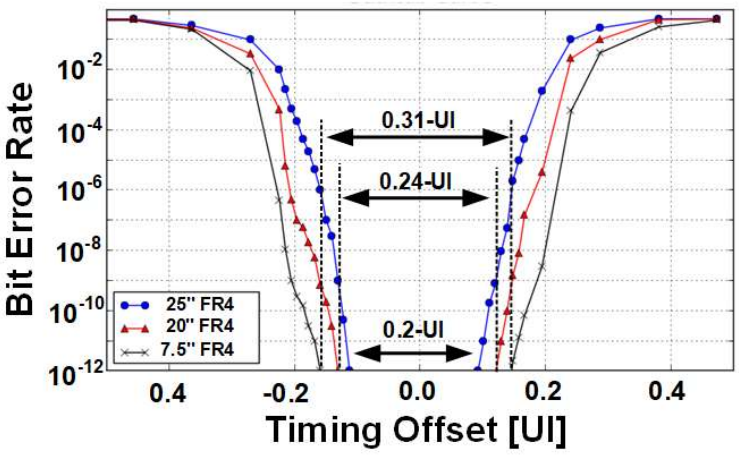


Figure 4.34: Measured bathtub curve with 7.5-, 20-, 25-inch FR4 channels.

of the even/odd front-ends and the selection signal (SEL) when the receiver operates with a 100ppm frequency offset between the data and blind-sampling clock; this demonstrates that the receiver can operate in a plesiochronous mode by supporting an infinite range of time adjustments. As expected, the receiver

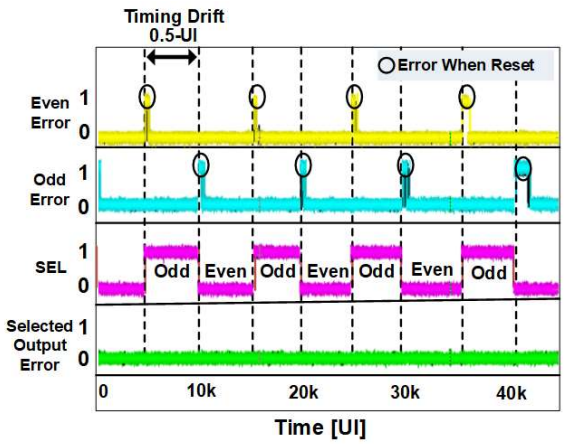


Figure 4.35: Measured waveforms of the bit-error and selection (SEL) signals with 100ppm frequency offset, demonstrating the infinite-range operation of the proposed receiver.

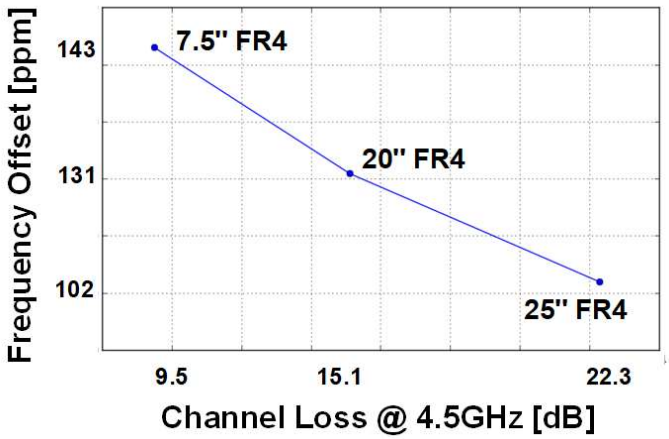


Figure 4.36: Maximum amount of frequency offset that the receiver can operate with BER of 10^{-12}.

periodically alternates its selection between the even and odd front-ends. While the unselected front-end may produce momentary bit errors because it resets its coefficients and waits for the next selection, the final multiplexed output from the selected front-ends is free of bit errors. Figure 4.36 shows the maximum

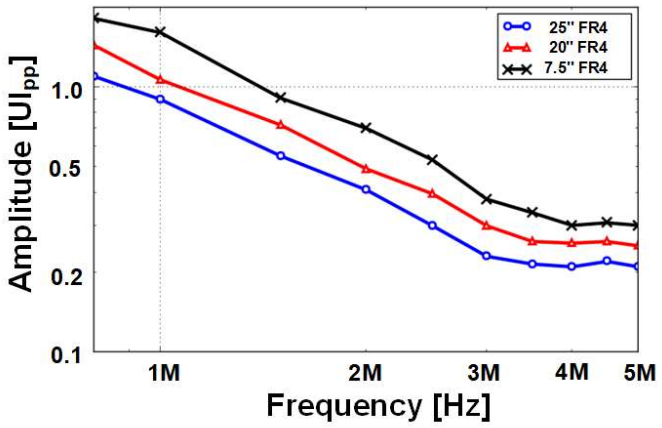


Figure 4.37: Measured jitter tolerance curve with 7.5-, 20-, 25-inch FR4 channels.

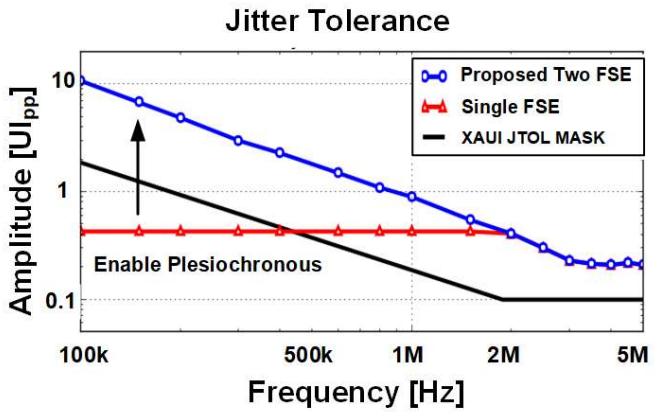


Figure 4.38: Measured jitter tolerance compared with the proposed fractionally spaced equalizer (FSE) receiver and previous FSE receivers.

amount of frequency offset that the receiver can operate with a BER of 10^{-12}. This shows the maximum amount of frequency offset that the receiver can track is decreased as the channel loss increases, as our analysis in Section II suggests.

Figure 4.37 shows the jitter tolerance (JTOL) curves with the 7.5-, 20-, 25-

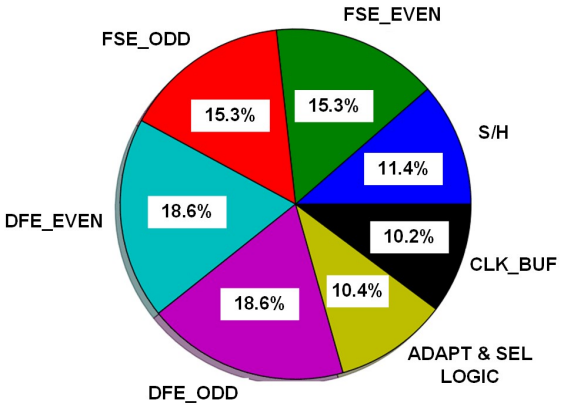


Figure 4.39: The simulated power breakdown.

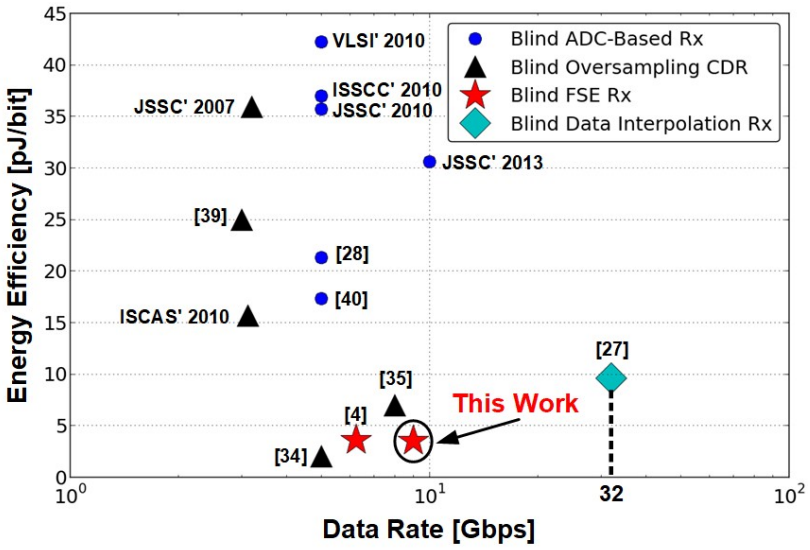


Figure 4.40: Comparison of the energy-efficiency values (pJ/bit) with blind sampling receivers.

inch long FR4 channels. The JTOL curve moves down as the channel loss increases. Figure 4.38 compares the JTOL between the proposed FSE receiver that uses two FSEs and the conventional single FSE receiver when the 25-inch FR4 channel is used. In the high frequency region, the proposed receiver and previous FSE receiver show the same performance, but in the low frequency region, the previous FSE receiver could not satisfy this JTOL mask because of its limited timing recovery range.

Table 4.1 compares the proposed receiver with the previously reported blind-sampling receivers. While the applications of the previous FSE receivers were limited to mesochronous systems, the proposed FSE receiver can support plesiochronous systems as well. The proposed FSE receiver achieves the best figure-of-merit (FOM) among the blind-sampling receivers. Figure 4.40 shows that the proposed receiver has a competitive power-efficiency when compared with various kinds of blind-sampling receivers such as the blind ADC-based receivers, blind-oversampling CDRs, blind FSE receivers, and blind data interpolation receivers.

The simulated power breakdown is illustrated in Figure 4.39. If the RX uses only single frontend, the power of DFE/FSE and adaptation/selection logic will be reduced to half. Therefore, about 39.1% from total power is used to as additional power consumption for the plesiochronous operation.

	This Work	[4]	[27]	[34]	[35]	[39]	[28]	[40]
Technology	28-nm	90-nm	28-nm	22-nm	28-nm	90-nm	65-nm	65-nm
Data Rate (Gbps)	9	6.25	32	5	8	3	5	5
Loss@Nyquist (dB)	22	N/A	22.3	8	N/A	N/A	20	12.9
CDR Type	FSE	FSE	Data-interpolation	Blind-oversampling	Blind-oversampling	Blind-oversampling	ADC-based	ADC-based
Plesiochronous	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
EQ Type	4-tap FSE 3-tap DFE	2-tap FSE 1-tap DFE	CTLE 2-tap DFE	N/A	N/A	N/A	CTLE	CTLE
Area (mm^2)	0.10	0.03	0.24	0.041	0.16	0.4	0.378	0.15
Power (mW)	31.5	22.5	308.4	10	56.8	75	106.4	86.5
Energy Efficiency (pJ/bit)	3.5	3.6	9.6	2	7.1	25	21.3	17.3
FOM (pJ/bit/dB)*	0.16	1.20**	0.43	0.25	2.37**	8.33**	1.06	1.34

* FOM = (Energy Efficiency)/(Compensated Channel Loss @ Nyquist)

** 3dB channel loss is assumed

Table 4.1: Performance Summary.

Chapter 5.

Conclusion

This thesis demonstrated that receiver designs which avoid the undesired interaction between equalization and timing recovery are realized with combined equalization and timing recovery.

First this thesis demonstrated that a low-power equalizing receiver with an efficiency of 0.46mW/Gbps can be realized by using combined adaptation for separated equalization and timing recovery loops. It can find and maintain both the optimal timing for the CDR and the optimal tap coefficients for the adaptive equalizer. The proposed two-step equalization adaptation algorithm minimizes the BER and finds the optimal coefficients using fewer iteration steps. The quick convergence is due to the determination of the initial equalizer coefficients based on the measured SBR and the use of a stochastic hill-climbing algorithm for subsequent updates.

Second, a combined equalization and timing recovery using fractionally spaced equalizer (FSE) is presented. A 2× blind-oversampling FSE receiver is proposed to support plesiochronous links with an infinite timing-recovery range.

To realize an infinite-range timing recovery, a set of two FSE/DFE front-ends is used to cover different half-UI periods and the selection is seamlessly switched between the two. The adaptation and selection algorithm were developed to update the FSE/DFE coefficients and decide which front-end should be selected. The low-power circuit implementation of S/H, 4-tap FSE and 3-tap DFE helps to realize a power-efficient design. The measurement results are consistent with the presented analysis on timing recovery of FSE and show that the proposed FSE receiver architecture is an efficient way to build a power-efficient plesiochronous blind-oversampling receiver with combined adaptive equalization and timing recovery. A prototype receiver fabricated in a 28-nm CMOS consumes 3.5pJ/bit and 0.10mm^2 at 9Gb/s, while compensating for a 22-dB channel loss and 100ppm frequency offset between the transmitted data and blind sampling clocks.

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초 록

제한된 대역폭의 채널을 통한 고속 데이터 전송은 데이터 전송 속도의 급격한 증가로 인해 낮은 비트 오류율 (BER) 을 얻기 매우 어려워 졌다. 이퀄라이제이션과 타이밍 복원 능력의 향상은 고 대역폭 입출력 (I / O) 링크의 구현을 위한 핵심 요소이다. 그러나, 2 개의 다른 제어 루프를 통해 구현되는 이퀄라이제이션 및 타이밍 복구는 원치 않은 상호 작용을 일으키며 이는 성능 및 전력 효율의 저하로 이어진다. 이러한 부정적인 현상을 피하기 위해 이 논문은 고속 데이터 전송을 위한 결합된 이퀄라이제이션과 타이밍 복구를 방법을 제안한다. 첫째, 분리된 이퀄라이제이션 및 타이밍 복원 루프에 대한 결합된 어뎁테이션을 수행하는 수신기가 설계되었다. BER 을 최소화 하는 최적의 이퀄라이저 계수와 최적의 CDR 타이밍을 찾고 유지하기 위해, 두 단계로 나누어진 어뎁테이션 알고리즘이 단일 비트 응답 측정과 stochastic hill climbing 알고리즘을 통해 구현되었다. 둘째, 이 논문은 부분 공간 이퀄라이져 (FSE) 를 사용하여 단일 제어 루프에서 적응 이퀄라이제이션 및 타이밍 복구를 하나의 제어 루프로 결합하는 효과적인 방법을 제안한다. Plesiochronous 방식의 Clocking 을 추가로 지원하기 위해 구현된 수신기는 무한 범위의 타이밍 복구를 위해 두개의 FSE 를 사용하여 각자 반 주기 범위를 담당하도록 설계 되었다. 그리고, 그 둘 사이의 선택은 끊임 없이 둘 사이를 전환하도록 구현되었다. FSE 의 타이밍 복구 능력을 분석하고 그 등가 타이밍 복구 루프 모델을 1 차 Bang-Bang Delay Locked Loop

(DLL)로 유도하였다. 낮은 전력 소비를 위해 전류 적분 덧셈기와 여러개의 입력을 가지는 regenerative latch 를 이용해 4-탭 FSE 및 3-탭 DFE 를 구현하였다. 28nm CMOS 공정으로 제작된 프로토타입 수신기는 22dB 채널 손실과 100ppm 주파수 오프셋을 보상할 수 있고 3.5pJ/bit 의 파워와 0.10mm^2 의 넓이를 소모하면서 9Gb/s 의 데이터 전송 속도로 동작한다.

주요어 : 적응 이퀄라이져, 클락 및 데이터 복원 (CDR), 결정 피드백 이퀄라이져, 부분 공간 이퀄라이져, 수신기, 유선, 고속 링크

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