Ph.D. DISSERTATION

A STUDY ON SWITCHLESS RECONFIGURABLE AMPLIFIER USING COUPLED-LINE STRUCTURE

결합선로 구조를 이용한 비 스위치형
가변증폭기에 대한 연구

BY
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A STUDY ON SWITCHLESS RECONFIGURABLE AMPLIFIER USING COUPLED-LINE STRUCTURE

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Abstract

In this thesis, the switchless reconfigurable amplifier using coupled-line-based diplexer for broadband power amplifier (PA).

First, the broadband amplifier using reconfigurable topology to obtain higher power added efficiency (PAE) characteristic than conventional reactively-matched PA (RMPA). The proposed reconfigurable amplifier has two operation mode and each mode cover the half of the full operation frequency. The operation mode of the reconfigurable amplifier can be switched by changing dc bias of transistors. For this switchless reconfigurable PA, the coupled-line-based diplexer is proposed and adopt in design of matching network.

Unlike the conventional diplexer, the proposed coupled-line-based diplexer has one output port for low-band frequency signal and two output ports for high-band frequency signal. The output signals at two high-band output ports has same amplitude and out-of-phase phase difference. The proposed diplexer is designed by quarter-wavelength coupled-line and it can be implemented with shorter than quarter-wavelength coupled-line when the diplexer uses inter-stage matching network of 2-stgae PA. To analyze operation principle of proposed diplexer, analysis with 50 Ω port impedance condition and expanded it to capacitive port impedance condition.

The proposed reconfigurable PA is designed for 6-18 GHz operation. For high output power characteristic, the PA is designed and fabricated by using commercial 0.25-μm gallium nitride (GaN) HEMT process. The input-stage matching network is designed by using conventional double-resonance topology. The inter-stage and output-stage matching networks are designed by using proposed diplexer structure. The fabricated PA shows over 15 dB small-signal gain at 5–11 GHz in the low-band

mode and 9–18 GHz in the high-band mode. The measured average output power and PAE is 35 dBm, 23% in the low-band mode and 37 dBm, 26% in the high-band mode.

Second, the bypass low noise amplifier (LNA) using proposed diplexer structure is proposed. The proposed bypass LNA uses proposed diplexer and one single pole single throw (SPST) switch instead of using multi switches. The proposed diplexer structure is implemented at the last stage of the LNA. Each operation mode, LNA mode and bypass mode, can be selected by change state of SPST switch. The proposed bypass LNA is designed for W-band (75-110 GHz) operation and fabricated with commercial 0.1-μm GaAs pHEMT process. The simulation results showed 15 dB small signal gain and 5.6 dB noise figure at 94 GHz in LNA mode. In bypass mode, the simulation results showed 3.8 dB of transmission loss and noise figure.

Keyword: Broadband amplifier, bypass low noise amplifier (LNA), high power amplifier (HPA), reconfigurable amplifier, monolithic microwave integrated circuit (MMIC)

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Chapter 1

Introduction

1.1. Motivation

Conventionally, the broadband high-power amplifiers (HPA) for frequency jamming in electronic warfare have been designed using travelling-wave-tube (TWT). The TWT HPA has advantageous broadband and high-power characteristic in millimeter-wave frequency. However, it has a disadvantage in terms of their large size and warm-up time. For this reason, the research is continuing to replace TWT HPA with high-power monolithic-microwave-integrated-circuit (MMIC). The PA MMIC have high power density and no worm-up time characteristics compared to TWT HPA.

Table 1.1 compares the physical properties of semiconductor devices for fabricating PA MMIC [1]-[2]. Since GaN has wide energy bandgap, high breakdown field, high electron mobility, and high saturation velocity, the GaN HEMT devices have high power density, high operating voltage level and high-frequency characteristics. Therefore, PA MMICs based on GaN HEMT process are most suitable as a substitute for TWT HPAs.

Table 1.1

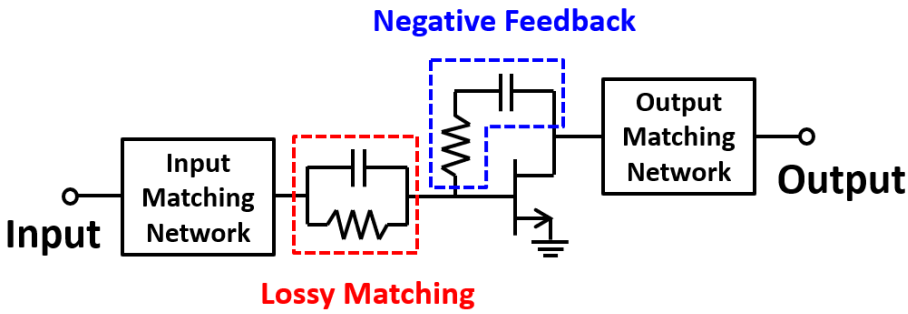
Si, GaAs, SiC, and GaN Material Properties

Property	Si	GaAs	SiC	**GaN**
Bandgap (eV)	1.11	1.43	3.2	**3.4**
Breakdown Field (MV/cm)	0.6	0.65	3.5	**3.5**
Electron Mobility (Cm^2/V-sec)	1350	6000	800	**1000**
Saturated velocity (10^7 cm/sec)	1	1	2	**1.5**

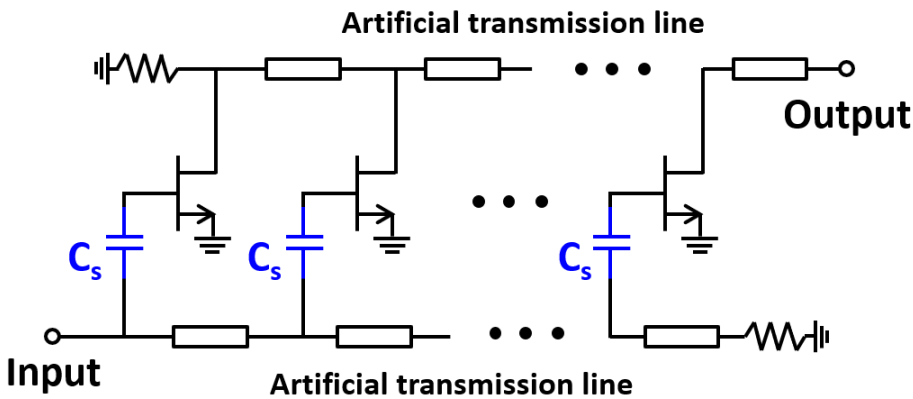
Design of a broadband PA MMIC is a challenging task. Recently, the broadband PA MMICs are desinged by using reactively-matched PA (RMPA) and distrubted amplifier (DA) structure. The Fig 1.1 (a) shows the conventional structure of RMPA. Conventionally, in this structure, broadband matching characterisic is obtained by using a series resistor or a negative feedback which reduce the Q-factor of the transistor [3]-[5].

The another designed topololy for broadband PA MMIC is the DA structure, the Fig 1.1 (b) dipict the conventional DA structure. The DA consists of parallel combied transistors and each input and output capacitance are used as parallel capacitor of input and output artificial transmission line. Therefore, input and output impedance of the DA can be determined by changing characterisitic impedance of input and output transmission line. This is advantageous in obtaining the broadband characteristic, but it suffers from low gain due to the absence of matching network [6]-[10].

In these two conventional broadband PA topologies, the matching networks are



(a)

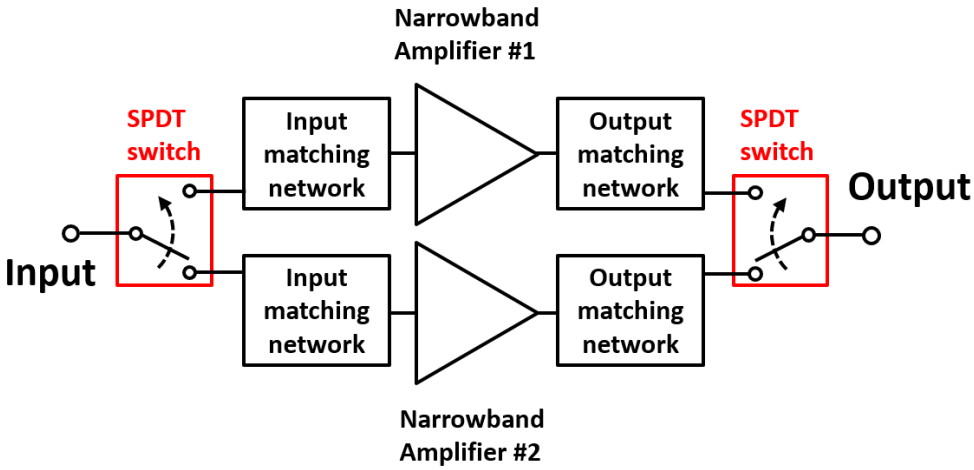


(b)

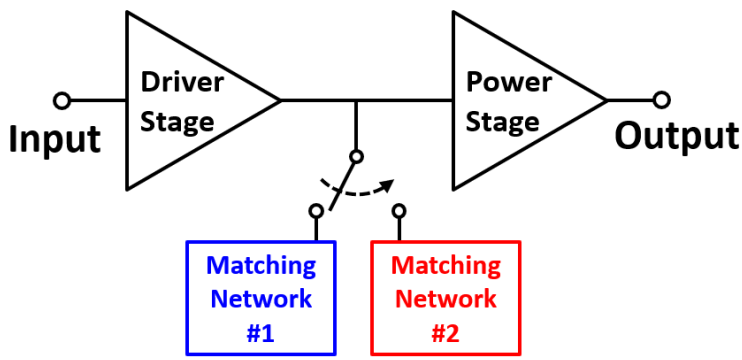
Fig. 1.1. Schematic of broadband power amplifier topologies, (a) RMPA and (b) DA.

deisnged to obtain maximum output power and power added efficiency (PAE) at maximum operating freuqency. Therefore, at the minimum operating frequency, the output power and PAE are lower than a narrowband PA due to the mismatch at the matching network. Therefore, the a method to reduce the input Q-factor of the transistor has been introduced by canceling the input capacitance using the non-Foster circuit [11]. However, the non-Foster circuit has the risk of instability, and the negative capacitance concept is difficult to apply to the output-stage due to the small power handling capability.

A multi-band, multi-mode PA architecture, which is used in mobile



(a)



(b)

Fig. 1.2. Schematic of reconfigurable power amplifier topologies, (a) PA combining topology and (b) matching network changing topology.

communication band PAs, is another approach to design broadband PAs. Since each matching network is designed for narrowband, high output power and power added efficiency (PAE) can be obtained. In [12] and [13], in order to implement multi-band operation, a reconfigurable matching network was used to switch operating mode of PA. The reconfigurable matching network is designed using varactor diodes and switches. However, the proposed reconfigurable matching network cannot be

applied in Ku-band frequency due to high loss and poor isolation characteristic of varactor diodes and switches. A dual-band PA design technique has been proposed in [14] using a diplexer to solve high switch loss problem. The proposed method combines two different input frequency signals using a diplexer and amplifies by a single amplifier. However, this method is only applicable when the input and output of two signals are separated.

1.2. Outline of This Thesis

This thesis is composed of six chapters and organized as follows. In the first chapter, chapter 2, a coupled-line-based diplexer is presented and analyzed. The chapter starts off with the introduce of the conventional diplexer structures and compare with proposed diplexer structure. Since the proposed diplexer operates as balun at high operation frequency, conventional planar balun topologies are also introduced. To better understand the proposed diplexer structure, a detailed analysis is performed based on a coupled-line theory. The analysis is confirmed at 50 Ω load impedance condition and then extended it to capacitive load condition.

In chapter 3, a reconfigurable amplifier using proposed diplexer is presented. The detailed design procedure of inter-stage and output-matching network is introduced. The operation of matching networks is verified by using circuit simulation with proper port impedance condition. At transition frequency, overlapped frequency of two power amplifier, the input signal is divided and transferred to both different amplifiers. To analyze signal canceling operation at transition frequency, the phase of the two signals is calculated using coupled-line theory and verified by using circuit simulator. Also, the optimum transistor off bias condition of unused PA is analyzed. To confirm the operation of the designed circuit, compares the simulation results with the measured results of fabricated PA.

In chapter 4, test setup and measured results of the fabricated MMIC is introduced. First the test fixture to mitigate self-heating effect and then the on-wafer measurement setup for S-parameters and output power is presented. The measured results of the reconfigurable amplifier are compared with simulated results. Also, the 2-way combined reconfigurable amplifier to increase output power is introduced. the 2-way combined amplifier is designed by using Wilkinson combiner for output

power combining.

In chapter 5, a bypass low noise amplifier (LNA) using proposed diplexer is presented. In this chapter, first, the issue of the conventional bypass LNA is introduced, and then the operation of the proposed bypass LNA is explained. The proposed bypass LNA is designed by using GaAs process and operation frequency is W-band. The detailed design procedure of bypass path and LNA is presented. The characteristics of designed bypass LNA are compared with previous conventional bypass LNA.

Finally, the thesis ends with conclusions in chapter 6 which summarizes the reconfigurable amplifier design using proposed diplexer.

Chapter 2

Coupled-Line-Based Diplexer Structure

2.1. Introduction

A diplexer is a three-ports passive device and the input signal is transferred to the one of the other two ports. The diplexer can be simply designed by combining low- and high-pass filters as shown in Fig 2.1. If the frequency of signal is low, the signal is outputted through low-pass filter and if the frequency of signal is high, the signal is outputted through high-pass filter. In frequency-division duplex (FDD) system, the diplexer can be used as a signal combiner and divider since transferred and received signal has different frequency.

The diplexer can be designed by using simple coupled-line structure. The Fig. 2.2 (a) and (b) show a diplexer using coupled-line structure and the equivalent circuit. In this structure, low-pass filter characteristic is obtained by using line-inductance of the coupled-line and additional shunt capacitor and high-pass filter characteristic is obtained by using coupling capacitance of the coupled-line and additional shunt inductor. In this structure, the operation frequency of each low- and high-pass filter can be controlled by designing dimension of coupled-line structure, shunt capacitor

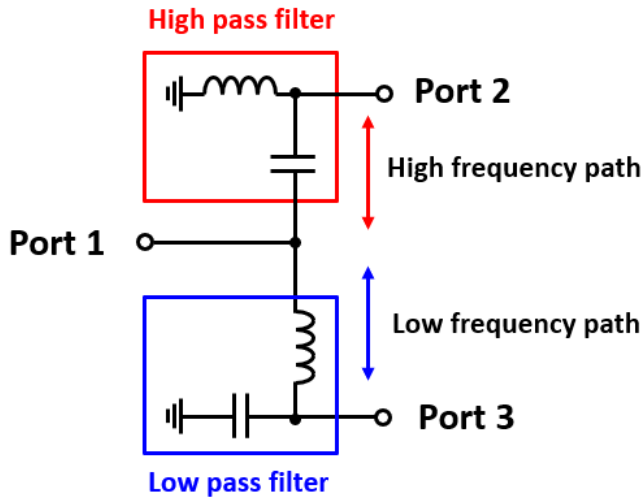
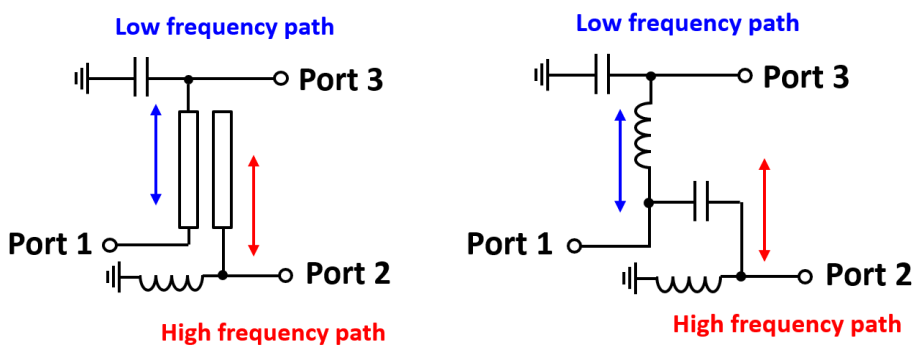


Fig. 2.1. Schematic of simple diplexer circuit



(a) (b)

Fig. 2.2. Coupled-line-based diplexer (a) layout and (b) equivalent circuit.

and inductor.

Conventionally, the passive circuits are designed and analyzed in 50 Ω port impedance condition. However, at inter-stage of a multi-stage PA, the input- and output-port have non-50 Ω port impedance. In inter-stage, the input port impedance is a drain impedance of transistor and is has complex impedance composed with

shunt capacitor and resistor. Also the output port impedance is a gate impedance of transistor and it has complex impedance composed with series capacitor and resistor. Therefore, if the passive elements use in inter-stage of PAs, the matching circuits have to add before and after the passive elements. This additional matching circuits increase the loss of matching network and total size of circuits.

In this chapter, the coupled-line-based diplexer for reconfigurable amplifier is proposed and analyzed. The proposed diplexer also operates as a balun in high frequency for signal dividing and combining. The analysis is stated with using basic coupled-line theory at 50 Ω port impedance condition and extended to capacitive port impedance condition. The analysis result shows the proposed diplexer can be adopted in inter-stage of PAs without additional matching circuits.

2.2. Coupled-Line-Based Diplexer Structure

2.2.1. Coupled-Line-Based Balun

The proposed reconfigurable PA divide the input signal by their frequency and the divided signal is amplified at each low- and high-band PAs. The Fig. 2.3 shows the block diagram of proposed reconfigurable PA using diplexer. In proposed reconfigurable PA, the diplexer is used to divide and combine the signal at input and output of each band PAs. Since the maximum output power of the transistor is decreased as frequency increase, the high-band path consists of two PAs for enough output power. For power dividing and combining at diplexer, the proposed diplexer is designed by using coupled-line balun structure.

In complementary metal-oxide-semiconductor (CMOS) process, the process has multi metal layers. Therefore, the transformer-based balun is commonly used since CMOS process. However, in III-V process such as GaAs or GaN process, the transformer structure cannot adopt by lack of the metal layer. Therefore, the proposed diplexer is designed by using planar type [15]. Fig 2.4 shows two conventional coupled-line based diplexers. The Marchand balun consists of two quarter-wavelength coupled-line [16]. It has good out-of-phase difference between two output signals. But this structure is hard to adopt in MMIC PA due to their large size. The coupled-transmission line balun is another coupled-line based balun using one quarter-wavelength coupled-line. This diplexer has advantage in component size. Since the small size of diplexer, it can be adopted MMIC circuit. However, it shows high out-of-phase difference between two output signals due to unbalance of through and coupled power.

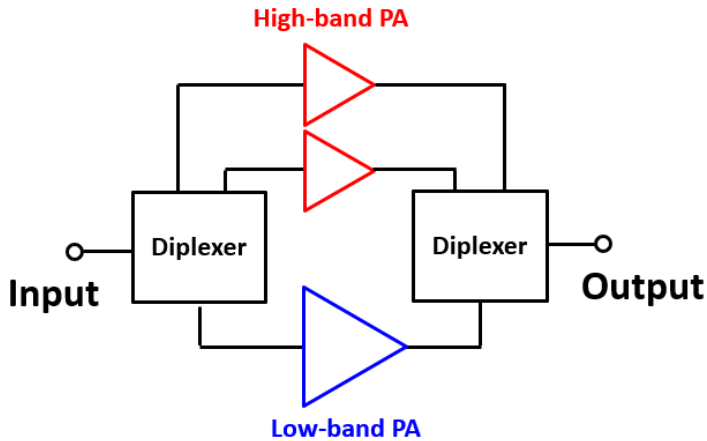
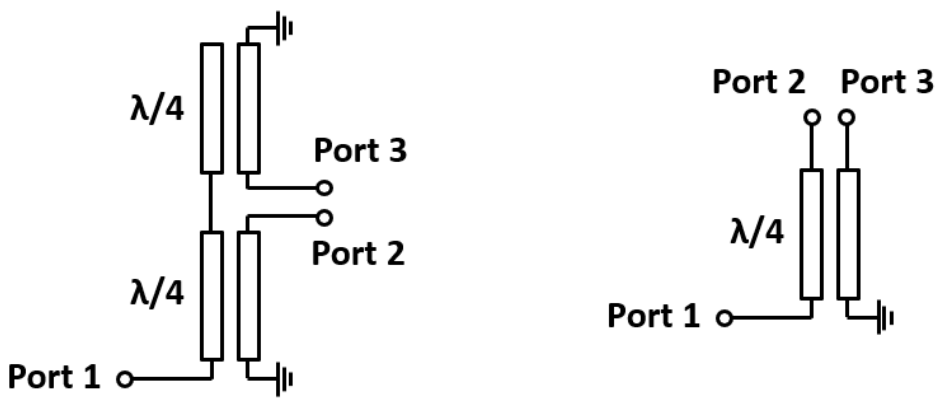


Fig. 2.3. Block diagram of proposed switchless reconfigurable amplifier.



(a) (b)

Fig. 2.4. Coupled-line-based diplexer (a) Marchand balun and (b) coupled-transmission line balun.

2.2.2. Proposed Coupled-Line-Based Diplexer

The Fig. 2.5 shows the simple schematic of the proposed coupled-line-based diplexer. The diplexer consists of one quarter-wavelength coupled-line and one shunt capacitor. It is similar to the balun structure in Fig 2.4 (b), but proposed diplexer uses a through-port for the low-band path and a coupled- and isolated-ports for high-band paths to diplexer and balun operation. The added shunt capacitor C_1 at through-port of the coupled-line operates as an open circuit at low-band frequency and operates as a short circuit at high-band frequency. Therefore, the transition frequency the, f_{sel}, can be determined by the capacitance of C_1 and the length of the coupled-line.

Fig. 2.6 (a) shows an equivalent circuit of the proposed diplexer at low-band frequency. In low-band frequency, the proposed diplexer operates as a conventional coupled-line due to the shunt capacitor C_1 operates as an open-circuit. Therefore, the low-band input signal is transferred to the through-port of the coupled-line. The low-band frequency output power at through-port of the coupled-line can be calculated by using basic coupled-line theory.

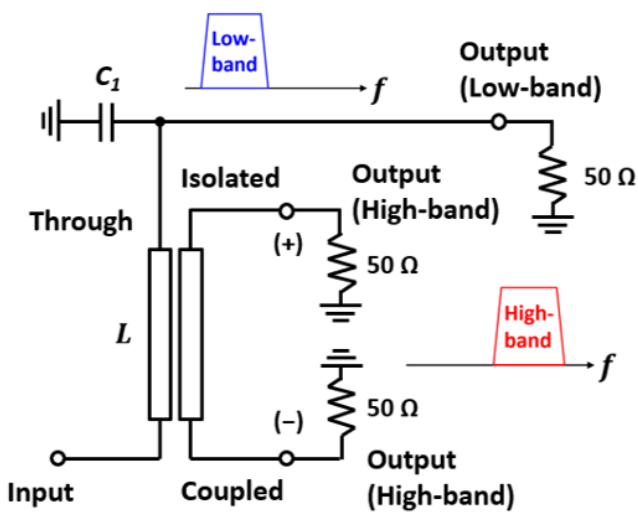
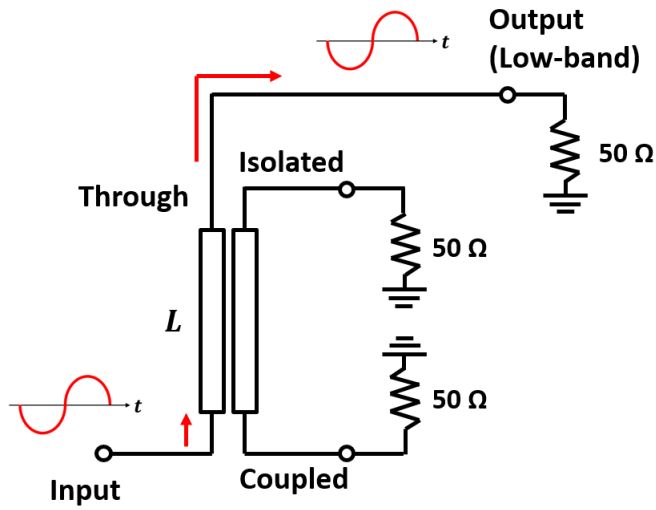
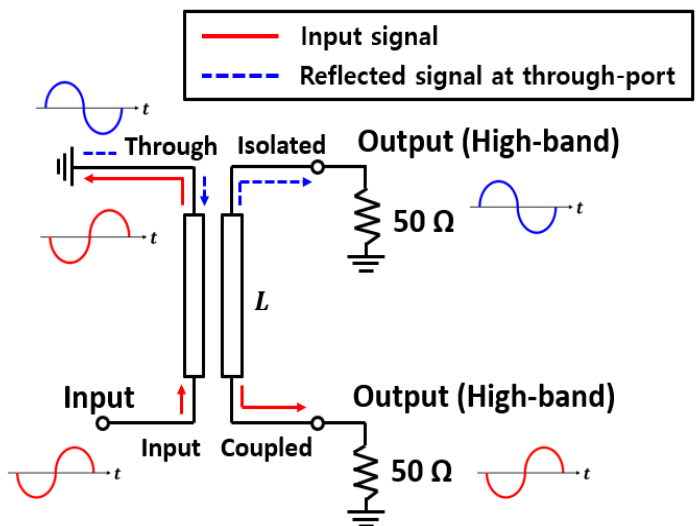


Fig. 2.5. Schematic of proposed coupled-line-based diplexer



(a)



(b)

Fig. 2.6. Equivalent circuit of proposed diplexer (a) at low-band frequency and (b) at high-band frequency.

In high-band frequency, C_1 has near short-circuit impedance, so the output signal at the through-port is reflected with 180° phase shift as shown in Fig. 2.6 (b). The reflected signal enters the coupled-line again and comes out of through- and isolation-ports of the coupled-line. Therefore, if the phase change from the coupled-line is ignored, the proposed diplexer operates as a balun at high-band frequency.

2.3. The Operation Principle of the Proposed Diplexer

To better understand the operation principle of the proposed diplexer, a detailed analysis is performed based on a coupled-line theory. To adopt the coupled-line theory, the load impedance Z_{load} and the characteristic impedance of the coupled-line Z_0 are assumed to be identical as shown in Fig 2.7. In this case, regardless of the frequency, the input impedance becomes Z_0. From basic coupled-line theory, the output voltage at coupled- and through-ports as a function of the input voltage V_{in} is given by

$$V_{through} = V_{in} \cdot \frac{\sqrt{1-K^2}}{\sqrt{1-K^2}\cos\theta + j\sin\theta} = A \cdot V_{in}, \tag{2.1}$$

$$V_{coupled} = V_{in} \cdot \frac{jK\tan\theta}{\sqrt{1-K^2} + j\tan\theta} = B \cdot V_{in}, \tag{2.2}$$

where

$$A = \frac{\sqrt{1-K^2}}{\sqrt{1-K^2}\cos\theta + j\sin\theta},$$

$$B = \frac{jK\tan\theta}{\sqrt{1-K^2} + j\tan\theta},$$

and K is the voltage coupling coefficient [17]. At low-band frequency, the output voltage from through-port is determined by K and the length of the coupled-line as shown in (2.1).

Fig. 2.8 illustrates the operation of proposed diplexer at high-band frequency. Since all the ports are assumed to be matched, the reflected signals (V_3^+ and V_4^+) are zero and the output voltage at coupled- and isolated-ports can be expressed as

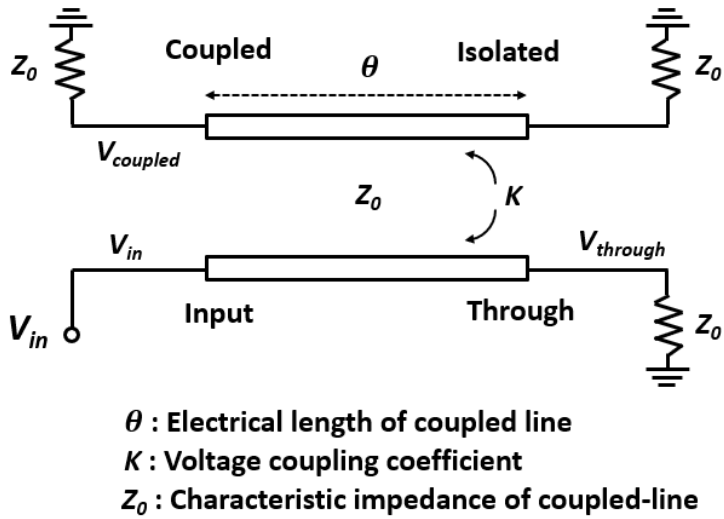


Fig. 2.7. Equivalent circuit of proposed diplexer at low-band frequency

$$V_3^- = V_{coupled} = B \cdot V_{in} = B \cdot V_1^+ , \tag{2.3}$$

$$V_4^- = B \cdot V_2^+ = B \cdot \Gamma \cdot V_2^- = -1 \cdot A \cdot B \cdot V_1^+ , \tag{2.4}$$

where Γ is the reflection coefficient at the through-port. The value of Γ is −1 for all frequency since we assumed an ideal short-circuit at high-band frequency. From (2.3) and (2.4), the condition for the minimum voltage difference between two output signals (V_3^+ and V_4^+) is calculated by

$$\left|V_4^-\right| = \left|V_3^-\right| = \left|A\right| \cdot \left|B\right| \cdot \left|V_1^+\right| = \left|B\right| \cdot \left|V_1^+\right| . \tag{2.5}$$

In (2.5), the two output signals have same voltage amplitude when |A| is 1. The |A| is actually determined by K and θ of the coupled-line. Fig. 2.9 (a) shows the

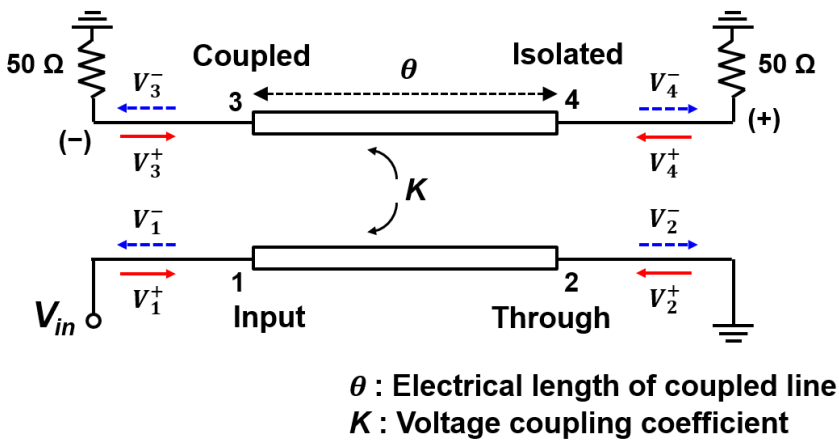
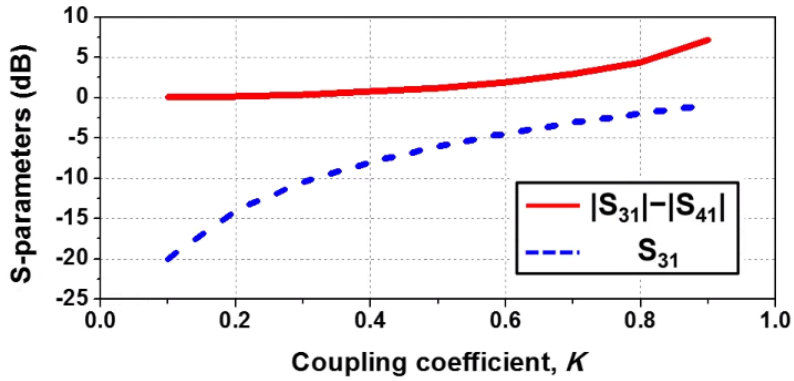


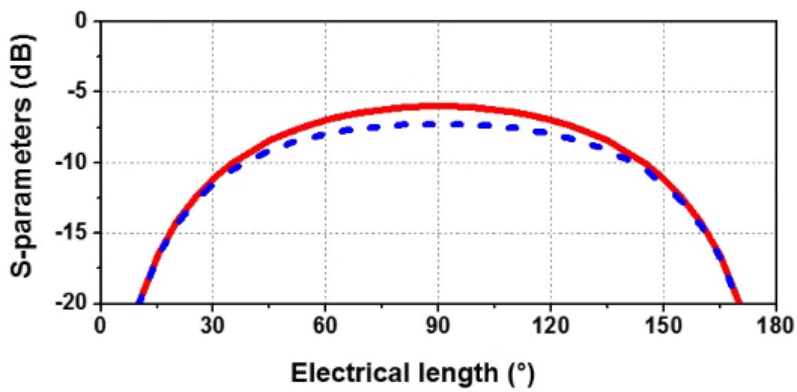
Fig. 2.8. Equivalent circuit of proposed diplexer at high band frequency

transfer function of coupled-port and amplitude difference between coupled- and isolated-ports as a function of *K* for quarter-wavelength coupled-line. For better amplitude balance of two output signals, small *K* is advantageous, but it leads to the reduced output signal. In addition, the signal balance improves as the coupled-line length decreases as shown in Fig. 2.9 (b). However, as the length of the coupled-line decreases, the output power at coupled- and isolated-ports also decreases.

The phase of the output signal can be calculated using (2.1) for the low-band frequency signal. Since the low-band frequency signal is directly output via the through-port of coupled-line, the output phase is offset by the phase shifted by the coupled-line length, which can be confirmed by (2.1). The phase difference between the two high-band frequency signals can be calculated using (2.3) and (2.4). Unlike Fig. 2.9 (b), the input signal and the reflected signal at the through-port do not have a 180° phase difference due to the phase change of the coupled-line itself. For example, when using a λ/4 length coupled-line, a phase difference of 90° is obtained.



(a)



(b)

Fig. 2.9. (a) Transfer function to the coupled-port (S_{31}) and signal difference between coupled- and isolated-ports (S_{41}), and (b) coupled power to coupled- and isolated-ports at high-band frequency (K=0.5).

As a result, assuming $Z_{load} = Z_0$ condition, the better phase balance between high-band frequency signals can be achieved when short-length coupled-line is used. However, the short-length coupled-line reduces the amplitude of the coupled signal due to the mismatch of the port and input impedance of the coupled-line. For this reason, the proposed coupled-line diplexer structure may not be useful with the conventional port termination conditions.

2.4. The Operation Principle of the Proposed Diplexer in Complex Load Condition

In $Z_{load} = Z_0$ condition, the proposed diplexer can be used as a diplexer and a balun at high-band frequency in short-length coupled-line condition. But in this condition, the input impedance is changed by the electrical length of the coupled-line and this impedance mismatch between port and input impedance requires the additional matching circuit for impedance matching. The additional matching network reduce the operation frequency of the proposed diplexer. However, the proposed diplexer can be used without additional matching network at the inter-stage of the PAs. In the inter-stage of the PAs, the input port impedance is the drain impedance of the transistor and the output port impedance is the gate impedance of the transistor. The Fig. 2.10 shows the proposed diplexer with inter-stage port condition. The gate equivalent circuit of a transistor consists of a small R_g and a large

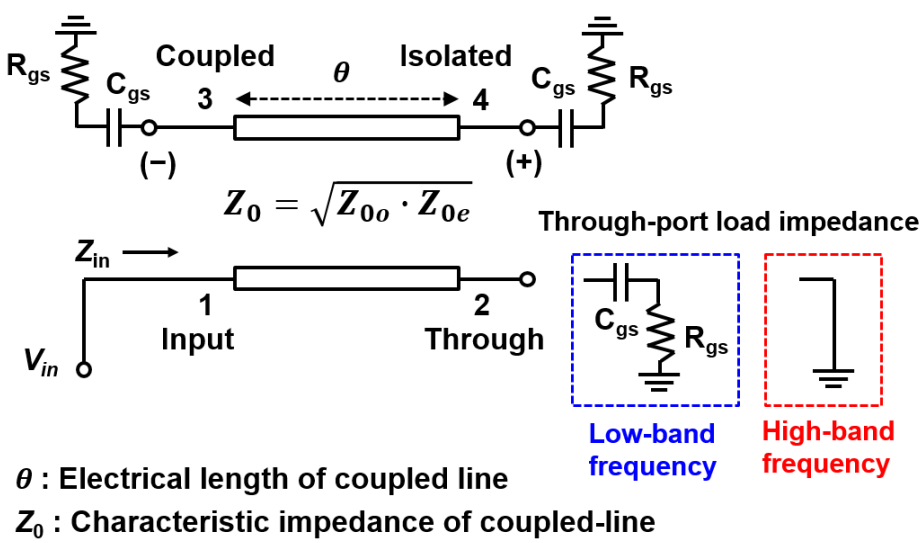


Fig. 2.10. Port condition of proposed diplexer at inter-stage of the PAs.

C_{gs}. Therefore, the analysis under the complex load impedance condition is required to analyze the proposed diplexer operation for the inter-stage of PAs.

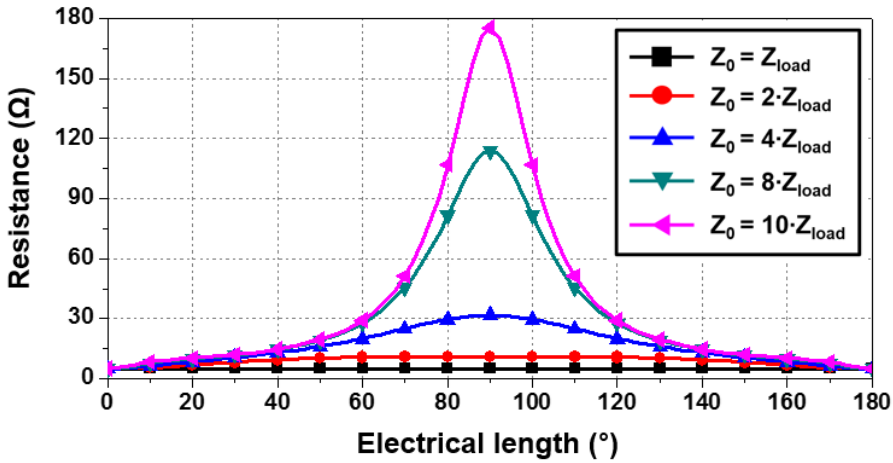
For non-50 Ω termination, port termination impedance affects the coupled-line operation. It is thus impossible to analyze the transfer characteristics using (2.1) and (2.2). Therefore, the input impedance of the coupled-line at $Z_{load} \ll Z_0$ calculated to analyze matching characteristic. From the coupled line equations, the input impedance can be expressed by the following equation

$$Z_{in} = Z_{load} + \frac{2\left(Z_{in}^{o} Z_{in}^{e} - Z_{load}^{2}\right)}{Z_{in}^{e} + Z_{in}^{o} + 2Z_{load}} \text{, where} \tag{2.6}$$

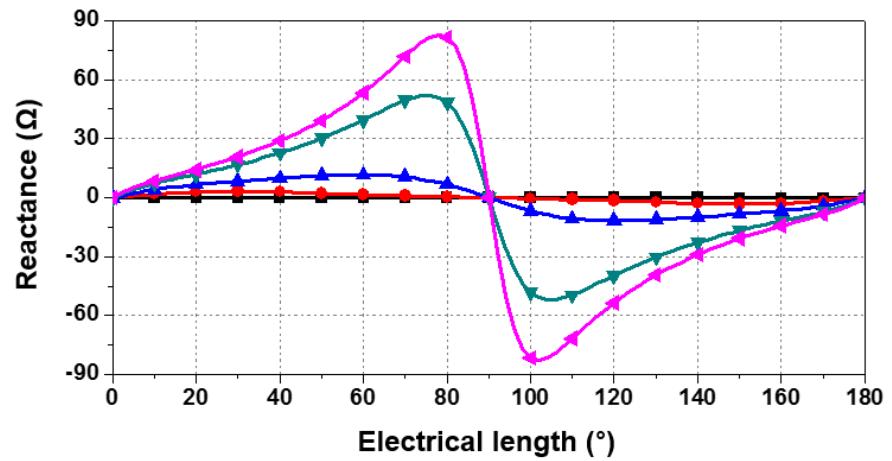
$$Z_{in}^{e} = Z_{0e} \cdot \frac{Z_{load} + jZ_{0e}\tan\theta}{Z_{0e} + jZ_{load}\tan\theta},$$

$$Z_{in}^{o} = Z_{0o} \cdot \frac{Z_{load} + jZ_{0o}\tan\theta}{Z_{0o} + jZ_{load}\tan\theta},$$

Z_{0e} and Z_{0o} are the odd and even mode characteristic impedance of the coupled-line, respectively. Fig. 2.11 (a) shows the input resistance of the coupled-line obtained from (2.6) according to Z_0 assuming a port impedance of 5 Ω. The input resistance starts at a minimum value of Z_{load} and increases with the length of the coupled-line. In the fixed coupled-line length, the input resistance is determined by the difference between Z_0 and Z_{load}. With 5 Ω termination impedance, the input resistance increases rapidly from 60°. Therefore, a coupled-line of less than 60° length can provide resistance close to the port resistance. At high-band frequency, the through-port of coupled-line operates as a short-circuit. Therefore, the resistance of even mode input impedance Z_{in}^{e} viewed from the input-port and Z_{load} becomes



(a)



(b)

Fig. 2.11. Input (a) resistance and (b) reactance of the coupled-line according to characteristic impedance (K=0.7).

zero. When applying this condition to (2.6), the minimum input resistance in Fig 2.11 (a) becomes zero. As a result, it is theoretically possible to obtain the same input resistance as the port resistance by selecting the appropriate coupled-line length.

Fig. 2.11 (b) shows the reactance of the input impedance obtained from (2.6). The input reactance starts at a minimum value of zero as in the case of the input

resistance and increases as the coupled-line length increases. If the coupled-line length is shorter than $\lambda/4$ length, the reactance is inductive. Therefore, when appropriate length coupled-line and Z_0 values are used, C_{gs} can be resonated out with half of the coupled-line inductance. The required equivalent inductance of the coupled-line can be expressed as

$$L_{eq} = \frac{1}{\omega \cdot C_{gs}} \cdot \frac{2}{\omega} = \frac{2}{\omega^2 \cdot C_{gs}} . \tag{2.7}$$

As a result, in complex load condition, the input matching can be achieved without additional matching circuit at the desired frequency by changing the structure and the length of the coupled-line.

For the optimum operation of the diplexer for wideband PA application, the low-band frequency signal should be transmitted to the through-port with minimum leakage to the coupled- and isolated-ports of the coupler. On the other hand, large coupling is required for high-band frequency signals so that most of the input power can be transferred to the coupled- and isolated-ports of the coupled-line. The output voltage at coupled-port for $Z_0 \neq Z_{load}$ condition can be calculated by

$$V_{coupled} = V_{in} \cdot \left[\frac{Z_{in}^{e}}{Z_{in}^{e} + Z_{load}} - \frac{Z_{in}^{o}}{Z_{in}^{o} + Z_{load}} \right] . \tag{2.8}$$

Fig. 2.12 shows the transfer characteristic to coupled-port according to Z_0 under the condition that Z_{load} is 5 Ω. For quarter-wavelength coupled line, the coupled power decreases when Z_0 increases. However, the opposite happens when the length of the coupled-line has a 10–20° electrical length. Therefore, a desired coupling

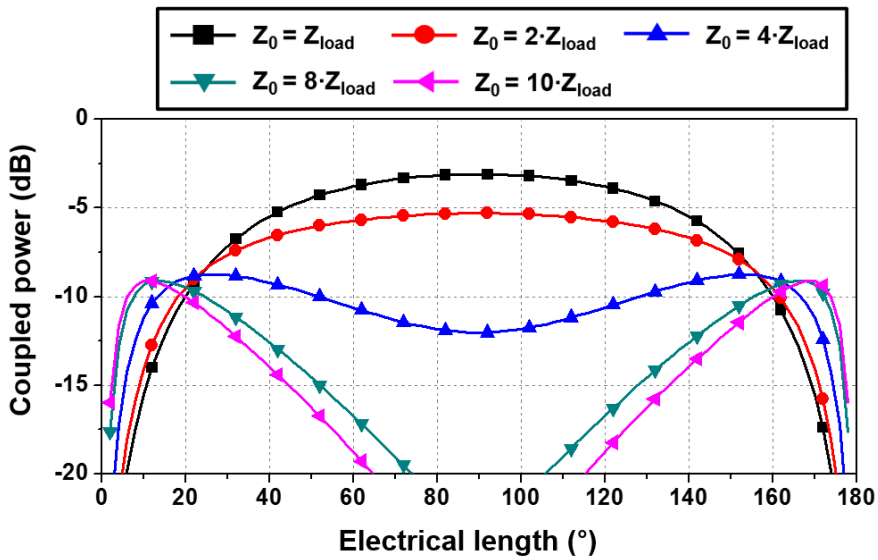


Fig. 2.12. Transfer characteristic to coupled-port according to characteristic impedance of coupled-line (K=0.7).

power can be obtained in a short-length coupled-line by changing the Z_0 of the coupled-line.

Fig. 2.13 shows the circuit schematic of proposed diplexer at high-band frequency when R_{gs} is 5 Ω and C_{gs} is 1.5 pF, and Fig. 2.14 (a) shows the simulation results according to Z_0 at 18 GHz. At this frequency, the required input reactance of the coupled-line for resonance with C_{gs} is 11.5 Ω. Assuming a coupled-line electrical length of 20°, input matching can be achieved when Z_0 is 50 Ω. With 50 Ω Z_0 condition ($10 \cdot Z_{load}$), simulation results show the desired balun operation with 10–20° electrical length. In addition, since the electrical length of the coupled-line decreases as the frequency decreases, the low-band frequency signal transfer to the coupled- and isolated-ports can be limited. The simulation results of phase are depicted in Fig. 2.14 (b). The simulation result shows 170-180° of phase difference between 0-20° coupled-line electrical length. Therefore, the proposed coupled-line-base diplexer can be used as balun at high-band frequency.

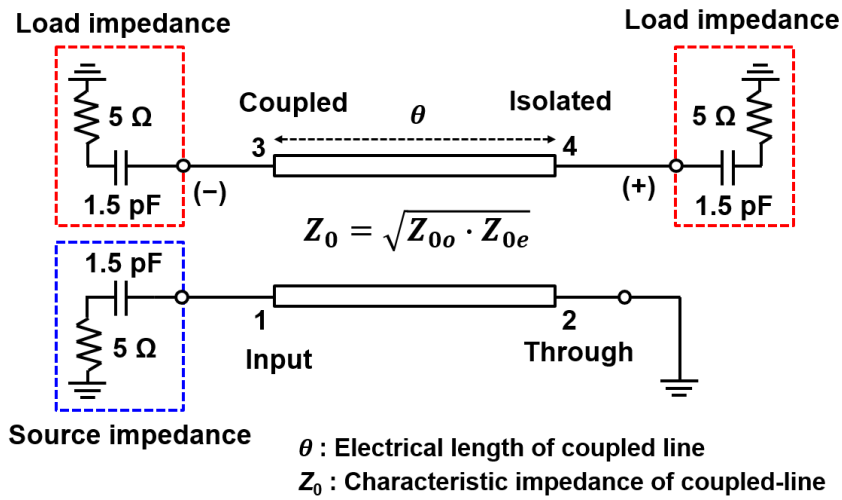
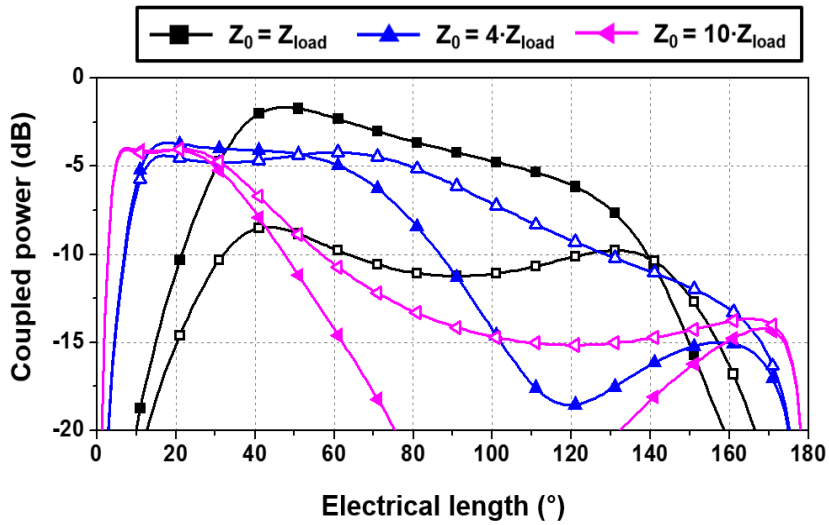
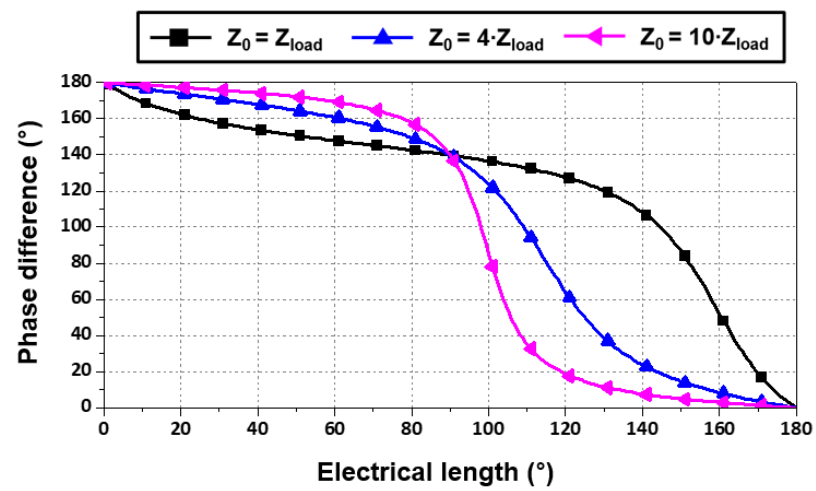


Fig. 2.13. Simulation port condition of proposed diplexer at high-band frequency.

The practical problem of the proposed diplexer structure is that the input matching frequency band is limited unlike the conventional coupled-line. This limitation comes from the fact that the input impedance varies according to the frequency. Therefore, an additional input matching circuit is required to cover the entire frequency range. The resonance frequency of C_{gs} and the coupled-line must be high in order to minimize the transfer of the low-band frequency signal to the coupled- and isolated-ports, which means that the additional input matching circuit is required to provide adequate matching at low frequency. In this case, the input impedance at low frequency has capacitance due to the finite inductance in coupled-line. This input capacitance can be matched using shunt inductance, and this inductance can be implemented by a bias line shorter than the quarter-wavelength.



(a)



(b)

Fig. 2.14. simulation results of (a) transfer characteristic and (b) phase difference to coupled-port (filled) and isolated-port (hollowed) according to characteristic impedance of coupled-line (K=0.7).

2.6. Conclusion

In this chapter, the coupled-line-based diplexer is proposed and analyzed. The proposed diplexer consists of one quarter-wavelength coupled-line and one shunt capacitor. The proposed diplexer operates as conventional diplexer and operates as a balun at high-band frequency. To better understand the proposed diplexer structure, a detailed analysis is performed based on a coupled-line theory. First the analysis is performed in conventional 50 Ω port impedance condition. The analysis result shows the proposed diplexer need additional matching circuits in 50 Ω port impedance condition. However, it is possible to use the proposed diplexer without additional matching circuits when the diplexer is used at inter-stage of PAs. At the inter-stage, the input impedance of the transistor becomes the port impedance of the diplexer. Therefore, additional analysis is performed in complex load condition. The proposed diplexer analysis result at the complex load condition shows the proposed diplexer can be adopt in inter-stage without additional matching circuits and operate as a balun at high-band frequency. Also, at the inter-stage, the proposed diplexer can be implemented shorter than quarter-wavelength coupled-line.

Chapter 3

Design of a Switchless Reconfigurable Amplifier using proposed coupled-line-based diplexer

3.1. Introduction

The reconfigurable amplifier design concept is used to design a multi-band, multi-mode PA for mobile application PAs. These reconfigurable amplifiers are designed by using switch or varactor diode to change operation band of the amplifier. The switch and varactor diodes can be used to change signal path and capacitance of the matching network. However, these components degrade the characteristics of the reconfigurable amplifiers over *Ku*-band frequency due to high loss and poor isolation characteristic of the components. To solve this problem, the technique which use the diplexer at input and output matching network is proposed. The proposed method combines two different input frequency signals using a diplexer and amplifies by a single amplifier. However, this method is only applicable when the input and output of two signals are separated.

In this chapter, a switchless reconfigurable amplifier is developed to cover 6–18 GHz frequency. The proposed amplifier combines two single-band PAs using a proposed diplexer for switchless split-band operation. Since the proposed diplexer in chapter 2 can be implemented with simple matching network at the inter-stage of the amplifier, the proposed switchless reconfigurable amplifier can be designed with compact size. For the output matching network, the modified proposed diplexer structure is adopted to output power combining since the port condition of the output matching network. The proposed amplifier has two operation mode, low-band and high-band mode and each operation mode can be selected by transistors off the unused mode PAs. The analysis of the best transistor off bias condition for each low- and high-band mode condition is performed.

3.2. Design of matching network

A block diagram of the proposed switchless reconfigurable amplifier is shown in Fig. 3.1. This reconfigurable amplifier consists of a drive amplifier, high/low-band PAs, and input/output diplexers. The diplexers at inter-stage and output-stage divide the operating frequency into the two-difference bands (low-band and high-band) based on the transition frequency (f_{sel}). The low-band and high-band PA amplify the signal divided by the diplexer. To achieve maximum PAE, the proposed PA operates in one of two modes, low-band, and high-band mode. Each mode can be selected by turning off the transistors of the unused mode PAs without an additional circuit. Considering the gain and output power in each mode frequency, the low-band PA consists of one PA, and the high-band PA consists of two PAs combined by the push-pull structure. The unit transistor size of all PAs is 6×125-μm, which has a maximum available gain (MAG) of 19 dB at 6 GHz and 12 dB at 18 GHz. The maximum output power in the load-pull simulation is 36.5 dBm at 6 GHz and 33 dBm at 18 GHz.

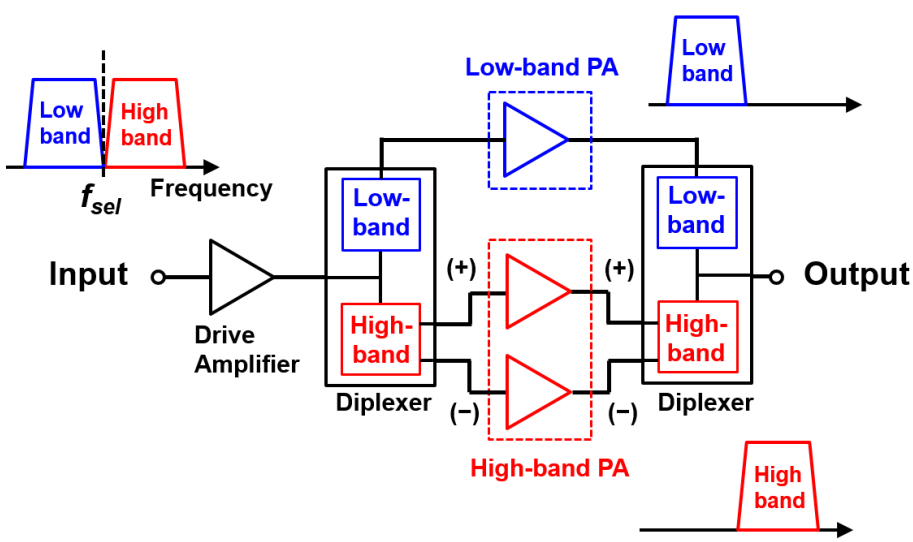
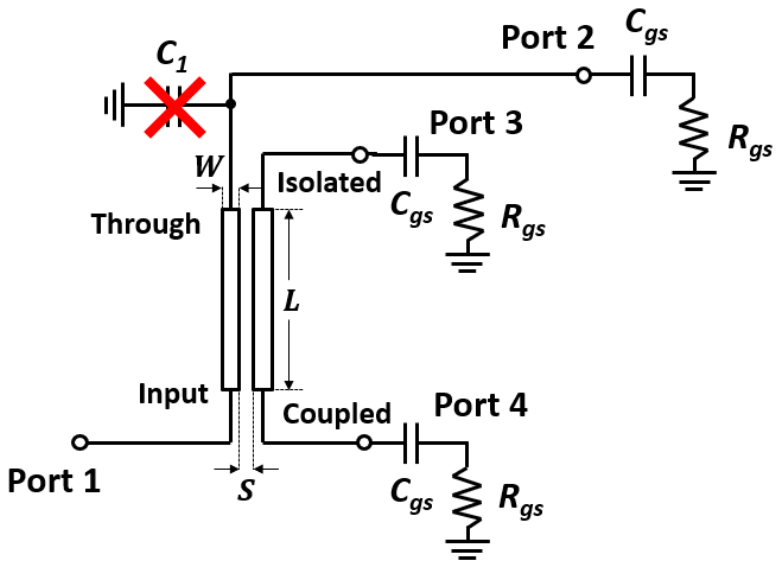


Fig. 3.1. Block diagram of the proposed switchless reconfigurable amplifier.

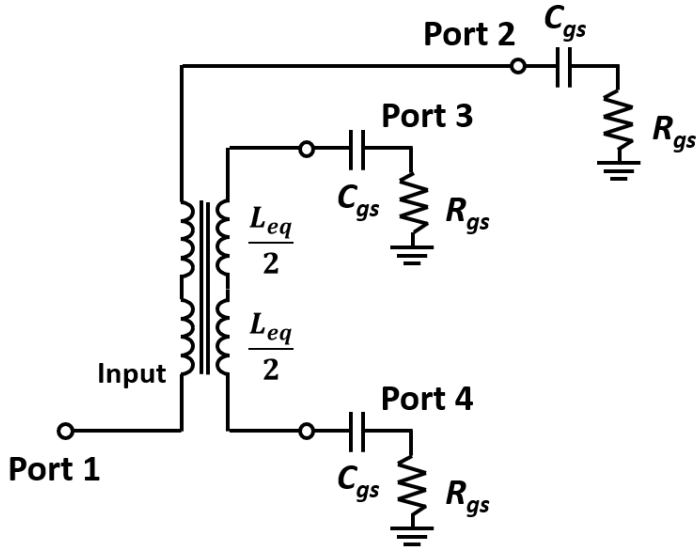
3.2.1. Design of Inter-Stage Matching Networks

Fig. 3.2 (a) shows the design concept of the inter-stage matching network using the proposed diplexer. Since the load impedance in the inter-stage matching is a complex load composed of C_{gs} and R_{gs} of the transistor, the proposed diplexer structure can be applied. The structure can be further simplified by using C_{gs} of the low-band transistor instead of C_1 in Fig 3.2 (a). The length of the coupled-line is designed to resonate with C_{gs} in high-band frequency as shown in Fig. 3.2 (b). The 6×125-μm sized transistor used has a R_{gs} of 3.5 Ω and a C_{gs} of 1.5 pF. The width and spacing of the line are adjusted so that the used coupled-line have Z_0 of 50 Ω and K is 0.55. Equivalent inductance value required for resonance with C_{gs} calculated from (7) is 100–300 pH for 18–10 GHz resonance frequency, and this inductance can be implemented with a line length of 150–450 μm. The electrical length of the coupled-line is approximately 10°. Thus, the coupled-line length is reduced more than 75% compared with 1700 μm for $\lambda/4$ length at 18 GHz.

Fig. 3.3 shows the detailed circuit schematic of the designed inter-stage matching network. To obtain the desired K at the coupled-line, a structure combining two coupled-lines is used to enhance the coupling. Since the coupled-line length used in the design is 400 μm, and it has an inductance of 280 pH, the resonance frequency with C_{gs} is 11 GHz. In addition, since the length of 400 μm has an electrical length of 10–20° at 10–18 GHz, sufficient coupling can be achieved as already analyzed. The matching circuit between the transistor output and the coupled-line is added to obtain the wideband input matching. The additional matching circuit is designed to obtain additional resonance at 6 GHz and 18 GHz using a double-resonance matching technique. The additional matching circuit consists of two resonators. The capacitance, C_{ds}, and the inductance of 300 μm length microstrip line forms a series



(a)



(b)

Fig. 3.2. Design concept of the (a) inter-stage matching network and (b) equivalent circuit.

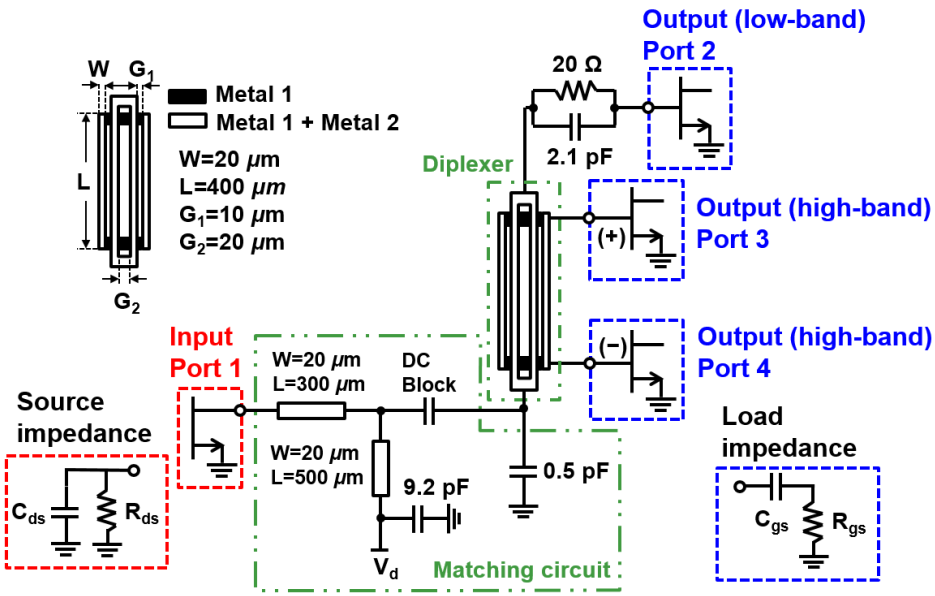


Fig. 3.3. Detailed schematic of the inter-stage matching network.

resonator with a resonance at 18 GHz. The shunt inductance from 500 μm-long bias line and shunt capacitance consisting of 0.5 pF capacitor and input capacitance operates as a shunt resonator with resonance frequency of 6 GHz. An RC circuit consisting of 20 Ω and 2.1 pF is added at the input of the low-band PA to prevent oscillation below 6 GHz.

The simulation results of the designed inter-stage matching network are shown in Fig. 3.4. The simulation is performed using the transistor model provided by the foundry and the S-parameters of the passive components calculated using EM simulation (Keysight ADS momentum). Simulation results show an fsel of 10.5 GHz and the phase error of the high-band differential signals less than 7°. There is non-negligible leakage of high-band frequency signal to the low-band output port (~3 dB). This is because C_{gs} of the low-band transistor is used instead of C_1 for fsel decision. Thus, the matching loss of the low-band signal is ~3 dB higher than the loss of the high-band frequency signals in the inter-stage matching network.

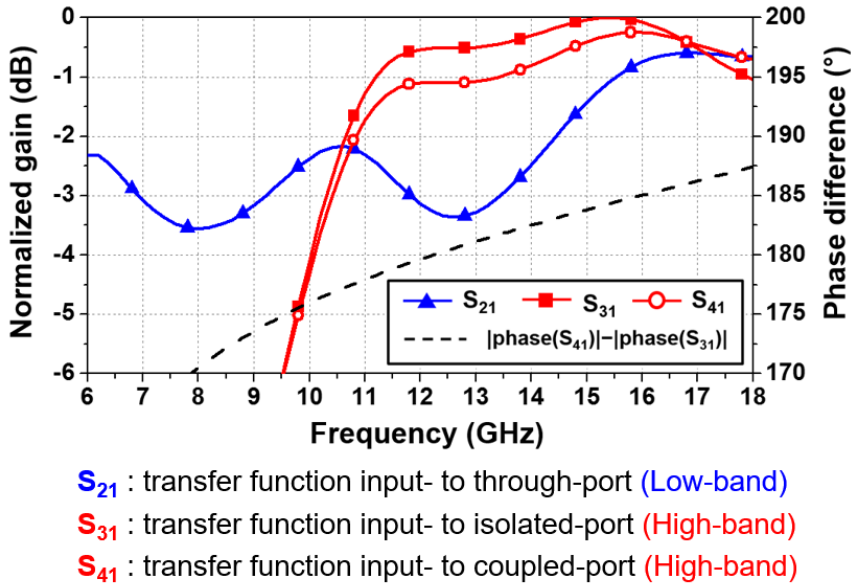


Fig. 3.4. Simulated results of the inter-stage matching network.

However, since MAG is higher at low frequencies, the loss can be compensated. If C_1 is used, the high-band signal transmitted to the low-band output port could have been prevented.

3.2.2. Design of Output-Stage Matching Networks

When the proposed diplexer structure is applied to the output-stage matching network design, the load impedance at the inter-stage becomes the drain impedance of the transistor. The drain equivalent circuit of a transistor is composed of a parallel circuit of a small C_{ds} and large R_{ds}. So, it is difficult to obtain enough capacitance value. Therefore, the output-stage matching network is designed by applying two diplexers to each transistor as shown in Fig. 3.5.

Fig 3.6 (a) shows the output matching network operation in low-band frequency

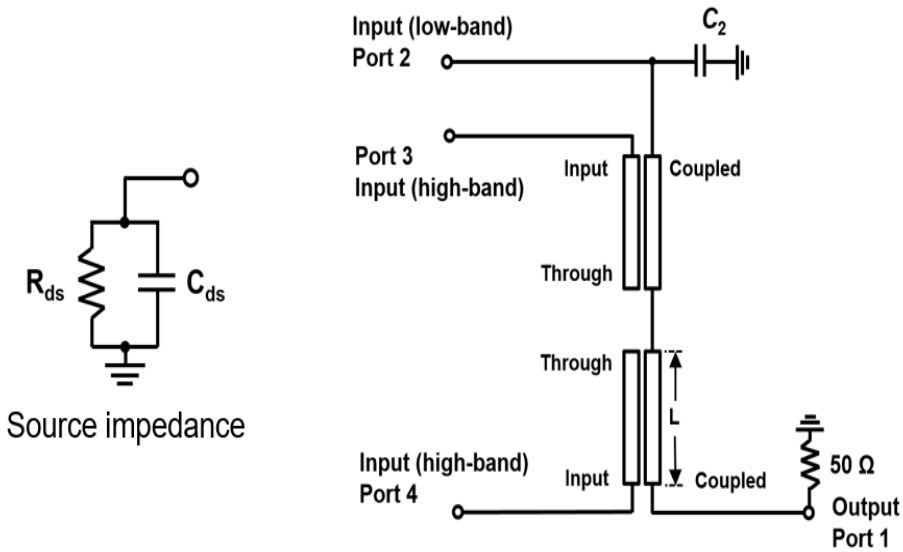
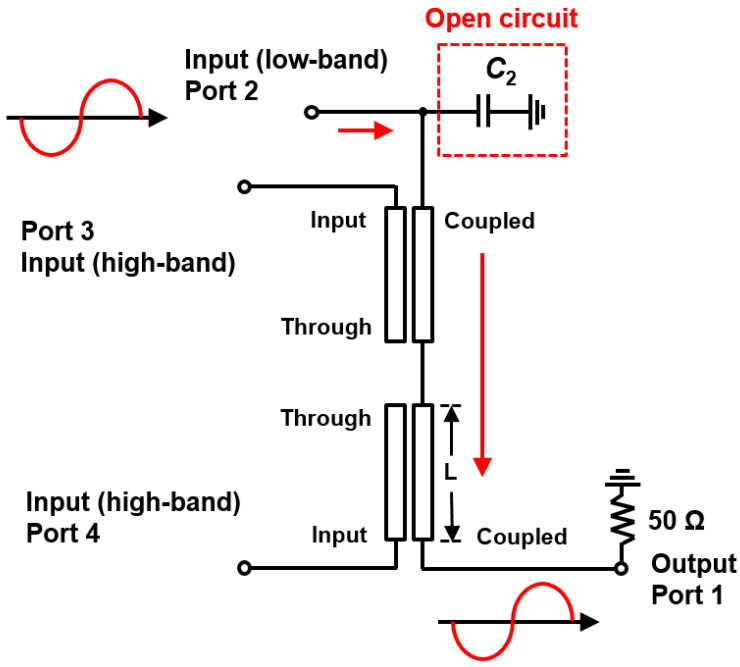


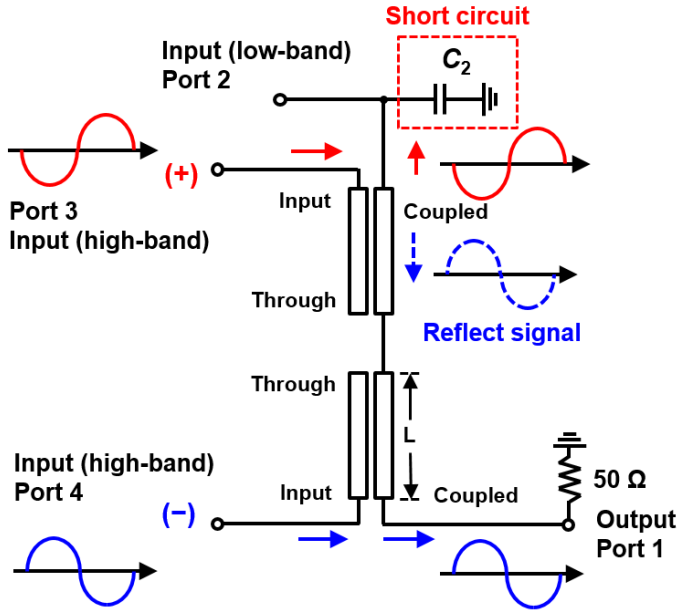
Fig. 3.5. Drain equivalent circuit of transistor and concept of output matching network

and high-band frequency. In ideal operation, a shunt capacitor C_2 operates as an open circuit at low-band frequency. The output signal from low-band PA is transferred to coupled-port of the upper coupled-line. Since the through port of the upper coupled-line is open, the input signal form coupled-port of the upper coupled-line is transferred to lower coupled-line. In lower coupled-line, the input signal is directly transmitted to the 50 Ω output port. Therefore, the in low-band frequency, input signal is transferred to output port with small loss.

Conversely, at high-band frequency, C_2 operates as a short-circuit, and each through-port of the coupled-line is an open-circuit as opposed to the inter-stage. Fig 3.6 (b) shows the operation of output matching network at high-band frequency. Since the resistance of even mode input impedance Z_{in}^{e} is infinite, assuming input matching condition, the input signal is delivered only to the coupled-port as shown in (8). Thus, the two coupled-lines transfer the input signal to each coupled-port



(a)



(b)

Fig. 3.6. Operation of output matching network (a) at low-band frequency and (b) at high-band frequency.

without loss. In this case, the output signal from the lower coupled-line is directly transferred to the 50 Ω output port, and the output signal from the upper coupled-line is reflected with the 180° phase difference through C_2 and transmitted to the 50 Ω output port. Since the length of the coupled-line is short enough, the signals out of the isolated-port of the upper coupled-line and the coupled-port of the lower coupled-line are combined at the output port with the negligible phase difference.

Fig. 3.7 is a circuit schematic of the designed output-stage matching network. The length of each coupled-line is 450 μm, similar to the coupled-line length used in the inter-stage matching network. A capacitor of 0.2 pF, C_3, is added to through-port for input matching. Since the resonance frequency between C_3 and the coupled-line

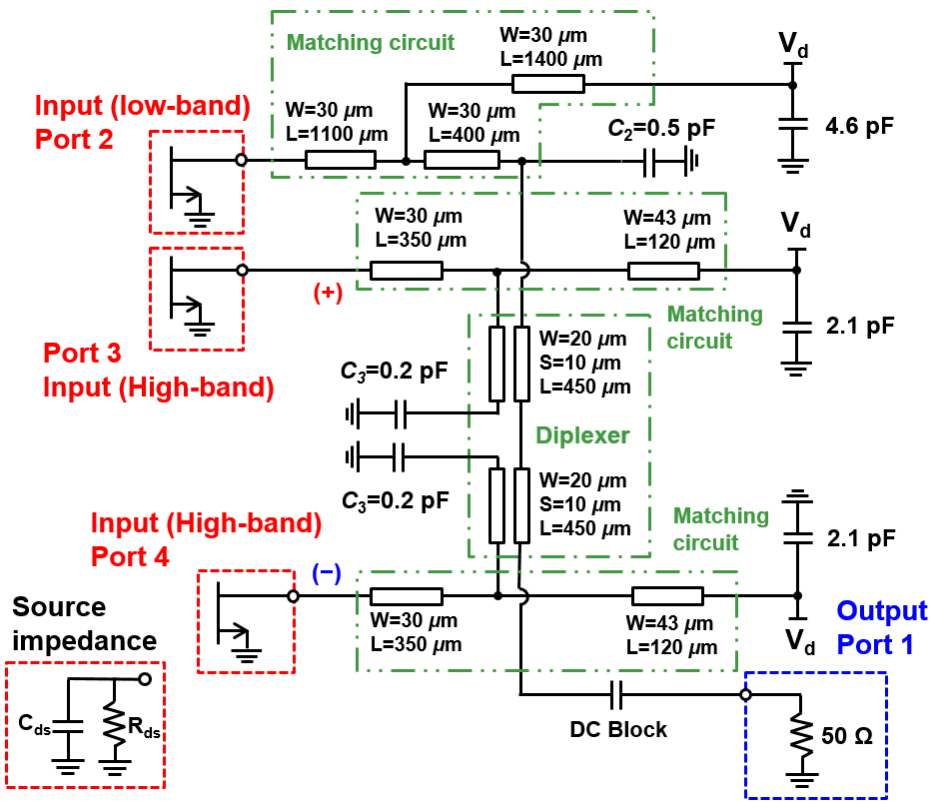


Fig. 3.7. Detailed schematic of the output-stage matching network.

is 36 GHz, higher than the target frequency band, it is impossible to apply the resonator-based matching method as presented earlier. Therefore, an additional matching circuit is added between the drain of each high-band transistor and the coupled-line. The additional matching circuits are intended to obtain wideband matching characteristics through resonance with C_{ds} (~12 GHz) and C_3 (~18GHz). The capacitance of C_2 is 0.5 pF, which makes the resonance with the coupled-line around 10 GHz at the output port. The matching circuit between the low-band transistor drain and the coupled-line is added for wideband matching. This matching circuit achieves wideband input matching at low-band frequencies through resonance with C_{ds} (~6 GHz) and C_2 (~10 GHz).

Fig. 3.8 shows the simulation results of the designed output-stage matching network. The simulation is performed with the respective port impedance shown in Fig. 3.7. Simulation results show that f_{sel} is 11 GHz and the similar loss is observed in both low-band and high-band paths. Unlike inter-stage, high-band frequency

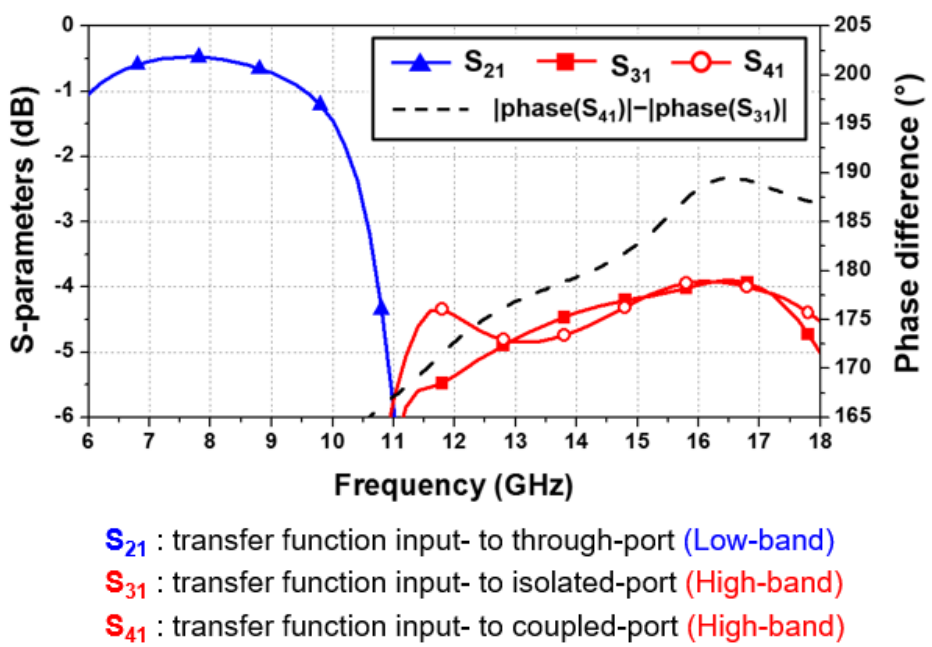


Fig. 3.8. Simulated results of the inter-stage matching network.

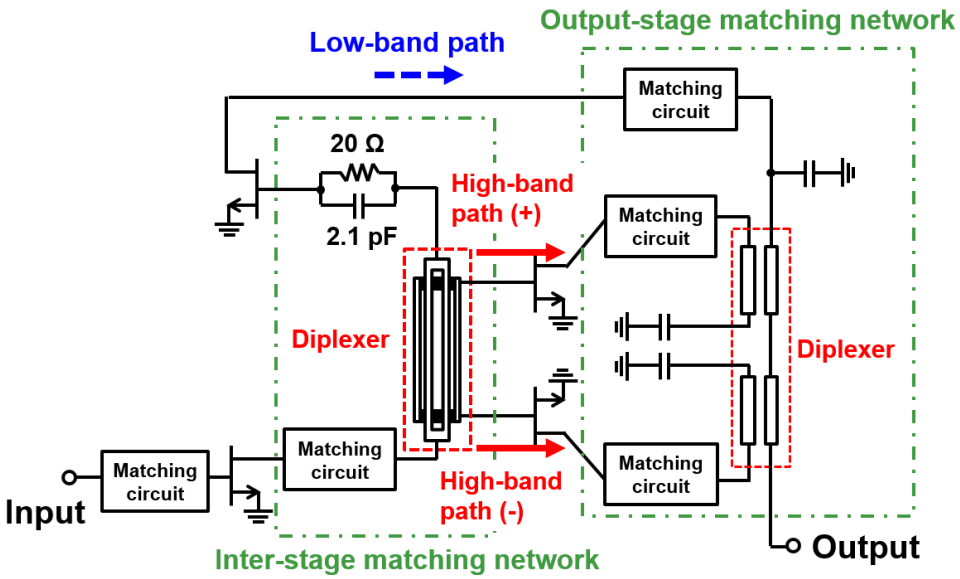


Fig. 3.9. Coupled-line-based diplexer (a) layout and (b) equivalent circuit.

signals are not transmitted through low-band path because C_{ds} of the low-band transistor is not used for the short capacitor. The maximum phase error of the high-band differential signals is about 15° at 11 GHz, which is due to the longer coupled-line length than inter-stage.

Fig. 3.9 shows the overall circuit schematic of the PA using the proposed diplexer structure. The input matching circuit is designed using the basic double-resonance matching method, and the inter-stage and output-stage use the coupled-line based diplexers described above.

3.2.3. Loss Analysis of Matching Networks

To compare the loss at the matching network, the 2-stage broadband PA is designed. The designed PA use same size of transistors as the proposed reconfigurable amplifier and it is designed by using RMPA topology. Fig 3.10 shows

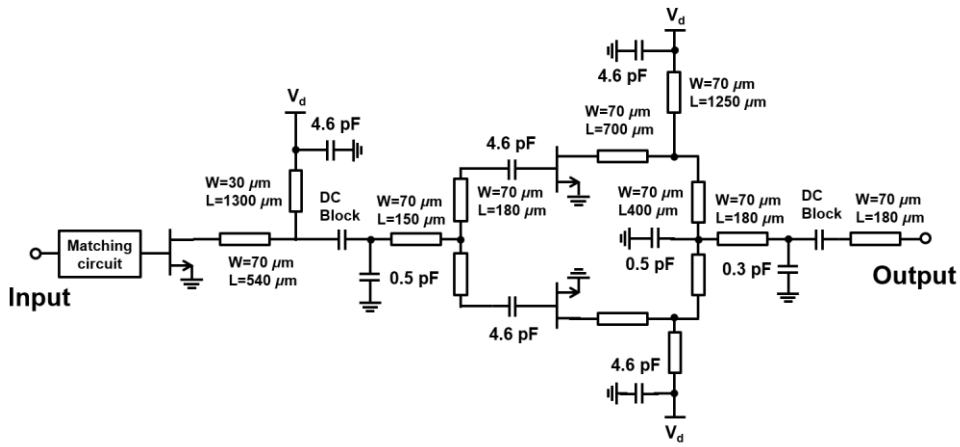


Fig. 3.10. Schematic of designed 6-18 GHz RMPA.

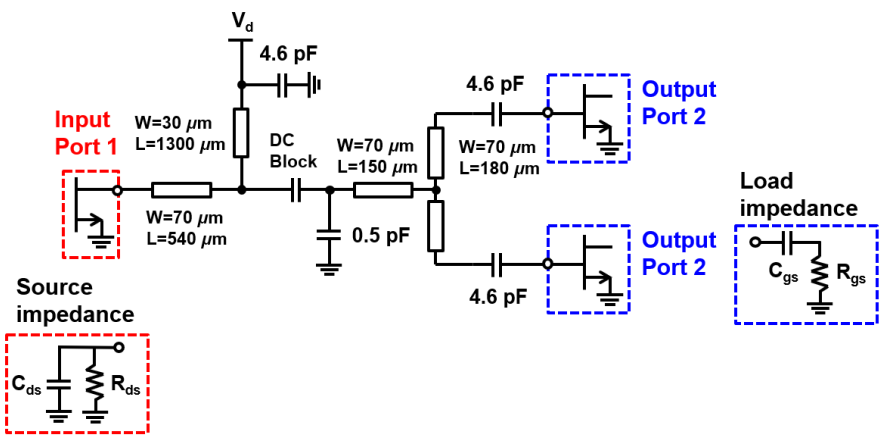
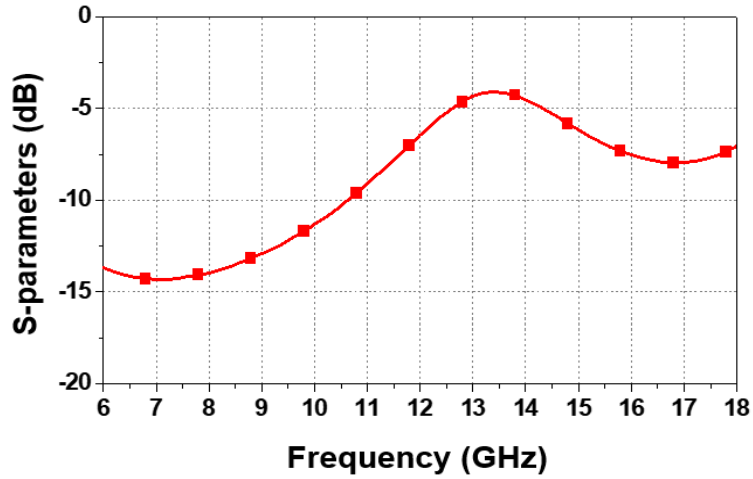


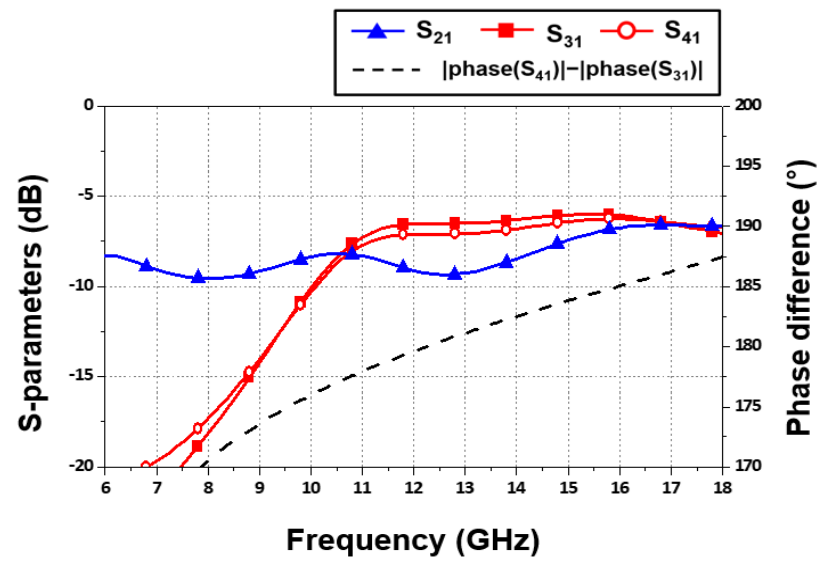
Fig. 3.11. Loss simulation condition of inter-stage matching network of RMPA.

the designed schematic of 6-18 GHz RMPA. To compare loss of matching network, each matching network simulate using Keysight ADS and compare transmission loss of the matching networks.

The designed inter-stage matching network has three resonances at 5, 13, and 19 GHz. Fig 3.11 shows the schematic and port condition of designed inter-stage matching network. The input port impedance is as same as drain impedance of the transistor and the output port impedance is gate impedance of the transistor. Fig. 3.12



(a)



(b)

Fig. 3.12. Simulation results of transmission loss at inter-stage matching network (a) using conventional transmission line, and (b) proposed structure.

(a) shows single path transmission loss of designed inter-stage matching network of the RMPA, and (b) shows the loss of inter-stage matching network using proposed diplexer structure. In Fig 3.12 (b), the S_{21} is a coupled-power of the low-band path in proposed structure. And S_{31} and S_{41} is the coupled-power of the each high-band path (coupled- and isolated-ports), respectively. In low-band frequency, the ideal transmission loss of the RMPA can be obtained by adding 3 dB to the single path transmission loss. Therefore, the inter-stage transmission loss of the proposed reconfigurable amplifier shows smaller than RMPA below 10 GHz. In high-band frequency, the simulated loss of the inter-stage matching network shows the proposed reconfigurable structure has smaller transmission loss than RMPA overall high-band frequency except 11.5–15 GHz.

Fig 3.13 shows the loss simulation condition of the output-stage matching network. The input port impedance is as same as drain impedance of the transistor and the output port impedance is 50 Ω port impedance. Fig 3.14 (a) shows the single path loss of output-stage matching network designed by using RMPA topology, and (b) shows the loss of output-stage matching network using proposed structure. In Fig. 3.14 (b), the S_{21} is a coupled-power of the low-band path in proposed structure and S_{31} and S_{41} is the coupled-power of the each high-band path (coupled- and isolated-ports), respectively. For output-stage matching network, the proposed structure shows smaller loss than RMPA structure in low-band frequency and shows similar average loss in high-band frequency.

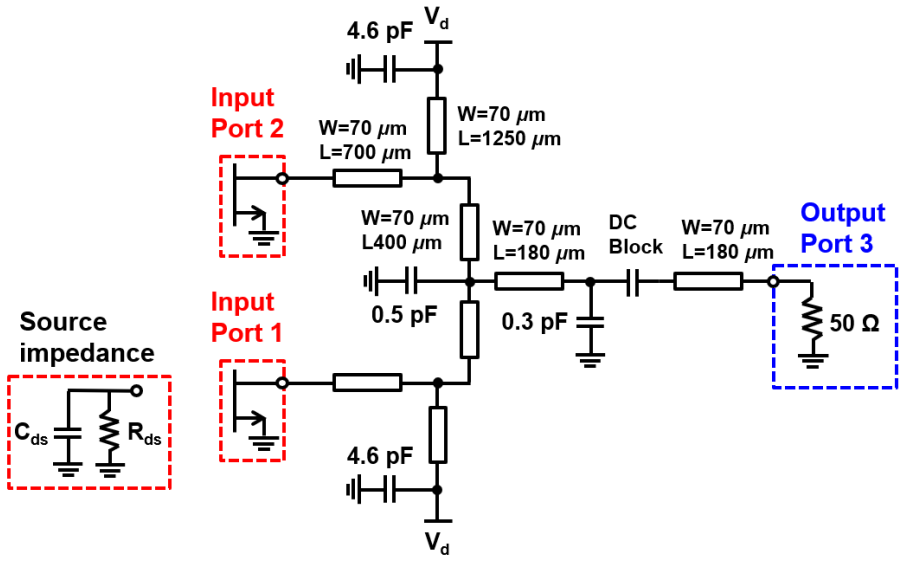
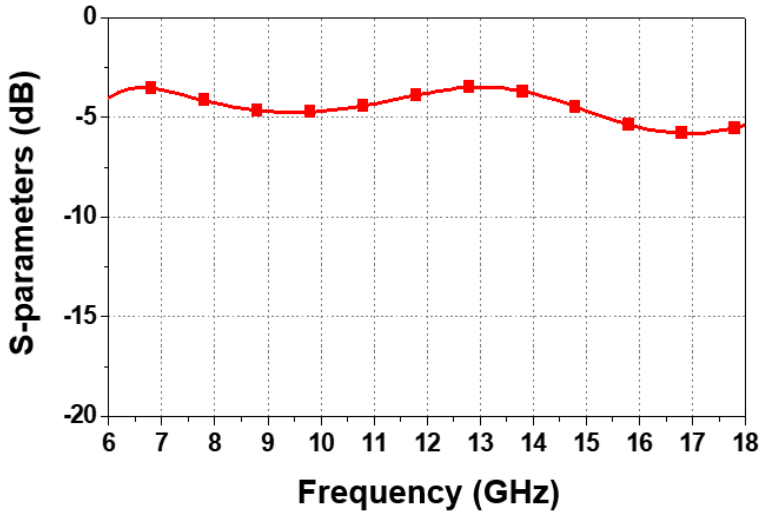
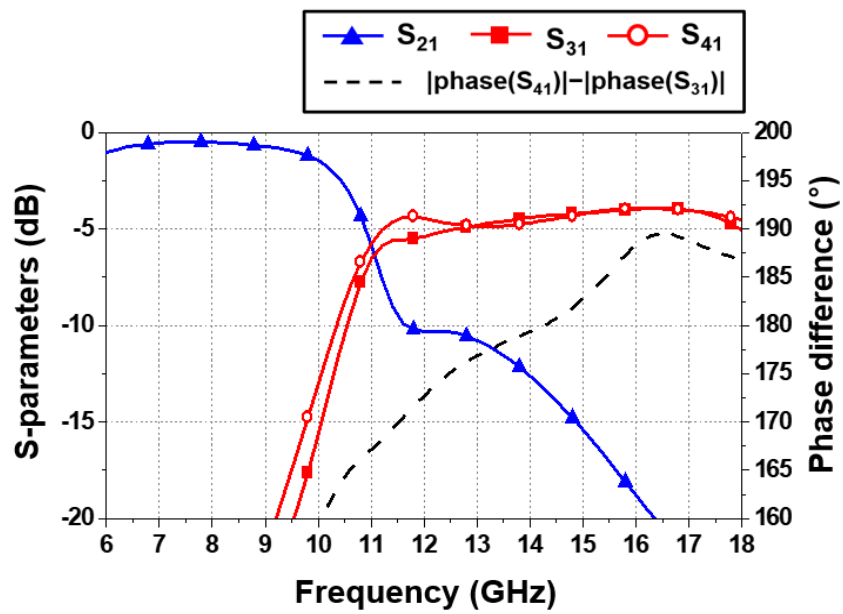


Fig. 3.13. Loss simulation condition of output-stage matching network of RMPA.



(a)



(b)

Fig. 3.14. Simulation results of transmission loss at output-stage matching network (a) using conventional transmission line, and (b) proposed structure.

3.3. Operation Analysis at Transition Frequency

The potential problem of the proposed structure is the power combining near the transition frequency. As shown in Fig 3.15, the proposed PA has one low-band frequency path and two high-band frequency paths. At the transition frequency, the input signal is equally divided and transferred to all three ports. Therefore, in this case, it is necessary to operate in the all-band mode in which both band PAs are turned on.

For power combining at all-band mode, the phase difference between all paths are 0 at the output port. To obtain phase difference between ports, use circuit simulator. Fig. 3.16 shows the phase difference in the other signal path relative to the high-band (−) path. Near the transition frequency (10–11 GHz), the phase difference in the high-band and low-band paths shows the out-of-phase relations at the output stage. Therefore, the output signal in each mode PA is canceled when operating in all-band mode.

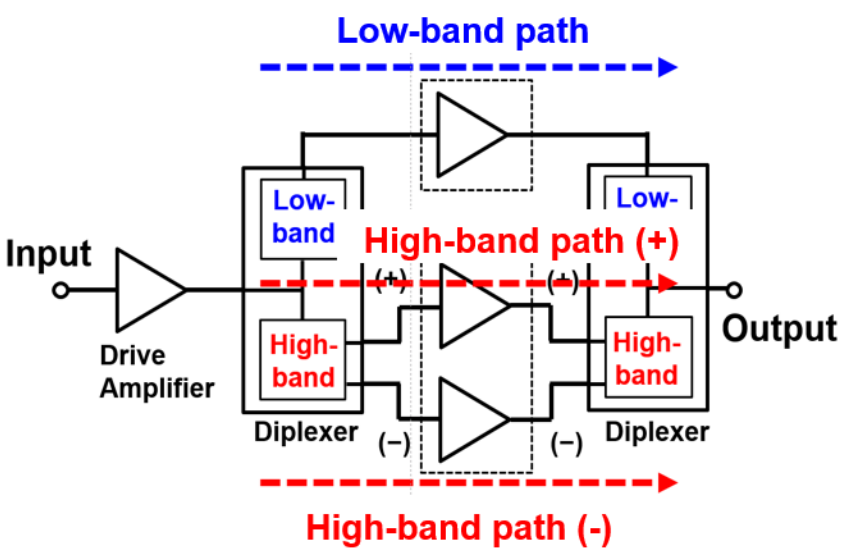


Fig. 3.15. Transmission paths at all-band mode.

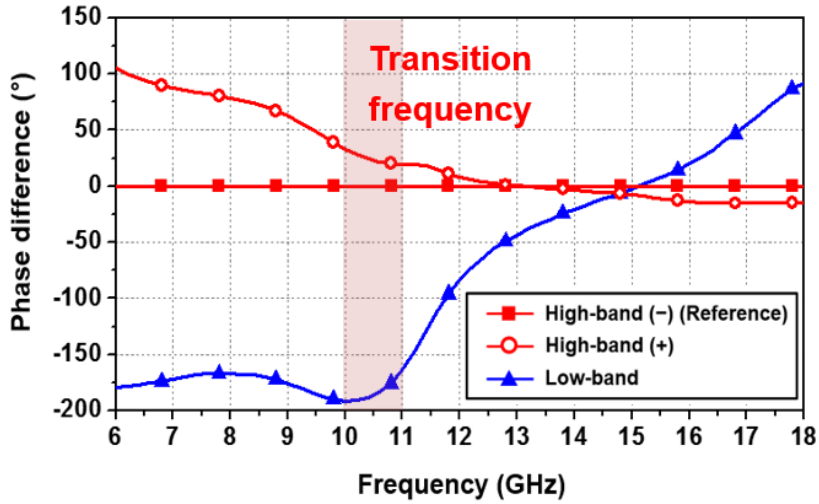


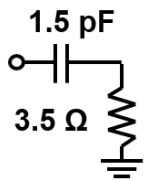
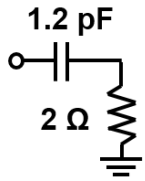
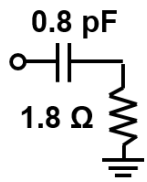
Fig. 3.16. Simulation results of the normalized phase difference for each signal path.

3.4. Analysis of Optimum Transistor Off Condition

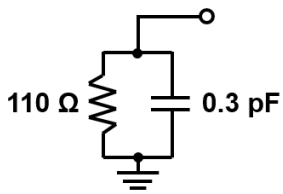
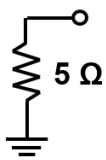
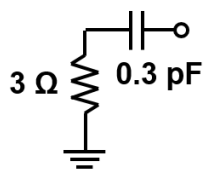
Since the off-state characteristic of the transistors in the inactive path affects the operation of the active path, the transistors of the unused mode need to be turned off. The off-state bias of the transistor refers to the case when the drain current is zero. It can be divided into “ohmic” and “cut-off” regions according to V_{gs} and V_{ds} biases of the transistor. Fig. 3.17 shows the bias conditions, and the gate and drain equivalent circuits of each off-state region for 6×125-μm sized transistor. As shown in the gate equivalent circuit, both C_{gs} and R_{gs} are reduced compared to the on-state. In contrast, the drain equivalent circuit of a transistor exhibits different models between the two off-state bias conditions. Therefore, the output matching network is more influenced by the off-state bias. The optimal off-state bias of each unused mode transistor is analyzed in terms of operating frequency band and overall PA gain.

For inter-stage circuit, reduced C_{gs} of high-band transistors increases the resonance frequency with the coupled-line inductance, which reduces the transferred power to high-band transistors. Therefore, in the low-band mode, a high gain can be obtained by setting the high-band transistor at “cut-off” off-state bias condition. In the high-band mode, the operating properties are determined by the termination condition at the through-port of the coupled-line. To provide impedance conditions close to short-circuit, the low-band transistor should be biased in “ohmic” condition to avoid capacitive loading.

In the output stage, as the capacitance of the transistor decreases, the resonance frequency increases, resulting in wide low-band mode operation, wider bandwidth can be achieved when the high-band transistor is turned off with “ohmic” off-state bias condition. The “ohmic” bias condition leaves a finite resistance, leading to potential power loss. However, since the power loss of the low-band frequency signal

State	On	Off : ohmic	Off : cut-off
Bias condition	V_{gs} = −2.4 V V_{ds} = 30 V	V_{gs} = 0 V V_{ds} = 0 V	V_{gs} = −4 V V_{ds} = 30 V
Equivalent circuit			

(a)

State	On	Off : ohmic	Off : cut-off
Bias condition	V_{gs} = −2.4 V V_{ds} = 30 V	V_{gs} = 0 V V_{ds} = 0 V	V_{gs} = −4 V V_{ds} = 30 V
Equivalent circuit			

(b)

Fig. 3.17. (a) Gate and (b) drain equivalent circuits of 6×125-μm transistor at on and off bias conditions.

to the high-band transistor is small, this loss is not a dominant factor in the design choices.

In the high-band mode, the operating frequency band and gain are determined by the drain impedance of the low-band transistor. Since the drain of the low-band transistor presents a small resistance without reactance in the “ohmic” off-state bias, wideband characteristics can be achieved. Fig 3.17 shows simulation results of the amplitude and phase difference between two high-band signals by transistor off

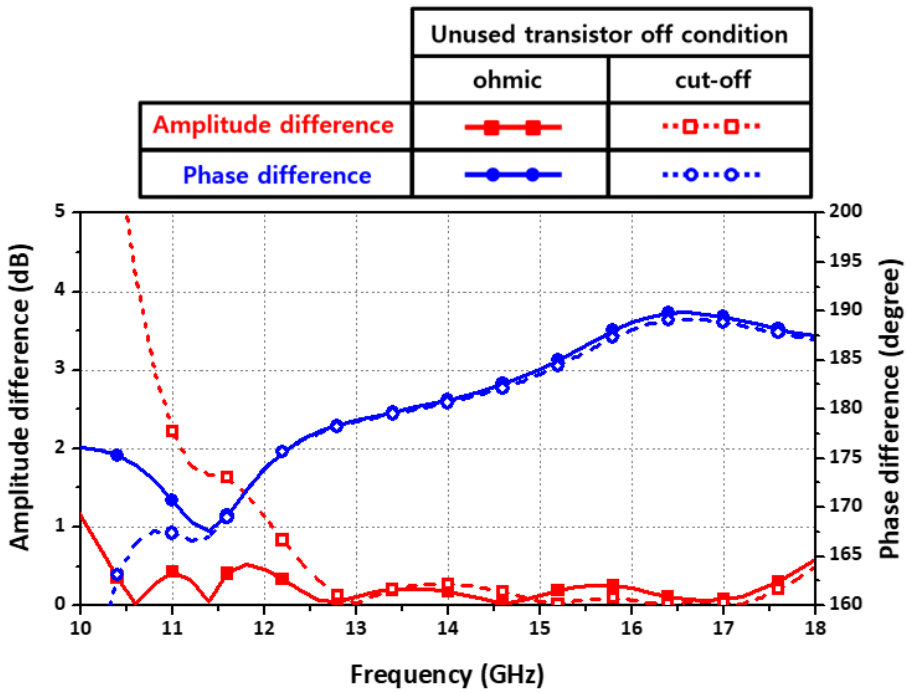


Fig. 3.18. Simulation results of amplitude and phase difference between two high-band frequency signals by transistor off condition.

condition. The amplitude difference is small when low-band PA transistor off with "ohmic" off-state bias and the phase difference is similar both "ohmic" and "cut-off" off-state bias condition.

For low-band mode operation, there is a trade-off between the operation bandwidth and PA gain. Wide operation bandwidth can be obtained when the high-band transistors are turned off with "ohmic" bias while higher gain can be achieved with "cut-off" bias. For better overall PA gain, we have biased high-band transistors with "cut-off" bias for low-band mode operation.

Chapter 4

Measured Results of the Reconfigurable Amplifier

4.1. Introduction

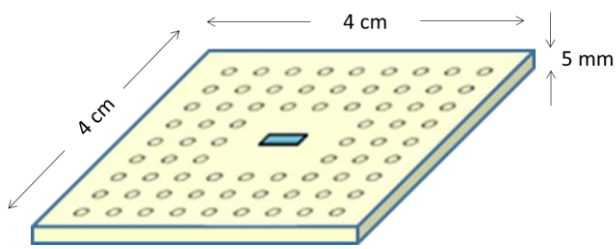
In the GaN process, the thermal compensation condition is important to obtain optimum electrical characteristic since the GaN PA produces large amount of RF output power with significant amount of dc dissipation power. Due to the high bias voltage and current, the GaN HEMT device has self-heat issue. This thermal issue reduces the drain current of the transistor and this also degrade the output power and break the transistor. To decrease temperature of the transistor, conventionally the die is attached to metal fixture using epoxy with high thermal conductivity.

In this chapter, introduce the measured condition and results of the fabricated MMIC. To thermal compensation, the metal test fixture was used, and the die was attached by thermal epoxy. Also, the measured setup of the S-parameters and output power and measured results are explained. The measured results are compared with other previous works.

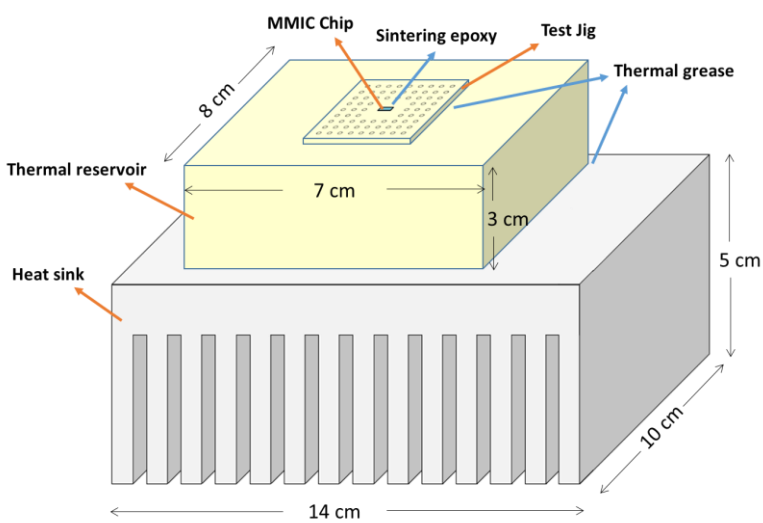
4.2. Measurement Condition

4.2.1. Die Attachment Condition for Heat Compensation

To mitigate the self-heating effect of the fabricated MMIC, the die is attached to an Au-plated Cu carrier with a high-thermal-conductive adhesive, as shown in Fig. 4.1. The used adhesive is EK2000 by Epoxy Technology Inc. with a thermal conductivity of 35.5 W/mK. The test fixture is composed of a 5-mm-thick Au-plated Cu carrier and a heat sink with thermal grease of 8.5 W/mK thermal conductivity.



(a)



(b)

Fig. 4.1. The illustration of the (a) test fixture and (b) heat sink configuration

4.2.2. S-parameters Measurement Setup

The S-parameters measurement confirmed by on-wafer probing condition. Fig 4.2 shows the on-wafer S-parameters measurement setup. To measure the S-parameters, use network analyzer of Anritsu MS4647A and RF probe of Cascade 67-A-GSG-150 probe. The calibration is conducted using on-wafer calibration substrate.

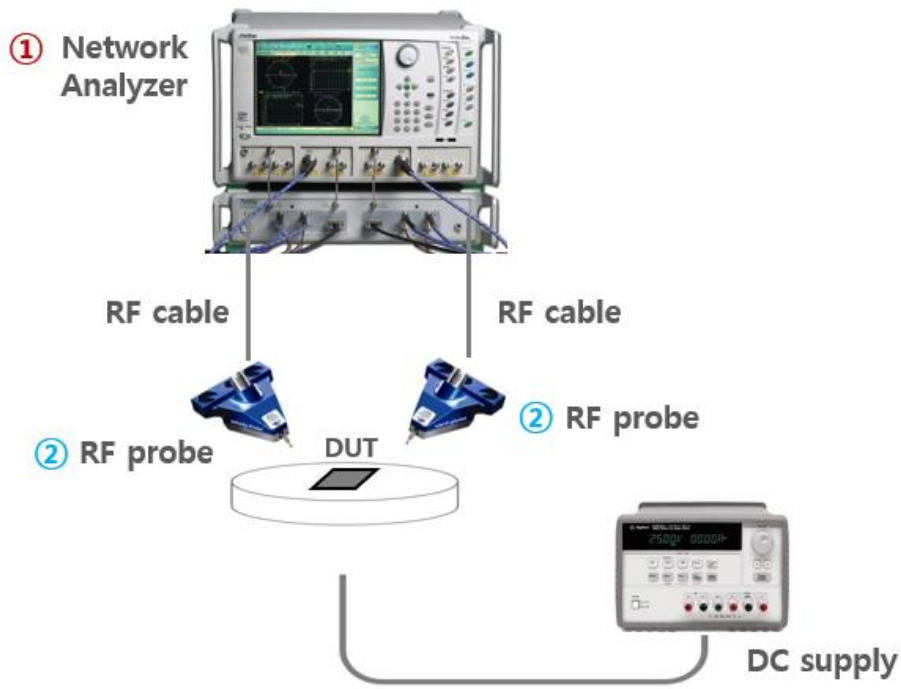


Fig. 4.2. S-parameters measurement setup.

4.2.3. Output Power and PAE Measurement Setup

The output power and PAE measurement confirmed by continuous wave (CW) condition with on-wafer probing. Fig 4.3 shows the on-wafer power and PAE measurement setup. The additional drive amplifier used for enough input power and spectrum analyzer used to check oscillation. the two power sensors used for measuring input and output power at DUT.

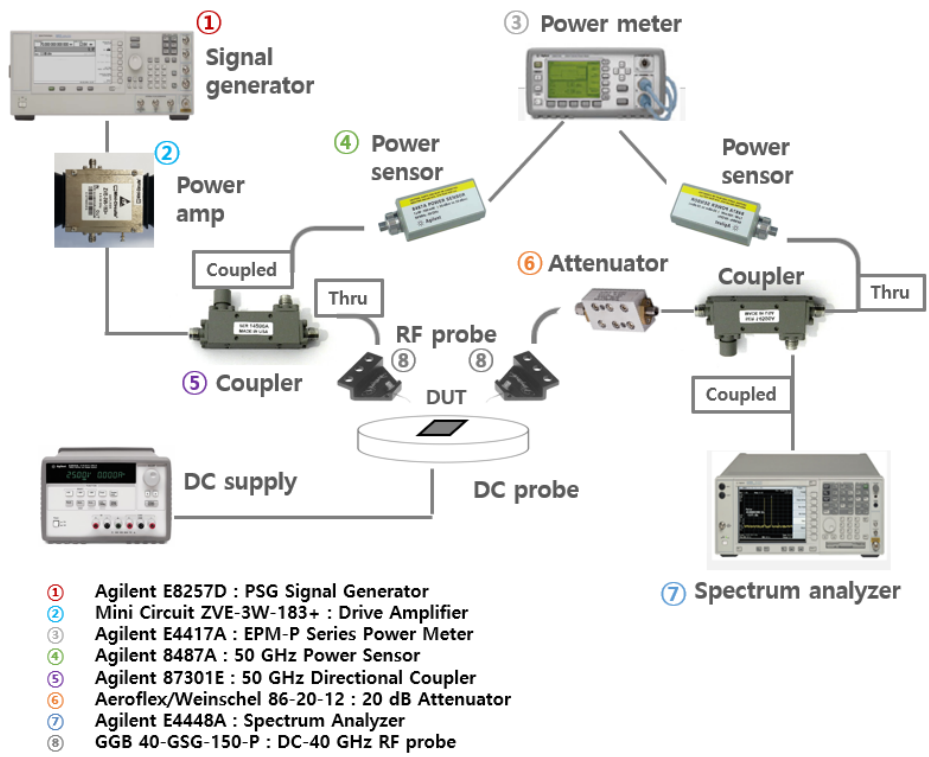
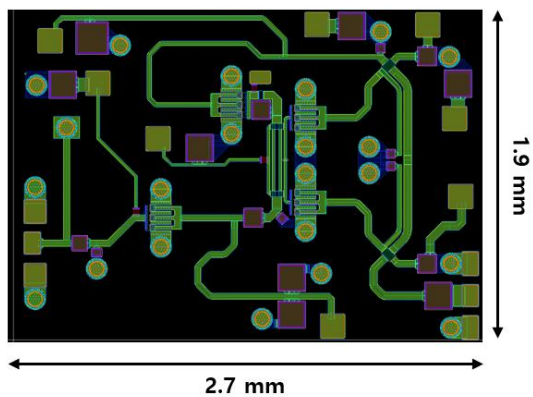


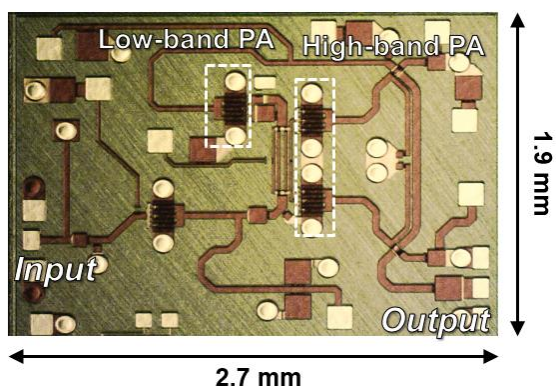
Fig. 4.3. Output power and PAE measurement setup.

4.3. Measured Results of the Switchless Reconfigurable Amplifier

The designed switchless reconfigurable amplifier is fabricated with commercial 0.25-μm GaN HEMT process of WIN semiconductors. Fig. 4.4 is a layout and die photograph of the fabricated PA, the total die size is 2.7×1.9 mm including all RF and dc probing pads.



(a)



(b)

Fig. 4.4. (a) The layout and (b) photograph of fabricated single reconfigurable PA MMIC.

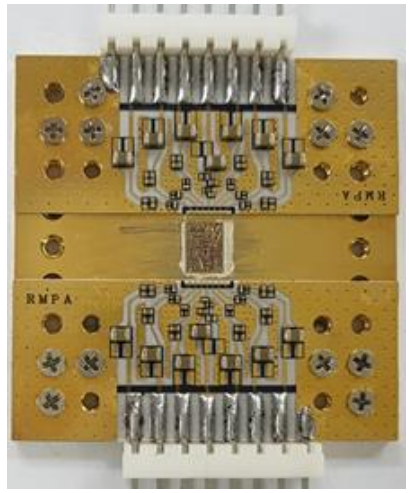
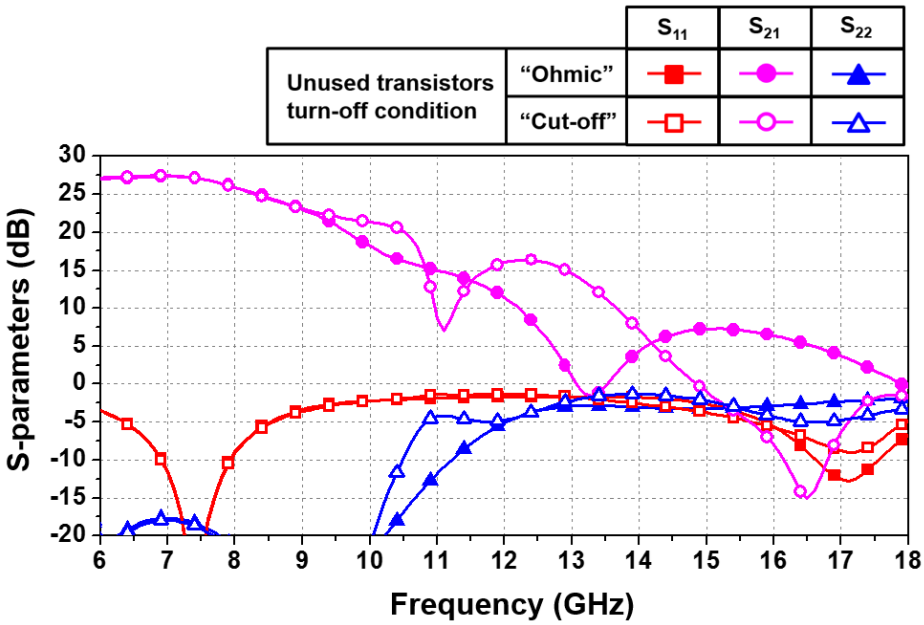


Fig. 4.5. The photograph of test fixture.

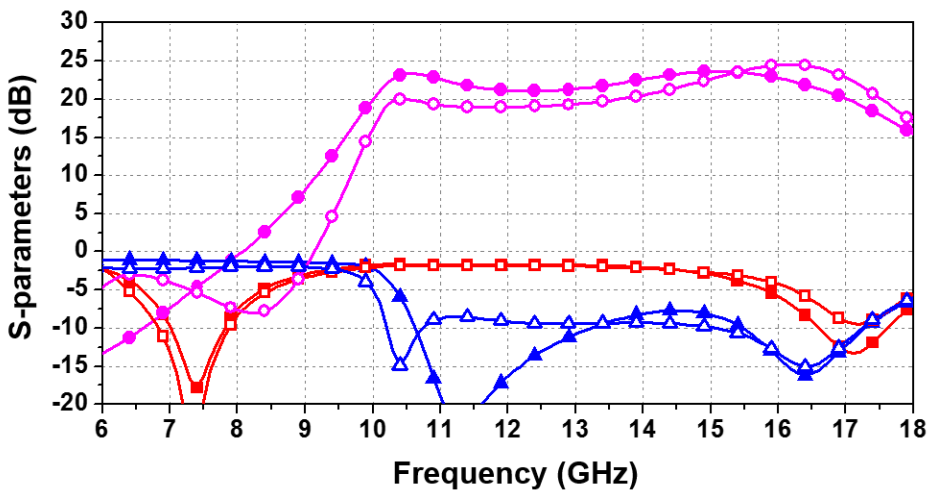
4.3.1. S-parameters Measured Results

Fig. 4.6 (a) shows the measured S-parameters of the low-band mode according to the off-state bias conditions of the high-band transistors. More than 20 dB gain can be achieved up to 9 GHz regardless of the off-state bias condition of the high-band transistors. However, when the high-band transistors are biased at “cut-off” condition, there is resonance around 11 GHz, which limits the operation bandwidth to 10.5 GHz. On the other hand, when the high-band transistors are biased at “ohmic” condition, a wider low-band operation bandwidth can be achieved. However, the PA gain rolls off from 9 GHz due to power loss at the gate and drain ports of the high-band transistors. To achieve low-band mode operation up to 10.5 GHz, “cut-off” off-state bias is thus preferred for high-band transistors.

The measured S-parameters at the high-band mode according to the off-state bias of the low-band transistor as shown in Fig. 4.6 (b). In the high-band mode, a



(a)



(b)

Fig. 4.6. Measured S-parameters results of (a) low-band mode and (b) high-band mode.

wider operating frequency band and a high gain can be obtained when the low-band transistor is biased at “ohmic” condition. Higher than 15 dB gain is achieved from 9.7 to 18 GHz with “ohmic” off-state bias condition of the low-band

Fig. 4.7 shows measured S-parameters of both modes simultaneously. The high-band transistors are biased at “cut-off” condition in the low-band mode while the low-band transistor is biased at “ohmic” conditions in the high-band mode. The gain higher than 15 dB can be obtained from 6 to 18 GHz by changing the mode at 10.5 GHz. The gain mismatch between simulation and measurements at high-band mode is due to the shifted frequency response of the output matching network, and inaccurate off-state transistor model at high-band frequencies. The measured S-parameters in all-band mode are shown in Fig. 4.8. As analyzed earlier in chapter 3, there is a gain drop in the transition frequency (10–11 GHz), since the signals through low-band and high-band PAs are combined out of phase at the PA output.

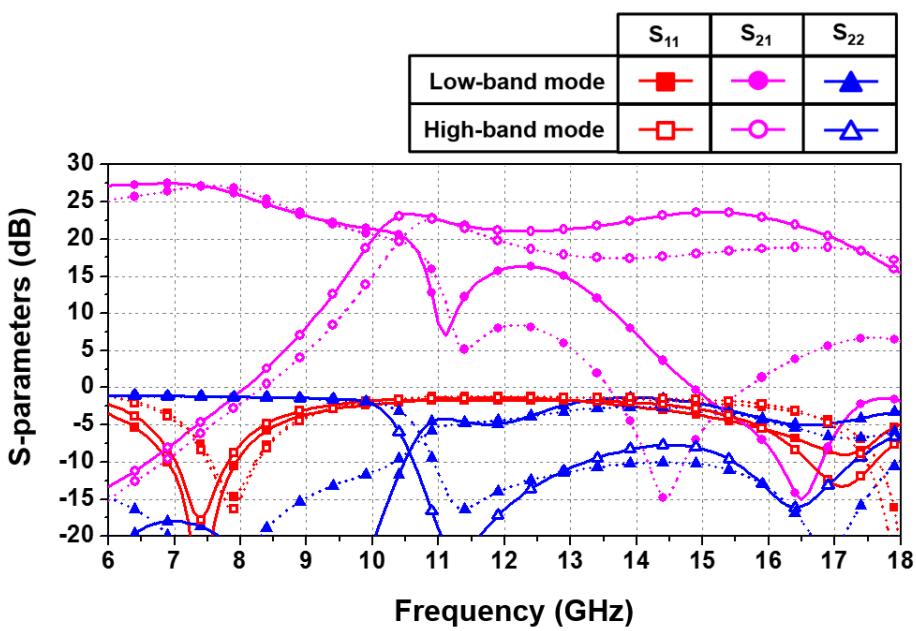


Fig. 4.7. Measured (solid) and simulated (dot) S-parameters results of low-band and high-band mode.

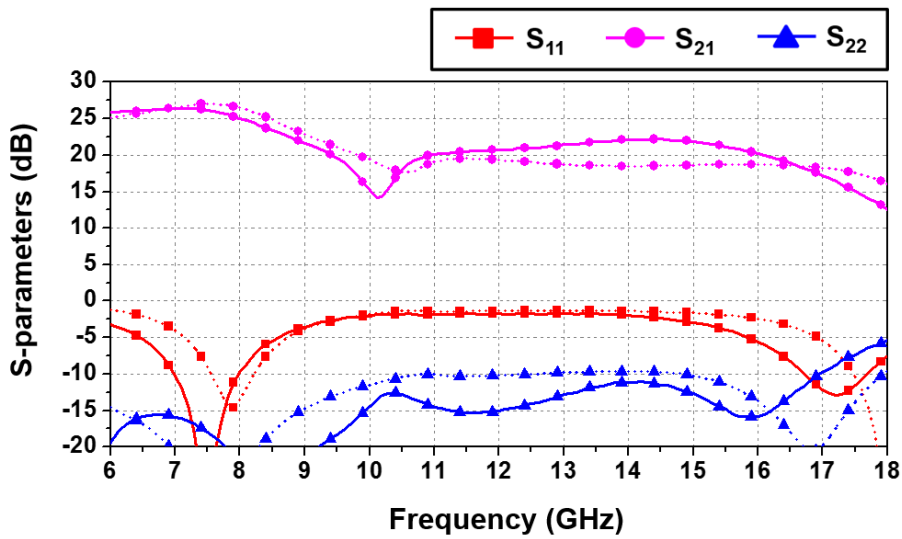
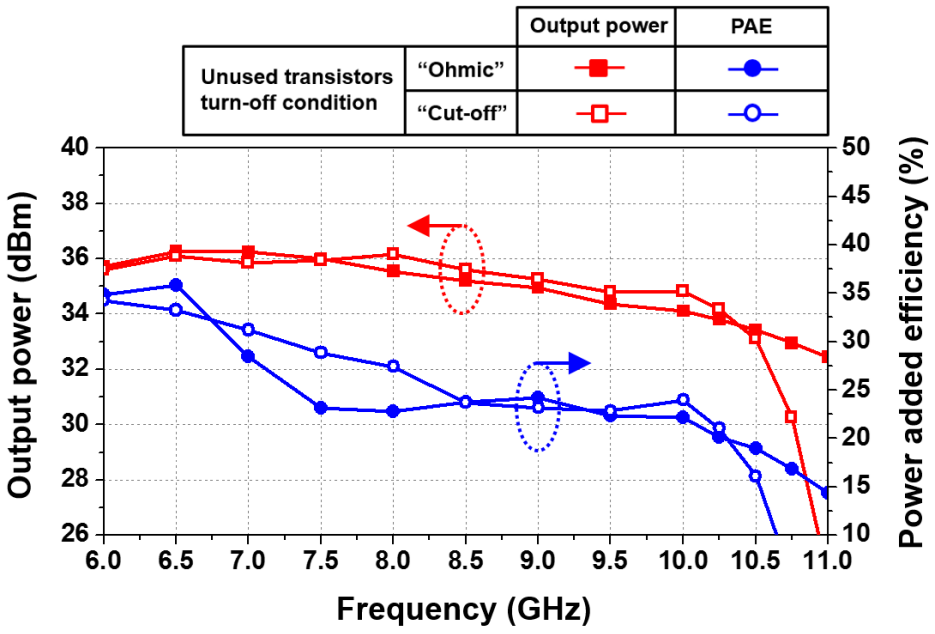


Fig. 4.8. Measured (solid) and simulated (dot) S-parameters results at all-band mode.

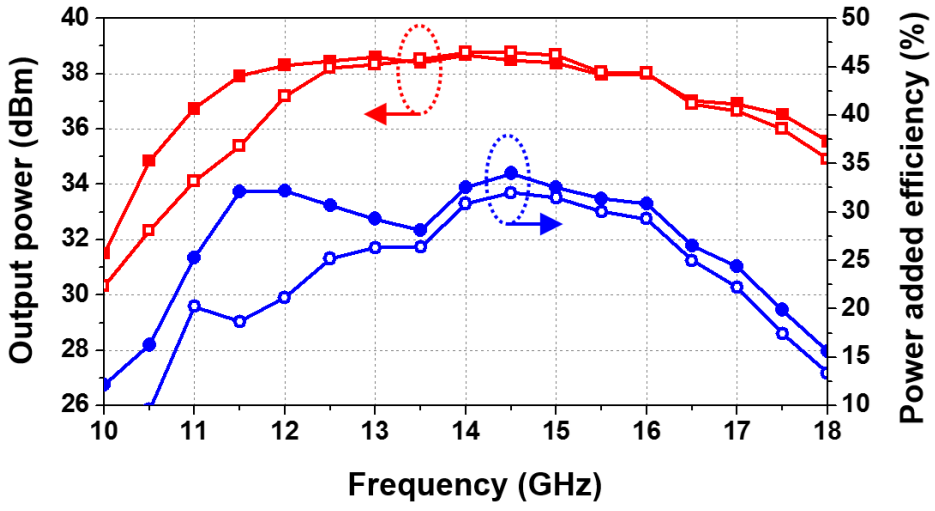
4.3.2. Power and PAE Measured Results

Fig. 4.9 (a) shows the measured output power and PAE in the low-band mode. Unlike the S-parameters characteristic, the output power and PAE showed similar performance regardless of the off-state bias condition of the high-band transistors. This is because the output power saturates at low-band frequencies due to high small-signal gain. This result also shows that the power dissipated at the drain resistor of the high-band transistors is less than 1 dB. The average output power and PAE from 6 to 10.5 GHz are 35 dBm and 23%, respectively while the maximum output power and PAE are 36 dBm and 34%, respectively.

Fig. 4.9 (b) shows the measured output power and PAE in the high-band mode. Unlike the low-band mode, the high-band mode shows different large-signal performance depending on the off-state bias conditions of the low-band transistor.



(a)



(b)

Fig. 4.9. Measured output power and PAE results of (a) low-band mode and (b) high-band mode.

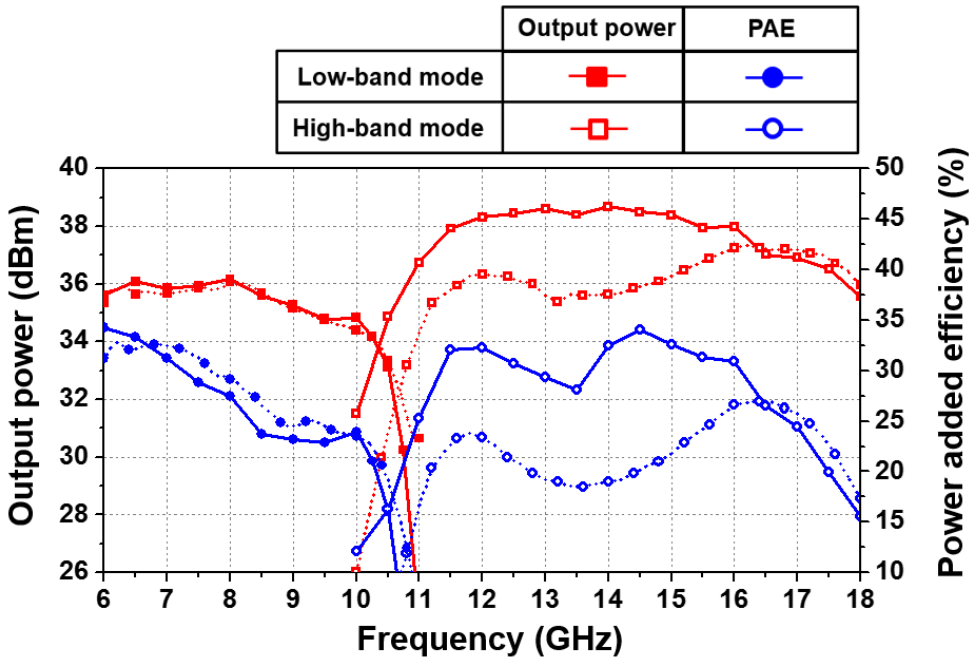


Fig. 4.10. Measured (solid) and simulated (dot) output power and PAE of low-band and high-band mode.

When the low-band transistor is turned off in “cut-off” condition, the average output power of 37 dBm and the average PAE of 23.5% are measured from 10.5 to 18 GHz band. The maximum output power was 38.7 dBm, and the maximum PAE is 32%. On the other hand, when the low-band transistor was turned off in “ohmic” off-stage bias condition, slightly higher average output power of 37.5 dBm and higher average PAE of 27% are achieved in the same band, and the maximum output power is 38 dBm and the PAE is 34%. For the high-band mode, better large-signal performance is achieved with “ohmic” bias condition. This is because, as in the S-parameters result, the better short-circuit characteristics can be obtained when the low-band transistor is turned off in “ohmic” off-state bias condition.

Fig. 4.10 shows the measured output power and PAE for both modes simultaneously. For this testing, the unused transistors in low-band and high-band

modes are turned off using “cut-off” bias and “ohmic” bias conditions, respectively. The worst-case performance is observed around 10.5 GHz with a power of 34 dBm and a PAE of 15%.

4.4. 2-way Combined Reconfigurable Amplifier

For better output power characteristic using proposed reconfigurable amplifier topology, the 2-way combined PA is designed. The designed 2-way combined switchless reconfigurable amplifier combine the output power using Wilkinson combiner. Fig. 4.11 shows the circuit block diagram of the designed 2-way combined reconfigurable amplifier. The input matching network is designed for matching and power dividing with simple TEE-divider structure.

The designed 2-way combined reconfigurable amplifier is fabricated with commercial 0.25-μm GaN HEMT process. Fig. 4.12 is a die photograph of the fabricated amplifier. the total die size is 3.8×3.4 mm including all RF and dc probing pads. The fabricated MMIC was measured by on-wafer probing with continuous

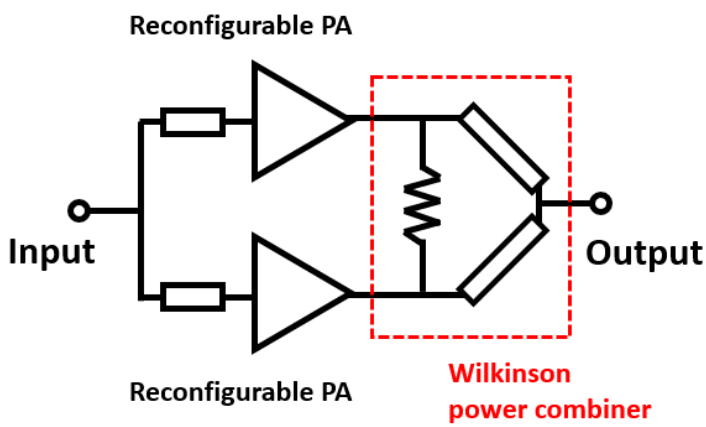
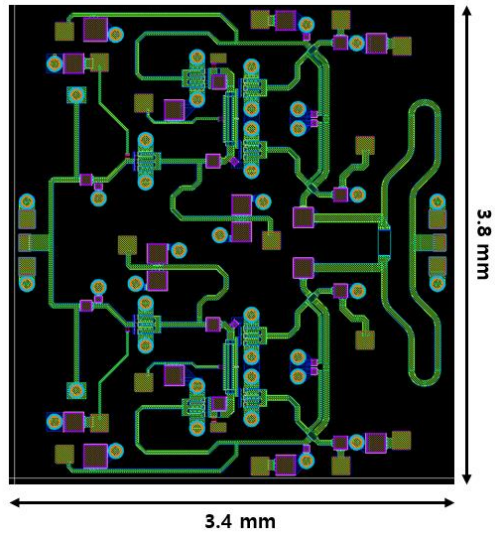
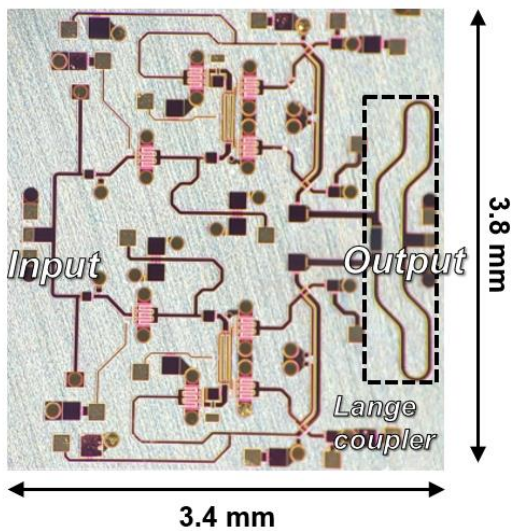


Fig. 4.11. Block diagram of the 2-way combined reconfigurable PA.



(a)



(b)

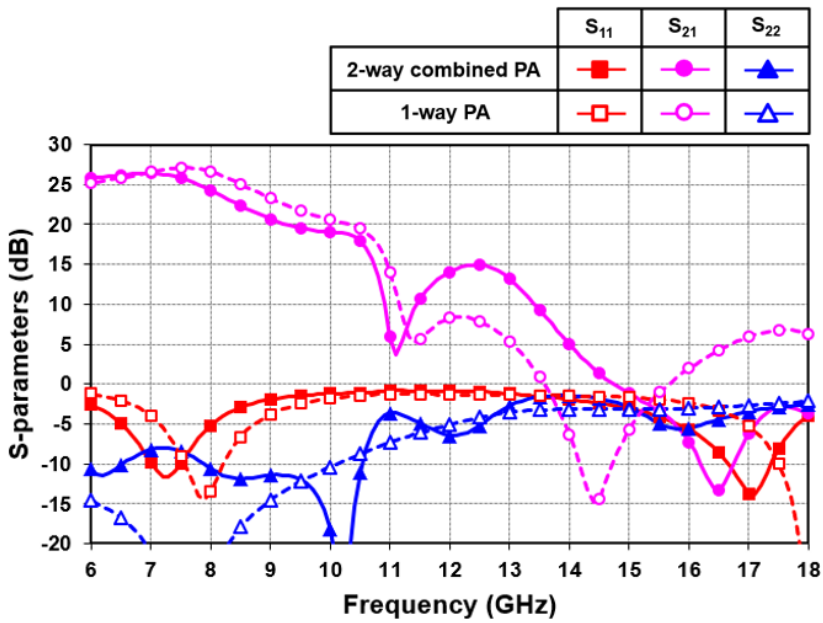
Fig. 4.12. 2-way combined reconfigurable amplifier (a) layout and (b) fabricated MMIC.

wave (CW) condition, and the die was mounted on a 5-mm-thick Au-plated Cu carrier to mitigate self-heating of the amplifier. The measurement bias of amplifier was 30 V and 100 mA for V_{ds} and I_{ds}, respectively.

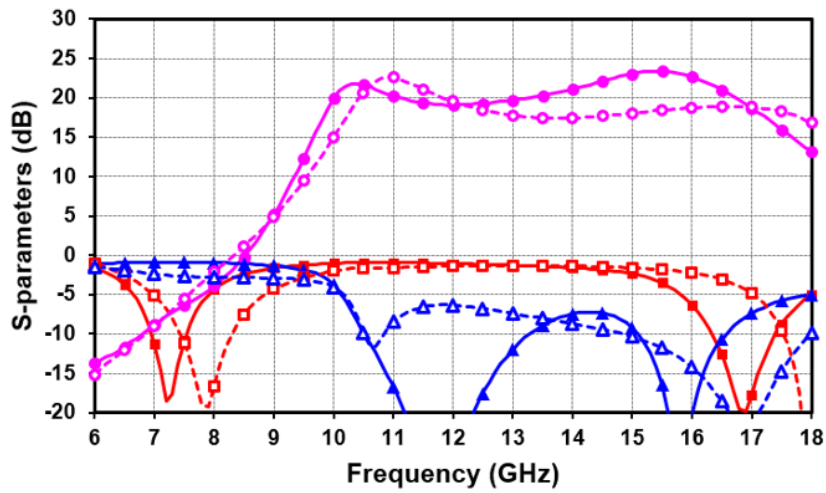
4.4.1. S-parameters Measured Results

Fig 4.13 shows the measured S-parameter results of single and 2-way combined reconfigurable amplifier at low- and high-mode. In low-band mode, the measured result of the 2-way combined amplifier shows over 15 dB gain at 6–10.5 GHz. The measured gain is decreased about 2 dB than single reconfigurable amplifier at 7.5–11 GHz. It is because the Wilkinson combiner loss and matching frequency shifting at input matching network. The measured results in Fig. 4.13 (a) shows the 1 GHz shifted S_{11} and this shift the gain to lower frequency.

In high-band mode, the measured result shows over 15 dB gain at 10–17 GHz. The gain compression over 17 GHz comes from matching frequency shifting at input and output matching network. The S_{11} and S_{22} measured result in Fig. 4.13 (b) shows 1 GHz down shifted matching resonance at both S_{11} and S_{22}. This matching frequency at matching network shift gain shape to lower frequency. Therefore, the measured 2-way combined amplifier shows higher gain than single reconfigurable amplifier at 13–16.5 GHz and lower gain at 18 GHz.



(a)



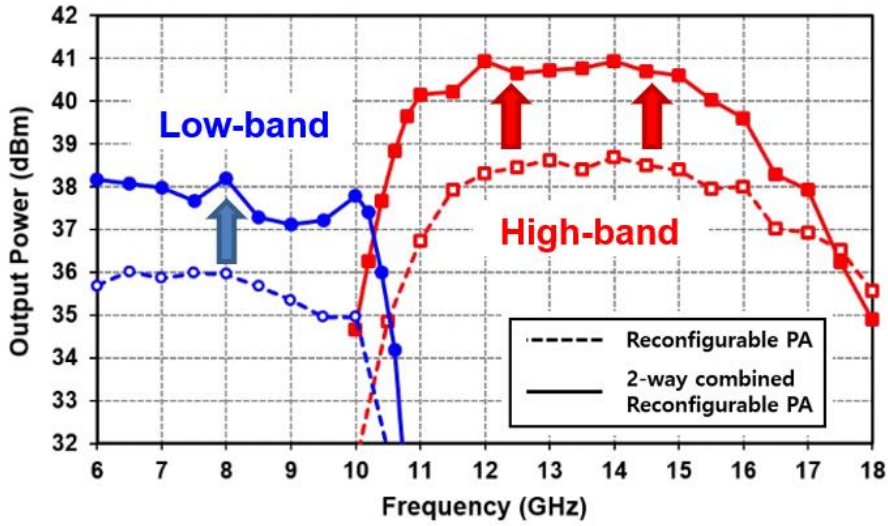
(b)

Fig. 4.13. Measured S-parameters results of 2-way combined reconfigurable amplifier at (a) low-band mode and (b) high-band mode.

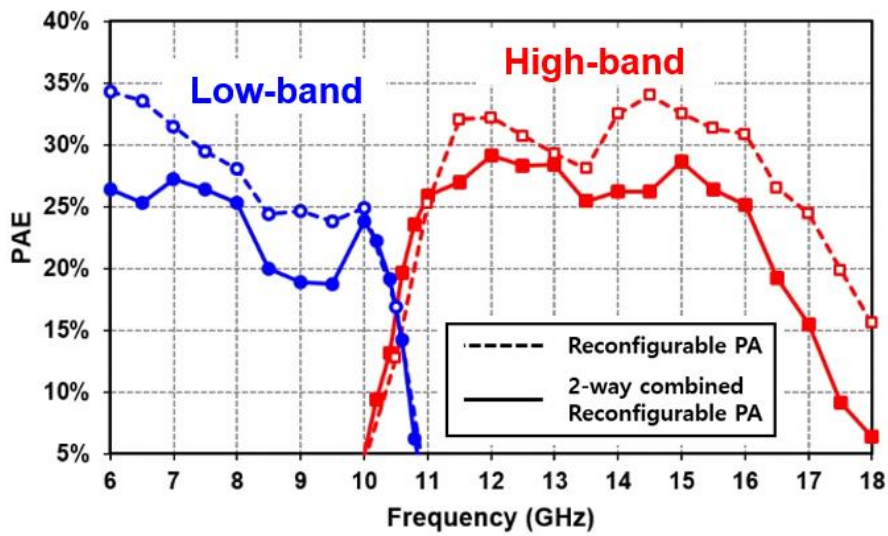
4.4.1. Power and PAE Measured Results

Fig 4.14 shows the measured output power and PAE characteristics of 2-way combined reconfigurable amplifier at the low- and high-band mode. In low-band mode, operation frequency of 6 to 10.5 GHz, the average output power is 37.5 dBm when high-band transistors are turned off in “cut-off” bias condition. In high-band mode, the measured output power showed frequency down shifted shape than single reconfigurable amplifier. This frequency down shifted output power is the same tendency of gain results, and it is because matching frequency shifted at Wilkinson combiner at output matching network. The measured average output power is 40 dBm over 10.5–17 GHz when low-band transistor is turned off with “ohmic” bias condition. Fig 4.14 (b) shows the measure PAE in the low- and high-band mode. In low-band mode. The PAE measured results showed same tendency as measured output power. The measured average PAE in low-band mode is 20% when high-band transistors are turned off with “cut-off” bias condition. And the measured average PAE in high-band mode is 20% when low-band transistor is turned off with “ohmic” bias condition.

Table 4.1 shows a comparison of the state-of-the-art broadband PAs using the GaN process. In the proposed structure, higher PAE can be obtained compared to the other broadband PAs since each band is covered with narrowband PAs. In addition, thanks to the proposed diplexer, the dual-band mode is implemented in a small size.



(a)



(b)

Fig. 4.14. Comparison of measured (a) output power (b) PAE of single reconfigurable PA and 2-way combined PA.

TABLE 4.1

Performance comparison table of GaN broadband PAs.

Reference		Gate length (μm)	Frequency (GHz)	Topology	f_{max} (GHz)	PAE (%)	Pout (dBm)	Gain (dB)	Area (mm^2)	Power density (W/mm^2)
TMTT, 2011		0.2	2–18	DA	N/A	5–15	29–33	18–21	8	0.1–0.25
ETRI J., 2017		0.25	6–18	DA	90	17–22	39.5–40.4	17.6–21.8	25	0.36–0.44
JSSC, 2009		0.25	2–18	DA	105	20–38	39.5–41.7	10–14	12.6	0.59–0.98
IMS, 2011		0.2	2–20	DA	121	15–36	40–43.3	N/A	38	0.26–0.57
EL, 2016		0.25	6–18	DA	74.6	8.8–18.4	41–45	13–17	21.0	0.60–1.40
TMTT, 2018		0.2	6–18	RMDA[1]	74.6	15.0–29.4	11.5–44.7	16.7–24.1	13.8	0.83–1.59
TMTT, 2013		0.25	6–18	RMPA	N/A	14–24	35–43	17–28	19.25	0.59–0.98
IMS, 2010		0.25	6–18	RMPA	N/A	13–25	37.7–40	18–24	19.8	0.30–0.51
ETRI, J., 2016		0.25	6–18	RMPA	90	10–23	40.9-43.8	20–29	27.5	0.45–0.87
TMTT, 2015		0.2	6–18	NMPA[2]	74.6	13–21	35.7–37.5	13.5–19.1	8.77	0.42–0.64
This work (1-way)	Low-band mode	0.25	6–10.5	Reconfigurable PA	74.6	15–34 (average 23)	34–36 (average 35)	17–27	5.4	0.46–0.74
	High-band mode		10.5–18			15–34 (average 27)	34–38.5 (average 37.5)	15–22		0.46–1.29
This work (2-way)	Low-band mode	0.25	6–10.5	Reconfigurable PA	74.6	15–28 (average 22)	37–38 (average 37.5)	16–26	12.9	0.38–0.49
	High-band mode		10.5–17			15–29 (average 25)	37–41 (average 39.3)	14–21		0.38–0.96

[1] Reactively matched distributed amplifier.
[2] Non-Foster matched power amplifier.

4.5. Conclusion

In this chapter, the switchless reconfigurable amplifier is proposed. The proposed reconfigurable amplifier used one low-band PA and two high-band PAs, and those PAs are combined by proposed coupled-line based diplexer. In inter-stage matching network, the proposed diplexer structure is directly adopted. In output-stage matching network, since the source impedance down have enough capacitance, the diplexer using two coupled-line structure is adopted. To verify loss at matching network, the conventional 2-stage broadband RMPA is designed, and the transmission loss of matching network is compared. The loss comparison results show the matching network using proposed diplexer has lower loss than conventional multi-resonance matching network. In contrast to these advantages, the operation at transition frequency is the issue of the proposed reconfigurable PA. This issue occurs from low isolation characteristic at inter-stage matching network and signal canceling operation at output port. The phase difference analysis of the paths at proposed PA is performed by using circuit simulator and phase simulation results shows the phase difference between low- and high-band path is out-of-phase relationship at transition frequency. Therefore, the proposed reconfigurable PA cannot operate when low-band and high-band PAs are turned-on simultaneously.

The designed reconfigurable PA is fabricated with commercial 0.25-μm GaN HEMT process. To reduce thermal effect in measurement, the MMIC is attached in test fixture. The S-parameters, output power, and PAE measurements were conducted with on-wafer probing. The fabricated PA shows over 15 dB small-signal gain at 5–11 GHz in the low-band mode and 9–18 GHz in the high-band mode. The measured average output power and PAE is 35 dBm, 23% in the low-band mode and 37 dBm, 26% in the high-band mode.

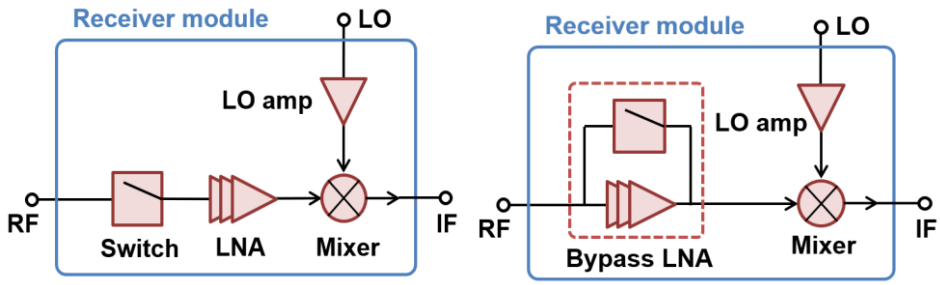
Chapter 5

Design of bypass Low noise amplifier using Coupled-line structure

5.1. Introduction

Conventionally, the receiver circuit consists of LNA, mixer, local oscillator (LO). The received signal is amplified at the LNA without additional noise and transferred to mixer to frequency down conversion. At the mixer, frequency of the input signal is down converted to intermediate frequency (IF). Since the received power from an antenna is very low, the LNA designed to obtain high small signal gain. From this reason, typically, the LNA is designed by using small sized transistors and these small sized transistors decrease input P_{1dB} characteristic of the LNA.

Due to the small input P1dB characteristic of LNA, the received high-power signal decease LNA gain and increase noise figure. To prevent gain compression form high input power, the switch is added in front of the LNA to prevent transmission of high-power signal to LNA as shown in Fig 5.1 (a). Another solution for preventing gain decease from high-power input signal is using mixer first



(a) (b)

Fig. 5.1. Block diagram of (a) conventional receiver and (b) receiver using bypass LNA.

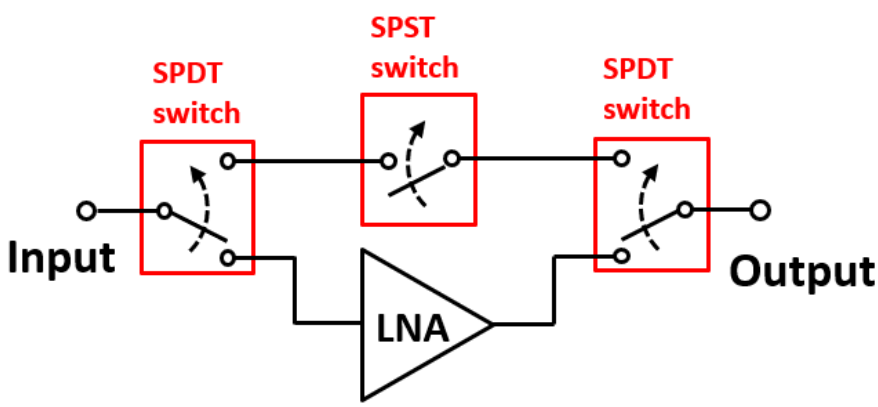


Fig. 5.2. Block diagram of conventional bypass LNA.

receiver topology. In mixer first topology, the received signal from antenna is transferred to mixer directly. Since the noise figure of the mixer is higher than LNA, the mixer first receiver needs enough received power from an antenna.

Another solution to increase input P1dB characteristic of LNA is the bypass LNA topology. The bypass LNA is a reconfigurable circuit which operates as LNA or transmission line. Fig 5.1 (b) shows the block diagram of receiver using bypass LNA. In this receiver topology, the bypass LNA operates as a switch when the power

of the receiver signal is enough to operate mixer. On the other hand, in case of small received power, the bypass LNA operates as an LNA and amplify the signal. The conventional bypass LNA is designed by using switches. Fig 5.2 shows the block diagram of conventional bypass LNA. The bypass LNA for mobile application use multiple switches to obtain enough isolation characteristic between LNA and transmission path. But over the *Ku*-band frequency, switch loss increases the noise figure of receiver.

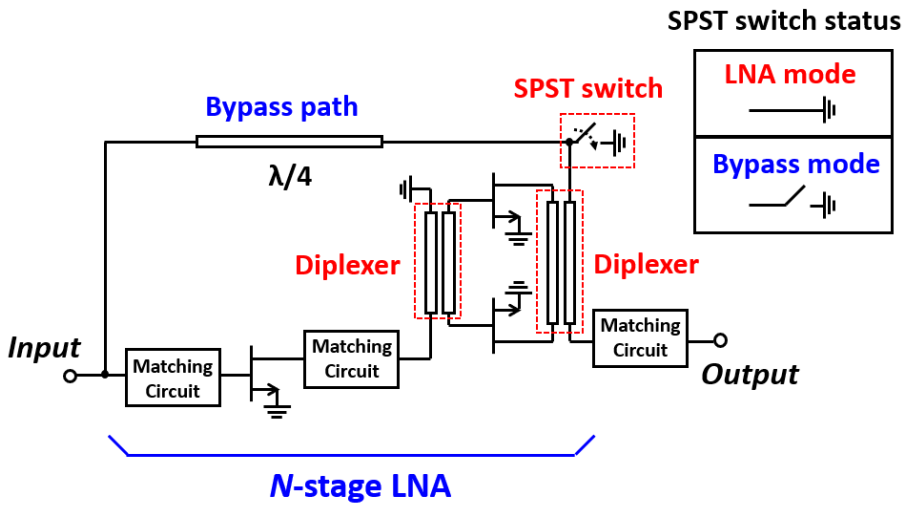
In this chapter, the bypass LNA using coupled-line structure is proposed. The proposed bypass LNA use coupled-line structure and shunt single pole single throw (SPST) switch at output-stage matching network. Since the proposed bypass LNA use one parallel SPST, the bypass path has small transmission loss. The proposed bypass LNA is designed by using commercial 0.1-μm GaAs pHEMT process.

5.2. Design of the Bypass Low Noise Amplifier

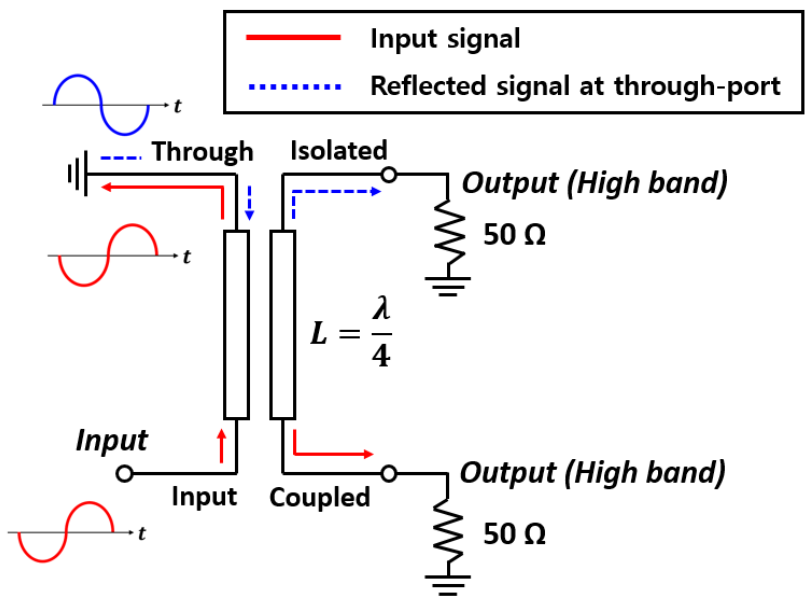
In bypass LNA, the switch loss increases transmission loss of bypass path and this loss increase noise figure. Therefore, it is necessary reduce number of the switch cell in bypass path for obtain small transmission loss at bypass path. But the switches at bypass LNA is needed for enough isolation characteristic between LNA and bypass path.

Fig 5.3 (a) shows the simple schematic of proposed bypass LNA. The proposed bypass LNA consists of 2-stage LNA, quarter-wavelength transmission-line, and one SPST switch. In LNA mode, the shunt SPST operates as short circuit. In this case, the bypass path is quarter-wavelength line with short termination, and this operates as open circuit. Therefore, the input signal is transferred to the multi-stage LNA. The last stage of the LNA use two transistors and these transistors are combined by proposed coupled-line-based diplexer structure. In the proposed coupled-line diplexer, the high-band signals are divided and transferred to coupled- and isolated-port of the coupled-line as shown in 5.3 (b). Previously analyzed in chapter 2, the proposed diplexer structure can be implemented at inter-stage matching network with shorter than quarter-wavelength coupled-line. At the output-stage of the proposed LNA, the output signals are combined by using proposed coupled-line diplexer.

In bypass mode, the SPST operates as an open circuit. In this case, the input signal is transferred to output port, directly. In this condition, the through-port impedance of output coupled-line is open circuit. Therefore, the reflected signal at the through-port of the coupled-line has same phase with input signal. So, the diplexer has high isolation characteristic between LNA and bypass path.



(a)



(b)

Fig. 5.3. Proposed bypass LNA (a) schematic and (b) coupled-line diplexer operation.

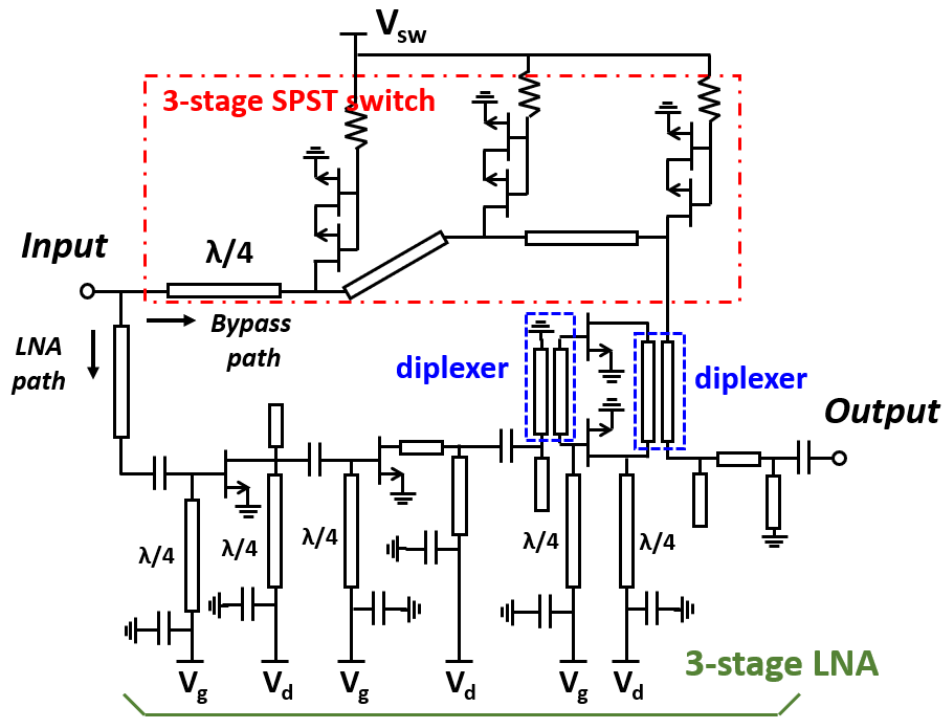


Fig. 5.4. Detailed schematic of designed *W*-band bypass LNA.

The LNA is designed to operate at *W*-band frequency. The target small signal gain is 15 dB at LNA mode, and the target transmission loss is under 5 dB at bypass mode. Fig 5.4 shows the detailed schematic of proposed bypass LNA. The multi-stage LNA is designed by 3-stage common-source topology using 2x25-μm sized transistors to obtain enough small signal gain at *W*-band frequency. The SPST switch is designed by using 3-stage shunt topology. Fig 5.5 shows the layout of designed *W*-band bypass LNA. The size of designed LNA is 1.5x1.5 mm^2 including dc and RF probing pads.

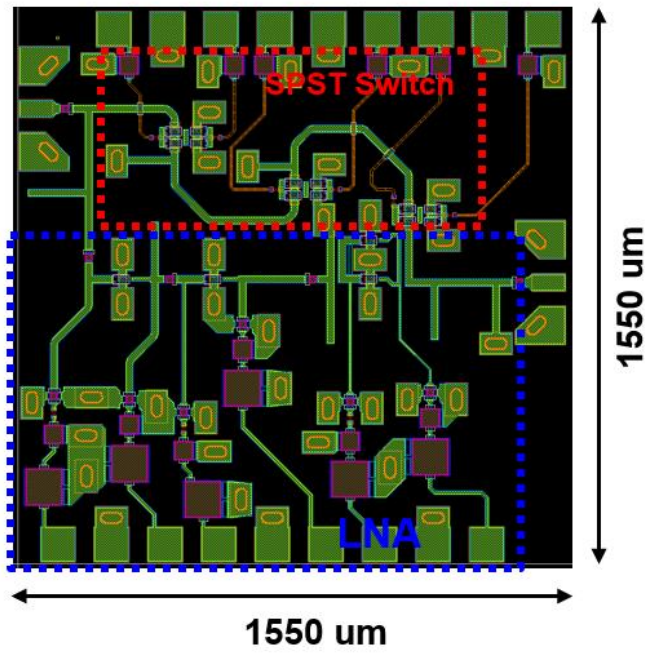


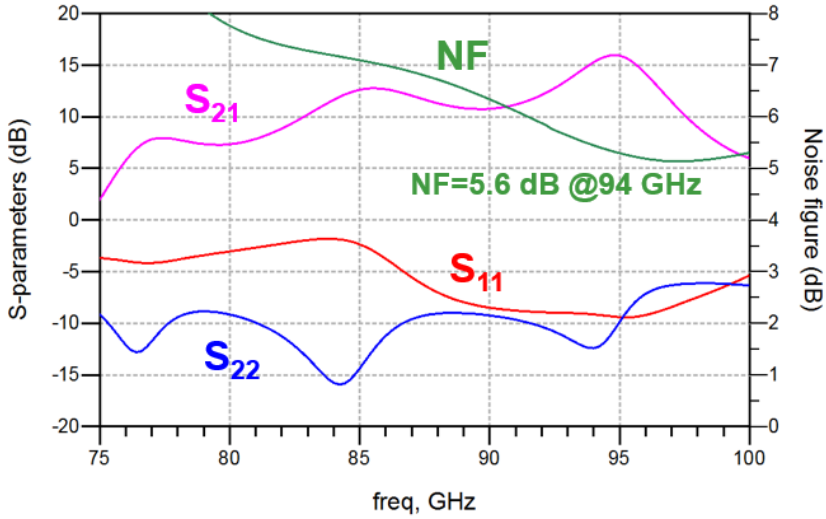
Fig. 5.5. Layout of designed *W*-band bypass LNA.

5.3. Simulation Results

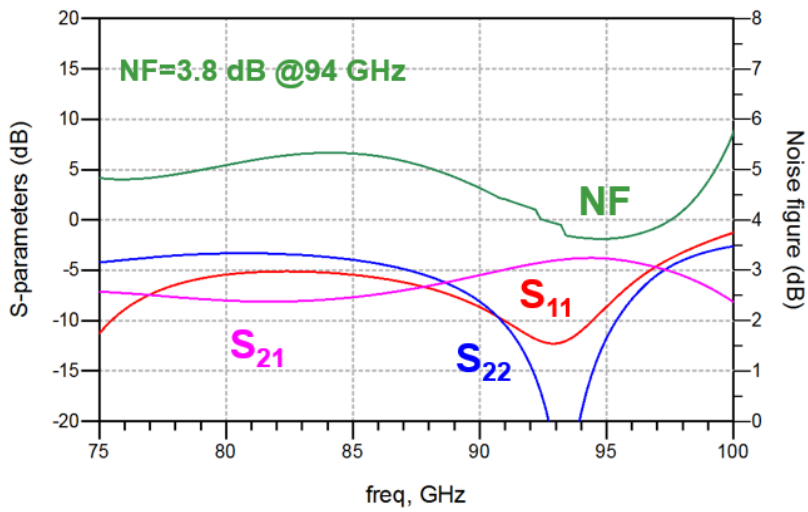
The designed bypass LNA is simulated by using circuit simulator (Keysight Advance Design Simulator, ADS). The circuit simulation conducted by using EM simulation results to consider the layout effect and increase simulation accuracy.

Fig 5.6 shows the simulation results of S-parameters and noise figure. In LNA mode, the simulation results showed over 15 dB small signal gain at 94 GHz and 5.6 dB noise figure. In bypass mode, simulation results showed 3.8 dB of transmission loss and noise figure. In both operating modes, the input and output return loss are less than 5 dB. The gain fluctuation in operation band at LNA mode is comes from quarter-wavelength line at bypass path. The quarter-wavelength of bypass line with short termination operates as open circuit but this open characteristic can be obtained at narrowband frequency range and this effect make gain fluctuation. ‘

Fig 5.7 shows the input P_{1dB} simulation results. In LNA mode, the simulate input P_{1dB} is -10 dBm at 94 GHz. The input P_{1dB} characteristic is increased since last stage of the LNA consists of two transistors. In bypass mode, simulation results showed 17 dBm of input P_{1dB} characteristic.



(a)



(b)

Fig. 5.6. Simulation results of designed bypass LNA (a) at LNA mode and (b) at bypass mode.

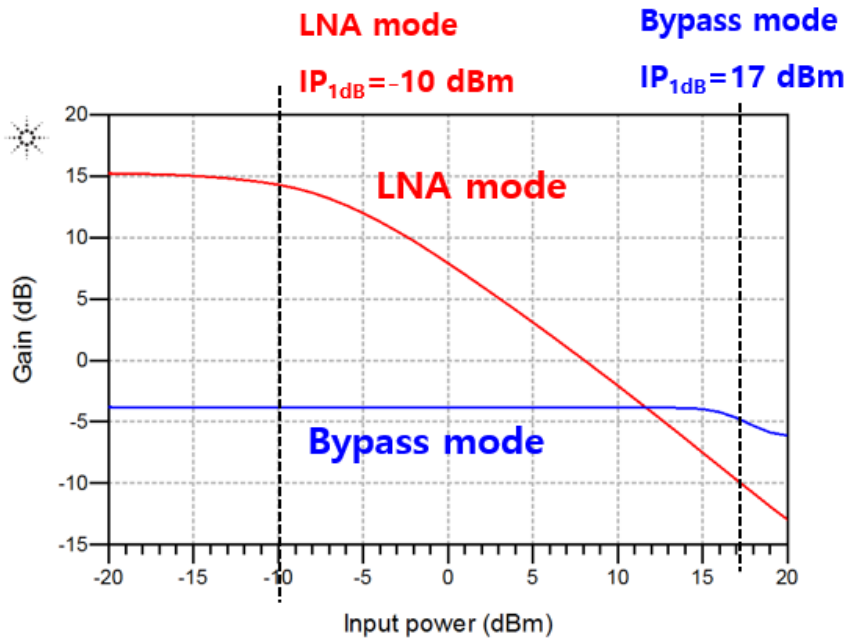


Fig. 5.7. Simulation results of input P_{1dB} at 94 GHz.

5.4. Conclusion

In this chapter, the bypass LNA using coupled-line structure is proposed. The proposed bypass LNA use proposed coupled-line-based diplexer structure at the last stage of the multi-stage LNA. The last stage of the proposed LNA consists of two transistors which combined by coupled-line diplexer. The proposed bypass LNA can be simply designed and showed small bypass path loss since the bypass path implemented with one SPST switch. The simulation is performed by using circuit simulator. The simulation results showed over 15 dB small signal gain and 5.6 dB noise figure at 94 GHz in LNA mode. In bypass mode, the simulation results showed 3.8 dB transmission loss and noise figure at 94 GHz. The input P1dB simulation results showed -10 dBm and 17 dBm characteristic at LNA mode and bypass mode, respectively.

Chapter 6

Conclusions

In this thesis, the switchless reconfigurable amplifier is proposed. To switchless reconfigurable operation, the coupled-line-based diplexer structure is also proposed and adopted in inter-stage and output-stage matching networks of power amplifier. The operation principle of proposed diplexer is analyzed by using conventional coupled-line theory. The proposed reconfigurable PA topology has advantages in high gain, output power, and PAE characteristic. But proposed PA cannot operate when both low-band and high-band PAs are turned-on simultaneously. To apply proposed coupled-line-based diplexer with other circuit, the new bypass LNA topology is also proposed. This thesis demonstrates that the new concept of reconfigurable PA can be a promising design method for high-gain and PAE PAs.

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초록

본 학위 논문에서는 광대역 전력증폭기를 위한 결합선로 구조를 이용한 비 스위치형 가변증폭기에 대한 연구를 제시하였다.

먼저 기존 광대역 전력증폭기 구조인 공액 정합 증폭기 및 분산증폭기 구조보다 높은 전력 부가 효율(power added efficiency) 특성을 얻기 위해 가변증폭기 구조를 이용한 광대역 전력증폭기를 제안하였다. 제안한 가변증폭기는 전체 주파수 대역을 크게 2 개의 주파수 대역으로 나누어 동작하는 구조이다. 가변증폭기의 동작 주파수는 스위치로 인한 손실을 제거하기 위해 각 증폭기에 사용된 트랜지스터의 입력 전압 변경을 통해 스위치 없이 동작 주파수 선택이 가능하도록 설계하였다. 이러한 비 스위치형 가변증폭기를 위해 결합선로 구조를 이용한 다이플렉서 구조를 제안하고 이를 적용하여 정합 회로를 설계하였다.

제안한 결합선로 구조를 이용한 다이플렉서는 일반적인 다이플렉서와는 달리 낮은 주파수 대역 신호는 하나의 출력 단으로, 높은 주파수 대역 신호는 두 개의 출력 단으로 나누어 출력하게 된다. 이 때 높은 주파수 대역 출력 신호는 서로 동일한 출력 전력과 180° 의 위상 차이를 가지게 된다. 제안한 다이플렉서는 $\lambda/4$ 길이의 결합선로 구조를 이용하였으며, 2 단 전력증폭기의 중간 단 정합회로에 적용할 경우 $\lambda/4$ 보다 짧은 길이로 구현이 가능하다. 제안한 다이플렉서의 동작 분석을 위해 일반적인 50 Ω 단락 임피던스에서의 분석을 먼저 진행한 뒤 중간 단 정합회로와 같은 커패시턴스를 가지는 단락 임피던스에서의 동작을 분석하였다.

제안한 다이플렉서를 이용한 가변증폭기는 6-18 GHz 주파수 대역에서의 동작을 목표로 설계를 진행하였다. 높은 출력전력 특성을 얻기 위해 Win semiconductor 사의 0.25-μm GaN (Gallium Nitride) 공정을 이용하여 설계 및 제작을 진행하였다. 가변증폭기의 입력 단 정합회는 일반적인 이중 공진 구조로 설계되었으며, 중간 및 출력 단 정합회로는 제안한 다이플렉서 구조를 이용하여 설계되었다. 각각의 전력증폭기를 구성하는 트랜지스터의 입력 전압에 따른 정합 회로의 전달 특성 분석을 통해 동작 주파수 선택을 위한 최적의 트랜지스터 입력 전압을 분석하였다. 제작된 가변증폭기의 측정결과 낮은 주파수 대역 동작 시 5-11 GHz 대역에서, 높은 주파수 대역 동작 시 9-18 GHz 대역에서 15 dB 이상의 소신호 이득을 확인하였다. 가변증폭기의 평균 출력전력 및 전력 부가 효율 측정결과 낮은 주파수 대역 동작 시 35 dBm 의 평균 출력전력과 23% 의 평균 전력 부가 효율을 확인하였으며, 높은 주파수 대역 동작 시 37 dBm 및 26% 의 특성을 확인하였다.

두 번째로는 제안한 다이플렉서 구조를 이용한 바이패스(bypass) 저잡음증폭기를 제안하였다. 제안된 바이패스 저잡음증폭기는 여러 개의 스위치를 이용하는 대신 제안한 다이플랙서 구조와 하나의 병렬 스위치를 이용하는 구조이다. 이를 위해 다단 저잡음증폭기의 마지막 단에 제안한 다이플렉서 구조를 적용하였으며, 다이플렉서에 연결된 병렬 스위치를 통해 바이패스 모드와 일반 저잡음증폭기 모드를 선택 가능하도록 하였다. 제안한 바이패스 저잡음 증폭기는 W-대역 (75-110 GHz) 주파수에서의 동작을 목표로 Win semiconductor 사의 0.1-μm GaAs 공정을 이용하여 설계를 진행하였다. 설계 결과 바이패스 동작 시 94 GHz 주파수에서 3.8 dB 의 전송손실을 확인하였으며, 저잡음증폭기 동작

시 94 GHz 주파수에서 15 dB 의 소신호 이득 및 5.6 dB 의 잡음지수를 확인하였다.

Keyword: 가변 증폭기, 고출력 증폭기, 광대역 증폭기, 마이크로파 집적회로, 저잡음 증폭기

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