creative commons
COMMONS DEED

저작자표시-비영리-변경금지 2.0 대한민국

이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:

저작자표시. 귀하는 원저작자를 표시하여야 합니다.

비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.

변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 이용허락규약(Legal Code)을 이해하기 쉽게 요약한 것입니다.

Disclaimer

dCollection

M.S. THESIS

Analysis of Stress and Recovery Characteristics of OFF-State Stress in 3 nm-node NPFET

3 nm 노드 나노플레이트 소자에서의 OFF-State Stress에 의한 열화 및 회복 특성 분석

BY

YEAJI YOO

February 2020

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

Analysis of Stress and Recovery Characteristics of OFF-State Stress in 3 nm-node NPFET

3 nm 노드 나노플레이트 소자에서의 OFF-State Stress에 의한 열화 및 회복 특성 분석

지도 교수 신 형 철

이 논문을 공학석사 학위논문으로 제출함
2020 년 2 월

서울대학교 대학원
전기정보공학부
유 예 지

유예지의 공학석사 학위논문을 인준함
2020 년 2 월

위 원 장 김 상 범 (인)

부위원장 신 형 철 (인)

위 원 강 명 곤 (인)

Abstract

OFF-State Stress had not been received much attention in the past. Hot carrier stress(HCS) or bias temperature instability(BTI) were main reliability issues. However, as the devices have been scaled down, there occurred some problems such as DIBL and off leakage current due to extremely thin oxide or short channel length. Correspondingly, gate-all-around field-effect transistors(GAA FETs) have been suggested for sub-7 nm technology node candidates due to strong gate controllability and operation characteristics. This advantage of good gate controllability of GAA FETs, however, has caused a strong horizontal electric field. It can consequently cause off state leakage more severely. In this study, the mechanism and degradation / recovery characteristics of OFF-state stress(OSS) in 3-nm NPFET had been investigated. The degradation is mainly from interface trap(N_{it}) generation which is due to hot hole injection-induced Si-O bond dissociation and hole trapped charges in HfO_2 defect band, consequently causing negative threshold voltage(V_T) shift, deterioration of subthreshold swing(SS) and off current(I_{OFF}) not to mention g_m. Comparison in three types of technology node had been

carried out using technology computer-aided design(TCAD). The degradation is the worst in 3 nm-node NPFET than other node transistors, and it can bring out degradation in input/output (I/O) circuits like complementary metal-oxide-semiconductor(CMOS) inverter as well as high power(HP) devices. Analysis in various stress bias and temperature dependency and recovery characteristics also had been carried out at different drain recovery conditions

Keyword: Nanoplate FET(NPFET), OFF-State Stress (OSS), Reliability, Technology Computer-Aided Design(TCAD), Hot hole injection(HHI), Interface traps, Oxide degradation

Student number: 2018-24881

CONTENTS

Abstract ――――――――――――――――――――――――i

Contents ―――――――――――――――――――――――― iii

1. Introduction ――――――――――――――――――――――1

2. Mechanism of OSS in NPFET――――――――――――――3

2 1 Introduction ――――――――――――――――――――3

2. 2 Hot hole injection－induced interface trap generation －5

2. 3 Hole trapping in HfO_2 defect band ―――――――― 7

2. 4 Conclusion ――――――――――――――――――――8

3. Device and Methodology ――――――――――――――――9

3. 1 Device structure ――――――――――――――――――9

3. 2 Simulation condition ―――――――――――――― 10

4. OSS Degradation characteristics in NPFET――――― 14

4. 1 Overall degradation characteristics in NPFET――――14

4. 2 Gate oxide thickness in same EOT condition――――16

4. 3 Comparison of various nodes of MOSFETs ―――――17

4. 4 Conclusion ――――――――――――――――――――19

5. Dependence on OSS degradation of temperature and stress bias condition ――――――――――――――――――22

5. 1 Bias dependency of OSS degradation――――――― 22

5. 2 Temperature dependency of OSS degradation――― 23

5. 3 Conclusion ―――――――――――――――――― 26

6. Recovery characteristics ―――――――――――――28

6. 1 Introduction ――――――――――――――――――28

6. 2 Method ――――――――――――――――――――29

6. 3 Results and discussion ――――――――――――29

6. 4 Conclusion ――――――――――――――――――32

7. Conclusion ――――――――――――――――――――33

References ――――――――――――――――――――36

Abstract in Korean ――――――――――――――――39

1. Introduction

Reliability issues usually have been a limitation for scaling into ultra-scaled nano devices. Although semiconductor devices have been aggressively scaled toward Moore's law standard, there occurred some problems such as drain induced barrier lowering(DIBL) and off leakage current due to extremely thin oxide or short channel length. Correspondingly, gate-all-around field-effect transistors (GAA FETs) have been suggested for sub-7 nm technology node candidates due to strong gate controllability and fine operation characteristics. This advantage of good gate controllability of GAA FETs, however, has caused a strong horizontal electric field. It can consequently bring about field-induced degradation such as hot carrier stress(HCS), bias temperature instability(BTI) or off-state stress(OSS). Although the first two cases of degradation in nanoplate FETs(NPFETs) have been actively studied, still there is not enough investigation of the overall deterioration characteristics of OSS not to mention degradation mechanism in GAA devices. However, it is necessary to investigate OSS in sub 5 nm technology node because higher carrier energy without scattering due to ballistic transportation in such small devices can cause severe off state

degradation than in case of larger devices. In this study, stress and recovery characteristics of OSS like trap distribution change over stress and relaxation time had been investigated as well as I_d-V_g properties like threshold voltage (V_T) shift or subthreshold swing(SS) degradation of the device.

First, mechanism of OSS and OSS recovery in NPFET is suggested in this paper. Then, implementation methods in 3-D TCAD are described. Calibration of the OSS simulation results such as V_T shift, SS, g_m and I_{OFF} versus time in 65 nm-node FET were carried out to the reference experimental data[1]. 3 nm-node NPFET structure for the stress simulation and simulation parameters are also suggested. Before implementing it into NPFET, ballistic transport was also considered using Monte Carlo(MC) simulation. I_{dsat} and I_{dlin} of Drift-Diffusion(DD) model simulation were finely calibrated to those of MC. After these two calibration steps mentioned above, OSS simulation were performed with NPFET and degradation characteristics were analyzed at several stress conditions. At the last, recovery properties such as V_T or SS in various recovery bias are also described.

2. Mechanism of OSS in NPFET

2. 1 Introduction

The OFF-State Stress is known for having different degradation characteristics other than HCS and BTI-induced degradation. First of all, OSS is the degradation when occurs at the OFF condition(i.e., V_g = 0 V and $V_d = V_{STRESS}$) like the illustration of OSS state in inverter circuit like Fig 1. (a). In this state, there occurs strong electric field near the gate-drain overlap region, both vertically and laterally. As in Fig. 2, due to the impacts of both high fields, impact ionization appears and hot hole and

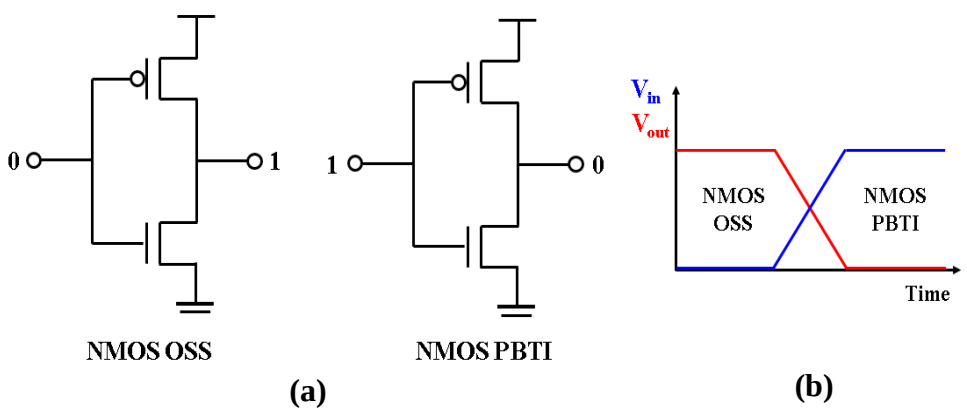


Figure 1. (a) Illustration of OSS and OSS recovery(PBTI) states in inverter circuit. (b) Schematic of two phases.

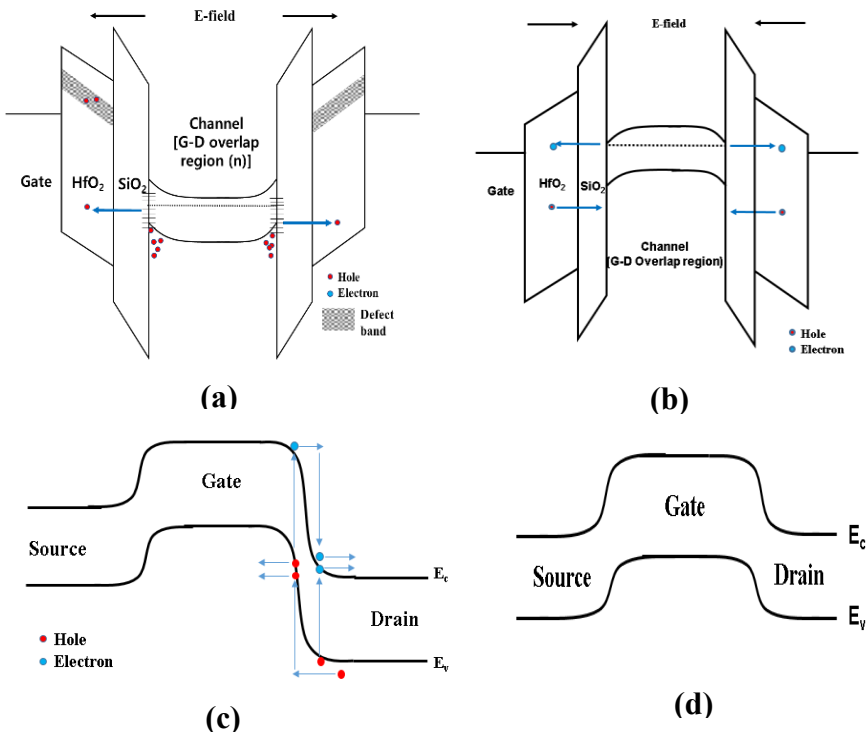


Figure 2. (a) Energy band diagram of 3-nm NPFET in Z-Z' direction at OSS condition. (b) Energy band diagram of 3-nm NPFET in Z-Z' direction at PBTI condition. (c) Impact ionization due to lateral electric field near the gate-drain overlap region. (d) lateral energy band diagram

electrons are generated. Along the vertical field direction, hot holes are accumulated to Si-SiO_2 interface, causing several degradation in gate oxides. On the contrary, at positive bias temperature instability(PBTI) condition as a recovery of OSS, trapped holes get out from HfO_2 defect band promtly, while electrons accumulating and trapping at the defects.

Concrete recovery characteristics will be mentioned again in last chapter.

In this work, overall mechanism of OSS was suggested in terms of hot hole injection(HHI)-induced interface traps generation and hole trapped charges at HfO_2 bulk using related equations.

2. 2 Hot hole injection-induced interface trap generation

It is well known that interface trap generation properties are different according to the stress bias because reacting carrier type varies for bias range[2]. For example, with high gate bias state, mainly hot electrons are activated for interface trap generation. In contrast, with low gate bias, hot holes are responsible for interface trap generation, breaking Si-O bond. These interface traps which are originated from Si-O bond depassivation are known for lack of recovery at the relaxation phase unlike Si-H bond dissociation-induced interface trap[3]. In addition, time exponent(n) for ΔN_{it} has higher value(0.72-0.88) than that of Si-H induced traps(0.25-0.5) due to hot holes induce Si-O bond catalyzing and activation energy lowering [4]. Thus, because hot holes are generated and accumulated to the $Si-SiO_2$ interface at

the OSS condition, HHI induced un-recoverable interface traps are generated. The traps in TCAD simulation can be described mainly by two models. The first is single particle(SP) process which is related to the hot carrier density, and the field-enhanced thermal degradation(FETD) process which is related to the hot hole induced Si-O bond catalyzing effect. In this research, multi particle(MP) process which occurs at lower electric field condition were hardly considered because the degradation mainly occurs at the position where the high field exists. Interface trap concentration along the time and collision frequency(k) which is related to the interface trap generation is described as formula below. Parameter a is an activation energy lowering factor determined from the surface state, which is set to be 7.85eÅ[4].

$$\mathrm{N}_{it}(\mathrm{t}, E_{SP}) = P_{SP} N_0 \left[1 - \mathrm{e}^{-\mathrm{k}(E_{SP})t}\right] \quad (1)$$

$$\mathrm{N}_{it}(\mathrm{t}, E_{TH}) = P_{TH} N_0 \left[1 - \mathrm{e}^{-\mathrm{k}(E_{TH})t}\right] \quad (2)$$

$$\mathrm{k}(E_{TH}) \geq \nu_0 \exp\left[-\frac{\frac{\Delta E_{TH0}}{2} - a \cdot E_{ox}}{k_B T}\right] \quad (3)$$

2. 3 Hole trapping in HfO_2 defect band

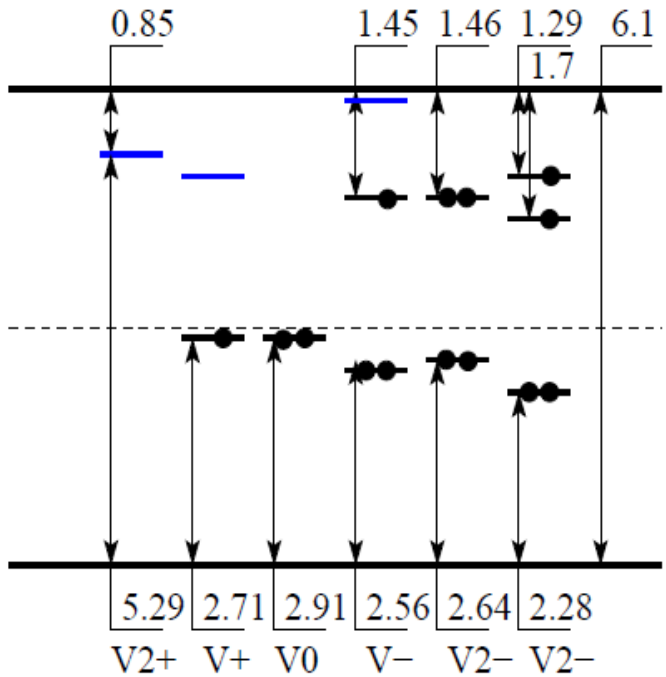


Figure 3. Defect energy diagram for oxygen vacancy in the HfO_2[5]

Along the direction of vertical electric field, holes are headed to the gate oxide. Due to the existence of defect band mostly in HfO_2, majority of holes are trapped to the defect band of HfO_2 than of SiO_2 bulk. Corresponding defect energy level is described in Fig. 3[5]. Consequently, trapped holes cause negative V_T shift, OFF current increase and oxide degradation resulting in SS and g_m deterioration. Trap degradation(TD) model which is field dependent model was used to describe hole trapping mechanism and the formula are below. ν means reaction constant which is related to hole trapping

frequency. k_{FN}, k_{HC} and k_{SHE} are the fitting parameters related to Fowler-Nordheim(FN) tunneling, hot carrier injection and the SHE distribution enhancement factor, respectively.

$$\nu = \nu_0 \exp\left(\frac{\varepsilon_A}{kT} - \frac{\varepsilon_A + \Delta\varepsilon_A}{\varepsilon_T}\right) k_{FN} k_{HC} k_{SHE} \quad (4)$$

$$N_{bond} = \frac{N_{bond}^0}{1 + (\nu t)^\alpha} \quad (5)$$

2. 4 Conclusion

In this chapter, overall mechanism of OSS was described mainly in two ways, one is HHI-induced Si-O bond depassivation and interface trap generation and another is HfO_2 defect band hole trapping. As impacts of both HHI-induced interface trap generation and hole trapped charge in HfO_2 bulk, nano devices can suffer from severe change of properties such as negative V_T shift, I_{OFF} increase, SS and g_m degradation. Thus, analysis and investigation of the phenomenon is of importance for predicting and optimization of device characteristics. Next chapter, 3 nm-node NPFET and simulation methodology are suggested.

3. Device and Methodology

3. 1 Device structure

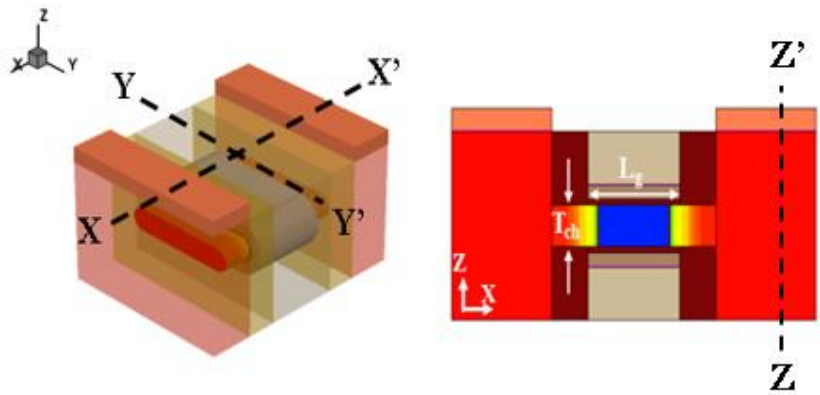


Figure 4. 3 nm-node NPFET structure

Fig. 4 shows the 3-D structure of 3 nm-node NPFET. Design specifications were determined according to international technology roadmap for semiconductor (ITRS) 2015[6]. Gate length(L_g) was set to be 10 nm. Channel width(T_w) and channel thickness(T_{ch}) is 16 nm and 5 nm, respectively. Contact gate pitch(CGP) which is distance from middle of the source to that of the drain was set to be 23.5 nm. Effective oxide thickness(EOT) was set to be 0.68 nm (T_{ox} = 0.43 nm, T_{hk} = 1.4 nm), ensuring the gate controllability and inversion layer thickness. Doping at source and drain were set to be 10^{16} cm^{-3} of phosphorus and at channel to be 10^{21} cm^{-3} of

boron. Contact resistance was set to be $3x10^{-9}$ Ω/cm^2 considering latest process technology. V_T was controlled by gate work function in TCAD simulation, value with I_{OFF} = 100 nA/μm.

3. 2 Simulation condition

For implementation of OSS degradation in 3 nm-node NPFETs in Synopsys TCAD, a 3-D hydrodynamic simulation was performed. Fig. 5 shows the calibration and implementation flow of OSS degradation. Hot hole-induced hot carrier stress degradation (hHCSDegradation) model mentioned above was used to N_{it} generation mechanism. This model uses spherical

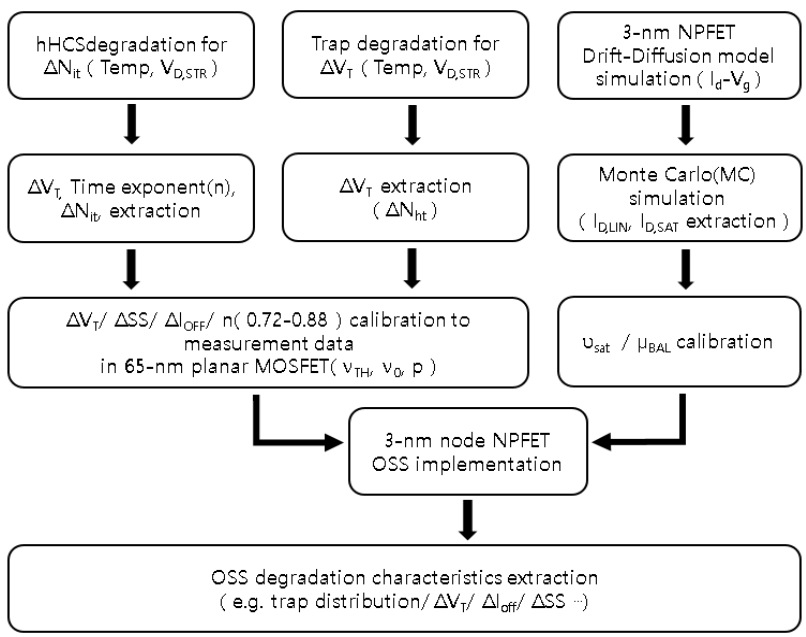


Figure 5. Flow chart of OSS calibration and simulation in 3 nm-node NPFET

Device Parameters	Value	Interface traps parameters	Value
Supply voltage, V_{dd} (V)	0.75	$N_{it,TH}(t, E_{TH}) = P_{TH}N_0\,[1- e^{-k_{TH}(E_{TH})t}]$ (1) $N_{it,SP}(t, E_{SP}) = P_{SP}N_0\,[1- e^{-k_{SP}(E_{SP})t}]$ (2) $k_{TH}(E_{TH}) = \nu_{TH}\exp(-E_{TH}/kT)$ $E_{TH} = E_{TH0} - pE_{ox}$ * p : dipole moment	
Gate length, L_g (nm)	10		
Channel width, T_w (nm)	16	Interface bond concentration, N_0 (cm^{-2})	$5x10^{12}$
Channel thickness, T_{ch} (nm)	5	Lattice collision frequency, ν_{TH} (s^{-1})	10
Contact gate pitch, CGP (nm)	22.5	HfO_2 bulk traps parameters	Value
Effective oxide thickness (nm)	0.7	$N_{ot} = N_{b0}(1-\frac{1}{1+(\nu t)^{(0.5+\beta)}})$ (3) $\nu = \nu_0\exp(\frac{\varepsilon_A}{kT} - \frac{\varepsilon_A+\Delta\varepsilon_A}{kT})$ $\beta = \beta_0 + \beta_{\perp}F_{\perp} + \beta_{//}F_{//}$ *β: Field coefficient	
Source/Drain doping (cm^{-3})	10^{21}		
Channel doping (cm^{-3})	10^{16}	Oxide bulk bond concentration, N_{b0} (cm^{-3})	$5x10^{20}$
Contact resistance (Ω-cm^{-2})	$3x10^{-9}$	Depassivation coefficient, ν_0 (s^{-1})	$5x10^{-8}$

Table 1. Device and simulation parameters.

harmonics expansion(SHE) method that calculates the microscopic carrier energy distribution function by solving the SHE of the Boltzmann transport equation(BTE). It is known for economic substitute for MC simulation because it takes much less time than MC[7]. However, this model describes mainly broken Si-H bond-induced interface traps generation and not enough description of Si-O bond dissociation-induced interface traps. Thus, lattice collision frequency (ν_{th}) parameter which is interface bond collision frequency that controls interface trap generation time exponent. Effective dipole moment(p) which can be changed by electric field and surface state was adjusted because time exponent(n) value and surface state

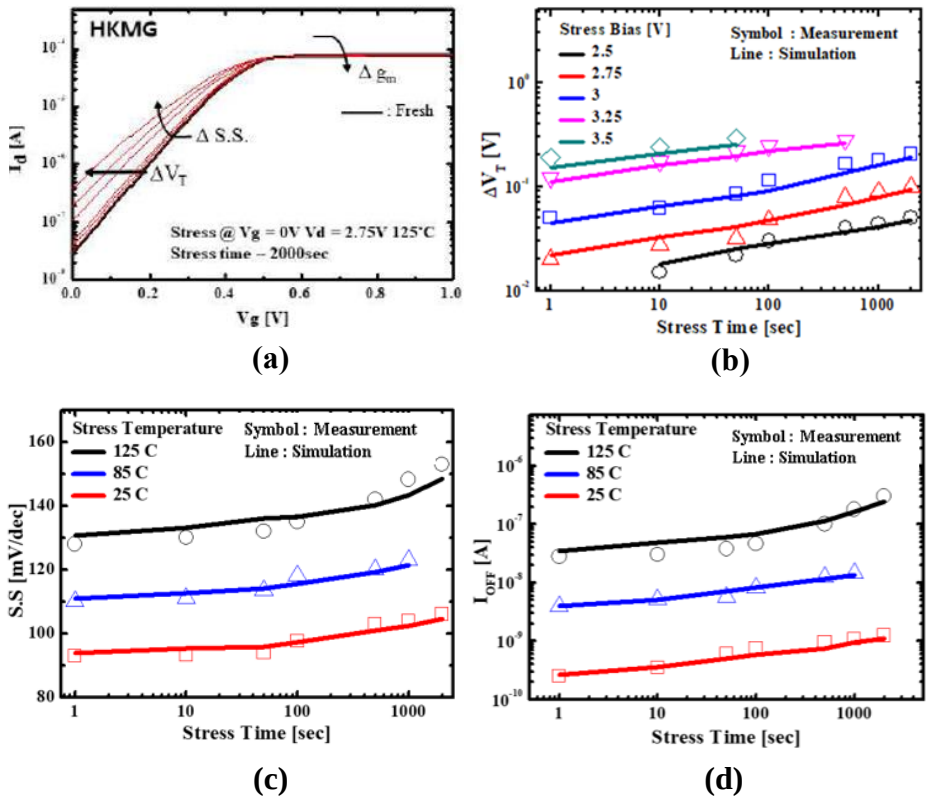


Figure 6. Calibration of OSS characteristics in 65 nm-node planar MOSFET[1]. (a) I_d-V_g curve after 2000sec stress at V_g = 0 V, V_d = 2.75 V, 125 ˚C. (b) SS at different temperature condition. (c) V_T shift at different stress bias condition. (d) I_{OFF} at different stress bias condition.

for Si-O bond dissociation-induced interface traps generation are not similar with that of Si-H bond dissociation. The value of p was set to be 7.85 eÅ according to the oxide effective field and surface state[8]. We had adjusted this value for implementation of accurate interface trap generation characteristics of OSS. In addition, trap degradation(TD) model had been applied for HfO_2 hole trapping mechanism, resulting in OSS-induced

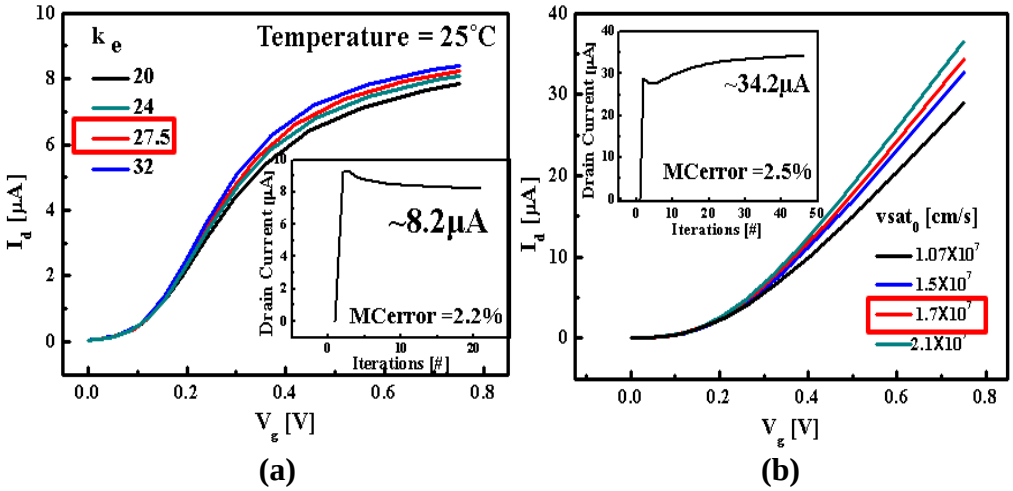


Figure 7. I_d-V_g curve calibration with MC simulation in (a) Linear region (b) Saturation region

negative V_T shift. The model is driven by an electric field and nonlocal tunneling was used to link two materials where carriers can move between. Rather than applying it directly into the NP device, first we applied it to 65 nm-node planar MOSFET and calibrated with experimental data of [1]. V_T shift, SS and I_{OFF} properties as stress time passes at different stress bias or temperature condition had been calibrated. In Fig. 6, the larger the bias and temperature, the severe degradation had occurred. The reason is that it is the phenomenon due to the high field and HHI. As stress bias get larger, the devices can get more affected by higher oxide field. Besides, carrier energy distribution function is changed at higher temperature so that holes with higher energy get increased as temperature become higher, causing more

interface trap generation and hole trapping. For 3 nm-node NPFET, MC simulation had been carried out because ballistic transport should be considered in sub-5 nm node MOSFETs. Ballistic parameters and saturation velocity(v_{sat0}) of drift-diffusion(DD) model simulation were finely calibrated with MC simulation results. In this simulation, electron saturation velocity was matched to be $1.7x10^7$ cm/s with error rate below 2.5 %, as shown in Fig .7. Parameters of structure and simulation are listed on the Table 1 with degradation model formula. After these several calibration steps, transient OSS simulation model was performed on 3 nm-node NPFET. To investigate OSS degradation characteristics in 3 nm-node NPFET, V_g = 0 V, V_d = 1.5 V bias was applied for 100 seconds in 125 ˚C condition. Study was carried out in various stress condition such as different node NPFETs, bias and temperature for degradation comparison. I_d-V_g characteristics like V_T, I_{OFF} and SS as well as interface traps and hole HfO_2 defect band trapped charges distribution versus time was also analyzed.

4. OSS Degradation characteristics in NPFET

4. 1 Overall degradation characteristics in NPFET

OSS degradation is due to the HHI-induced interface trap generation and hole trapping in HfO_2 defect band. Thus, both have influences on degradation characteristics. It is usually known that transconductance g_m shifts according to charge types like interface traps or oxide bulk traps. For example, reduction of $g_{m,max}$ means generation of interface states while lateral shift of g_m is due to the charge injection into the oxide bulk defect bands[9]. In Fig. 8 (a), as stress time passes, both lateral and vertical shifts of g_m are

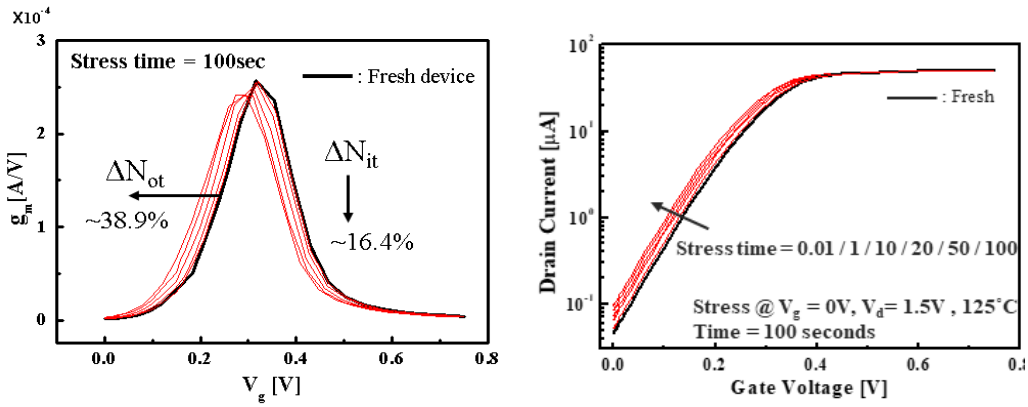


Figure 8. (a) g_m curve after 100 s stress
(b) I_d-V_g curve after 100 s stress

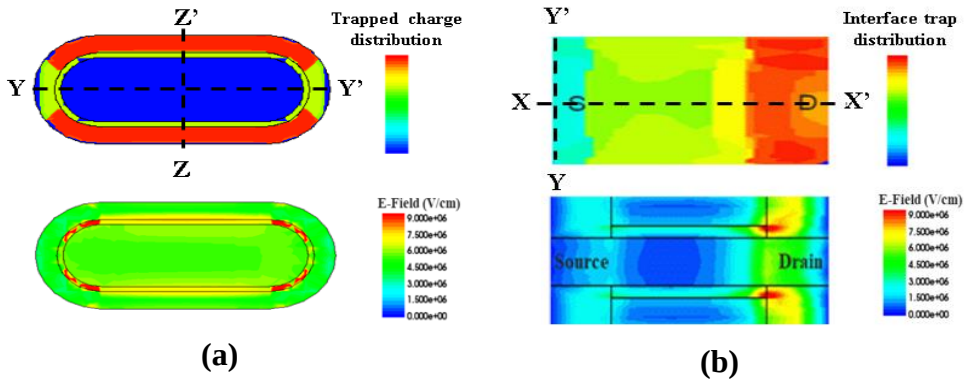


Figure 9. Charge distribution and electric field (a) Channel cross section view near gate-drain overlap region (b) Interface traps distribution of channel top view and electric field at X-Z cross sectional view

observed, presenting both interface traps generation and hole trapping in HfO_2 bulk defect band occurred as OSS time. In addition, due to the impacts of both, negative V_T shift and SS, I_{OFF} increase are observed as OSS time like in Fig. 8 (b). The degradation of the device gets more severe as stress time increases.

While, generated traps or trapped charges were obeserved to be distributed througout the channel but were most concentrated in the gate-dratin overlap region where maximum electric field occurred. Corner and top-down regions of the channel cross section were also the region where many charges existed. Corresponding electric field and charge distribution are showed in Fig. 9.

4. 2 Gate oxide thickness under same EOT condition

Investigation of gate oxide composition dependency was also carried out. Generally, the thicker high-κ layer is preferred to prevent direct tunneling caused by extremely thin oxide thickness through thickening physical thickness of gate oxide layer. However, as in Fig. 10 (a), OSS degradation

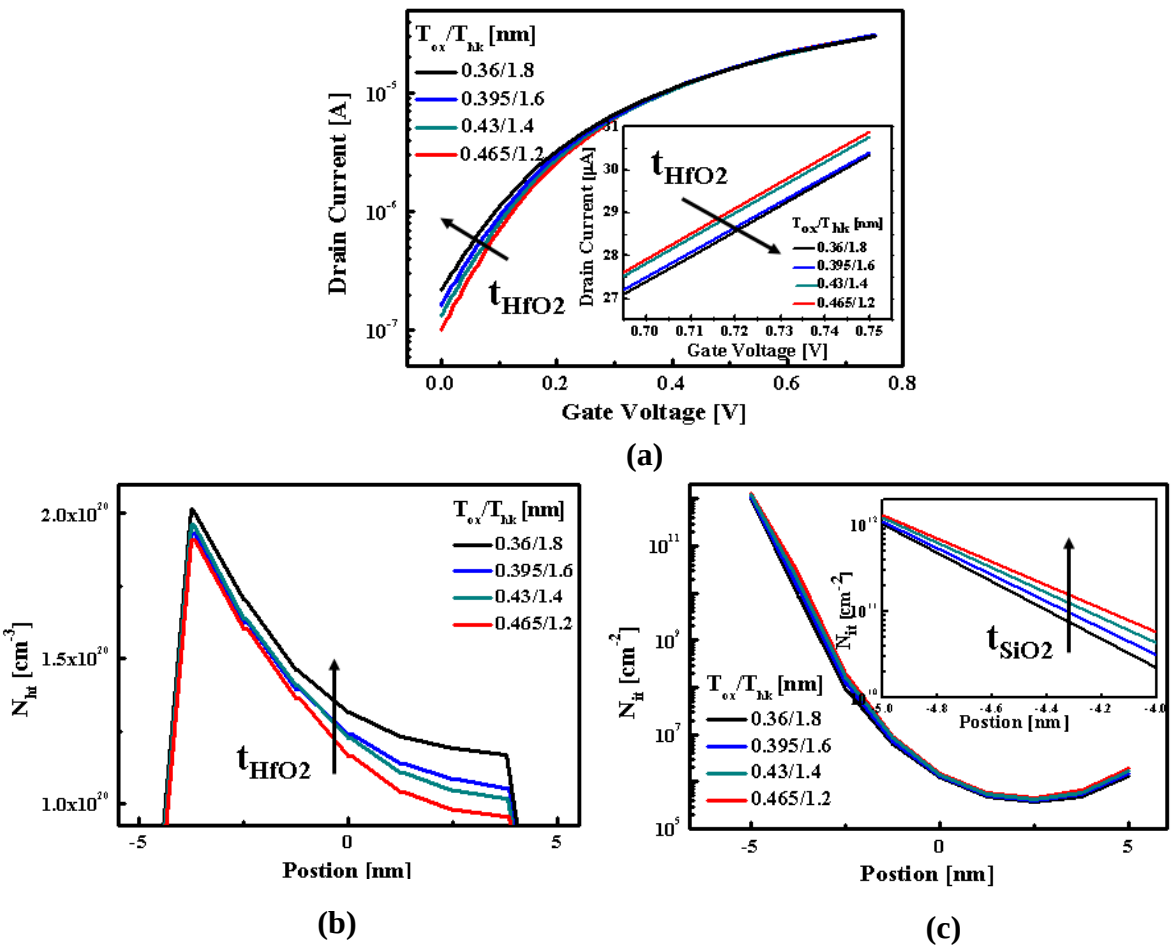


Figure 10. Degradation characteristics in different T_{ox}/T_{hk} and same EOT condition after 100 s stress (a) I_d-V_g curve
(b) Hole trapped charge (c) Interface trap distribution

were more severe in thicker HfO_2 layer condition. It is due to that hole trapping is dominant in HfO_2 so that if thickness of HfO_2 get thicker, hole trap region become larger so that more holes are trapped in defect region as in Fig. 10 (b). On the contrary, the effect of T_{SiO2} on N_{it} was negligible, showing only slight change of N_{it} as shown in Fig. 10 (c). Thus, contrary to the notion of taking large T_{hk} to prevent direct tunneling, it is better get small T_{hk} while in same EOT condition in terms of OSS.

4. 3 Comparison of various nodes of MOSFETs

Fig. 11 shows overall degradation characteristics in 65 nm-node MOSFET and 3/5/7 nm-node NPFETs versus stress time. Same overdrive voltage(V_{OV} = 1.41 V) was used in inter-node simulation and same maximum electric field condition was applied in 3 nm and 65 nm-node MOSFET.

NPFET	7	5	3
Gate length, L_g (nm)	14	10	10
Channel width, T_w (nm)	30	26	16
Channel thickness, T_{ch} (nm)	6	6	5
Contact gate pitch, CGP (nm)	42	32	23.5
T_{inv} (nm)	0.9	0.85	0.8

Table 2. Device specification of 7/5/3 nm node NPFETs

Entirely, 3 nm-node NPFET showed the most serious degradation among them. Design specification of each node FET is described in Table. 2. First of all, comparing 3 nm- node FET and HKMG 65 nm-node FET in same maximum electric field condition, more degradation occurred in 3 nm-node FET than planar one as shown in Fig. 10 Because NPFET is surrounded by gate, channel and the gate dielectrics can get affected by the stress condition and traps. Thus, effective degradation region of NPFET is larger and get suffer from OSS more severely. Comparing with 5 and 7 nm-node NPFET, with

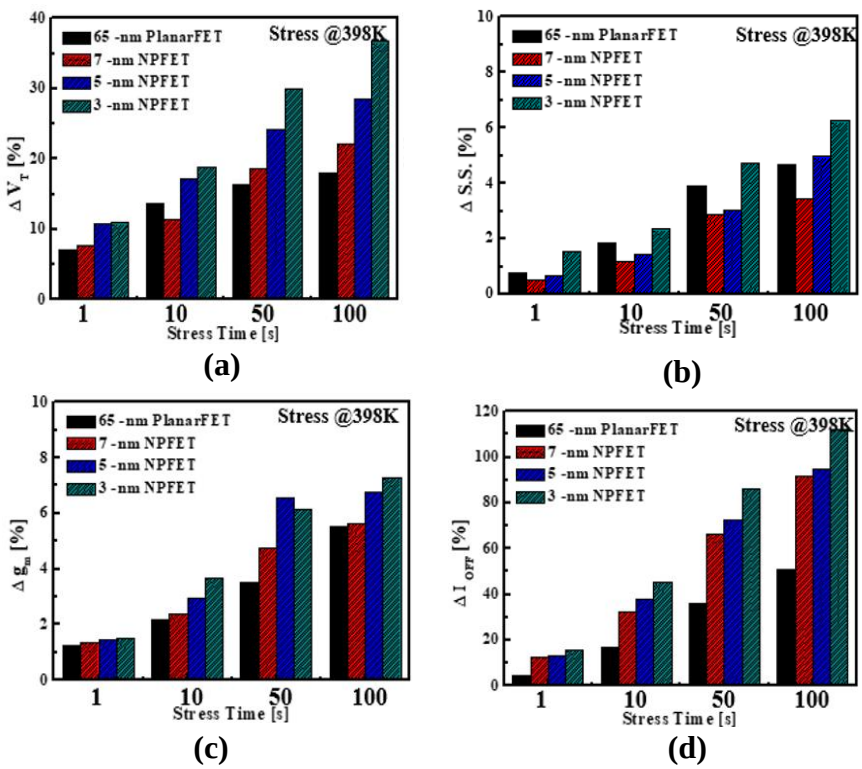


Figure 11. Degradation characteristics in 65 nm-node planar FET, 3/5/7 nm-node NPFET at 125 ˚C. (a) Δ V_T (b) Δ SS (c) Δ g_m (d) Δ I_{OFF}

same V_{OV} condition, the oxide field at the gate-drain overlap region is much higher in 3-nm node NPFET. Besides, in sub 5 nm-node FET, ballistic transport is applied in terms of carrier transport mode. Then scattering rates can get lower and consequently, the density of carriers which moves without losing energy becomes higher, causing more degradation from the HHI[10]. Thus, we confirmed that in GAAFETs, and as devices get scaled down, they suffer from OSS degradation more severely in terms of overall device properties.

4. 4 Conclusion

In this chapter, overall degradation properties of OSS were studied. First of all, due to the impacts of both HHI-induced interface trap and hole trapping in HfO_2 defect band region, several degradations occurred in the 3 nm-node NPFET. For example, negative V_T shift and off current increased and SS and g_m also showed deterioration. Besides, it showed worst degradation in 3 nm node-NPFET than other node FET when stress was applied due to structural reason. Trap and charge distribution were throughout

the region, but showed most at the gate-drain overlap region, top-down and corner of oxide region where maximum electric field exists and hot hole injection occurs. Z-Z' direction has more charge distribution as electric field across the shorter direction is higher due to the width difference between Y-Y' and Z-Z' direction. In addition, as mentioned in fig. 1, there occurs high field at gate-drain overlap region so that charge distribution is concentrated near the drain position.

5. Dependence on OSS degradation of temperature and stress bias condition

5. 1 Bias dependency of OSS degradation

Degradation characteristics at different stress bias also were studied. To examine the OSS degradation property at various drain bias, NPFET was investigated at V_g = 0 V, V_d = 1.25 / 1.5 / 1.75 V, respectively. Fig. 12 (a) shows the V_T shift over stress time. At the largest stress bias condition (V_d = 1.75 V), the device suffered more V_T shift due to additional hole trapped charge in HfO_2 at larger stress bias, as expected. In terms of interface trap generation ΔN_{it}, generated interface trap concentration was higher in large

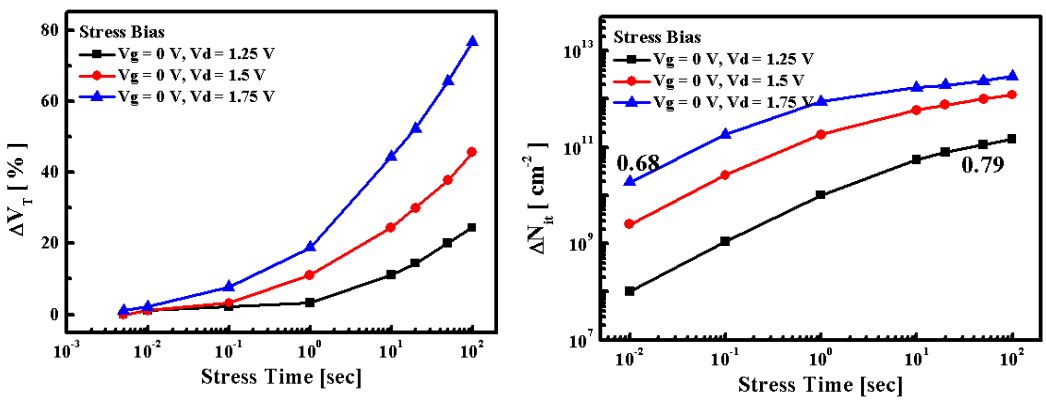


Figure 12. (a) ΔV_T by stress time at different stress bias (b) ΔN_{it} and n by stress time at different stress bias

drain stress condition. On the other hand, time exponent value n was much higher at the V_d = 1.25 V condition as in Fig. 12 (b). It is due to rapid saturation of trap generation in larger off state drain bias condition. When trap formation reaches a certain point, saturation of interface trap generation occurs. That is, trap formation occurs continuously under conditions that do not reach the saturation point, keeping high value of n

5. 2 Temperature dependency of OSS degradation

As hot carriers are involved in the OSS degradation, it can be affected by stress temperature as well. As is well known, when temperature increases, carrier energy distribution spreads, lowering distribution of lower energy

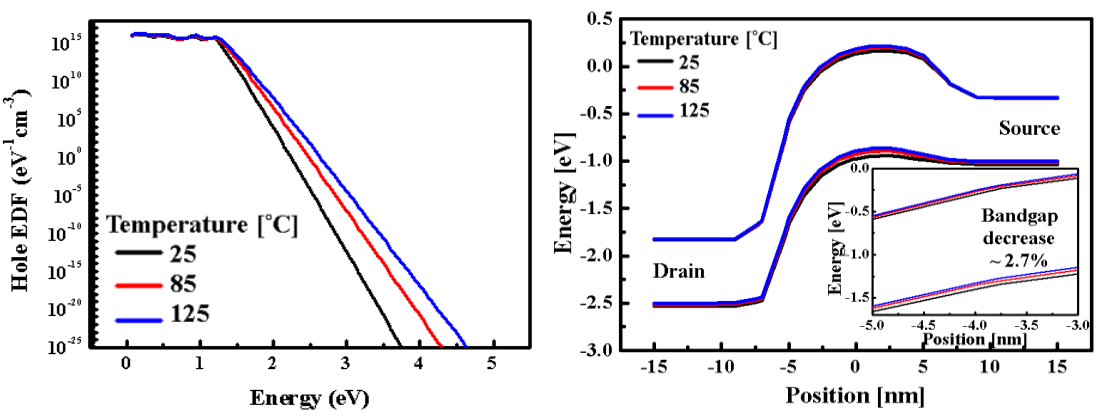


Figure 13. (a) Hole energy distribution function at different stress temperature condition (b) Energy band diagram of channel lateral direction at different temperature condition

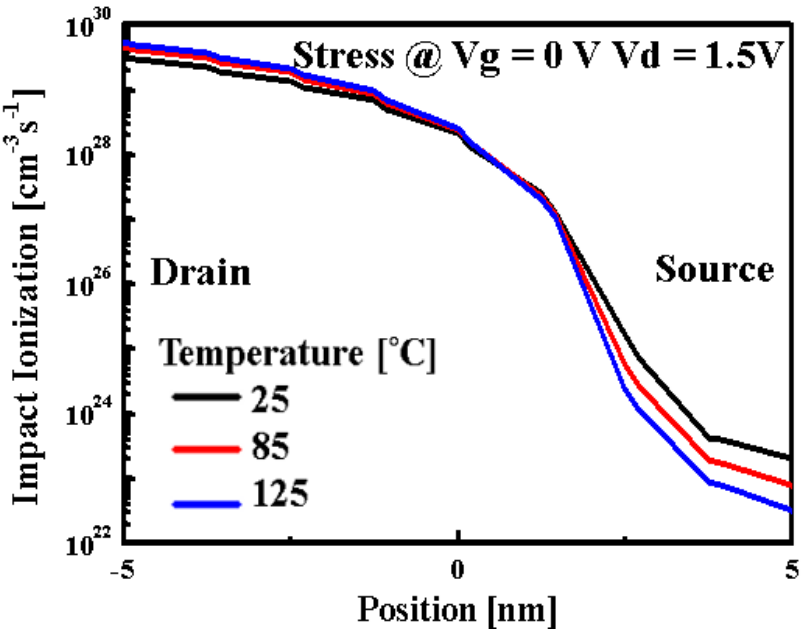
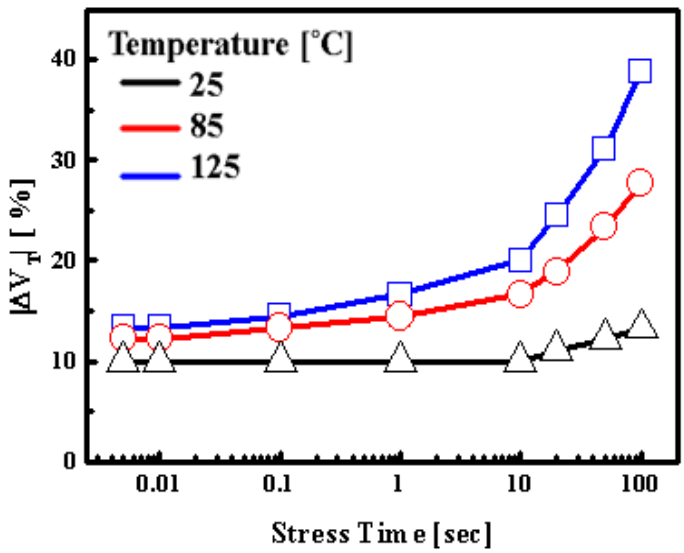
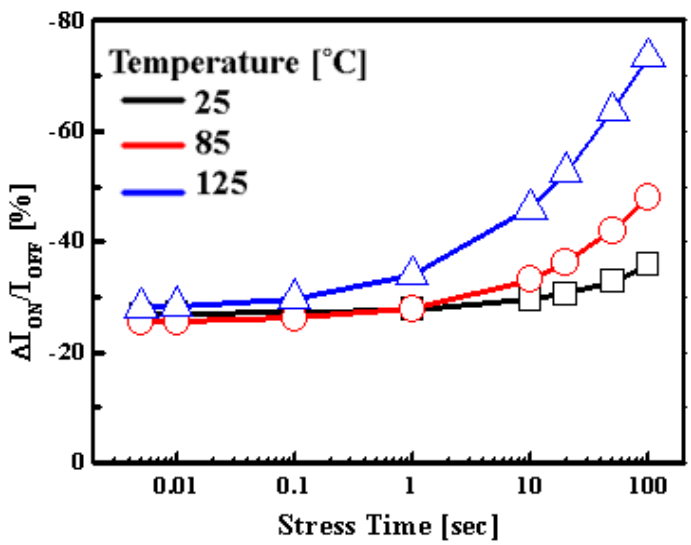


Figure 14. Impact ionization rate at different temperature condition

distribution while increasing of higher one. As expected, in Fig. 13 (a), hole energy distribution function changes as increase of temperature. At higher temperature, hole distribution of lower energy decreases and increases of higher energy, oppositely. In addition, silicon bandgap decreases about 2.7 % as device temperature gets higher as presented in Fig. 13 (b). Due to the influence of this change of the energy distribution and bandgap, impact ionization rate increases at high temperature condition as shown in Fig. 14, causing more hot hole generation and severe degradation of the device as in Fig. 15. As a result, both V_T shift and $\Delta I_{ON}/I_{OFF}$ got severe degradation in high temperature due to considerable generation of interface trap and hole trapping



(a)



(b)

Figure 15. (a) Δ|V_T| at different temperature condition
(b) ΔI_{ON}/I_{OFF} as stress time passes at different temperature

in HfO_2. In terms of interface trap and time exponent, Fig. 16 shows that total generated interface trap concentration is higher at 125 ˚C but n has larger value at lower temperature. It means that at higher temperature, initial trap

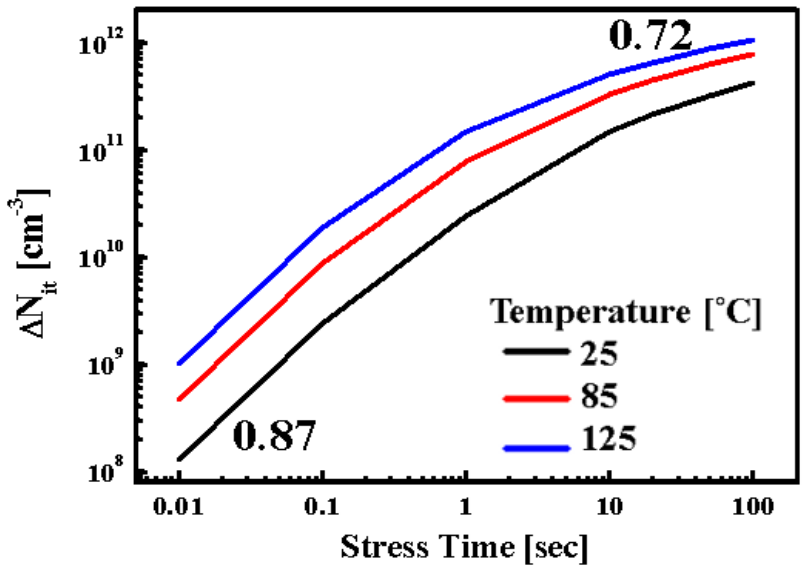


Figure 16. ΔN_{it} over time at different temperature

generation frequency was faster than at lower one because of difference in initial hot carrier density between at high/low temperature condition. Consequently, in 125 ˚C, the traps reach the saturation point earlier than in the lower temperature condition, with comparably low n value of 0.72.

5. 3 Conclusion

Dependency of OSS according to temperature condition was analyzed. As temperature become higher, hole energy distribution which affects impact ionization and interface trap generation, got spread so that energy distribution of higher one increased. Thus, overall degradation was severe in high temperature condition. On the other hand, in terms of interface

trap generation, time exponent value was higher in lower temperature although total generated interface trap concentration was much more in 125 ˚C condition. It is because at high temperature, while carriers react faster initially, reaching the saturation point early than at 25 ˚C condition. Thus, n had lower value at higher temperature condition.

6. Recovery characteristics

6. 1 Introduction

As described in the first chapter, OSS recovery is enacted in PBTI state. That is, in $V_g = V_{dd}$, $V_d = 0$ V condition. Thus, before investigate OSS recovery properties in 3 nm-node NPFETs, it is of importance to understand PBTI mechanism first.

PBTI refers to the positive bias temperature instability, which is different from OSS in terms of degradation mechanism. Unlike OSS, in PBTI, electrons are accumulated to the SiO_2-HfO_2 interface and injected to the interface or HfO_2 bulk defect, causing Si-H bond depassivation-induced

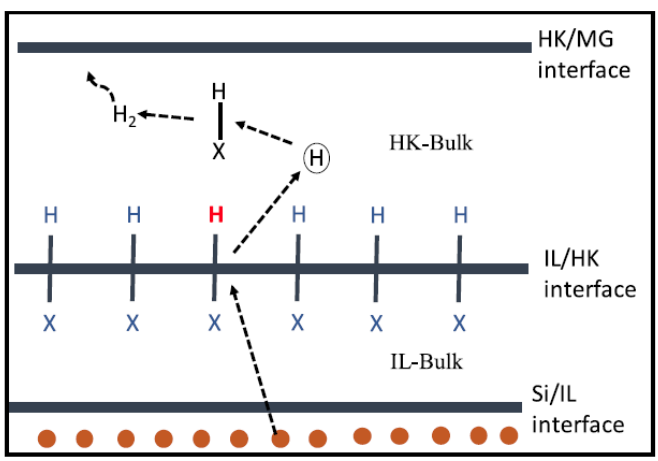


Figure 17. Trap generation mechanism under PBTI stress in an HKMG NMOS [25]

interface trap generation and electron to be trapped in oxide bulk as described in Fig. 17[25]. Consequently, devices suffer from another degradation such as SS degradation, positive V_T shift.

6. 2 Method

PBTI-OSS recovery was simulated as in Fig. 1 in other node with different physics from OSS because PBTI degradation has another mechanism. To implement OSS recovery, similar with OSS case, two types of TD model were applied to describe electron interface traps and electron oxide trapped charges. HfO_2 electron defect band energy level was set to be 1.26 eV, which is described in PBTI two-state model[11]. Recovery phase was simulated separately with OSS. To investigate OSS recovery properties in 3 nm-node NPFETs, three different drain recovery biases with case of ***1)*** $V_g = 0.8\ V, V_d = 0\ V$ ***2)*** $V_g = 1\ V, V_d = 0\ V$ ***3)*** $V_g = 1.2\ V, V_d = 0\ V$ were applied to the device simulation. Recovery PBTI time was set to be100 seconds.

6. 3 Results and discussion

Analysis of PBTI as OSS recovery was carried out. Unlike OSS, at PBTI state where is the recovery phase of OSS, Si-H bond depassivation

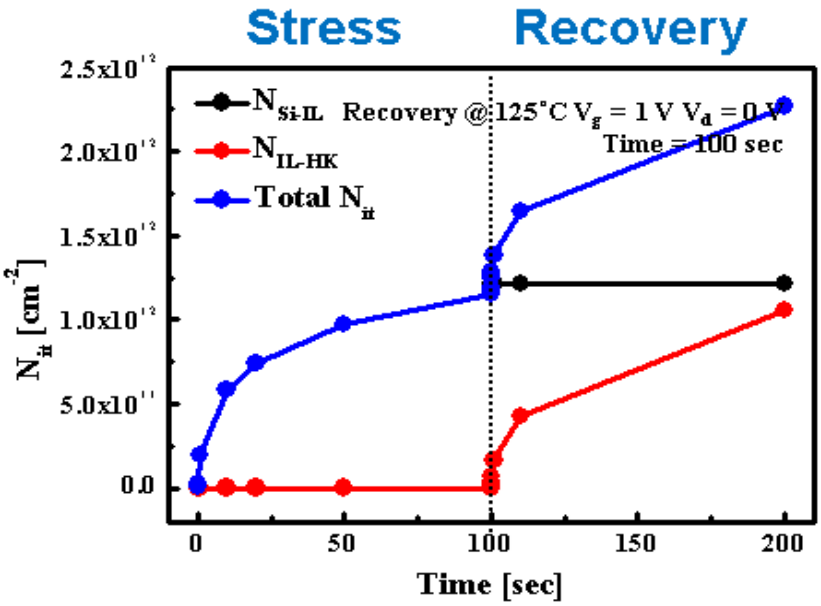


Figure 18. Interface trap for Si-IL interface and IL-HK interface over recovery time

induced interface trap generation at interfacial layer and high-κ layer(IL-HK) interface is dominant. Thus, as seen in Fig. 17, interface trap at the Si-IL interface had not reduced rather negligible change at the PBTI state while the

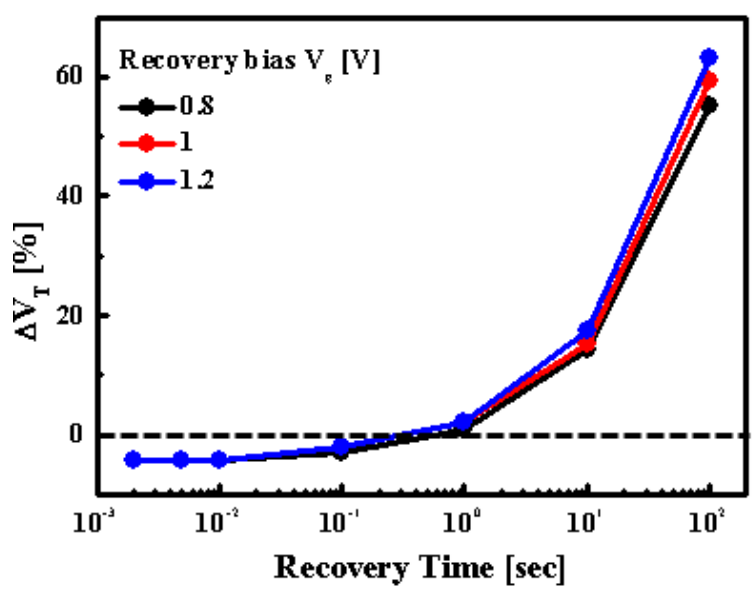


Figure 19. V_T recovery over time as recovery bias

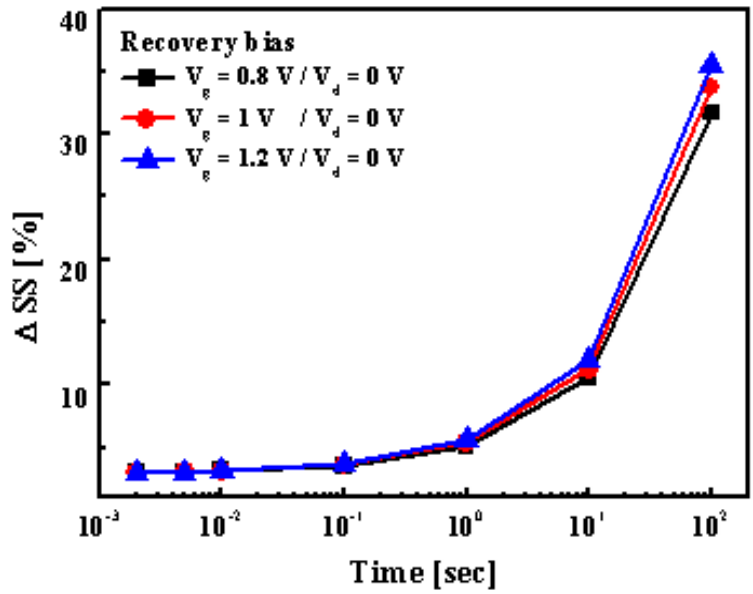


Figure 20. SS degradation over recovery time

trap at IL-HK interface increased at recovery phase, showing total increase of interface traps. In the case of V_T relaxation, comparing three other recovery bias over recovery time was investigated as in Fig. 18. As in the figure, fast recovery due to hole detrapping and electron-induced hole neutralize was shown. While after certain recovery time, more positive V_T shift occurred due to the electron accumulation at higher recovery bias. On the contrary, Fig. 19 shows lack of recovery in terms of SS degradation compared to the V_T recovery property. It is easily confirmed because interface trap generation from OSS cannot be re-passivated because it is induced from Si-O bond depassivation which is hard to be relaxed if once the bond break. Besides,

mentioned above, interface traps near IL-HK interface rather increase resulting in total interface trap increase at the PBTI state, also having an effect on lack of SS recovery.

6. 4 Conclusion

In this chapter, PBTI as recovery of OSS degradation was investigated in various type of recovery bias. In the PBTI state, holes which were trapped in HfO_2 bulk detrapped and electrons are trapped in defect so that negative V_T shift was recovered. However, unlike other reliability issues such as HCI or BTI, perfect recovery of OSS was impossible in terms of generated interface traps and SS because of lack of recovery of interface trap which is induced from Si-O bond dissociation and additional interface trap generation at recovery phase. Thus, it is necessary to prevent and minimize the degradation from OSS by structural or process optimization.

7. Conclusion

In this paper, overall analysis of OSS in 3 nm-node NPFET was investigated. First of all, mechanism of OSS in GAAFET was described and the simulation methodology was introduced, considering ballistic transport which is necessary in sub-5 nm technology node. Due to OSS, devices have been confirmed to be suffered from both interface trap generation and hole trapped charges, inducing negative V_T shift, SS degradation and OFF current increase. It could also be found in g_m shift tendency as OSS time passes.

In addition, gate oxide thickness with same EOT condition and various node dependency were studied. In terms of OSS, increasing of high-κ layer has caused more OSS degradation due to the larger charge trapping region. With structural simulation using same over drive voltage condition, 3 nm-node NPFET showed the most severe degradation due to the stronger electric field or structural reason of GAA which can be affected by field, as compared to the planar MOSFET.

Stress bias and temperature dependency of OSS were also investigated. It was interesting in terms of interface trap generation tendency.

At the larger stress bias condition, overall property change was more severe than at the lower one but interface trap time exponent was higher at the lower bias condition, about value of 0.79. OSS analysis in the different temperature condition, as well as the bias condition, was also considered because interface trap generation or dielectric layer quality can be changed at lower or higher temperature condition. It is known that in Si/HfO_2 system, leakage current increase at higher temperature[24]. At 125 ˚C, as predicted, both interface trap and hole trapped charge increased than the 25 ˚C condition, inducing more overall degradation of the device. On the other hand, interface trap generation time exponent value was higher at 25 ˚C due to the trap generation speed and saturation point difference with the different temperature condition.

Lastly, OSS recovery was analyzed. Relaxation simulation was carried out at PBTI state, inducing V_T recovery by hole detrapping or electron-induced hole neutralizing. On the contrary, SS showed lack of recovery because the generated interface trap which was due to Si-O bond depassivation could not be relaxed with recovery condition unlike Si-H bond dissociation-induced interface trap. Besides, ironically, degradation was showed at PBTI state, which was OSS relaxation phase by IL/HK interface

trap generation or electron trapping at HfO_2.

Thus, according to these overall degradation characteristics or recovery properties, OSS has been confirmed to have a different physics other than HCI or BTI. It can cause severe degradation as devices get aggressively scaled down so that comprehensive analysis of three reliability issues-HCI, BTI and OSS- should be considered for prediction and optimization of nano-scaled devices.

Reference

[1] A. Spessot et al., "Impact of Off State Stress on advanced high-K metal gate NMOSFETs," 2014 44th *European Solid State Device Research Conference (ESSDERC)*, Venice, 2014, pp. 365-368. doi: 10.1109/ESSDERC.2014.6948836

[2] S. Mahapatra, D. Saha, D. Varghese and P. B. Kumar, "On the generation and recovery of interface traps in MOSFETs subjected to NBTI, FN, and HCI stress," in *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1583-1592, July 2006. doi: 10.1109/TED.2006.876041

[3] D. Varghese, H. Kufluoglu, V. Reddy, H. Shichijo, S. Krishnan and M. A.Alam, "Universality of Off-State Degradation in Drain Extended NMOS Transistors," *2006 International Electron Devices Meeting*, San Francisco, CA, 2006, pp. 1-4. doi: 10.1109/IEDM.2006.346895

[4] A Computational Model of NBTI and Hot Carrier Injection Time -Exponents for MOSFET Reliability Kufluoglu, H. & Alam, M.A. J Comput. Electron (2004) 3: 165. https://doi.org/10.1007/s10825-004-7038-9

[5] Gavartin, Jacob & Muñoz Ramo, David & Shluger, Alexander & Bersuker, Gennadi & Lee, Byoung. (2006). "Negative oxygen vacancies in HfO_2 as charge traps in high-k stacks."*Applied Physics Letters*, doi: 89. 10.1063/1.2236466.

[6] (2015). *International Technology Roadmap for Semiconductors*. [Online]. Available: http://www.itrs2.net/itrs-reports.html.

[7] S. Jin, A. Wettstein, W. Choi, F. M. Bufler and E. Lyumkis, "Gate Current Calculations Using Spherical Harmonic Expansion of Boltzmann Equation," *2009 International Conference on Simulation of Semiconductor Processes and Devices*, San Diego, CA, 2009, pp. 1-4. doi: 10.1109/SISPAD.2009.5290216

[8] J. McPherson and H. Mogul, *J. Appl. Phys*. 84, 1513 ~1998, "Underlying physics of the thermochemical E model in describing low-field time dependent dielectric breakdown in thin SiO2 films" doi: 10.1063/1.368217

[9] M. Cho *et al*., "Channel Hot Carrier Degradation Mechanism in Long/Short Channel n-FinFETs," in *IEEE*

Transactions on Electron Devices, vol. 60, no. 12, pp. 4002-4007, Dec. 2013. doi:10.1109/TED.2013.2285245[10] Wen-Chin Lee and Chenming Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," in *IEEE Transactions on Electron Devices*, vol. 48, no. 7, pp. 1366-1373, July 2001. doi: 10.1109/16.930653

[10] Clerc, Raphael & Ghibaudo, Gerard. (2014). "Analytical models and electrical characterisation of advanced MOSFETs in the quasi ballistic regime," 10.1142/9789814583190_0002

[11] G. Rzepa *et al*., "Efficient physical defect model applied to PBTI in high-κ stacks," *2017 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, 2017, pp. XT-11.1-XT-11.6. doi: 10.1109/IRPS.2017.7936425

[12] D. Son, I. Myeong, H. Kim, M. Kang, J. Jeon, and H. Shin, "Analysis of electrothermal characteristics of GAA vertical nanoplate-shaped FETs," *IEEE Trans. Electron. Devices*, vol. 65, no. 7, pp. 3061–3064, Jul. 2018. doi: 10.1109/TED.2018.2832239

[13] J. W. McPherson, "Quantum Mechanical Treatment of Si-O Bond Breakage in Silica Under Time Dependent Dielectric Breakdown Testing," *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, Phoenix, AZ, 2007, pp. 209-216. doi: 10.1109/RELPHY.2007.369893

[14] N. Lee, D. Baek and B. Kang, "Effect of off-State Stress and Drain Relaxation Voltage on Degradation of a Nanoscale nMOSFET at High Temperature," in *IEEE Electron Device Letters*, vol. 32, no. 7, doi: pp. 856-858, July 2011.: 10.1109/LED.2011.214535.

[15] P. Ren *et al*., "New Insights into the Off-state Stress Induced Degradation in Ultra-scaled FinFET Technology," *2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Qingdao, 2018, pp. 1-3. doi: 10.1109/ICSICT.2018.8564811

[16] Wen-Tai Lu *et al*., "The characteristics of hole trapping in HfO_2 SiO_2 gate dielectrics with TiN gate electrode," *Applied Physics Letters* 85, 3525 (2004); doi: 10.1063/1.1808228

[17] Y. Hashim, "Temperature effect on ON/OFF current ratio of FinFET transistor," *2017 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)*, Batu Ferringhi, 2017, pp. 231-234. doi: 10.1109/RSM.2017.8069160

[18] M. Cho *et al*., "Off-state stress degradation mechanism on advanced p-MOSFETs," *2015 International*

Conference on IC Design & Technology (ICICDT), Leuven, 2015, pp. 1-4. doi: 10.1109/ICICDT.2015.7165893

[19] Kupke, Steve & Knebel, Steve & Roll, Guntrade & Slesazeck, Stefan & Mikolajick, Thomas & Krause, G & Kurz, G. (2012). OFF-state induced threshold voltage relaxation after PBTI stress. *IEEE International Integrated Reliability Workshop Final Report(IIRW).* 95-98. 10.1109/IIRW.2012.6468928.

[20] J. W. McPherson, R. B. Khamankar, and A. Shanware, "Complementary model for intrinsic time dependent dielectric breakdown in dielectrics", *Journal of Applied Physics* 88, 5351 (2000); doi: 10.1063/1.1318369

[21] P.C. McIntyre, "Bulk and Interfacial Oxygen Defects in HfO_2 Gate Dielectric Stacks: A Critical Assessment", *ECS Transactions*, 11 (4) 235- 249 (2007) 10.1149/1.2779564

[22] D. Varghese, S. Mahapatra and M. A. Alam, "Hole energy dependent Interface trap generation in MOSFET Si/SiO/sub 2/ interface," in *IEEE Electron Device Letters*, vol. 26, no. 8, pp. 572-574, Aug. 2005. doi: 10.1109/LED.2005.852739

[23] Tse-En Chang, Chimoon Huang and Tahui Wang, "Mechanisms of interface trap-induced drain leakage current in off-state n-MOSFET's," in *IEEE Transactions on Electron Devices*, vol. 42, no. 4, pp. 738-743, April 1995. doi: 10.1109/16.372079

[24] Vladimir A. Gritsenko, Timofey V. Perevalov, Damir R. Islamov, "Electronic properties of hafnium oxide: A contribution from defects and traps," Physics Reports, Volume 613, 2016, Pages 1-20, ISSN 0370-1573, https://doi.org/10.1016/j.physrep.2015.11.002.

[25] Mukhopadhyay, Subhadeep & Parihar, Narendra & Goel, N. & Mahapatra, Shayan. (2017). A Comprehensive DC and AC PBTI Modeling Framework for HKMG n-MOSFETs. IEEE Transactions on Electron Devices. PP. 1-8. 10.1109/TED.2017.2670260.

초 록

OFF-State Stress(OSS)는 과거 다른 신뢰성 이슈에 비해 많은 관심을 가지지는 못하였다. **Hot carrier stress(HCS)** 나 **Bias temperature instability(BTI)** 가 주요 신뢰성 이슈로 다뤄져 왔다. 그러 소자가 점점 스케일링 되면서 급격히 얇은 **oxide** 두께나 짧아진 채널 길이의 영향으로 **DIBL**이나 **OFF** 상태에서의 누설 전류 같은 문제가 발생하게 되었다. 그에 따라서 **gate-all-around field-effect transistors(GAA FET)** 가 강한 게이트 제어성과 훌륭한 동작 특성을 보이며 **7 nm** 이하 기술 노드에서 대안으로 제시되었다. 그러나 좋은 게이트 제어성을 가진다는 것은 강한 수평 전계를 야기하였고 이는 오프 상태의 누설 전류를 더욱 심화시키게 되었다. 이 연구에서는 **3 nm** 노드 나노플레이트 소자에서 **OSS**에 대한 메커니즘에 대해 다루며, 열화와 회복 특성에 대해 분석하였다. **OSS**에 의한 열화는 주로 강한 수직 및 수평 전계에서 비롯된 **hot**

hole injection(HHI)으로 인한 계면 트랩 형성 및 HfO_2 defect band에서 발생하는 hole trapping 의 영향으로 인한다. Hole trapping으로 인해 Negative V_T shift가 발생하며, 계면 트랩의 형성으로 인해 SS 와 I_{OFF} 및 g_m의 열화가 나타나게 된다. 계면 트랩의 경우 HHI로 인해 주로 Si-O bond를 깨뜨리며 발생하며, Si-H depassivation 에서 비롯된 계면 트랩과는 다르게 회복 단계에서 다시 passivation이 되지 않는다는 특징을 가진다. 결과적으로 이 회복 불능의 특징은 OSS가 신뢰성 이슈에서 필수적인 요소이며 이를 제할 수 없음을 의미한다. Technology computer-aided design(TCAD)를 활용하여 OSS 를 구현 후 참고 논문 상의 특성에 calibration을 진행 하였다. 이후 ballistic transport 를 고려하기 위해 Monte Carlo(MC) 시뮬레이션에서의 포화 속도와 ballistic coefficient 등의 시뮬레이션 변수들을 조정하여 I_{DSAT}, I_{DLIN}의 calibration 또한 진행 되었다. 이후 나노플레이트 소자에 OSS physics를 적용하여 세 가지 노드의 나노플레이트 및 참고 논문의 구조와의 특성 열화가 비교되었다. 열화는 GAA 구조상의 이유 및 최대 전계

차이로 인해 3 nm-node NPFET에서 가장 심하게 나타났으며, 이는 high power(HP) device 뿐만 아니라 nano 단위의 complementary metal-oxide-semiconductor(CMOS) 인버터 회로와 같은 input/output(I/O) 회로에서 심각한 특성 열화를 불러올 수 있게 된다. 따라서 NP device에서의 OSS에 대한 분석이 필요하며, 전압 및 온도 등의 다양한 스트레스 조건에서의 특성 분석이 진행되었다. 또한 recovery의 경우 positive bias temperature instability(PBTI) state에서 진행 되는데 이때의 state 조건에 따른 OSS의 회복 특성에 대해서도 분석하였다.

주요어 : 나노플레이트(NPFET), OFF-State Stress(OSS), 신뢰성, Technology Computer-Aided Design(TCAD), Hot hole injection(HHI), 계면 트랩, 절연체 열화

학번 : 2018-24881