M.S. DISSERTATION

Simulation of the Effect of Parasitic Channel Height on Characteristics of Stacked Gate-All-Around Nanosheet FET

적층형 GAA 나노시트 전계효과 트랜지스터에서 기생 채널의 높이가 소자의 특성에 미치는 영향 분석

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지도 교수 박 병 국

이 논문을 공학석사 학위논문으로 제출함

2020 년 2 월

서울대학교 대학원

전기정보공학부

최 윤 호

최윤호의 공학석사 학위논문을 인준함

2020 년 2 월

위 원 장 이 중 호 (인)

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Abstract

By using technology computer-aided design (TCAD) simulation, the aim of this paper is to investigate the effect of Si parasitic channel, which is placed under stacked nanosheet channels, on the electrical characteristics of stacked nanosheet GAA FETs. We have controlled the parasitic channel height, and evaluated the effect on electrical performance of the device. Trade-off in performance of the nanosheet FET is observed: the increase in parasitic channel height results in improvement in subthreshold swing and on/off current ratio, while it also causes capacitance to increase which brings worse RC delay and active power. The parasitic channel height control in devices with ground plane doping is also investigated and implementing ground plane doping and parasitic channel control at the same time is not that effective. Also, it is shown that parasitic channel control is more effective in nanowire-like shaped FETs than nanosheet FETs.

Keywords : Stacked nanosheet GAA FETs, TCAD simulation, Parasitic channel, Ground plane doping.

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Chapter 1

Introduction

Semiconductor devices have been continuously scaled down according to Moore's Law [1]. But scaling of the devices was limited by the short channel effect (SCE) problem. To mitigate SCE, the device structure has been changed from a planar structure to FinFET structure, which has enhanced gate controllability. Nonetheless, the FinFET still represented insufficient electrostatic gate controllability and severe parasitic components. In order to compensate for this insufficiency, a gate-all-around (GAA) structure was suggested where the gate covers the entire channel. [2-11]. Furthermore, by introducing vertically stacked nanosheet structure, greater drive currents with greater effective channel widths under the same footprint are obtained [12-16].

During the fabrication of stacked nanosheet FETs on bulk Si substrates, Si nanosheets are released by wet etching of SiGe sacrificial layers. These Si nanosheets are surrounded by high-κ/metal gate (HK/MG) materials and become multiple channels for the FETs [17-18]. However, HK/MG materials are also deposited on the remaining Si bulk and this results in the formation of another tri-gate FET under Si nanosheet channels. This parasitic channel can act as a leakage

path, affecting the overall performance of the nanosheet FETs. In earlier studies, attempts have been made to suppress leakage through this channel such as ground plane (GP) doping [18], and back biasing of the tri-gate FET [19].

In this paper, we observe the effect of the parasitic channel on electrical characteristics of the device by using TCAD simulation. It is reported that the change of the height of this parasitic channel causes subthreshold swing (SS), I_{on}/I_{off} ratio and parasitic capacitance to change. We also investigated device with ground plane doping.

Chapter 2

Simulation Setup

Three stacked nanosheet FETs are simulated using Sentaurus TCAD. Fig. 1(a) shows the schematic diagram and doping concentration of the n-type nanosheet FET. Geometric parameters of the nanosheet FETs are defined in Table 1. The channel and substrate regions are doped with boron at 10^{17} cm^{-3} and source/drain regions are doped with phosphorus at 10^{20} cm^{-3}. The operation voltage (V_{dd}) is set to 0.7 V. There is a parasitic channel under nanosheets and the height exposed above shallow trench isolation (STI) filling (H_{ch}) is controlled. This channel is similar to tri-gate FET since three sides of the channel is surrounded by HK/MG. As H_{ch} increases, the area surrounded by gate increases, therefore increasing influence of the tri-gate FET (Fig.1(b)). The dependency of effective channel width (W_{eff}) should also be considered since the area of the parasitic channel surrounded by bottom gate differs as H_{ch} changes, which is described in Fig.1(b).

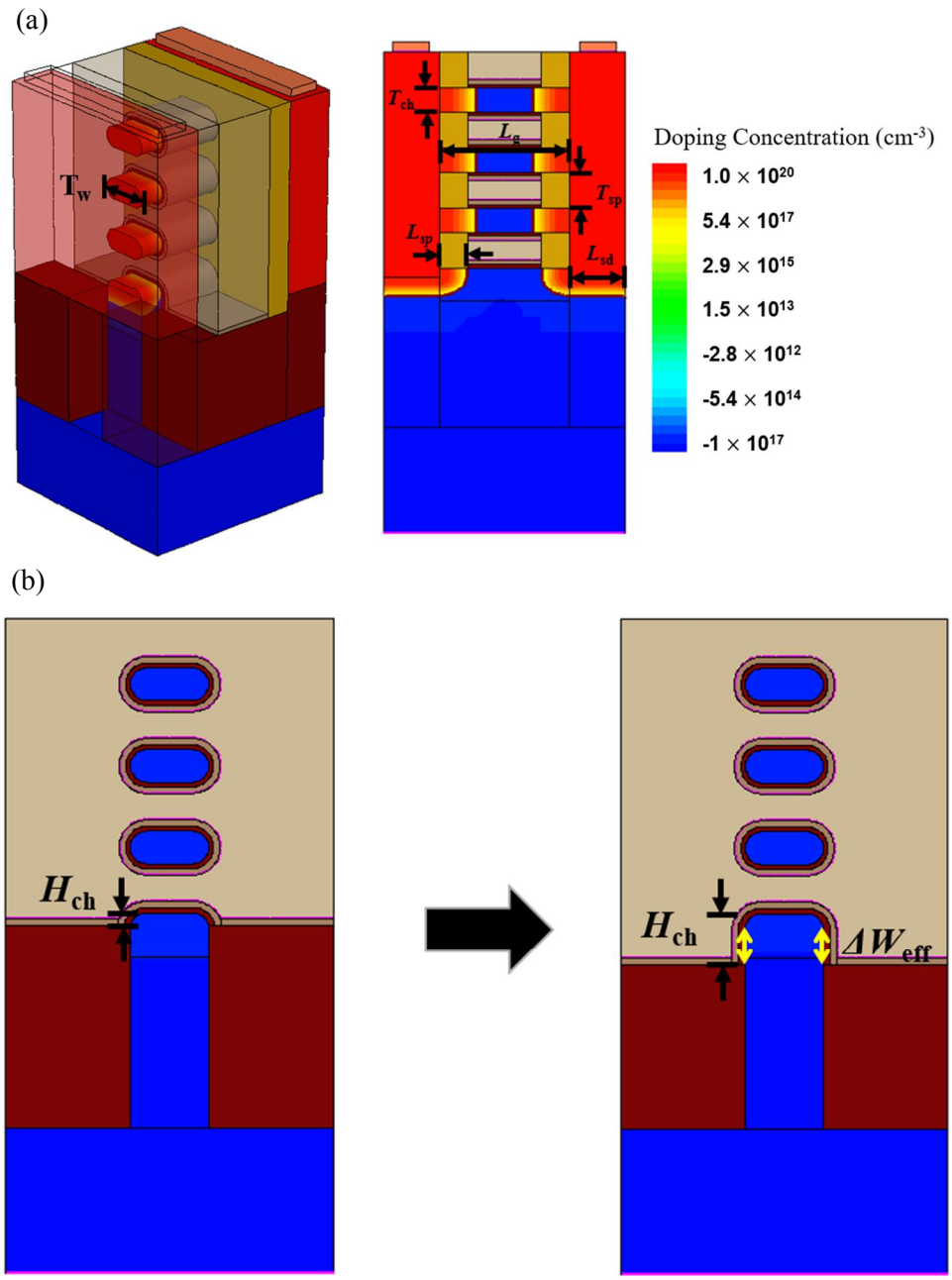


Fig. 1. (a) Schematic diagram of the n-type nanosheet FETs. Doping concentration and geometric parameter definitions are also shown. (b) Cross section view and geometric parameters. H_{ch} is defined and ΔW_{eff} for H_{ch} change

Table 1. List of physical parameters used in simulation

Parameter	Value (nm)
L_{G}	15
T_{ch}	5
T_{w}	12
T_{sp}	7.4
L_{sp}	6
L_{sd}	11.6
T_{ox}	0.7
T_{hk}	1

Chapter 3

Results and Discussion

3.1. Parasitic Channel Height Control in Nanosheet FET

Fig. 2(a) shows the transfer characteristics of the nanosheet FETs having different H_{ch} values. The off-currents (I_D @ V_g = 0 V) are lower for higher H_{ch}. This is due to the enhancement in gate controllability over parasitic channel since leakage path surrounded by HK/MG gets wider. Fig. 2(b) shows the electron current density of nanosheets and parasitic channel at off-state (V_G = 0 V). As gate control coverage increases, leakage through the parasitic channel reduces. The off-current decreasing trend seems to be weaken at high H_{ch}. This is due to the fact that the bottom part of the parasitic fin has little to do with conduction. This part is far from source/drain extended doping and its influence as channel is very weak. So the off-current converges to the value of the parasitic channel's sole minimum off-current. In contrast, the on-current (I_D @ V_g = 0.7 V) increases as H_{ch} increases since total conduction area broadens for higher H_{ch}. However, the on-current per W_{eff} is lower for higher H_{ch} since GAA FETs have better I_{on}/W_{eff} ratio than tri-gate FETs and the dominance of the tri-gate FET gets stronger as H_{ch} increases.

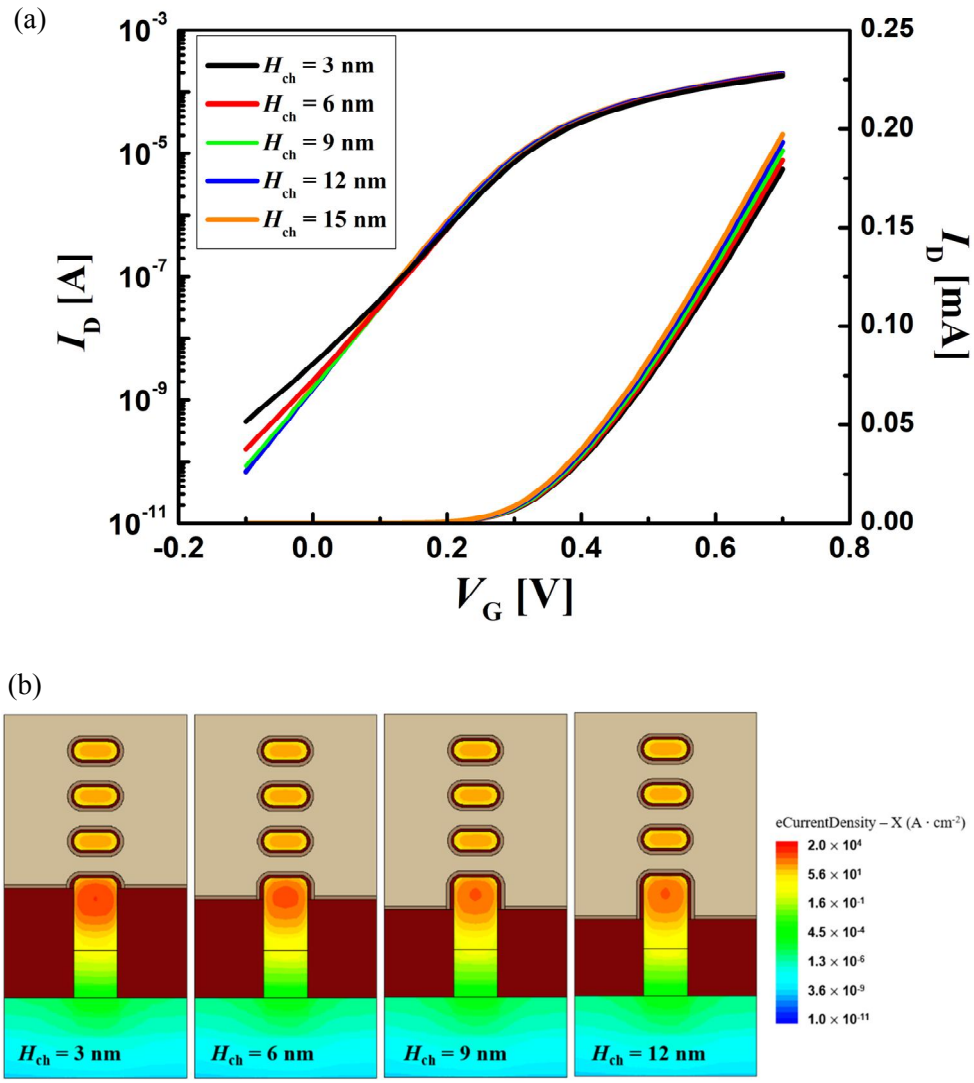
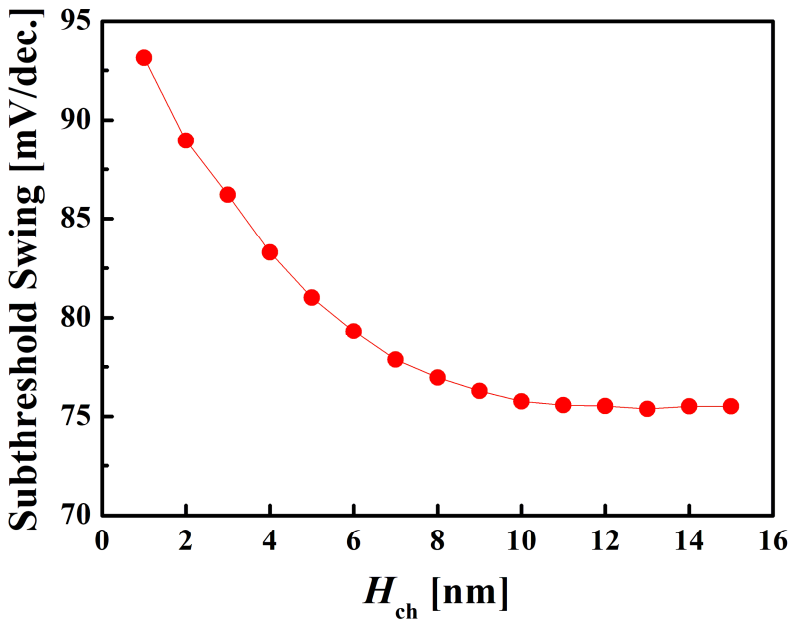


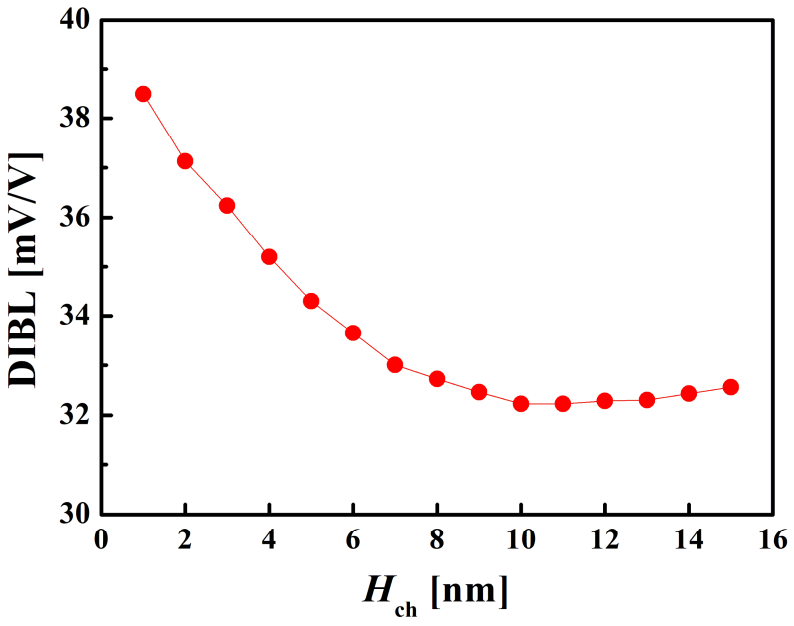
Fig. 2. (a) Transfer characteristics of nanosheet FET with H_{ch} variance (b) Electron current density of nanosheet FET at V_G = 0 V with H_{ch} change

The dependency of SS upon H_{ch} (from 1 nm to 15 nm) is reported in Fig. 3(a). This expresses point swing at V_g is 0.1 V. The subthreshold swing when the parasitic channel is almost not exposed is around 90 mV/decade and it goes down to near 70 mV/dec. Nanosheet FET without parasitic channel is simulated for comparison and its SS is 63.4 mV/dec. This means SS of the nanosheet FET is mostly dominated by the parasitic channel. There is obvious improvement of SS as H_{ch} increases. As mentioned, this is due to the enhancement in gate controllability over parasitic channel. The subthreshold swing also seems to saturates for higher H_{ch}, for the same reason with the off-current decreasing trend which is explained earlier. Fig. 3(b) shows drain induced barrier lowering (DIBL) and it has similar trend with SS. Fig. 3(c) displays I_{on} / I_{off} ratio. As we have shown, for H_{ch} increase, Ion increases and I_{off} decrease, so the on/off ratio gets better. However, at high H_{ch} (over 11 nm), I_{off} slightly increases because threshold voltage of the nanosheet FET decreases as H_{ch} increases, while SS almost does not change at high H_{ch}. So the ratio has maximum point around 11 nm and gradually decreases. Therefore, for better I_{on} / I_{off} ratio, H_{ch} should not be too high.

(a)


Subthreshold Swing [mV/dec.]
95
90
85
80
75
70
0
2
4
6
8
10
12
14
16
H_{ch} [nm]

(b)


DIBL [mV/V]
40
38
36
34
32
30
0
2
4
6
8
10
12
14
16
H_{ch} [nm]

(c)

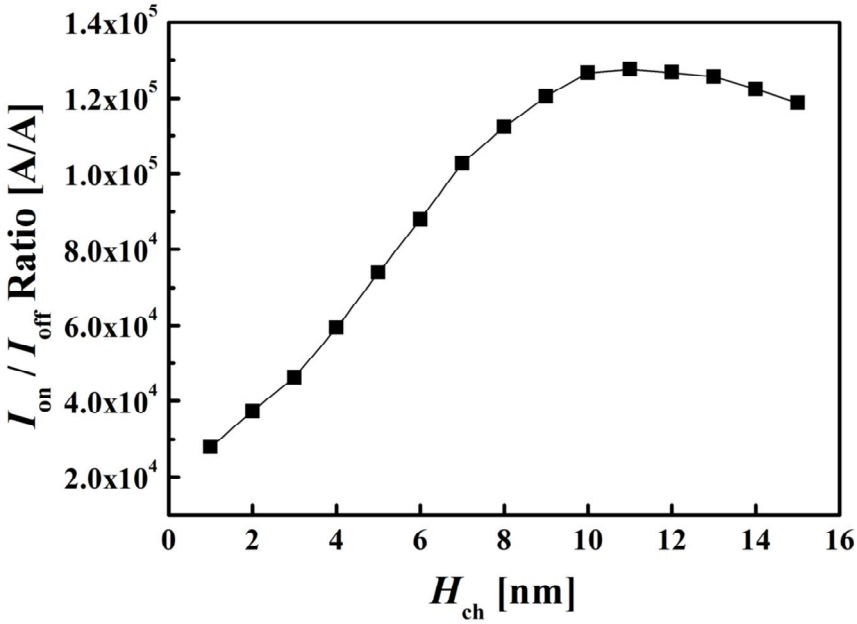
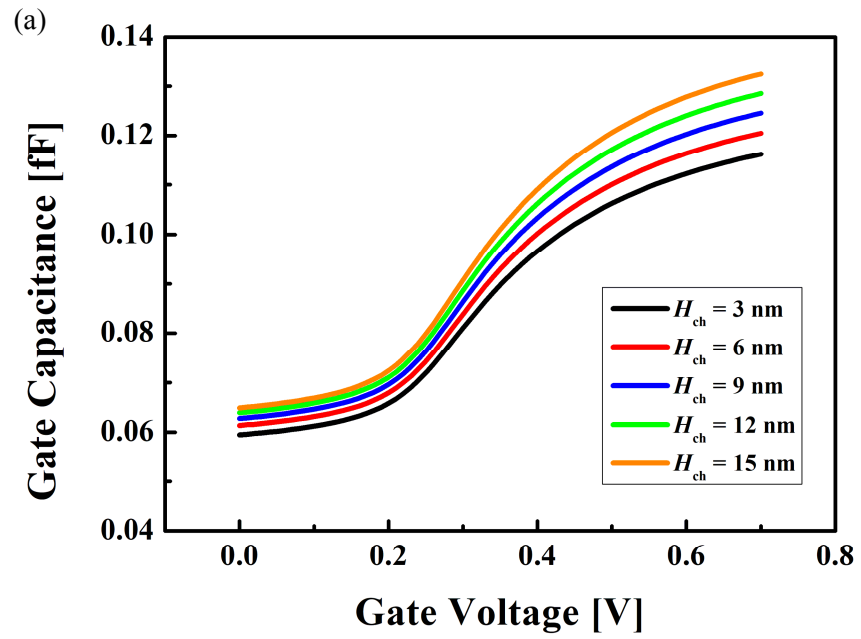


Fig. 3. (a) Subthreshold swing (b) DIBL (c) I_{on}/I_{off} ratio of nanosheet FET with H_{ch} change.

Capacitance impacts circuit performance by increasing the capacitive load and thus increasing delay. In addition, active power is proportional to capacitance, thus, reducing capacitance is important for GAA FETs [20]. However, increasing H_{ch} also results in the higher capacitance due to the increase of gate capacitance area, which is shown in Fig. 4(a). The total gate capacitance at frequency 1 GHz (C_g) rises as H_{ch} increases for all gate voltage (Vg) region. Because C_g is proportional to area, the increase of C_g at V_g = 0.7 V shows almost proportional increase as H_{ch} increases, which is about 0.0014 aF/nm (Fig. 4(b)).



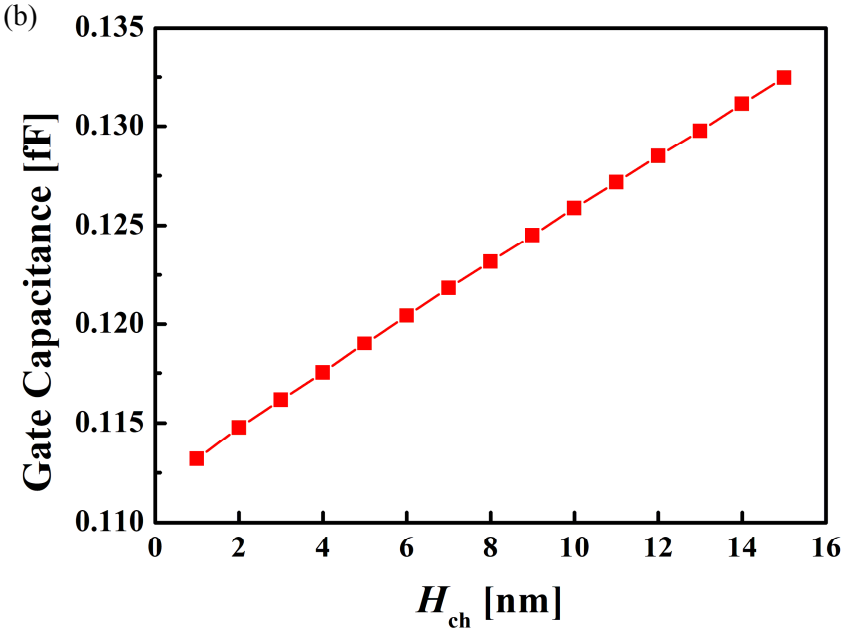


Fig. 4. (a) C_g for different H_{ch} at 1 GHz as V_g changes. (b) C_g for different H_{ch} at V_g = 0.7 V.

Fig. 5(a) shows RC delay of FETs with different H_{ch}. RC delay can be calculated through this formula.

$$\text{RC delay (sec)} = \frac{V_D}{I_D} \times C_g$$

C_g refers to total gate capacitance and I_D is drain current when the drain voltage and gate voltage are set to 0.7 V which is mentioned as Ion above. As mentioned, both Ion and gate capacitance increases with H_{ch}. But the increase of gate capacitance is greater because the conducting area increase as H_{ch} increases but it becomes less effective when it is far from source/drain area. So RC delay increases depending on H_{ch}. Fig. 5(b) depicts RC delay considering fan-out of circuit.

(a)

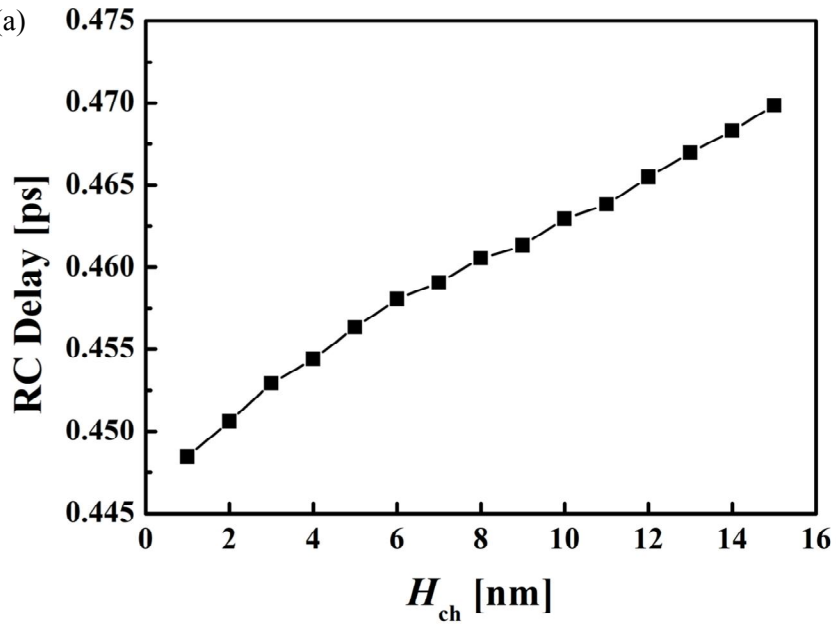
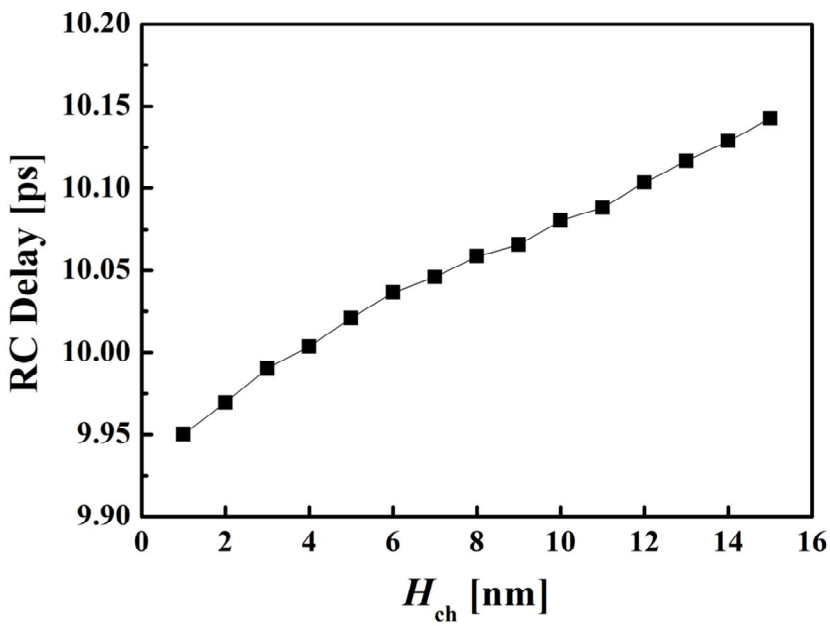

RC Delay [ps]
0.475
0.470
0.465
0.460
0.455
0.450
0.445
0
2
4
6
8
10
12
14
16
H_{ch} [nm]

Fig. 5. (a) Calculated RC delay of nanosheet FET. (b) RC delay considering fan-out.



As shown above, trade-off in electrical characteristics is observed. This indicates that as H_{ch} increases, leakage current goes down but RC delay increases which brings lower operating speed, and power consumption also becomes higher. C_g shows almost linear increase as H_{ch} rises, SS, on the other hand, has saturation point, which should be close to original SS of tri-gate FET. Too high H_{ch} only aggravate device performance and the level of SS improvement weakens if H_{ch} is far deeper than source/drain junction depth. These results suggest another point to consider when fabricating GAA nanosheet FETs. We can design devices with appropriate value of SS and capacitance by controlling H_{ch}

3.2. Nanosheet FET with Ground Plane Doping

It has been reported that ground plane doping technique suppresses the parasitic channel in nanosheet FETs and enhances SS. At the first stage of fabricating nanosheet FETs on bulk Si, ion implantation is done before SiGe/Si epitaxial growth, which makes the parasitic channel has higher doping concentration than channel region. By implementing ground plane doping, punch through is suppressed and the threshold voltage of the parasitic channel increases, so the parasitic channel has less influence on the overall device performance [21, 22]. We also investigated the impact of parasitic channel height in devices with ground plane implantation. The simulated device has same structure, but additional doping in the parasitic channel is implemented with boron, which is described in Fig. 6. The doping concentration and position is decided through reference [23].

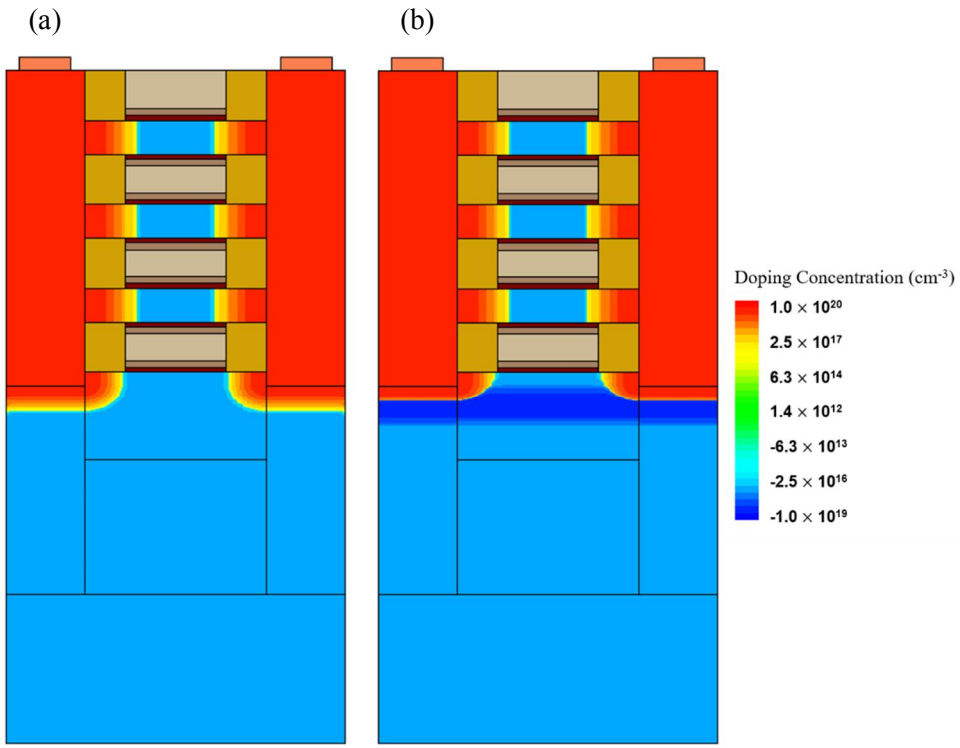


Fig. 6. (a) Nanosheet FET without ground plane implantation (b) Nanosheet FET with ground plane implantation and their doping concentration

Fig. 7 illustrates the electron current density of nanosheet FETs with and without ground plane implantation. In Fig. 7(b), additional boron doping with concentration of 10^{19} cm^{-3} is implemented in the parasitic channel and H_{ch} is 3 nm for both nanosheet FETs. It is obvious that leakage current which flows through the parasitic channel is suppressed in Fig. 7(b) thanks to the ground plane implantation.

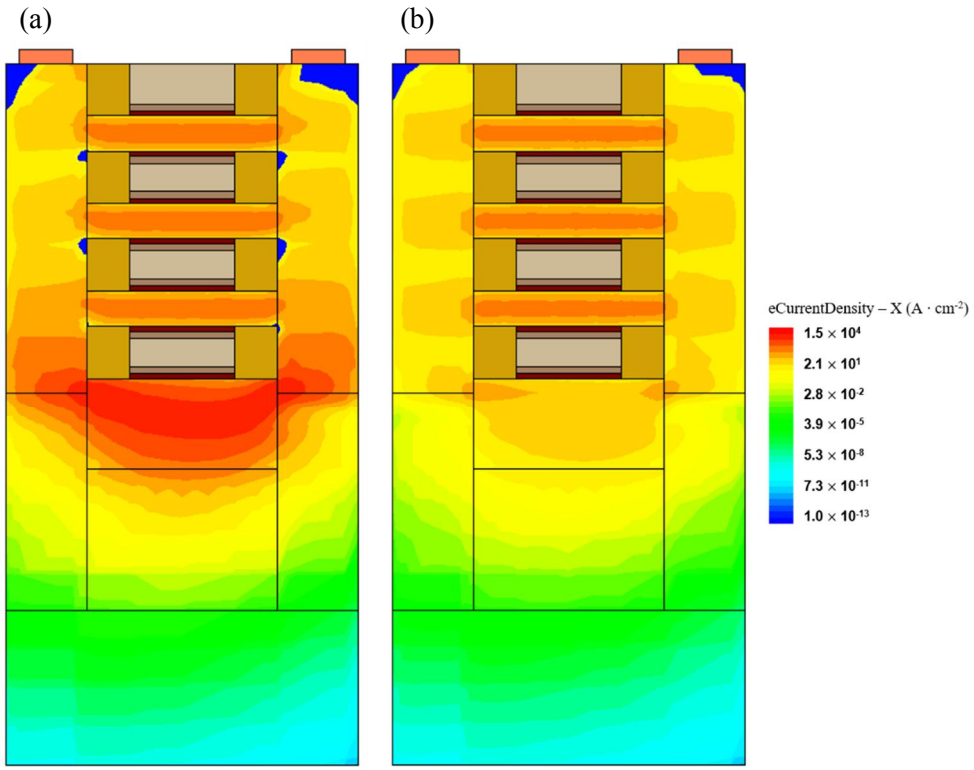
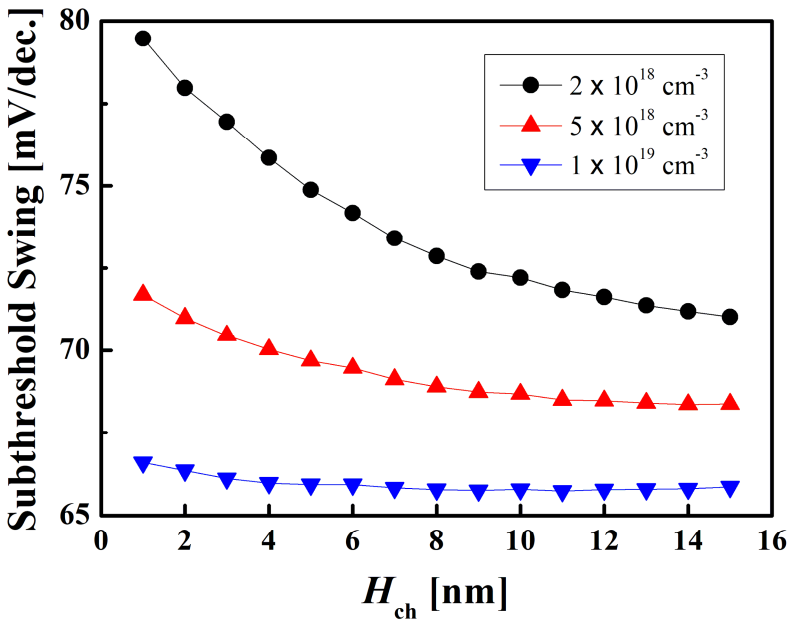


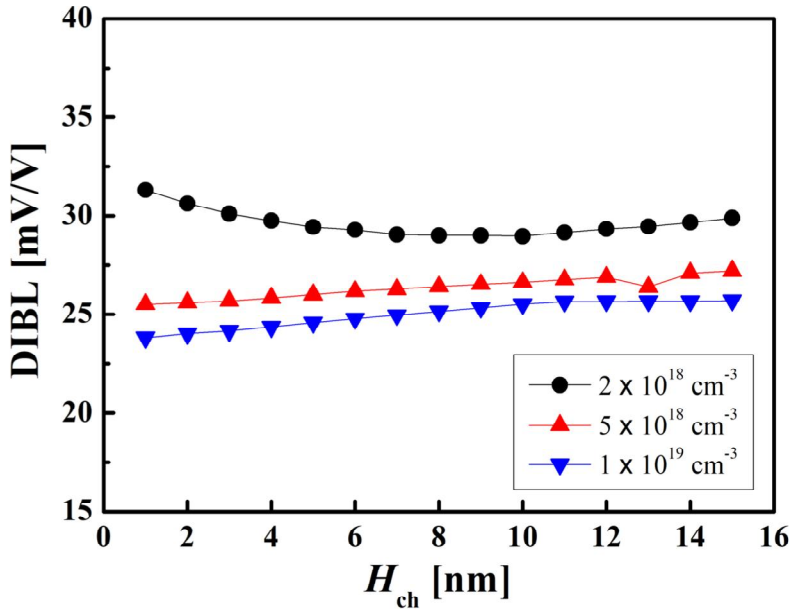
Fig. 7. (a) Nanosheet FET without ground plane implantation (b) Nanosheet FET with ground plane implantation and their electron current density

The simulation result is shown in Fig 8. SS (Fig. 8(a)) change by H_{ch} with different ground plane doping concentration is depicted. SS improves as H_{ch} increases but the rate of increase gets lower for higher doping concentration. It also saturates much earlier for higher ground plane implantation. DIBL (Fig. 8(b)) shows very little change. I_{on}/I_{off} ratio (Fig. 8(c)) shows similar result with others. By implementing ground plane doping, the conduction in tri-gate FET becomes very weak so the effect of controlling the tri-gate FET also becomes less effective. In contrast, the gate capacitance increases proportionally regardless of ground

plane implantation. It is inefficient to apply H_{ch} controlling and ground plane doping at the same time.

(a)

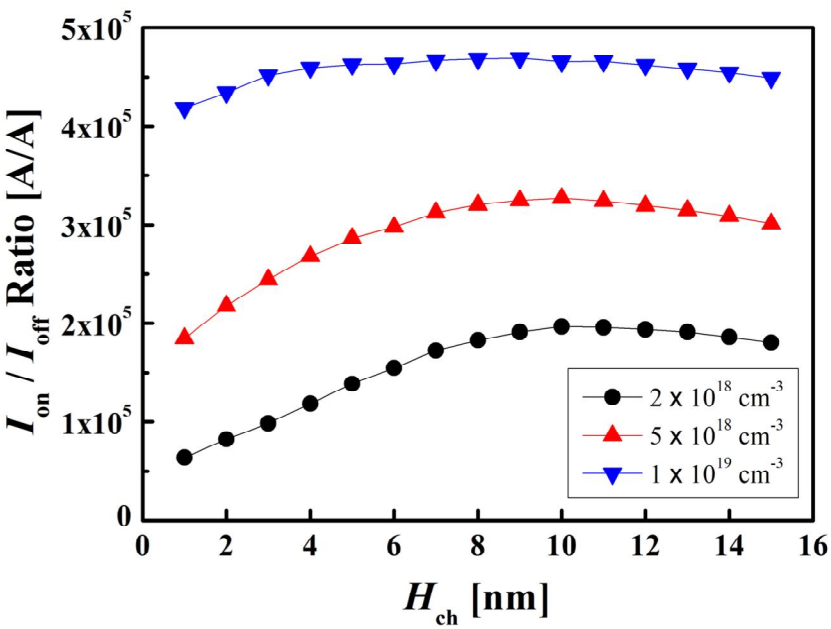



DIBL [mV/V]
40
35
30
25
20
15
0
2
4
6
8
10
12
14
16
H_{ch} [nm]
2 x 10^18 cm^-3
5 x 10^18 cm^-3
1 x 10^19 cm^-3

(b)

(c)

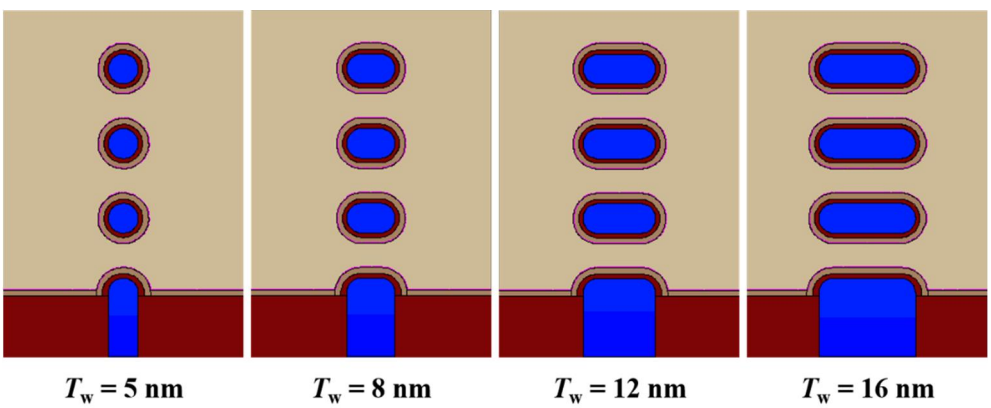
Fig. 8. (a) Subthreshold swing (b) DIBL (c) I_{on}/I_{off} ratio of nanosheet FET with various ground plane doping as H_{ch} changes.



3.3. Parasitic Channel Height Control in Various Nanosheet shape

Nanosheet width (T_w), which is originally set to 12 nm in section 3.1, can be varied and affects device performance. Nanosheet FETs with varying T_w are shown in Fig. 9, and their dependency upon parasitic channel height is investigated in this section. As T_w gets narrower, gate controllability over each channel improves but Ion gets smaller When T_w = 5 nm (1st structure in Fig. 9), the channel is nanowire shape.

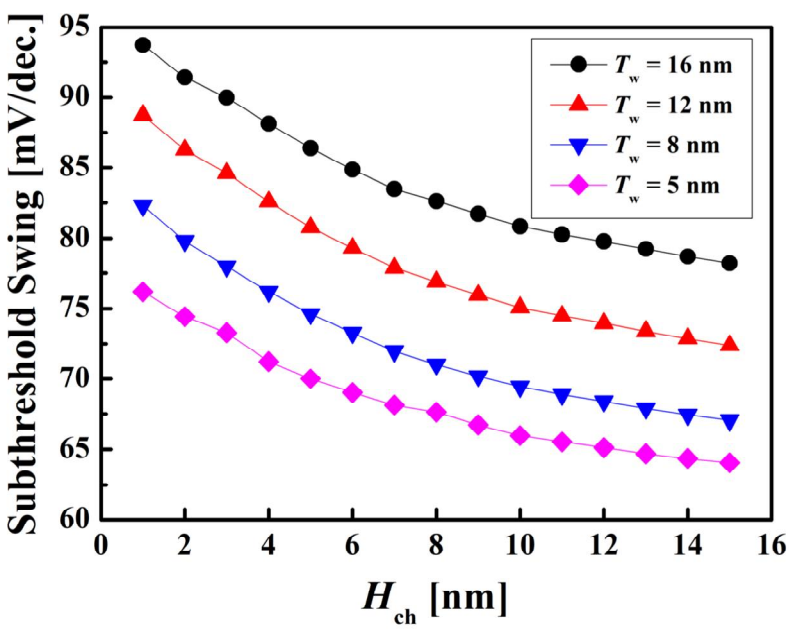
Fig. 9. Nanosheet FETs with different nanosheet width (T_w)



The result is presented in Fig 10 below. SS change by H_{ch} with different ground plane doping concentration (Fig. 10(a)) is depicted. SS shows almost constant improvement trend as H_{ch} increases regardless of T_w. But I_{on}/I_{off} ratio (Fig. 10(b)) shows quite different aspect. The ratio of nanosheet with narrow Tw is much more affected by H_{ch} control. If the channel shape become similar to nanowire, gate controllability among conduction region gets better, and the same applies to parasitic channel. So leakage current through parasitic channel is suppressed better

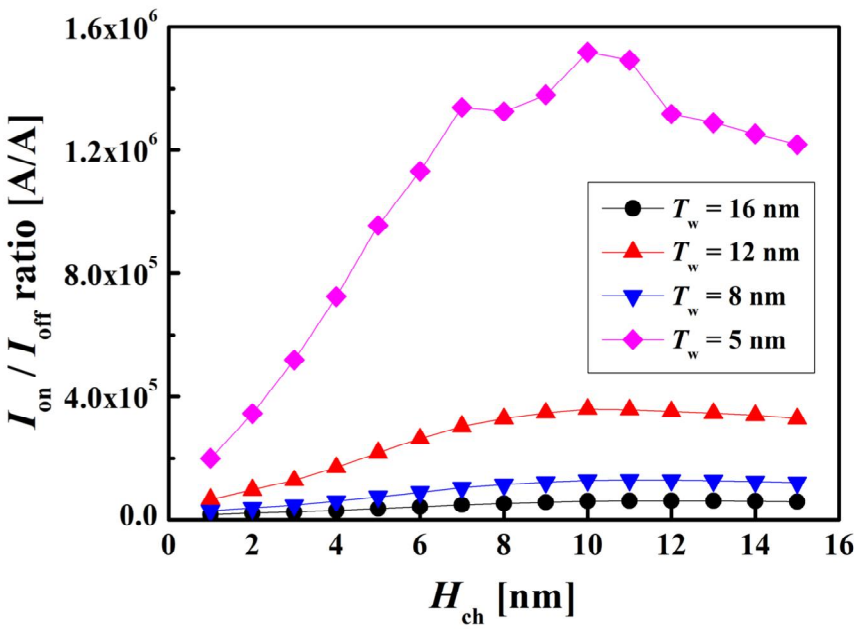
in nanowire-like channel, while I_{on} is just related to total channel area increase. SS improvement would show similar effect but it is not clearly shown because SS approaches to its thermoionic limit, 60 mV/dec, for nanosheet FETs with narrow T_w.

(a)



(b)

Fig. 10. (a) Subthreshold swing (b) I_{on}/I_{off} ratio of nanosheet FET with various T_w as H_{ch} changes.



Gate capacitance increase in the devices is mentioned as demerit of

increasing H_{ch} in section 3.1. The cap increase is proportional to the channel, so cap increase rate would not be significantly affected by T_w. The capacitance change and RC delay increase would show similar trend which is shown in section 3.1.

In conclusion, it is more effective to enhance device performance by increasing H_{ch} in nanowire-like shaped FETs, since I_{on}/I_{off} ratio gets much better whereas capacitance increasing trend does not change as T_w gets narrower.

Chapter 4

Conclusions

Stacked Nanosheet GAA FET has attracted much attention as one of the most promising candidates for finFET replacement in transistor size scaling. As reported in prior works, parasitic Si channel is formed under nanosheet channels during stacked GAA nanosheet FET fabrication, and attempts have been made to suppress leakage through this channel. In this study we have investigated electrical characteristic of nanosheet FET according to the variation of H_{ch}. We have found that the increase of H_{ch} results in improvement of SS, I_{on}/I_{off} ratio, and DIBL, because gate controllability over parasitic channel enhances for higher H_{ch}. But it also causes capacitance to increase, which brings increase in power and RC delay. When ground plane doping is implemented in the device, the effect of controlling

parasitic channel height become slight for higher ground plane doping concentration. Also, it is shown that parasitic channel control is more effective in nanowire-like shaped FETs than nanosheet FETs. This is the first trial to utilize parasitic tri-gate for different electrical characteristics while previous works just tried to mitigate its effect. Our result provides a new consideration about the fabrication of nanosheet GAA FETs.

Further verification is needed if the results apply to real cases, however, since this study shows simulated results. Future work should include fabrication of nanosheet FETs for varying H_{ch} and measurements for each case.

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초 록

본 논문에서는 적층형 나노시트 GAA(Gate-all-around) 전계효과 트랜지스터에서 적층형 나노시트 채널 아래에 형성되는 실리콘 기생 채널이 소자의 전기적 특성에 미치는 영향을 TCAD(Technology computer-aided design) 시뮬레이션을 통하여 분석해보았다. 기생 채널의 높이를 조절하며 소자의 전기적 특성 변화를 관찰하였다. 기생 채널의 높이를 증가시키면 문턱 전압 이하 스윙(subthreshold swing), 온오프 전류 비율, DIBL(Drain induced barrier lowering) 특성이 향상되었다. 하지만 게이트 커패시턴스 또한 증가하였으며 RC 딜레이와 유효 전력 면에서는 소자 성능이 떨어지는 단점 또한 있었다. 그라운드 플레인 도핑(ground plane doping)이 적용된 소자에서 기생 채널 높이 조절의 효과도 분석하였다. 그라운드 플레인 도핑과 기생 채널 높이 조절을 동시에 적용하는 것은 비효율적인 것으로 보였다. 또한 다양한 형태의 채널을 가진 전계효과 트랜지스터를 분석한 결과, 채널의 형태가 나노와이어에 가까울수록 기생 채널 높이 조절이 더 효과적이라는 것도 알 수 있었다.

주요어 : 적층형 나노시트 GAA 전계효과 트랜지스터, TCAD 시뮬레이션, 기생 채널, 그라운드 플레인 도핑, 나노와이어
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