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Uniform resistive switching memory using localized charge trapping

by

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Abstract

The Memristor was firstly introduced by the professor Chua in 1971 and has been researched by many groups such as Hewlett-Packard (HP) since 2008. Resistive switching memory (ReRAM) has simple structure of metal-insulator-metal and has potential usage for recent ongoing topics of neuromorphic, synapse, and logic. Due to simple structure, it can be fabricated with low cost and has advantage of crossbar array with a unit cell of $4F^2$, where F means minimum feature size. Whereas, DRAM, NAND, NOR, and Flash Memory have $6F^2$, $5F^2$, $10F^2$, respectively. Since the memristor has the smallest unit cell among the other memory, it has a significant potential to replace NAND flash memory for high integration system. Although the recent technology of the vertical NAND flash memory increases the integration, it has a couple of limitations. First is its fabrication difficulty after layers of 100. Higher height also derives limitation of the high operation voltage in the Flash memory due to thicker insulating layer. On the other hand, ReRAM has many advantages over the flash memory such as low operation voltage, high integration, and potential compatibility of the vertical devices. Despite the advantages, it has a low reproducibility due to formation of the multiple conductive paths. These paths affect the variation of the operation voltage in the process of the formation and destruction of the paths. To address this problem, many researches have to be done not only for a high integration but most importantly for uniformity of the operation in the array.

In the first part, insertion of Au nanodots in $Pt/Ta_2O_5/HfO_2/TiN$ was introduced to improve cell-to-cell variation and cyclic variation. The mechanism of the HfO_2 was that electrons were trapped and detrapped in the shallow trap sites. When the electrons were trapped, it showed the low resistance state, whereas the high resistance for the detrapping state. In addition, when Ta_2O_5 was deposited on the HfO_2, its plasma created the deep trap states, which acted as a conducting path. If Au nanodots were inserted in this layer, they assisted the conducting path and improved the memory switching because

of the electric field concentration effect. The device without Au nanodots could exhibit around 200 cycles, but more than 1000 cycles could be done with the Au nanodots inserted. The Au nanodots inserted device was also capable of doing the multi-level operation by creating the stable 8 current level states under controls of the number of trapped electrons with compliance current.

In the second part, electric switching operation based on the location of the inserted Au nanodots was addressed along with the COMSOL simulation tool for the electric field concentration. Two different locations, atomic layer deposited HfO_2 and Ta_2O_5, were examined. Ta_2O_5 was well known for non-resistive switching layer and diode-like rectifying behavior from the Schottky barrier between high work function of Pt. Therefore, insertion of the Au nanodots might not affect this switching behavior. Switching behavior in Ta_2O_5, however, was improved after insertion of the Au nanodots. This unexpected behavior was confirmed through COMSOL simulation that if the location of the Au nanodots was sufficiently away from the interface, its improvement of the endurance was faded out along with the weaker field concentration effect. As a result, this experimentally confirms that the switching behavior was occurred at the interface.

In the third part, fabrication of the Au nanodots in the localized area with electron beam (e-beam) deposition was addressed. There were many methods to deposit nanodots such as AAO, but those methods could not control the size or distribution of the nanodots since they used the circular shape nanostructure. The distribution of the nanodots is important factor because it could cause the cell-to-cell variation. To control the two factors, e-beam deposition was used. Au nanodots could be fabricated with these steps in order, e-beam exposure, deposition of the Au thin film and subsequent lift-off process. To achieve the fine size of the Au nanodots, reducing stress to the Au thin film and fine control of the e-beam power were important. Reducing stress could be achieved by controlling side slope of the photoresist (PR) in the exposure process. Two layers of PMMA with different molecular weight were deposited to create

undercut slope PR, which reduced stress to the Au thin film. E-beam power was also important, which determined number of electrons emit to the PR layer. Too small of the power caused not enough reaction to create the pattern, whereas too high of the power caused broader pattern of the PR. Therefore, fine control of the power was necessary. As a result, the minimum size of 50 nm Au nanodots could be fabricated. After insertion of the Au nanodots, atomic force microscopy (AFM) was used to confirm locations of the conductive path on the surface. In the device, the conductive path showed in the nanodots, which confirmed successful induction of the electric field concentration. Therefore, this field concentration around the nanodots showed improvement in the switching properties.

Keywords: resistive switching memory, memristor, nanodots, field concentration, self-rectifying, uniformity, HfO_2, Ta_2O_5

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List of Abbreviations

AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscope
ALD	Atomic Layer deposition
BE	Bottom Electrode
BRS	bipolar resistive switching
CAFM	Conductive Atomic Force Microscope
CBA	crossbar array
CBRAM	Conductive Bridge Random Access Memory
CF	conductive filament
CMOS	Complementary Metal Oxide Semiconductor
DC	direct current
DRAM	Dynamic Random Access Memory
ECM	Electrochemical metallization
FESEM	Field Emission Scanning Electron microscopy
FFT	Fast Fourier Transformation
FIB	focused ion beam
GIXRD	Grazing Incidence X-Ray Diffraction
HRS	high resistance state
HRTEM	High Resolution Transmission Electron Microscopy
I_{cc}	compliance current

I-V	Current-Voltage
LRS	low resistance state
MEMS	Micro electro mechanical system
MIM	metal-insulator-metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
PCRAM	Phase change random access memory
PR	Photoresist
ReRAM	Resistive switching random access memory
RS	resistive switching
RT	room temperature
SEM	Scanning electron microscopy
TCM	thermal change mechanism
TE	top electrode
TEM	Transmission Electron Microscopy
URS	unipolar resistive switching
VCM	Valence change Mechanism
XRD	X-ray Diffraction

1. Introduction

1.1. Resistive switching Random Access Memory

By definition, the resistive switching is the change of resistance states either from a high-resistance state (HRS) to a low-resistance state (LRS). Figure 1.1 shows many mechanisms for resistive switching (RS) which categorized to electronic effects mechanism, electrochemical metallization (ECM), valence change mechanism (VCM), thermo-chemical mechanism (TCM) and phase change mechanism (PCM)[1]. Among them, one of the most popular types of RS device is the ionic motion-based filamentary type RS device with oxides, where either oxygen vacancies[2–4] (ex> valence change memory) or highly mobile cations[5–7] (ex> electrochemical metallization cell) serve as the mobile species for switching. In such type devices, the electroforming process is necessarily required in most cases to construct RS inducible condition with a relatively higher voltage for subsequent switching. Unfortunately, this high voltage and the current process often induce damage to the selector device in 1-selector-1-RS device (1S1R) configuration for large scale array and imposes a heavy burden on the operation circuit[8,9]. Also, this process is responsible for substantial device-to-device variance due to its random nature of filament formation. After the electroforming process, either oxygen vacancy percolation paths or metal (Ag or Cu) conducting bridges are formed in the shape of a continuous filament that connects the top and bottom electrode, exhibiting high current (> μA) low resistance state (LRS). The electronic effects mechanism could be regarded as a potential contender to solve various issues with resistive switching random access memory

(ReRAM) based ionic RS mechanisms generally cause the movement of ionic species during the device operations. Electronic effects mechanism, which is mediated by electron trapping/detrapping in the switching layer, is the working principle. In this mechanism, an additional electroforming step is not required, and the operational instability caused by formation and rupture of CFs is somewhat solved[10,11].

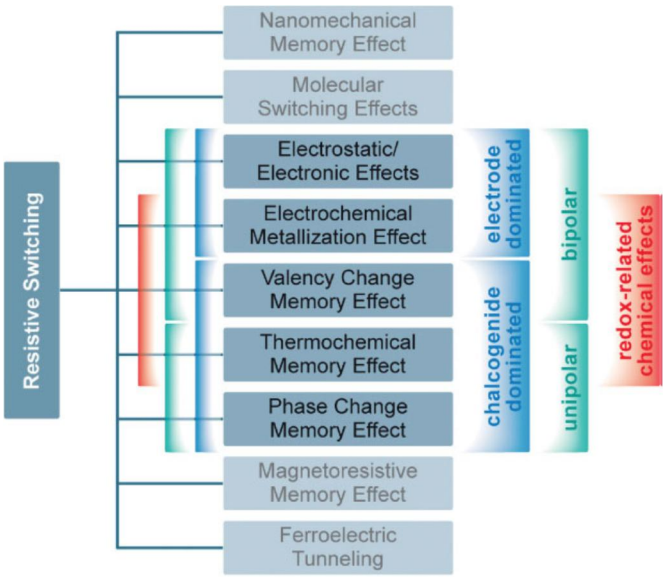

Figure 1.1 Classification of the resistive switching effects. Adapted from [1].

1.2. Critical factor for a high-density array

Although ReRAM has been studied for the past decade, there are some unsolved problems to produce high-density array such as line resistance, sneak current, overset, and etc. Overset is a problem in which the conducting path is excessively formed during the set operation of the device, causing a reset failure. To address the overset problem, controlling the compliance current or pulse width is important to prevent hard breaking down. Also, low line resistance must be adopted, which can be achieved by using a low-resistivity metal such as Cu. The difficult part is the sneak current path. As shown in Figure 1.2, unwanted current path of 2-3-4 is formed to read number 1 cell. This problem is severe when the desired cell has high resistance state whereas nearby cell has low resistance state[12]. Therefore, an appropriate selector such as a diode or nonlinear selector should be adopted to mitigate the reverse bias current.

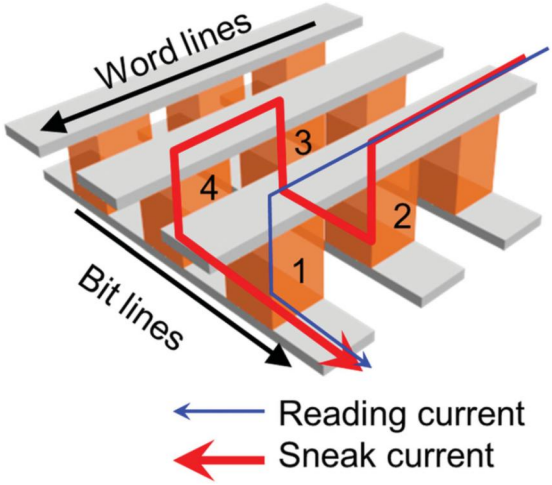

Figure 1.2 Schematic figure of sneak current problem in CBA structure. Adopted from [12].

1.3. Research scope and objective

One of the major difficulties is finding the device that could be operated at low power and has extremely uniform RS behavior with self-nonlinearity. When this problem is solved, it can be applied to various applications. Although current memory technology is expected to face limitations to improve further integration in about ten years, ReRAM must improve the operation stability to replace the next-generation memory.

In Chapter 2, to address issue in the stability of ReRAM, Pt/Ta_2O_5/HfO_2/TiN device with Au nanodots inserted is introduced. Comparison of the electrical properties between devices with and without Au nanodots is made. The device with Au nanodots induces the electric field concentration and shows the stable endurance property. The reason is explored with COMSOL simulation tool.

In Chapter 3, the electric effect depending on different locations of the inserted Au nanodots at the interface and inside for Ta_2O_5 and HfO_2 is examined. With the aid of COMSOL simulation, it is verified that Au nanodots has an effective range, which its effect is only valid at the interface.

In Chapter 4, the fabrication process of the Au nanodots is modified from the previous e-gun evaporator method to e-beam lithography and subsequent metal lift-off process. The new process can control the distribution and size of the nanodots preventing the cell-to-cell variation.

2. Improvement of resistive switching uniformity by embedding Au nanodots in the $Pt/Ta_2O_5/HfO_2/TiN$ structure

2.1. Introduction

Defects are random, which is an intrinsic property of nature. Therefore, any type of solid-state devices that exploit the performance based on the creation, modification, migration, and coalescence of defects, especially point defects, usually suffer from the lack of uniformity and reproducibility[13–16]. Contemporary memory devices record information bits, zero and one, in nanoscale devices, such as a capacitor in dynamic random access memory (DRAM) or floating gate in NAND flash memory, in the form of charge. However, the information bits are not necessarily be represented by the presence or lack of appropriate charge; variable resistance could also be a viable alternative. The newly introduced 3D X-point memory of Intel in 2015 was built on the reversible resistance change between the crystalline, which has low resistance, and amorphous, which has high resistance, phases of chalcogenide $Ge_2Sb_2Te_5$ material[17,18].

In this regard, the metal-insulator-metal (MIM) structure could be an intriguing device that can be used as either capacitor, as in DRAM, or reversibly switching resistive element, in resistive switching random access memory (RRAM). For the former case, the device performance relies on its fundamental bulk property, such as dielectric constant, and macroscopic physical dimension, such as electrode area and insulator thickness. Therefore, these properties are under precise control, allowing a

huge-scale integration possible. The current 16 Gb DRAM chip has fully working sixteen billion cells (capacitors) on ~1 cm^2 area, which is an amazing outcome of elaborate design and fabrication processes and capital expenditure for them. In contrast, the latter can be accomplished by forming a percolated conduction path, or conducting filament (CF), between the two metal electrodes through the insulating layer[19–21]. Such a device configuration usually suffers from random variation because the CFs are usually composed of clustered or percolated point defects, such as oxygen vacancies (VO) in the transition metal oxides (TMO). The creation of VO's must be random, and their percolation should also be arbitrary in TMO upon the bias voltage application, making the CF formation highly uncontrolled and non-uniform[22–24].

The inherently small size of the CF (<< 10 nm in diameter) is also unfavorable in achieving uniformity, although it has been regarded as the critical importance of the RRAM for ultra-high density integration. Any portion of the device with a higher area than the CF cross-section could be the location of CF making its formation, rejuvenation, and creation of a new one non-uniform[25].

Ion-migration invokes issues related to power consumption. Compared with the current mass-production memory, DRAM and NAND flash, both of which migrate the electronic charges to store the data bits, RRAM needs to move ions to form and rupture the CFs, which requires generally high power consumption. While the total power consumption can be decreased by making a smaller cell size or confining the CF to a highly localized area of the cell, the local power density at the CF must still be quite high. This always accompanies with the problems of local Joule heating,

which further aggravates the non-uniformity issue[26]. Therefore, decreasing power consumption is essential not only for energy-efficient computing but also ensuring the cell-to-cell, device-to-device, and switching-by-switching uniformities.

Because an ultra-large-scale integration of memory fundamentally requires the uniformities mentioned above, solving the non-uniformity issue is an impending task for the commercialization of RRAM. Multilevel memory functionality (4, 8, 16 or even 32levels) is also critical for the RRAM to compete with the NAND flash, which now even exploits the quintuple bits (32 levels). The application of RRAM to the neuromorphic computing field requires analog-like memory functionality. All these applications critically require uniformity of the resistance values[27–29].

In this regard, the authors' recent works for in TiO_2-based thermochemical RRAM containing the metal nano-dot (ND)[30], and electronic self-rectifying RRAM using the Ta_2O_5/HfO_2 bilayer[31,32] are eye-catching. The former significantly decreased the well-known non-uniformity in TiO_2 RRAM, which relies on the formation and rupture of Magnéli CFs, by confining the electric field to the area between the Ru NDs. Under this circumstance, the location where the Magnéli CF forms became limited to a small portion of the entire memory area, which significantly enhanced the switching uniformity. Nonetheless, the ion-migration issue remained to make the improvement limited[33,34]. The electronic switching mechanism in the Ta_2O_5/HfO_2 bilayer system solved the ion-migration related issues, i.e., the power consumption was significantly decreased which also accompanied with the enhanced uniformity but with limited success. In this case, the switching was mediated by the electron trapping/detrapping in the HfO_2 layer, whereas the Ta_2O_5 layer provided the memory

cell with the diode functionality by forming a high the Schottky barrier with the Pt electrode. The electrons migrated between the trapping sites in the HfO_2 layer and TiN electrode, which formed a quasi-Ohmic contact.

This work exploits the RRAM functionality, therefore, when these two previous (partially) successful methods are combined. The RRAM cells in this work are similar to the Ta_2O_5/HfO_2 cell in the previous work, where the Ta_2O_5 (10 nm) and HfO_2 (10 nm) layers contact with the Pt top electrode and TiN bottom electrode. However, uniform Au ND's were included at the controlled location from the Ta_2O_5/HfO_2 interface. Here, the Ta_2O_5 and HfO_2 layers were grown by the atomic layer deposition techniques, and Au NDs were formed by the electron-beam evaporation and post-annealing.

It was found that the RRAM cell showed almost no variation in the switching curve during 100 consecutive DC current – voltage sweeps as well as AC pulse-type switchings when the Au NDs located at the Ta_2O_5/HfO_2 interface.

To understand such intriguing phenomena, conductive atomic force microscopy and simulations for identifying the local potential (or field) inside the memory cell are performed. It was found that the local field concentration at the Ta_2O_5/HfO_2 interface was the critical factor that has improved the switching uniformity. This work also elucidated that the charge trapping occurs at the interface, which will provide the community with further insights for implementing the high-performance RRAM and synapses for neuromorphic circuits.

While this work adopts a relatively large cell area (2 x 2 μm^2 to 10 x 10 μm^2), there is no reason that the critical idea of this work could not be utilized in nano-scale

cells. In fact, the methodology would result in an even more improved performance in such smaller cells.

2.2. Experimental

The Au embedded device was fabricated by depositing 50nm thick TiN Bottom Electrode(BE) on Si/SiO_2 substrate, 10nm thick HfO_2 switching layer, 10nm Ta_2O_5 and 50nm thick Pt Top Electrode(TE), in sequence. The TE and BE were patterned into a cross-point structure through a lift-off process, using photolithography. TiN BE was deposited by the reactive sputtering technique using a commercial sputtering tool(Applied Materials, Endura), Ti target with a diameter of 4 inches was used with 20 sccm of Ar gas and 3 sccm of N_2 gas. The RF power and the substrate temperature were set to 500 W and room temperature, and the base and operating pressure were $\sim 10^{-7}$ torr and 1 mtorr, respectively. The HfO_2 layer was formed via thermal atomic layer deposition (ALD), with $Hf[N(CH_3)(C_2H_5)_4$, and O_3 as a Hf precursor and an oxygen source, respectively at a 340°C substrate temperature. The Ta_2O_5 layer was deposited in another shower-head-type ALD reactor using tert-butylimido-bis(diethylamido)cyclopentadienyl)tantalum and H_2O-activated plasma (300W) as the Ta precursor and oxygen source, respectively, the wafer temperature during the deposition was set to 200°C. Scanning electron microscopy (SEM, Hitachi, S-4800) and atomic force microscopy (AFM, JEOL, JSPM 5200) were used to observe the morphology of the Au thin film and Au NDs. The cross-sectional transmission electron microscope images of the $Pt/Ta_2O_5/HfO_2/TiN$ sample were observed using a high-resolution transmission electron microscopy (HRTEM, JEOL, JEM-2100F). The depth profile was estimated by Auger electron spectroscopy (AES, ULVAC-PHI, PHI-700). The I-V characteristics were measured using an HP4145B semiconductor

parameter analyzer. During the measurement, the Pt TE was biased, and the TiN BE was grounded. The electric field concentration simulation data at each sample was obtained by COMSOL.

2.3. Results and Discussions

Figure 2.1(a) was the schematic diagram of the Au nanodots inserted device, which were located at the Ta_2O_5 and HfO_2 interfaces. Since the deep trap sites are located at the HfO_2 after deposition of the $Ta2O_5$, Au nanodots were inserted in this area. Figure 2.1(b) showed the top and bottom electrodes of the device. It has line widths of 4, 6, 8, and 10 μm. Thin film of the Au layer, which was almost negligible, was deposited with a slow deposition rate of 0.1~0.2 Å/s. The purpose of this was to reduce the interface energy between Au and substrate and induce Ostwald ripening growth. As a result, Au NDs could be formed without having further rapid thermal annealing (RTA) or heat treatment in the furnace. Figure 2.2 was a result of the SEM images of the Au NDs. For the case of (a), (b), and (c), thickness was controlled to be 2, 3, and 7 nm to not form a thin film, respectively. Then, non-thin film of the Au layer transformed to Au NDs by self-agglomeration under the Ta_2O_5 deposition temperature even without separate heat treatment. Although the self-agglomeration cannot be controlled by changing the thickness, the size and distribution of the NDs could be controlled. Since its top view of SEM analysis could not verify the height of the Au NDs, AFM analysis was used. Figure 2.3 (a), (b), and (c) were AFM results of the non-heat treatment samples. Notice that Rq values did not have significant variation for different deposition thickness, but Rq values did increase about 2~5 times after heat treatment in the chamber when Ta_2O_5 was being deposited. This supported the SEM analysis result where Au NDs were formed by self-agglomeration. In addition, AFM results support that the higher optimal thickness of the Au NDs was

formed from the thicker thin film. The term 'optimal' was used because 15 nm Au thin film, which was above the optimal thickness, did not form Au NDs. This result was verified using surface image using SEM and similar R_q values throughout the surface using AFM analysis. Figures 2.4 (a), (b) showed the cross-section transmission electron microscopy (TEM) images of the $Pt/Ta_2O_5/HfO_{2-x}/TiN$ structure embedded with Au NDs at the interface between HfO_2 and Ta_2O_5 and in the HfO_2, respectively. The figures show a well-distinguishable layer structure and Au NDs. Figure 2.4(c) showed Auger electron spectroscopy (AES) to check formation of the Au NDs at the interface. From the result, Au NDs were formed at the interface of the Ta_2O_5 and HfO_2. Also, amount of the carbon showed low for both of the oxide layers. The significant carbon amount in HfO_2 layer often showed the leaky property. Since the carbon content was low, the switching properties was determined by the trapped electron at the oxygen vacancy (VO).

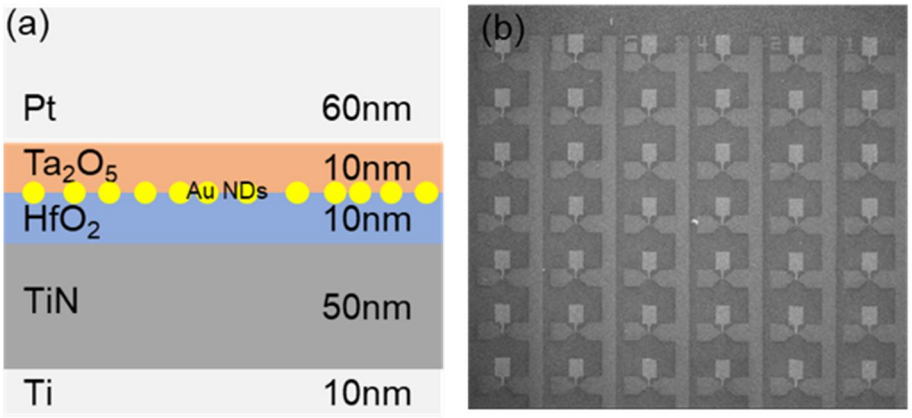

Figure 2.1 (a) Schematic diagram of the Pt/Ta_2O_5/HfO_2/TiN stack cell embedded Au NDs into the interface between Ta_2O_5 and HfO_2 and Scanning electron microscope image of (b) top-view

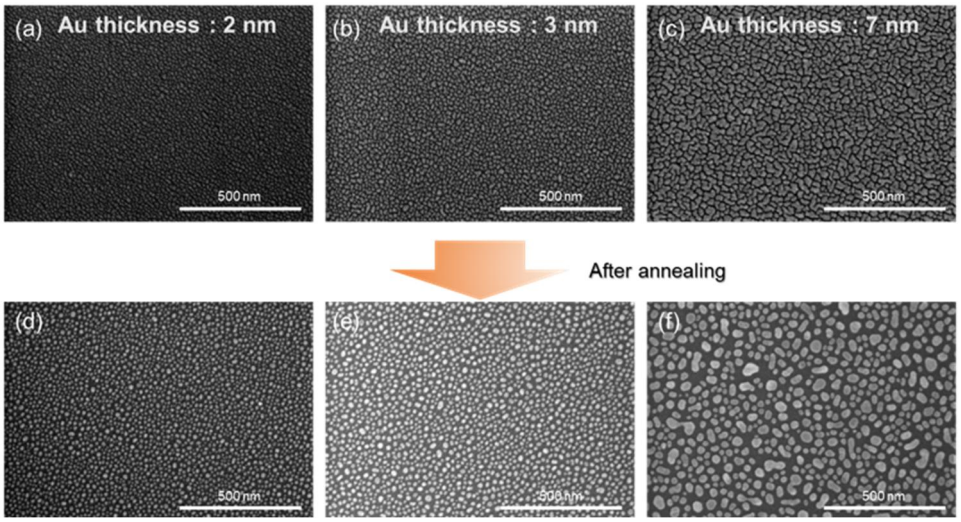

Figure 2.2 The SEM images depending on the different Au deposition thickness (a)2nm (b)3nm (c)7nm and (d)2nm (e)3nm (f)7nm after annealing

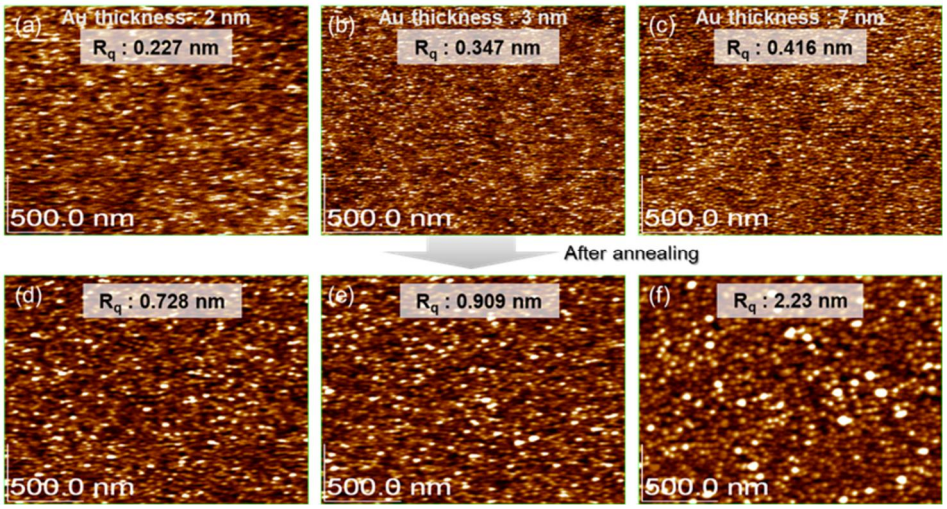

Figure 2.3 (a) The AFM analysis of depending on the different Au deposition thickness (a)2nm (b)3nm (c)7nm and (d)2nm (e)3nm (f)7nm after annealing

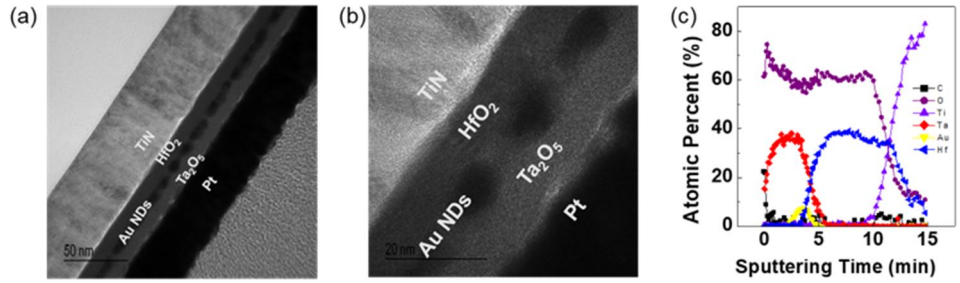

Figure 2.4 (a), (b) Cross-sectional TEM images of the device embedded Au NDs between HfO_2 and Ta_2O_5 interface (c) depth profile AES data of the device with Au NDs inserted at the interface.

Figures 2.5(a), (b) showed the RS current-voltage(I-V) properties of the Pt/Ta_2O_5/HfO_{2-x}/TiN and Pt/Ta_2O_5/Au NDs/HfO_{2-x}/TiN samples, respectively, and the inset figures showed the on-off ratio which was resistance ratio between high resistance state(HRS) and LRS. I-V behavior was measured according to Figure 2.5(a) in the indicated order. Pt TE was biased, and TiN BE was ground. The compliance current of 100 nA was applied to prevent the complete breakdown of the device. As figure 2.5(b) indicated, electroforming-free, high rectification ratio and increased variation for consecutive operation could be found, which were well-known in the previously reported devices. When Au NDs were inserted into the device, as shown in Figure 2.5(b), the considerable improvement in switching uniformity could be found. In addition, although the current was reduced at the low voltage, the on/off ratio still remains, referring to the inset of Figure 2.5 (a) and (b).

Figure 2.6 shows electrical properties in different size of the nanodots created by the variation of the deposition thickness. Figure 2.6 (a), (b), and (c) only varied deposition thickness while other conditions remain same. Thus, electrical properties depending on the Au nanodots were shown. In Figure 2.2 and 2.3, size and distribution of the Au NDs were different but electrical properties remain same. Additional experimental data [not shown] for 1 nm thickness showed improvement in the variation but the effect was not significant. On the other hand, 2 nm thickness and above started to emerge the effective improvement, which was considered as the critical thickness.

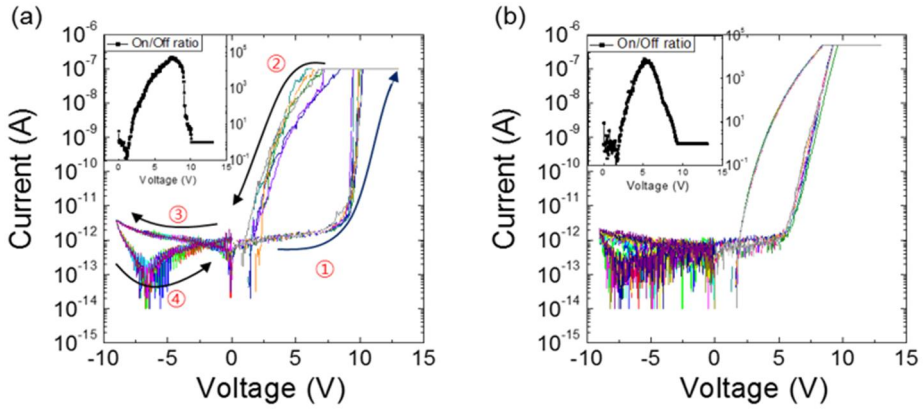

Figure 2.5 Resistive switching in DC measurements of the (a) Pt/Ta_2O_5/HfO_2/TiN device. (b) embedded Au NDs between Ta_2O_5 and HfO_2 interfaces of the device. (Inset figures of (a) and (b) are on/off current ratio)

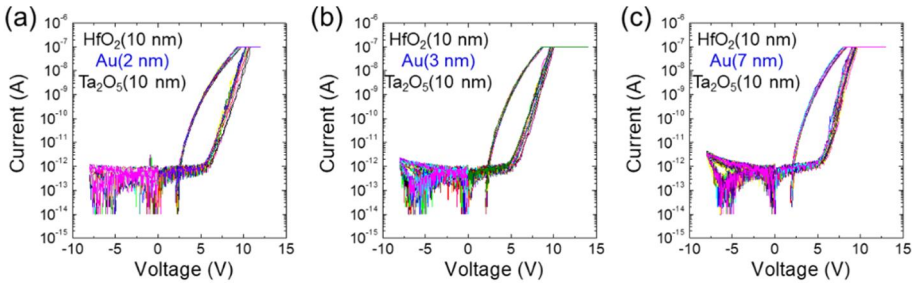

Figure 2.6 Resistive switching in DC measurements of the Pt/Ta_2O_5/HfO_2/TiN device embedded Au NDs between Ta_2O_5 and HfO_2 interfaces of the device. Au NDs formed with different Au deposition thickness (a) 2 nm, (b) 3 nm, (c) 7 nm

Subsequently, the stability of the device operation was shown in Figure 2.7. Cumulative probability of the single cell was shown in Figure 2.7 (a), which could be obtained after 100 cycles of the operations. The current level was low and significant noise level was existed for the high resistance state (HRS), so the cell-to-cell variation was difficult to distinguish between with and without NDs devices. For the low resistance state (LRS), the significant distribution improvement could be observed. Figure 2.7 (b) showed the cell-to-cell uniformity, which was conducted by 15 different cells after switching three times. Consequently, most of the device showed almost identical electrical properties, so it was a good candidate to fabricate the devices in array layer.

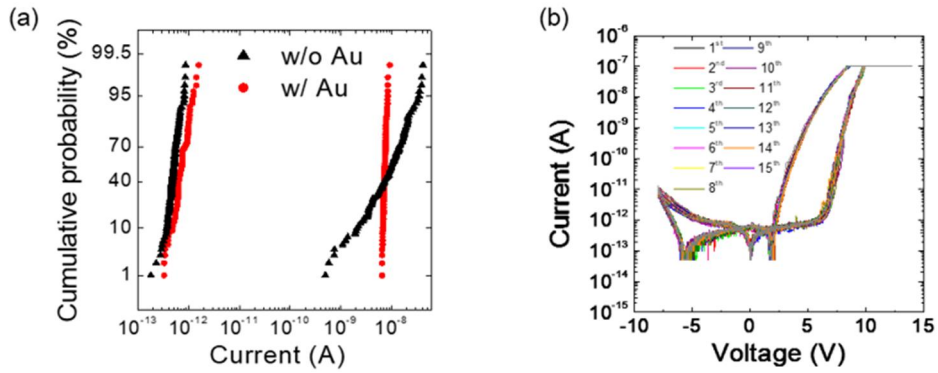

Figure 2.7 (a) The cumulative probability graphs of high resistance stats(HRS) and the low resistance state(LRS) The black triangle shows the data of the device without Au NDs inserted, and the red circle shows the data of the device with Au NDs inserted. (b) DC measurement results of 15 different devices which obtained cell-to-cell switching variation

Figure 2.8 introduced coefficient of variation to define an extent of electric field concentration effect by inserted Au NDs. The coefficient of variation could be defined as average standard deviation of the cyclic current level at the read voltage of 6 V. The reason for using coefficient of variation rather than the standard deviation was to see how much improvement had been made without considering the current level of desired group. The coefficient of variation depending on the Au thin film was also examined as shown in Figure 2.8(a). The red color represented the Au thickness of 0, and its coefficient of variation was decreased along with significant improvement in distribution. Whereas, the thickness variation showed the insignificant change of the coefficient of variation, so not much improvement was expected. In addition, cell area had also insignificant change as shown in Figure 2.8(b). Then, area dependency and its retention were verified in Figure 2.9. As the cell area was increased, the resistance in HRS was decreased and had high current level. The slope of the current increase depending on the area was almost linear, 1.08. However, same current level was remained with the variation of the area, and this showed the localized switching since it had a similar shape of the filamentary switching of electronic bipolar resistance switching (e-BRS). Figure 2.9 (b) showed the retention of 10^4 sec at 85℃ for LRS and HRS without deterioration. This stable retention can be useful for the multi-level device, which requires stable retention to prevent from overlap between the states.

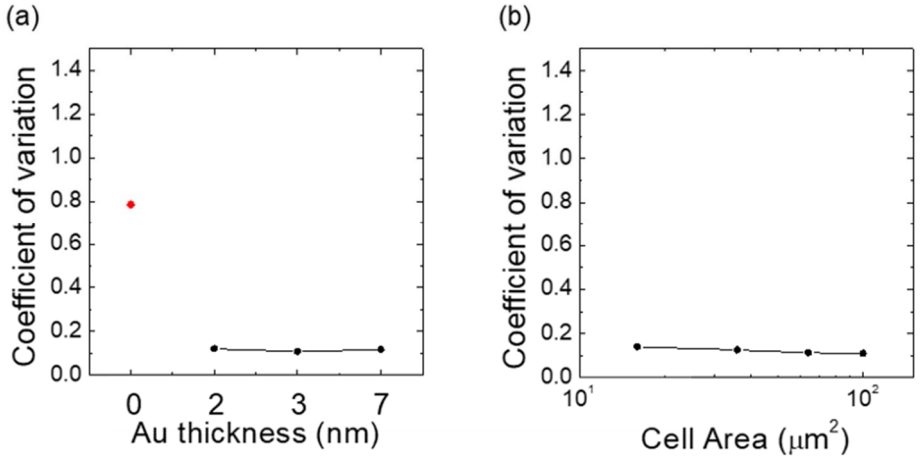

Figure 2.8 Coefficient of variation graph with (a) different Au thickness (b) cell area to confirm the degree of switching uniformity improvement

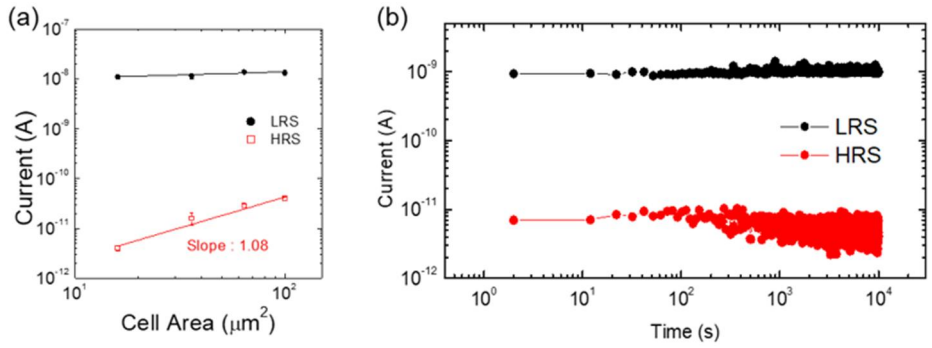

Figure 2.9 (a) Area dependency of current at 7 V for HRS, and LRS of $Pt/Ta_2O_5/HfO_2/TiN$ device (b) retention data of the LRS and HRS at 85℃ (measured at 6V)

DC sweep mode was also included to check the stability of the cyclic operation. Figure 2.10(a) showed the shape of the switching was largely changed for the non-Au NDs cell after 100 cycles. After 400 cycles, switching failure was happened, and total breakdown of the cell prevented from the further operation. In contrast, Au NDs inserted device showed stable switching behavior even after the 1000 operation cycles without having the distribution in operation voltage. In order to understand this significant improvement,

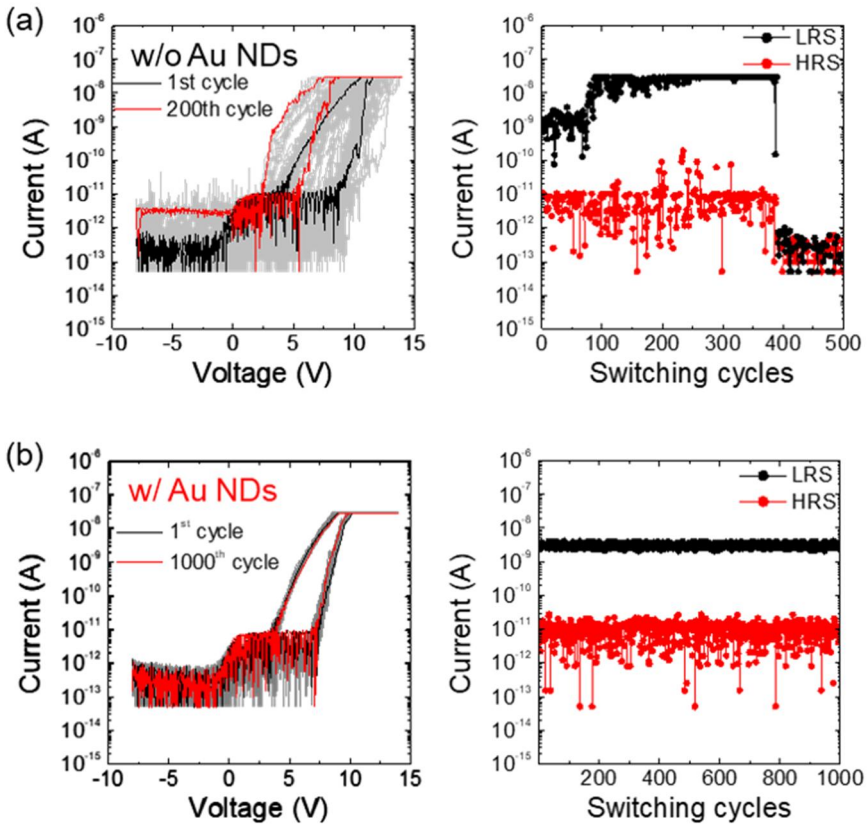

Figure 2.10 More than 1000 cycles endurance test of the device (a) without Au NDs (b) with Au NDs

COMSOL simulation was used to check the electric field concentration. In Figure 2.11(a), Ta_2O_5 and HfO_2 have 25 and 18 dielectric constants, so HfO_2 has higher electric field than Ta_2O_5. The right side of the graph was the line profile extracted from the left simulation data of the electric field located at the black line in HfO_2 thin film. This black line had many trap sites and was expected to be a switching area. In the simulation, the location of the black line was -1 nm away from the interface. In figure 2.11(b), simulation results for the Au NDs inserted cell were shown. The size, shape, and distribution of Au NDs were defined based on the Figure 2.4 HRTEM image for the simulation. Similar to Figure 2.11(a), electric field value at the line profile for the same area was measured, and concentrated electric field occured at the bottom of Au NDs. Figure 2.12 showed the simulation based on the different size and distribution of Au NDs. Figure 2.12 (a), (b), and (c) showed the cases for the size of 2 nm, 3 nm, 7 nm of Au thin film. The lower electric field for the inserted Au-NDs device than planar device was observed in simulation results of Figure 2.11(b). In Figure 2.12, the lower electric filed region than the reference value was labeled in white color to emphasize the electric field concentration.

In Figure 2.12(d), electric field based on size and distribution was shown. As the size of Au NDs increased, the electric field concentration effect was minimized. The reason for this was that the curvature of the dot was reduced as the size of the dot increases, but NDs inserted devices had higher electric field than the reference value marked in red line, which proved the electric field concentration effect.

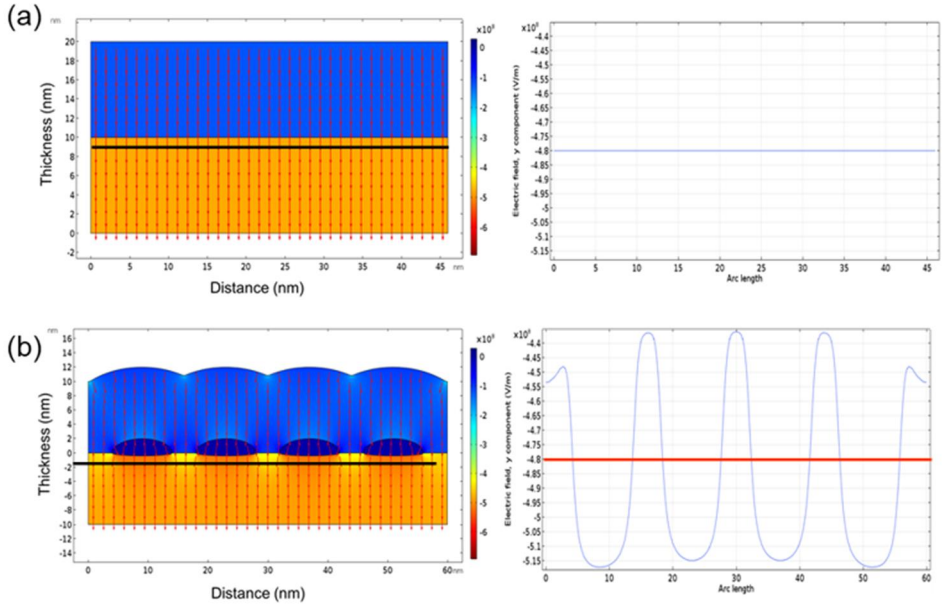

Figure 2.11 COMSOL simulations showing the electric field distribution (a) without Au ND and (b) with Au NDs inserted at the interface between Ta_2O_5 and HfO_2 layers.

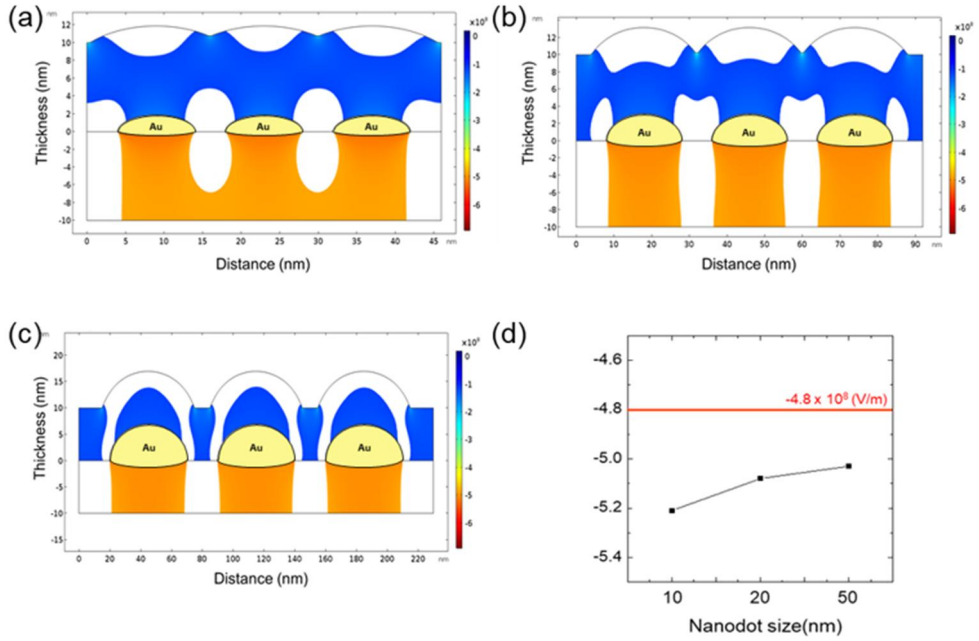

Figure 2.12 COMSOL simulations showing the electric field distribution with different size of Au NDs (a) 10 nm, (b) 20 nm, (c) 50 nm, (d) electric field graph of Au NDs with different size and red line shows electric field of the device without Au NDs.

In order to experimentally prove this, CAFM analysis was used. Figure 2.13 (a), (b), and (c) show 2D topo-image, 3D topo-image, 3D current-mapping image of the non-inserted NDs device, respectively. Figure 2.13 (d), (e), and (f) were for the inserted NDs device. The non-inserted NDs device had a planar surface, and current cannot pass the device. For the inserted NDs device, Au NDs could be verified using the topo-image, and high current level was observed around the NDs location from the current-mapping image. Also, there was no area dependency in contrary to the aforementioned cell area dependency results. From the CAFM results, the localized switching happened around NDs, which improved distribution of the operation. Then, this improvement enabled to develop the multi-level switching as shown in Figure 2.14. By controlling the compliance current from 30 nA to 7 μA, the number of electrons filled in the trap site at LRS current level could be controlled to make the multi-level switching. From each compliance current, 50 repetitive cycle had been conducted, and its result was shown in Figure 2.14(a). Making 8 different non-overlapping states except the off state, more than 3-bit multi-level was possible. In Figure 2.14(b), the result showed that multi-level switching was even possible for broader read voltage from 6.5 V to 8 V.

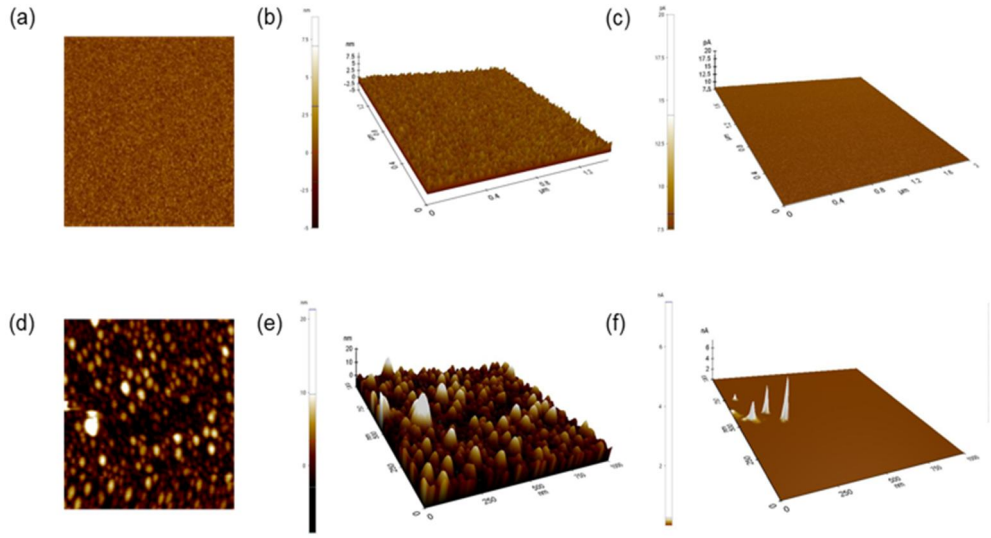

Figure 2.13 AFM (a) 2D topography and (b) 3D topography image of the device without Au NDs. (c) The CAFM current image of the device without Au NDs. AFM (d) 2D topography and (e) 3D topography image of the device with Au NDs inserted at the interface between Ta_2O_5 and HfO_2 layers. (f) The CAFM current image with Au NDs inserted at the interface between Ta_2O_5 and HfO_2 layers.

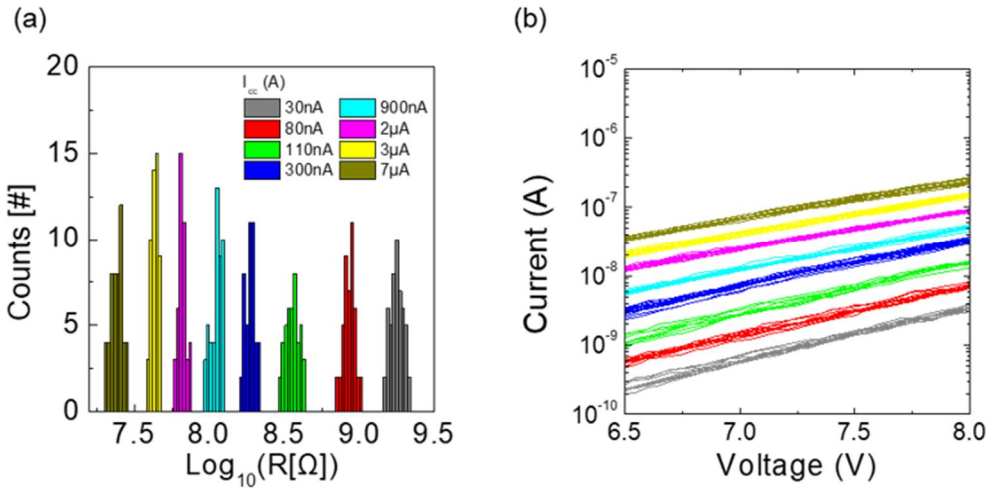

Figure 2.14 (a) Distribution of the eight levels without off-state that included on-states induced by changing the compliance current from 30 nA to 7 μA (b) Distribution of resistance values of discrete eight on-states at the region of read voltage between 6.5 and 8 V.

2.4. Summary

In summary, it was elucidated that the insertion of Au NDs in Pt/Ta_2O_5/HfO_2/TiN improved resistive switching uniformity. Previous device without Au NDs also showed electroforming-free, self-rectifying switching but had variation problem caused by principle of operation. As mentioned above, bi-layered dielectric structure, where HfO_2 works as the resistance switching layer by trapping and de-trapping the deep trap site while Ta_2O_5 created Schottky barrier with Pt which has high work function. In addition, when Ta_2O_5 was deposited on the HfO_2, its plasma created the deep trap states, which acted as a conducting path. Deoxidation effect due to plasma made the HfO_2 had enough density of oxygen vacancies to induce the fluent resistive switching within the layer. Therefore, Au NDs were inserted at the interface of HfO_2 and Ta_2O_5, which are switching layers. The Au NDs assisted the conducting path and improved the memory switching due to the electric field concentration effect. Compared to a device without Au NDs, various switching characteristics such as retention, endurance as well as switching uniformity were improved.

3. Effect of electric field concentration depending on the location of Au nanodots in the device

3.1. Introduction

Resistive random access memory (ReRAM) has become one of the most promising device candidates for future computing applications[35], such as analog[36], neuromorphic computing[37,38], bio-mimicking emulator[39], and next-generation nonvolatile memory[19,40–42]. Although many different types of resistive switching (RS) devices have been suggested so far for device-level demonstration of such applications in labs, large-scale demonstrations have not been achieved so far. One of the major hurdles is the lack of device that could be operated at low power and has extremely uniform RS behavior with self-nonlinearity. One of the most popular types of RS device is the ionic motion-based filamentary type RS device with oxides, where either oxygen vacancies (ex> valence change memory) or highly mobile cations (ex> electrochemical metallization cell) serve as the mobile species for switching. In such type devices, the electroforming process is necessarily required in most cases to construct RS inducible condition with a relatively higher voltage for subsequent switching. Unfortunately, this high voltage and the current process often induce damage to the selector device in 1-selector-1-RS device (1S1R) configuration for large scale array and imposes a heavy burden on the operation circuit[43–45]. Also, this process is responsible for substantial device-to-device variance due to its random nature of filament formation. After the electroforming process, either oxygen vacancy

percolation paths or metal (Ag or Cu) conducting bridges are formed in the shape of a continuous filament that connects the top and bottom electrode, exhibiting high current (> μA) low resistance state (LRS)[33,46,47]. Recently, as a solution to such crucial problems, Yoon et al. suggested electron motion-based electroforming-free and self-rectifying RS device in the Pt/Ta_2O_5/HfO_{2-x}/Ti, TiN structure which could be operated at low power[31,48]. Here, the entire switching operations were responsible for the trapping/de-trapping of electrons in the pre-conditioned traps in the HfO_{2-x} layer. While repeated switching, Pt/Ta_2O_5 interface Schottky barrier remained intact, giving a rectification functionality. The current conduction in the LRS follows the Poole-Frenkel conduction through distant shallow traps having around 0.7eV trap depth, exhibiting very low current (< μA) LRS. However, as the operation current decreases, the distribution of current levels of the LRS became vary a lot. Therefore, this device, even though very useful for many applications, still need improvement for achieving extremely uniformity even in operation under μA current range.

In this work, we demonstrated that more uniform RS behaviors were induced when Au NDs were formed not only at the interface between Ta_2O_5 and HfO_2 but also within each layer. From this result, it was more feasible to understand the switching mechanism of the device precisely and COMSOL simulation was performed to verify the induced field concentration depending on the location of the inserted Au NDs. When the ND location became remote from the interface, the positive influence became weaker and eventually disappeared when they located at positions > 2 nm

from the interface, where the distance effect was more serious when the NDs were inside the HfO_2 layer than the Ta_2O_5 layer.

Metal NDs in oxide thin film have been reported so far; Hota et al[49]. found an improvement in endurance by inserting Au NDs in Nb_2O_5, and Chang et al.[50] reported that switching uniformity is also improved by inserting Pt NDs in the TiO_2 switching layer. Many papers reported the improvement in uniformity by controlling a formation and rupture of the CFs with the insertion of NDs, but there is an important missing spot, mechanism, and analysis of the improvement in the sense of NDs[51]. Moreover, some of the reported methods have issues in the treatment of the heat by oxidizing the electrode and crystallizing the oxide layer. To address and minimize these issues, the reported method in this study does not include the separate heat treatment process and use AAO plate fabrication and etch process[52] or dip-pen[53] to form Au NDs.

3.2. Experimental

The Au embedded device was fabricated by depositing 50nm thick TiN Bottom Electrode(BE) on Si/SiO_2 substrate, 10nm thick HfO_2 switching layer, 10nm Ta_2O_5 and 50nm thick Pt Top Electrode(TE), in sequence. The TE and BE were patterned into a cross-point structure. TiN BE was deposited by the reactive sputtering technique using a commercial sputtering tool(Applied Materials, Endura), Ti target with a diameter of 4 inches was used with 20 sccm of Ar gas and 3 sccm of N_2 gas. The RF power and the substrate temperature were set to 500 W and room temperature, and the base and operating pressure were ~10^{-7} torr and 1 mtorr, respectively. In order to create pattern for the bottom electrode, following etching processes using Inductively Coupled Plasma (ICP, Oxford, PlasmaPro System100) etcher was done after photolithography. The etching conditions are BCl_3 50 sccm, Cl2 33 sccm, foward power of 250W, and back bias of 1000 W. The HfO_2 layer was formed via thermal atomic layer deposition (ALD), with $Hf[N(CH_3)(C_2H_5)_4$, and O_3 as a Hf precursor and an oxygen source, respectively at a 340 ℃ substrate temperature. The Ta_2O_5 layer was deposited in another shower-head-type ALD reactor using tert-butylimido-bis(diethylamido)cyclopentadienyl)tantalum and H_2O-activated plasma (300W) as the Ta precursor and oxygen source, respectively, the wafer temperature during the deposition was set to 200 ℃. The substrate temperature was set room temperature, and the base and operating pressure were ~10^{-7} torr. The I-V characteristics were measured using an HP4145B semiconductor parameter analyzer.

During the measurement, the Pt TE was biased, and the TiN BE was grounded. The electric field concentration simulation data at each sample was obtained by COMSOL.

3.3. Results and Discussions

The cross-section transmission electron microscopy (TEM) images of the Pt/Ta_2O_5/HfO_2/Au NDs/HfO_2/TiN structure were shown in Figure 3.1 (a). The figure showed a well-distinguishable layer structure with a crystallized monoclinic HfO_2 layer, confirmed by the fast-Fourier-transformed image of the crystalline lattice fringes, and an amorphous Ta_2O_5 layer structure. The inset image located at upper left side showed the crystal structure of HfO_2 deposited on the bottom electrode of TiN layer, while right side showed the crystal structure of HfO_2 deposited on top of the Au NDs. After fast-Fourier-transformed image analysis, both of them had same crystal structure of monoclinic HfO_2 layer, thus the factor of crystal structure could be neglected due to the same structure of HfO_2 and could consider only Au NDs effect. The well-distinguished Ta_2O_5/HfO_2/TiN structure was also confirmed by the depth profiling in Auger electron spectroscopy (AES), as shown in Figure 3.1 (b). The existence of the Au NDs inside HfO_2 can also be verified using AES analysis.

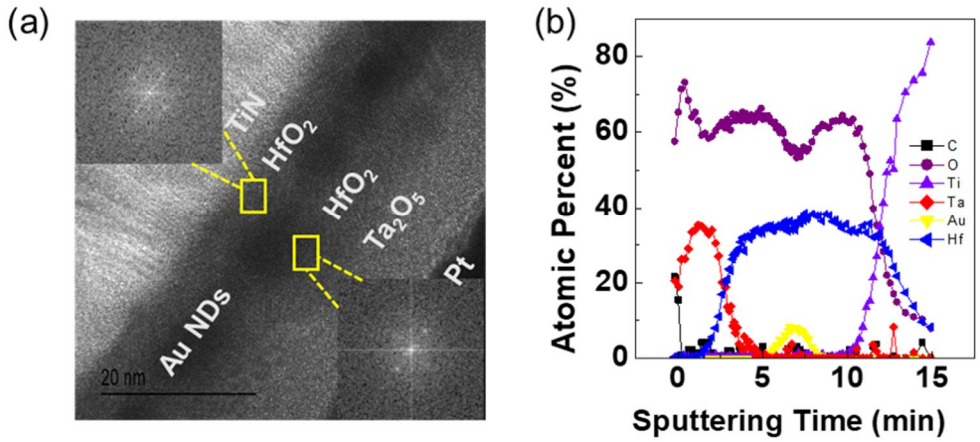

Figure 3.1 (a) Cross-sectional TEM images of the device embedded Au NDs in the HfO_2 layer. Fast-Fourier transformed images of the HfO_2 layer on TiN(upper left inset of figure(b)) and Au NDs(lower right inset of figure(a)) (b) depth profile AES data of the device with Au NDs inserted in the HfO_2.

Note that the insertion location of Au NDs is inside of the Ta_2O_5, not interface, which could be seen as schematic diagram in Figure 3.2 (a). The method to insert Au NDs was as follows: deposit partial fraction of Ta_2O_5, insert Au NDs, and then deposit Ta_2O_5 again. The total thickness was set to be 10 nm. Figure 3.2 (b), (c), (d), (e), and (f) represented electrical characteristic of the insertion location at different distances from the Ta_2O_5 interface, 2nm, 5nm, 6nm, 7nm, and 8nm, respectively. Each measurement was repeated for 20 cycles, and their results were shown in Figure 3.2(b) and 3.2(c) showing the operation distribution was repeated as well. Also, comparing with Figure 3.2(b) and 3.2(c), the operation voltage was reduced in Figure 3.2(b), so current level was increased at low voltage. Note that the operation voltage distribution happened again in Figure 3.2 (d), (e), and (f). For the non-Au NDs samples of $Pt/Ta_2O_5/HfO_2/TiN$, the layer of Ta_2O_5 only acted as Schottky barrier between Pt without contributing to switching characteristic. If this theory was correct, it was expected to have no effect on the switching characteristic depending Au NDs inserted location, but the experimental result was different that the location affects the operation distribution as in Figure 3.2 (b), (c). Not only NDs were inserted into Ta_2O_5 but also it was inserted into HfO_2, which is shown in Figure 3.3 (a). The method to insert Au NDs into Ta_2O_5 was same as the previous method. Figure 3.3 (b)-(g) were electrical characteristics when Au NDs were located at 1~5 nm away from the interface. For Figure 3.3(b), it showed the improvement in operation variation, and Figure 3.3(c) showed a slight improvement, but some variations were existed. Figure 3.3 (e)-(g) now had variations, much bigger than the non-Au NDs devices.

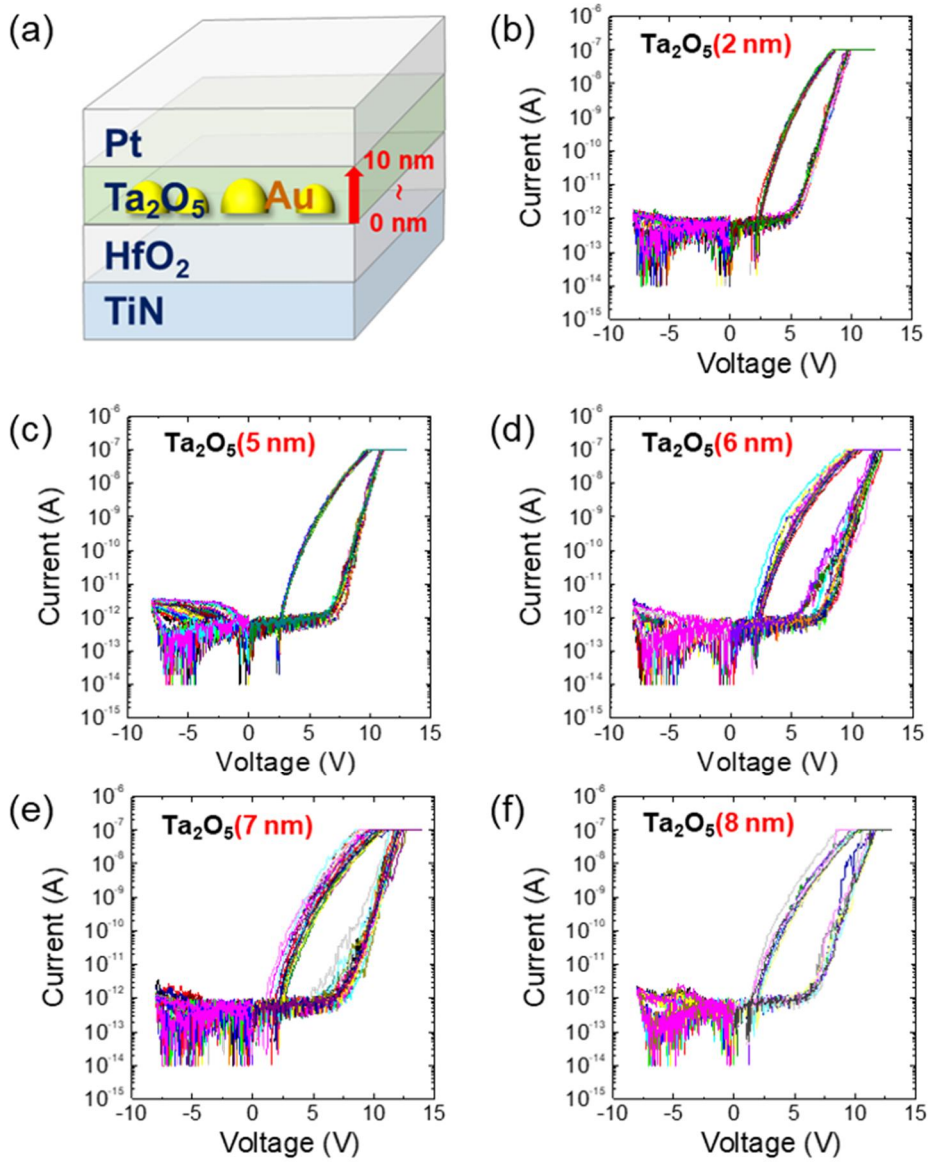

Figure 3.2 (a)Schematic of the device stack with Au NDs in Ta_2O_5 thin film. The degree of uniformity improvement where Au NDs is located at 0 to 10 nm from the interface between HfO_2 and Ta_2O_5 thin film (b) 2 nm, (c) 5 nm, (d) 6 nm, (e) 7 nm, (f) 8 nm.

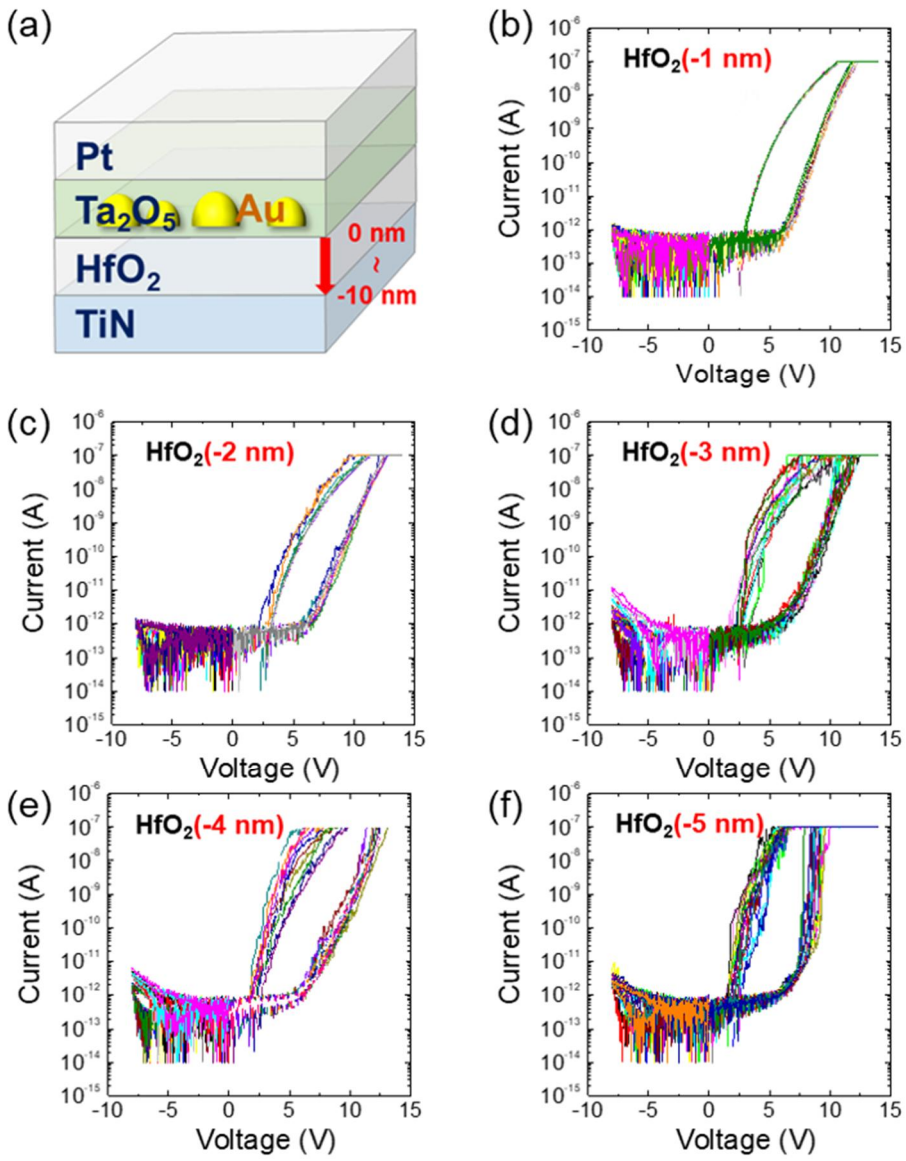

Figure 3.3 (a)Schematic of the device stack with Au NDs in HfO_2 thin film. The degree of uniformity improvement where Au NDs is located at 0 to -10 nm from the interface between HfO_2 and Ta_2O_5 thin film (b) -1 nm, (c) -2 nm, (d) -3 nm, (e) -4 nm, (f)- 5 nm.

Figure 3.4 was cumulative probability of the improvement by insertion of Au NDs. In Figure 3.4(a), the devices 2 nm and 5 nm away from interface had very narrow current level and significantly improved operation variation, whereas non-Au NDs device had large variation. This improvement effect was less significant for HRS state which was possibly due to noises in low current level. In Figure 3.4(b), devices 6 nm, 7 nm, and 8 nm away from interface had no difference whether it was LRS or HRS compared to Au NDs inserted device. For the case with HfO_2 inserted with Au NDs, cumulative probability of improvement was shown in Figure 3.5. In Figure 3.5(a), devices 1 nm and 2 nm away from the interface had significant improvement compared to non-inserted devices. Between HRS and LRS, LRS had higher tendency to the effect as in Ta_2O_5. Figure 3.5(b) showed the devices 3 nm, 4 nm, and 5 nm away from the interface, which had an almost similar variation as non-inserted Au NDs. From this, its condition was not affected by Au NDs.

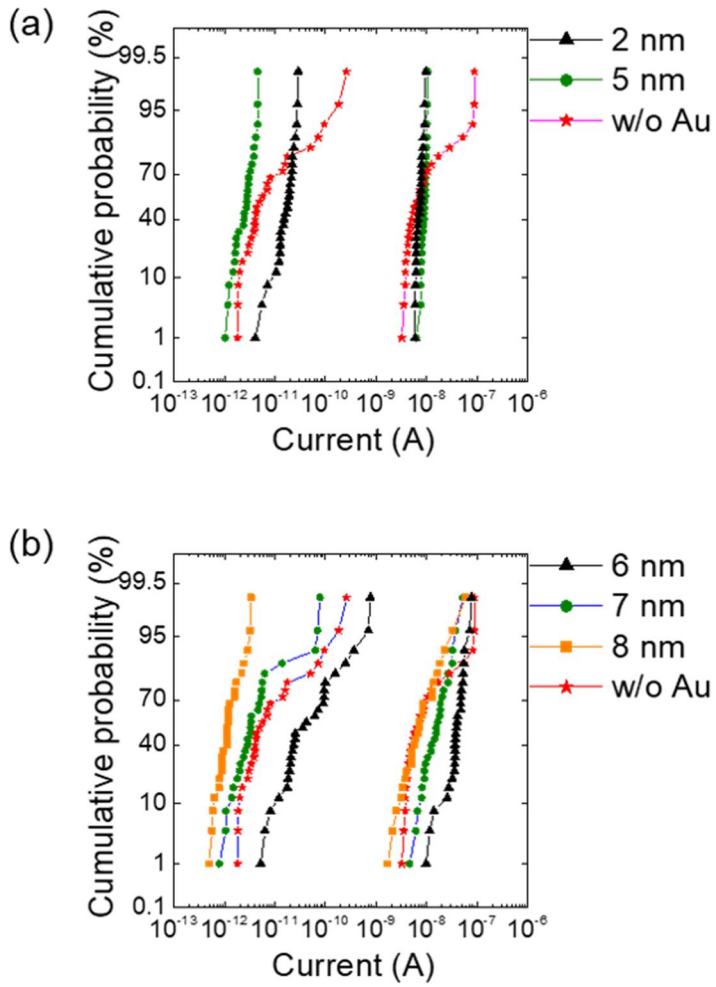

Figure 3.4 Cumulative probability of the current levels of the LRS and HRS of the multiple devices (a) 2 nm, 5 nm and (b) 6 nm, 7 nm, 8 nm away from the interface.

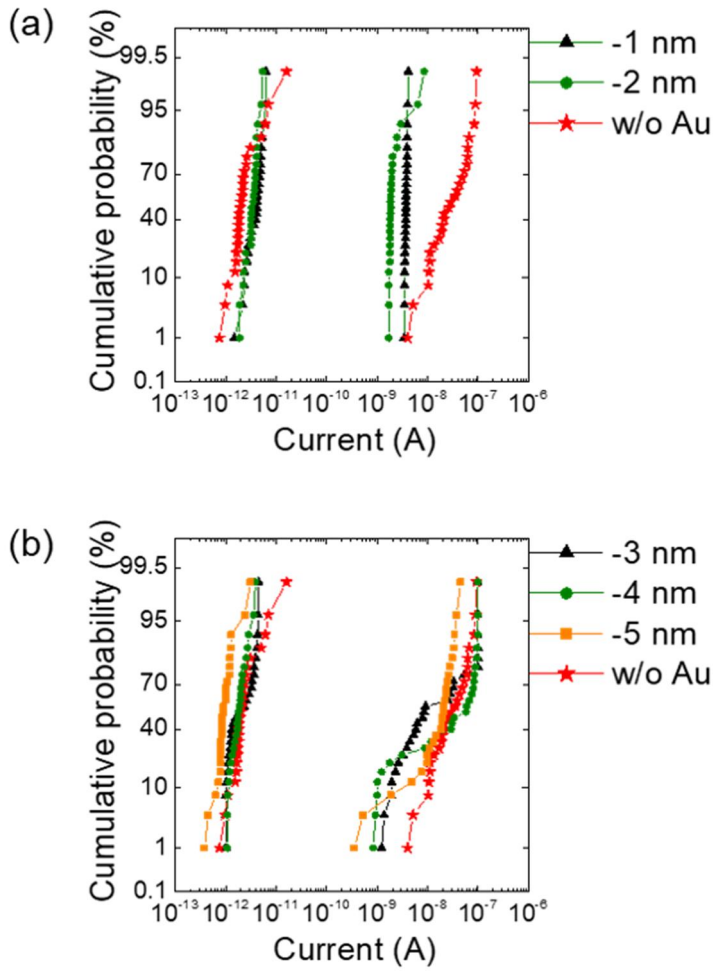

Figure 3.5 Cumulative probability of the current levels of the LRS and HRS of the multiple devices (a) -1 nm, -2 nm and (b) -3 nm, -4 nm, -5 nm away from the interface.

Those extents of operation improvement were summarized in Figure 3.6. In order to analytically measure improvement in variation by Au NDs, coefficient of variation was defined. Au NDs located near the interface (ND position = 0) had small coefficient of variation, which means the operation variation was improved. On the other hand, as the location was far away from the interface, coefficient of variation was increased, and improvement in variation was negligible. The distance where the improvement disappear could be defined as effective distance, and this was different for Ta_2O_5 and HfO_2, 2 nm and 6 nm, respectively. Considering dielectric constant only, HfO_2 with relatively low dielectric constant had more field concentration effect. Therefore, it was expected to be that HfO_2 should have more effective distant, but the actual result was different from this. To understand this, COMSOL simulation tool was used to variation in electric field depending on the location of the inserted Au NDs.

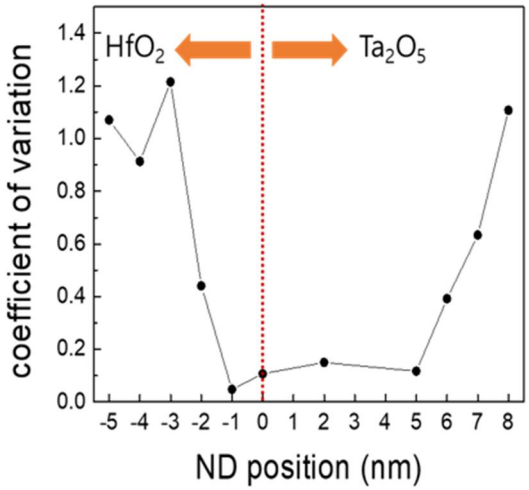

Figure 3.6 Coefficient of variation graph depending on the position of Au NDs in HfO_2, Ta_2O_5 thin films

Figure 3.7 was result of the COMSOL simulation when Au NDs are inserted in Ta_2O_5. Figure 3.7 (a)-(f) was the result when Au NDs were inserted in different location 1-6 nm away from the interface. Other than the position of the NDs, other conditions were fix on the simulation tool. To emphasize the electric field concentrated region, region where smaller value compared to non-Au NDs was marked as white color. The result showed that highest electric field happened below the Au NDs in HfO_2 and near the interface. This region was diminished until 5 nm away from interface shown in Figure 3.7(e) and completely disappeared at 6 nm shown in Figure 3.7(f). This simulation tendency matched with the previous experimental data. Figure 3.8 represented COMSOL simulation results when Au NDs were inserted in HfO_2. When Au NDs were inserted at 1 nm away from the interface as in Figure 3.8(a), high electric field was induced between Au NDs and interface. As insertion distance was away from the interface, electric field between interface and Au NDs was lower than the non-inserted device marked by white color in Figure 3.8(b), (c), and (d). From this result, Au NDs inside HfO_2 only affected within the distance of 1 nm from interface and had no effect above its distance.

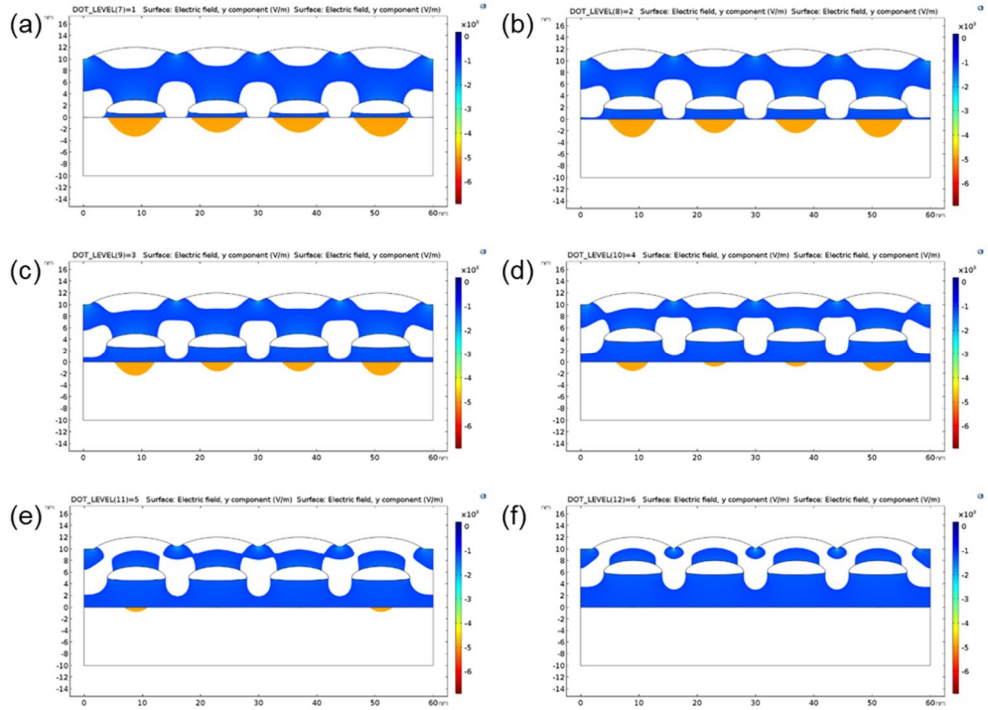

Figure 3.7 COMSOL simulations showing the electric field distribution with different Au NDs embedded position in Ta_2O_5 thin film (a) 1 nm, (b) 2 nm, (c) 3 nm, (d) 4 nm, (e) 5 nm, (f) 6nm.

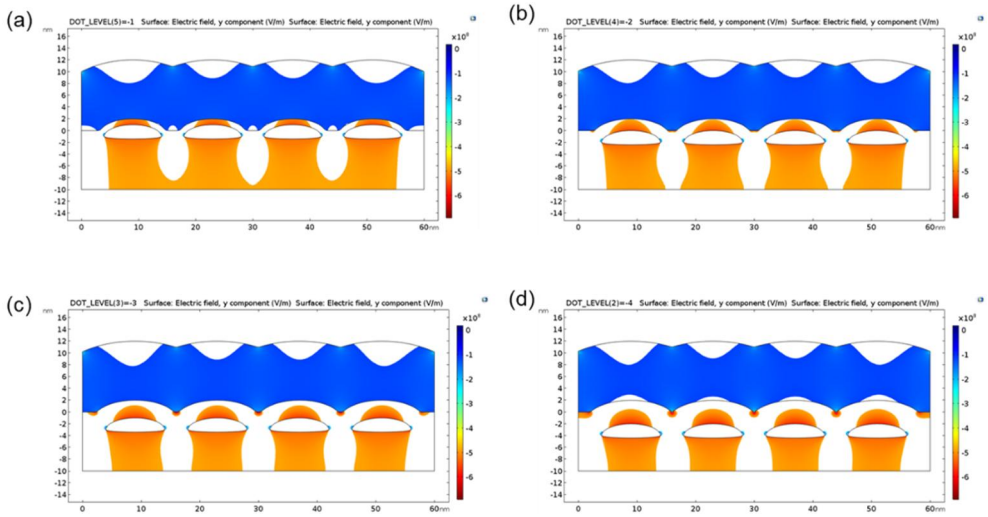

Figure 3.8 COMSOL simulations showing the electric field distribution with different Au NDs embedded position in HfO_2 thin film (a) -1 nm, (b) -2 nm, (c) -3 nm, (d) -4 nm.

Figure 3.9(a) showed the electric field when Au NDs were inserted at the 1 nm distance away from HfO_2 interface, which was considered as switching area in previous research results. Figure 3.9(b) showed maximum electric field. Figure 3.9(c) represented the result depending on the inserted locations of Au NDs. These results were analogous to the simulation results based on the interface electric field, whereas the results showed larger electric field happens as further away from the interface but not affect the operation variation in the case of maximum field. This was because of the non-switching area. In conclusion, Au NDs only affected at the location near the interface due to many trap sites.

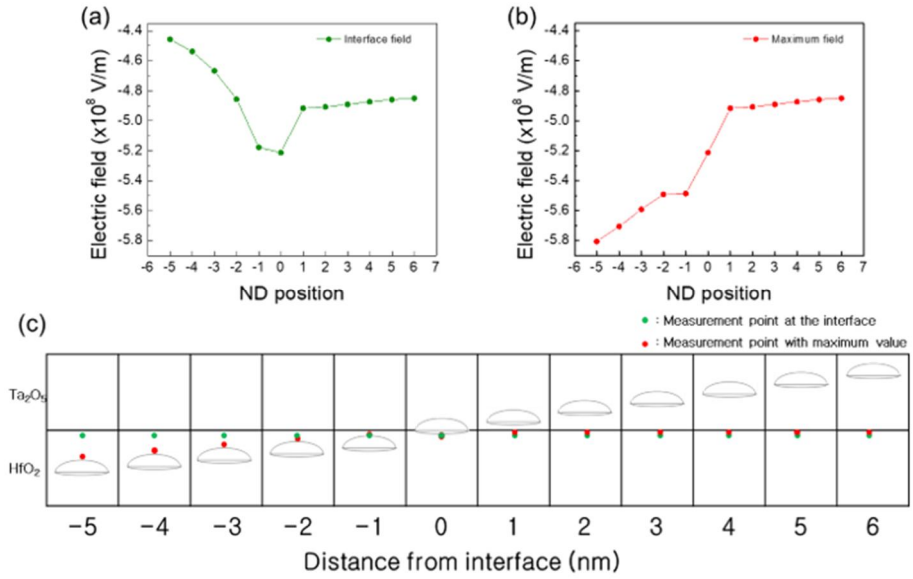

Figure 3.9 (a) Electric field (a) measured at the interface and (b) measured with maximum value graph of the device embedded Au NDs with different position.

3.4. Summary

In conclusion, the device was fabricated with different insertion positions in order to confirm the role of Au NDs in the device. The method to insert Au NDs in HfO_2 thin film was deposition partial fraction of HfO_2, insert Au NDs, and then deposit HfO_2 again. The total thickness was set to be 10 nm. Au NDs were also inserted in Ta_2O_5 thin film in the same process. The electrical properties of Au NDs in each thin film were analyzed. As a result, it was confirmed that switching characteristics were improved not only when Au NDs were inserted into the interface, but also when inserted into each thin film. Ta_2O_5 was well known for non-resistive switching layer and diode-like rectifying behavior from the Schottky barrier between high work function of Pt. Therefore, insertion of the Au nanodots might not affect this switching behavior. Switching behavior in Ta_2O_5, however, was improved after insertion of the Au nanodots. This unexpected behavior was confirmed through COMSOL simulation that if the location of the Au nanodots was sufficiently away from the interface, its improvement of the endurance was faded out along with the weaker field concentration effect. As a result, this experimentally confirms that the switching behavior was occurred at the interface.

4. Quantification of Au nanodots in the nanoscale devices

4.1. Introduction

RRAM has properties of scaling-down potential, lower operation power consumption, simple structure, and cost effective fabrication, which get attention to replace NAND-flash memory for future non-volatile memory[54]. It has good electrical characteristics compared to flash memory such as endurance of more than 10^{12} cycles[36], fast operation speed of ns[20,55], low operation voltage of 2~3 V[56,57]. Even those good sides compared to NAND flash memory[58,59], the reason for not being commercialized is the stability[60,61]. In order to develop high density memory, the circuit has to be in the shape of crossbar array[12,62]. Since RRAM has a property of operation variation, this makes difficult to construct the circuits, and set/reset failure can be occurred. Many researches are ongoing to solve the problem such as Au[63] and N[64] doing in the perspective of defect engineering to improve the unstable operation principle. Misha et al. reported N-doping on Ta/TaO_x/Pt structure can improve switching uniformity significantly[65]. According to the result, the role of the N in insulator layer limits the oxygen migration and creates local conductive filament to improve device operation. Similarly, another way to improve the operation is insertion of the metal NDs such as Ru, Pt, and Au into TiO_2, IrO_x and, Nb_2O_5[31,50,66,67]. There are many ways to deposit metal NDs. NDs can be created by controlling the conditions of ALD deposition to prevent thin film formation. Also, porous AAO template can be used as a layer of the NDs[31,68,69]. At last, NDs can be created by the

dip-pen shattering method[70,71]. Those inserted NDs have a role to reduce set/reset voltage by electric field concentration effect[72], or to increase stability by limiting CF formation to the local region[73,74]. In addition, it can increase trapping ability as the flash memory[75]. Despite some improvements from the previous methods, they were just improvement in a single device, not device-to-device perspective. So, the biggest problem is that each device has different property along with the variation. The main reason to device-to-device variation is that uncontrollable fabrication process of metal NDs in size and distribution. The different size and distribution are main source to create the distribution in electrical properties of the cells even inserted with metal NDs. As a result, in order to mitigate the device-to-device variation, the size and distribution of metal NDs must be same. In this paper, the research was about the uniform size and distribution of metal NDs through patterning by e-beam lithography and metal lift-off process.

4.2. Experimental

The Au embedded device was fabricated by depositing 50nm thick TiN Bottom Electrode(BE) on Si/SiO2 substrate, 3nm thick HfO_2 switching layer, 3nm Ta_2O_5, in sequence. TiN BE was deposited by the reactive sputtering technique using a commercial sputtering tool(Applied Materials, Endura), Ti target with a diameter of 4 inches was used with 20 sccm of Ar gas and 3 sccm of N_2 gas. The RF power and the substrate temperature were set to 500 W and room temperature, and the base and operating pressure were ~10^{-7} torr and 1 mtorr, respectively. The HfO_2 layer was formed via thermal atomic layer deposition (ALD), with $Hf[N(CH_3)(C_2H_5)_4$, and O_3 as a Hf precursor and an oxygen source, respectively at a 340 ℃ substrate temperature. The Ta_2O_5 layer was deposited in another shower-head-type ALD reactor using tert-butylimido-bis(diethylamido)cyclopentadienyl)tantalum and H_2O-activated plasma (300W) as the Ta precursor and oxygen source, respectively, the wafer temperature during the deposition was set to 200 ℃. Au NDs were inserted by using E-beam lithography(JEOL, JBX-6300FS) process. 100 kV of accelerating voltage was used to minimize proximity effect. The gun type and beam shape were set thermal field emitter and gaussian beam. Also two types of resist(ZEP-520A, PMMA) were used to control verical profile. Scanning electron microscopy (SEM, Hitachi, S-4800) and atomic force microscopy (AFM, Parksystems, NX10) were used to observe the morphology of the Au thin film and Au NDs. Conductive atomic force microscopy (C-AFM, Parksystems, NX10) mode was also used to check current mapping. During

the analysis, the During the measurement, the cantilever was biased, and the TiN BE was grounded.

4.3. Results and Discussion

Fabrication methods of Au NDs in part 2,3 could form Au NDs quickly but has limitation to control size and distribution of dots. To solve this problem, the device was patterned by e-beam lithography, and following lift off process was used after Au was deposited. The fabrication schematic diagram was shown in Figure 4.1. First, high resolution positive tone e-beam resist known as ZEP-520A was used on the substrate with spin coater. The reason to use positive tone resist for lift-off process was that E-beam lithography takes longer time. After soft baking, the exposure condition for the equipment was set to be maximum acceleration voltage of 100 kV to increase straightness of the beam and dose of 220 $\mu C/cm^2$ known as clear dose of ZEP-520A. The clear dose means the dose that react all of the thickness of the resist. If its slope is steep, only react above the clear dose, and under the clear dose do not react so that vertical resist slope can be obtained. After develop process and deposition of the metal, the final step of removing resist was used. Figure 4.2(a), however, showed that pattern was getting narrow as e-beam react with the resist and reducing the amount of the dose. Therefore, higher dose amount than the clear dose of 220 $\mu C/cm^2$ for ZEP-520A was required. Figure 4.2(b) represented this inclement of the dose of 300 $\mu C/cm^2$. Due to larger amount of dose, the shape of the pattern had larger compared to Figure 4.2(a) in spite of narrowing shape at the edge. It was important to notice that the final pattern after lift-off process was not narrower than the patterning, rather the side of the residual resist connected with the metal could attach with the original metal pattern and could remove it from the lift-

off process. Therefore, to create more undercut shape at the bottom of ZEP-520A, the dose was increased to be 1200 $\mu C/cm^2$ as shown in Figure 4.2(c). From the result, the patterning at the bottom had broader but hard to see it had undercut shape. Also, the mentioned residual resist problem was still not resolved. In conclusion, increase in dose induced broader patterning with longer exposure time, which was bad patterning way due to accumulation of the charge.

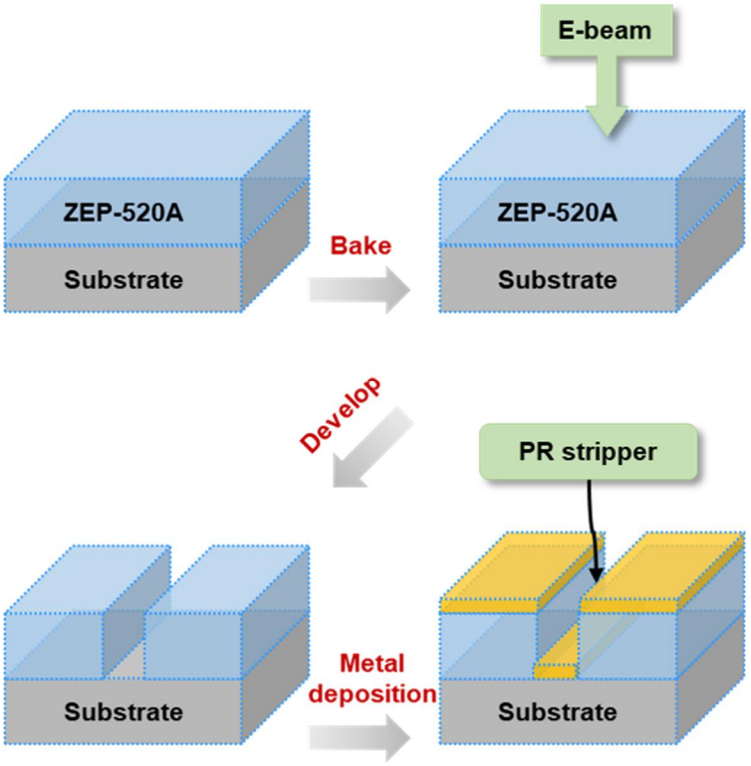

Figure 4.1 A schematic drawing of the e-beam lithography fabrication process using ZEP-520A single layer.

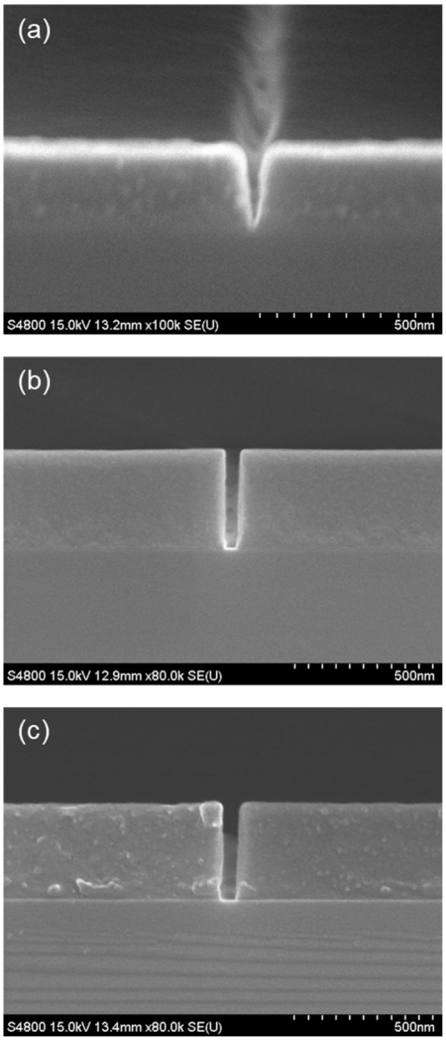

Figure 4.2 SEM images of e-beam exposed with electron beam (a) under clear dose, (b) clear dose, (c) over clear dose at the device on ZEP-520A single layer resist.

So, to form the undercut layer without changing the dose amount, bi-layer deposition was used instead of the single layer, shown in Figure 4.3. The bi-layer was with the previous ZEP-520A resist layer, PMGI layer was firstly deposited before the layer. After the exposure, top of the bi-layer of ZEP-520A will react with the electron beam but PMGI. With this state, wet etching of the PMGI using AZ-300 will has isotropic etch profile and create the undercut as side etching is occurred along with perpendicular direction. As shown in schematic, since there is no connection with the metal, there will be no physical damage when removing residue resist. However, another problem for undercut formation happened as in Figure 4.4. Since wet etching was isotropic etching, which also had direction of side way, nearby cell and current cell had overlapping etch region so that the pattern was destroyed as shown in Figure 4.4(a) and a SEM image of Figure 4.4(b). Especially, ReRAM requires crossbar array (CBA) structure, which has smaller pattern size over time. Therefore, wet etching process is not suitable to apply in CBA in future.

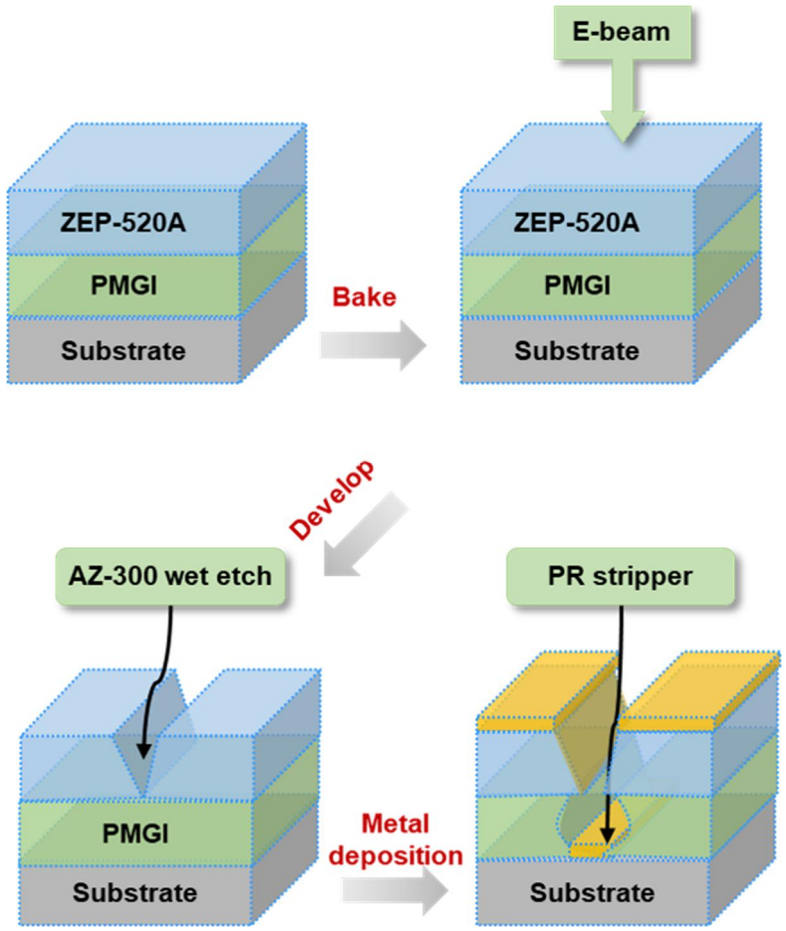

Figure 4.3 A schematic drawing of the e-beam lithography fabrication process using PMGI and ZEP-520A bi-layer.

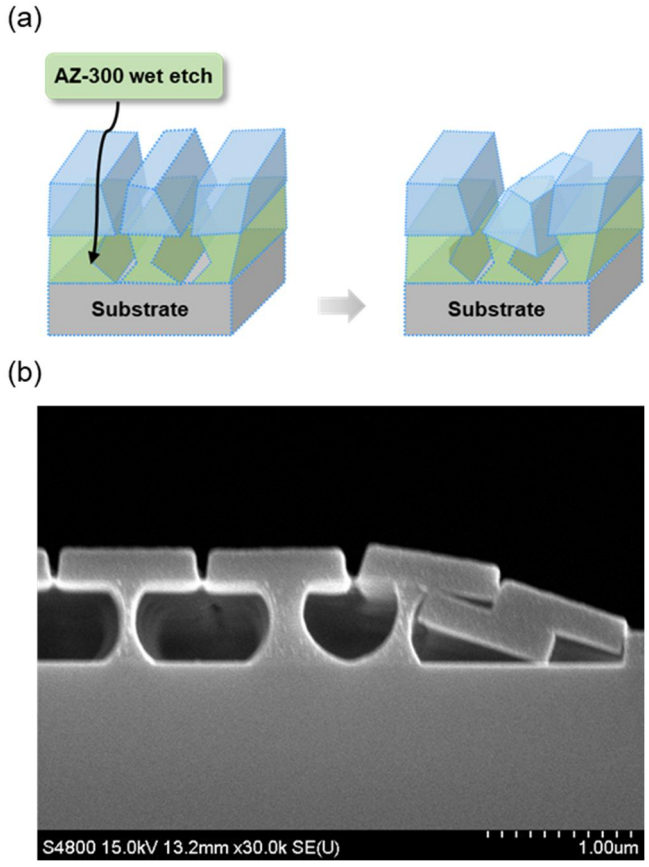

Figure 4.4 (a) A schematic drawing of the PMGI and ZEP-520A bi-layer to expose patterns located closely (b) SEM analysis result in the pattern of the crossbar array

In order to explore another way to create undercut shape, PMMA along with ZEP-520A was used. Comparing with ZEP-520A, PMMA has less slope. It has disadvantage in resolution due to scattering effect during exposure process, but sensitivity of the electron beam can be modulated by controlling molecular weight. PMMA with high molecular weight has less sensitivity. As molecular weight gets smaller, number of the bonds to break them by electron beam are decreased, so it will have high sensitivity. Likewise, two different PMMA can be stacked as bi-layers by controlling molecular weight can modulate the sensitivity to have the undercut formation. Similar to schematic diagram in Figure 4.5(a), upper region was coated with PMMA having relatively low sensitivity and high molecular weight, whereas lower region has high sensitivity. As a result, the pattern of the lower region had broader and forms the undercut. The results of the patterning using different molecular weight of 950 K PMMA and 495 K PMMA were shown in Figure 4.5(b).

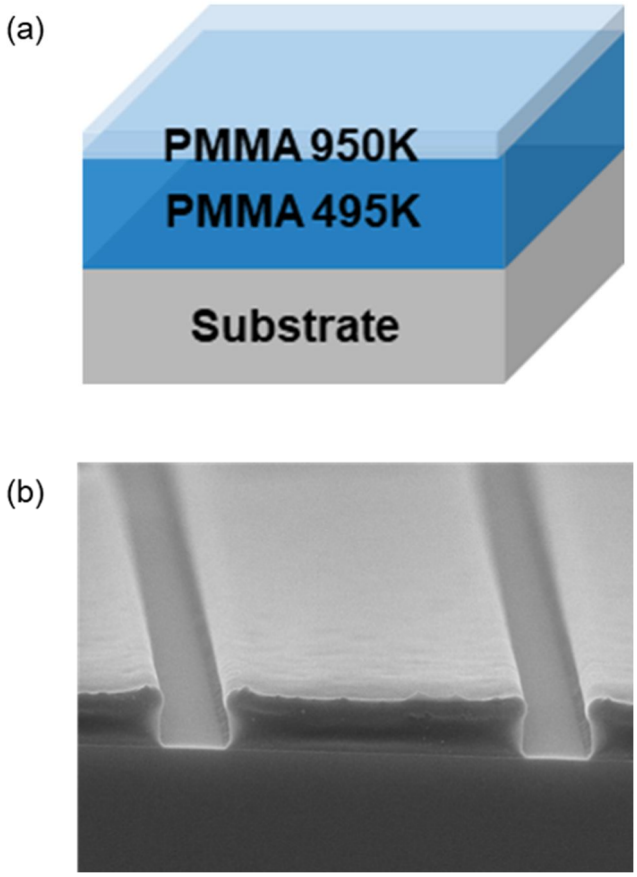

Figure 4.5 (a) Schematic diagram of two types of PMMA bi-layer deposited with different molecular weight. (b) SEM image of device after e-beam exposure.

Thus, using molecular weight control, undercut could be created in a flexible size. Dose test was then conducted to verify whether the patterning could be formed with nearby pattern or not using PMMA bi-layer fabrication. The range of the dose was set to be 700 $\mu C/cm^2$ ~ 1300 $\mu C/cm^2$. As a result, line:space = 1:1 pattern was successfully form at the dose of 1000 $\mu C/cm^2$ as shown in Figure 4.6(a). Beyond the dose, all of the patterns were well formed but the pattern had widening effect as shown in Figure 4.6(b). Comparing with the previous ZEP 520A and PMMA, the pattern of former method did not affect by the increase in the dose, but the inclement in width was observed for the latter method. For example, Figure 4.6(a) and 4.6(b) had width of 50 nm and 60 nm, which was at least 10 nm broader. In Figure 4.7, no pattern damage after the metal lift-off for the minimum pattern size of 50 nm was checked. Figure 4.7(a) was the SEM result of deposition of 3 nm Au layer on 500 nm pattern after the lift-off process with heat treatment inside the chamber. Despite of the very thin layer, patterning was well formed due to undercut formation during the bi-layer fabrication method preventing physical damage. About 20 nm Au nanodots were successfully formed as in part 2. Also, 50 nm size of the pattern using e-beam lithography can be verified using SEM image in Figure 4.7(b). About 20 nm Au NDs were well split into 2~3 NDs without interference. In part 2, about 50 nm nanodots was formed when thickness of Au was set to 7 nm. When the thickness was larger than 7 nm, identical Au NDs size to the its size of the pattern after metal lift-off was observed in Figure 4.7(c).

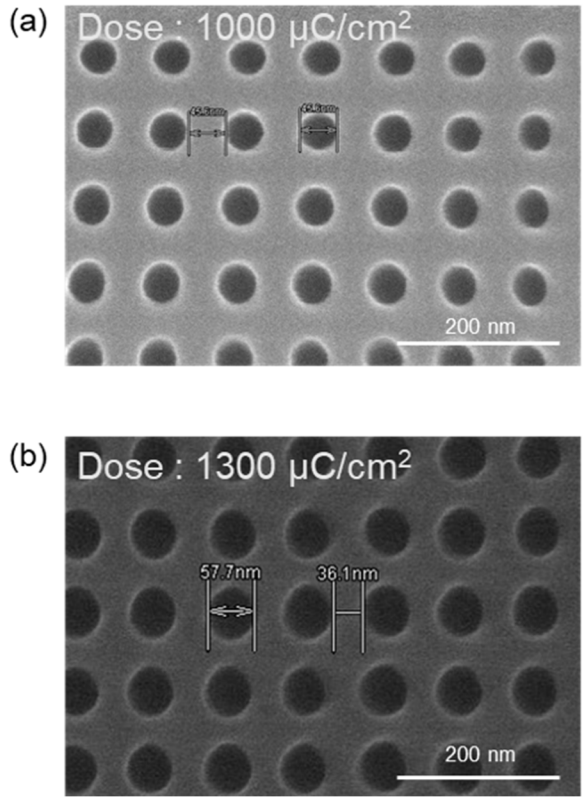

Figure 4.6 Results of different electron beam dose of PMMA bi-layer resist (a) 1000 $\mu C/cm^2$ (b) 1300 $\mu C/cm^2$

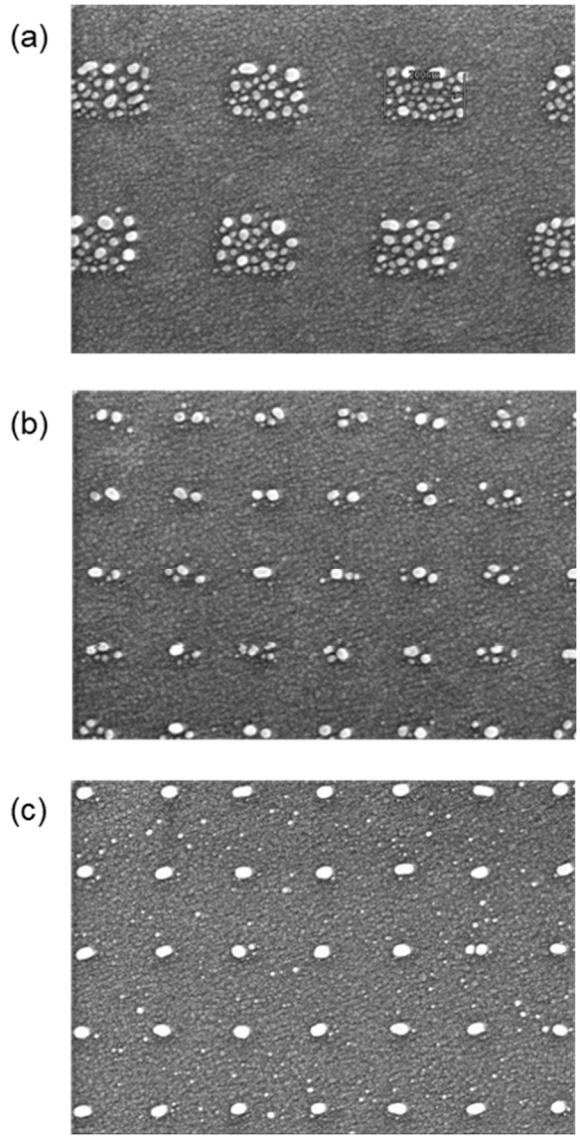

Figure 4.7 SEM images after Au NDs formation of (a) 500nm pattern size and 3nm Au thickness, (b) 50nm pattern size and 3nm Au thickness, (c) 50nm pattern size and 7nm Au thickness

Then, AFM was proceeded for these Au NDs in Figure 4.8(a). SEM image was also added to support that Au NDs were formed in right location as of the patterning. Then, C-AFM was used to see its current mapping in figure 4.8(b). High current flow near the Au NDs was verified as topo analysis in Figure 4.8(a). In this work, from this result, It was confirmed that a small number of NDs were inserted through the E-beam lithography process, and a local switching area could be formed by utilizing a higher current flowing through the NDs.

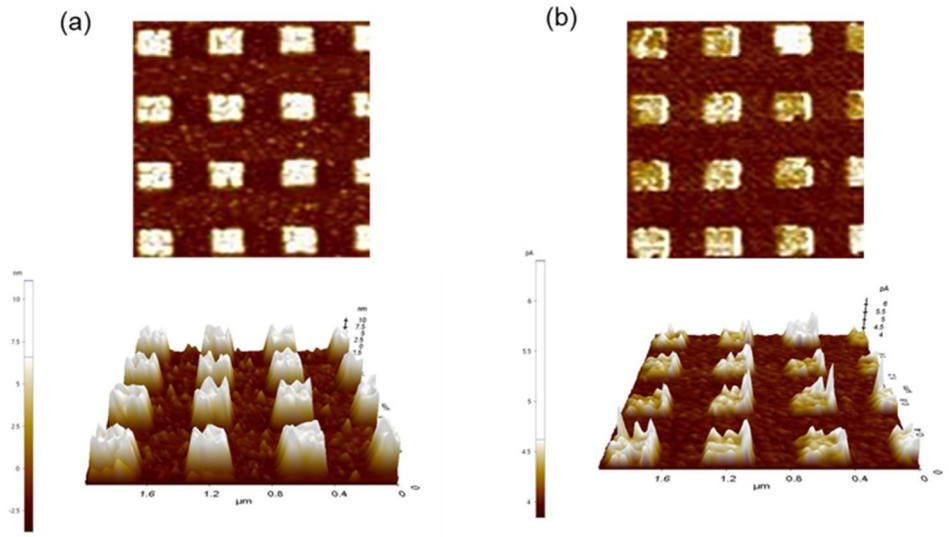

Figure 4.8 (a) AFM 2D and 3D topography image (b) the CAFM current image of the device with quantified Au NDs inserted.

4.4. Summary

In conclusion, a fabrication process method, in order to quantify Au NDs and insert NDs at the correct location, was addressed by using an e-beam lithography method rather than a conventional formation method. There were many methods to deposit nanodots such as AAO, dip-pin methods but those methods could not control the size or distribution of the nanodots since they used the circular shape nanostructure. The Au NDs formed in this way must have a difference in the amount of each device. The distribution of the nanodots is important factor because it could cause the cell-to-cell variation. To control the two factors, e-beam deposition was used. Au nanodots could be fabricated with these steps in order, e-beam exposure, deposition of the Au thin film and subsequent lift-off process. In this process, Au thin film was deposited only 2~3 nm, so adhesion problems can easily occur even with weak force. To achieve the fine size of the Au nanodots, reducing stress to the Au thin film and fine control of the e-beam power were important. Reducing stress could be achieved by controlling side slope of the photoresist (PR) in the exposure process. Two layers of PMMA with different molecular weight were deposited to create undercut slope PR, which reduced stress to the Au thin film. E-beam power was also important, which determined number of electrons emit to the PR layer. Too small of the power caused not enough reaction to create the pattern, whereas too high of the power caused broader pattern of the PR. Therefore, fine control of the power was necessary. As a result, the minimum size of 50 nm Au nanodots could be fabricated. After insertion of the Au nanodots, atomic force microscopy (AFM) was used to confirm locations

of the conductive path on the surface. In the device, the conductive path showed in the nanodots, which confirmed successful induction of the electric field concentration. Therefore, this field concentration around the nanodots showed improvement in the switching properties.

Conclusion

In this dissertation, resistive switching based on the e-BRS mechanism was examined, and the Au NDs were embedded to improve switching uniformity by field concentration effect. For more accurate analysis of the switching mechanism of the device and the field concentration effect, the devices were fabricated by changing the insertion location of nanodots. Furthermore, E-beam lithography process was used to quantify Au NDs and insert NDs at the correct location. The device was fabricated by alignment with the Au NDs of 50nm to the correct position by optimizing the E-beam lithography process conditions and characteristics of resist.

Chapter 2 shows the improvement of resistive switching uniformity by embedded Au NDs. Although many studies have been conducted so far, the problem of stability is the biggest point why RRAM is not commercialized. Stability has various factors such as retention and switching endurance, but among them, the dispersion in repetitive motion remains the biggest problem that cannot be solved. Devices with excellent characteristics such as operation speed, on/off ratio, and low power consumption have been developed, but devices satisfying all the characteristics have not been developed yet. In order to fabricate a device that satisfies all conditions rather than each characteristic, Au NDs were inserted into Pt/Ta_2O_5/HfO_2/TiN devices that had excellent performances(high on/off ratio, forming-free, self-rectifying, etc,).

Bi-layered dielectric structure, where HfO_2 works as the resistance switching layer by trapping and de-trapping the deep trap site while Ta_2O_5 created Schottky barrier with Pt which has high work function. In addition, when Ta_2O_5 was deposited on the

HfO_2, its plasma created the deep trap states, which acted as a conducting path. Deoxidation effect due to plasma made the HfO_2 had enough density of oxygen vacancies to induce the fluent resistive switching within the layer. Therefore, Au NDs were inserted at the interface of HfO_2 and Ta_2O_5, which are switching layers. The Au NDs assisted the conducting path and improved the memory switching due to the electric field concentration effect. Compared to a device without Au NDs, various switching characteristics such as retention, endurance as well as switching uniformity were improved.

Chapter 3 the device was fabricated with different insertion positions in order to confirm the role of Au NDs in the device. Many studies have been published to improve various properties by inserting metal nanodots into devices. The inserted metal nanodots causing various effects in resistive switching, form a part of the conducting path, or cause the effect of electric field concentration. However, there is a lack of accurate analysis why the switching properties are improved. Many studies have been conducted on the filamentary switching mechanism, and accurate analysis such as the difference in the location of the metal nanodots or the degree of field concentration effect has not been conducted. Therefore, in this work, mechanism analysis was performed by inserting Au NDs into each thin film. The method to insert Au NDs in HfO_2 thin film was deposition partial fraction of HfO_2, insert Au NDs, and then deposit HfO_2 again. The total thickness was set to be 10 nm. Au NDs were also inserted in Ta_2O_5 thin film in the same process. The electrical properties of Au NDs in each thin film were analyzed. As a result, it was confirmed that switching

characteristics were improved not only when Au NDs were inserted into the interface, but also when inserted into each thin film. Ta_2O_5 was well known for non-resistive switching layer and diode-like rectifying behavior from the Schottky barrier between high work function of Pt. Therefore, insertion of the Au nanodots might not affect this switching behavior. Switching behavior in Ta_2O_5, however, was improved after insertion of the Au nanodots. This unexpected behavior was confirmed through COMSOL simulation that if the location of the Au nanodots was sufficiently away from the interface, its improvement of the endurance was faded out along with the weaker field concentration effect. As a result, this experimentally confirms that the switching behavior was occurred at the interface.

In Chapter 4, a fabrication process method, in order to quantify Au NDs and insert NDs at the correct location, was addressed by using an e-beam lithography method rather than a conventional formation method. There were many methods to deposit nanodots such as AAO, dip-pin methods but those methods could not control the size or distribution of the nanodots since they used the circular shape nanostructure. The Au NDs formed in this way must have a difference in the amount of each device. The distribution of the nanodots is important factor because it could cause the cell-to-cell variation. To control the two factors, e-beam deposition was used. Au nanodots could be fabricated with these steps in order, e-beam exposure, deposition of the Au thin film and subsequent lift-off process. In this process, Au thin film was deposited only 2~3 nm, so adhesion problems can easily occure even with weak force. To achieve the fine size of the Au nanodots, reducing stress to the Au thin film and fine control

of the e-beam power were important. Reducing stress could be achieved by controlling side slope of the photoresist (PR) in the exposure process. Two layers of PMMA with different molecular weight were deposited to create undercut slope PR, which reduced stress to the Au thin film. E-beam power was also important, which determined number of electrons emit to the PR layer. Too small of the power caused not enough reaction to create the pattern, whereas too high of the power caused broader pattern of the PR. Therefore, fine control of the power was necessary. As a result, the minimum size of 50 nm Au nanodots could be fabricated. After insertion of the Au nanodots, atomic force microscopy (AFM) was used to confirm locations of the conductive path on the surface. In the device, the conductive path showed in the nanodots, which confirmed successful induction of the electric field concentration. Therefore, this field concentration around the nanodots showed improvement in the switching properties.

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List of publications

1. Refereed Journal Articles (SCI)

1.1 Domestic

1.2. International

1. Jung Ho Yoon, Kyung Min Kim, Seul Ji Song, Jun Yeong Seok, Kyung Jean Yoon, Dae Eun Kwon, Tae Hyung Park, **Young Jae Kwon**, Xinglong Shao, and Cheol Seong Hwang* "Pt/Ta_2O_5/HfO_{2-x}/Ti Resistive Switching Memory Competing with Multilevel NAND Flash", Advanced Materials, 25, 27, 3811-3816 (2015).
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2. CONFERENCES

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Abstract (in Korean)

국부화된 영역에서의 전하 트래핑을 통한 균일한 저항변화 메모리 개발

멤리스터는 1971년 추아 교수에 의해 그 개념이 소개 되고, 2008년 휴렛팩커드(HP) 사에서 연구 개발을 발표한 기점으로, 많은 연구가 지속적으로 진행되고 있다. 최근에는 뉴로모픽과 로직, 신경모사들 다양한 분야로의 연구가 진행되고 있는 저항변화메모리는, 금속-절연막-금속의 간단한 구조를 가지며 간단한 공정방법으로 인해 적은 비용으로 제작이 가능하다는 이점 및 크로스바 어레이 구조에서 단위 셀 크기가 $4F^2$로 제작이 가능하다. 여기서 F는 구현 가능한 최소 선폭을 나타낸다. 반면 DRAM, NAND, NOR 플래시메모리는 각각 $6F^2$, $5F^2$, $10F^2$ 의 단위 셀 크기를 갖고 있다. 즉, 멤리스터는 고집적 메모리 소자의 구현에 가장 적합한 소자라고 할 수 있다. 이러한 점에서 저항변화메모리는 기존의 NAND 플래시 메모리를 대체할 차세대 저장메모리로 주목받고 있다. NAND 플래시 메모리 또한 연구 개발이 꾸준히 이루어지고 있으며 수직소자의 개발로 인해 집적도가 크게 증가하였다. 하지만 현재의 수직 플래시 메모리의 경우 100단 이상의 개발에 성공하였지만 갈수록 공정 난이도가 올라가고 있는 추세이며 약 10년 내에 한계에 직면할 것으로 예상되고 있다. 동작 전압이 큰 플래시메모리의 특징으로 인해 수직소자 제작 과정에서 절연막의

두께가 두꺼워지게 되는데, 이는 제품 내 장착되는 메모리 칩의 최대 높이에 수직 소자가 도달하였을 때 더 이상 집적도를 향상시킬 수 없는 한계점으로 작용하게 된다. 저항변화 메모리는 낮은 동작 전압과 높은 집적도, 수직 소자로의 연구 개발 가능성 등으로 차세대 저장메모리로의 장점들을 많이 가지고 있다. 하지만 저항변화 메모리의 상용화 단계에서 가장 큰 문제점으로 작용하는 것은 바로 안정성 문제이다. 저항변화 메모리의 동작 원리 특성상 여러 개의 전도성 경로(conductive path)가 동시다발적으로 생기며, 이 경로들은 생성과 파열이 반복적으로 일어나며 동작하게 되는데, 그 과정에서 발생하는 동작 산포가 안정성에 영향을 주게 된다. 앞서 언급한 다양한 분야로의 연구 개발이 이루어지고 있지만 이러한 연구에 저항변화 메모리가 사용되기 위해서는 고집적 메모리의 개발 뿐 아니라 소자 내 반복 동작에서의 안정성 및 어레이에서 모든 소자들이 동일한 동작 특성을 보이는 소자간 동작 산포의 개선이 우선적으로 이루어져야 한다.

본 논문의 첫 번째 파트에서, 저항변화 메모리에서 가장 큰 문제점으로 지목되고 있는 반복 동작간 산포, 소자와 소자간 산포를 개선하기 위하여 $Pt/Ta_2O_5/HfO_2/TiN$ 소자 내 Au nanodots이 삽입되는 실험을 진행하였다. 이 소자는 HfO_2 막내에 존재하는 shallow trap sites에 전자가 trapping/detrapping 하는 현상으로부터 trapping 되었을 때 낮은 저항 상태를, detrapping 되었을 때 높은 저항 상태를 보이는 저항변화 메모리 거동을 보인다. Ta_2O_5 박

막을 증착 하는 과정에서 HfO_2 박막에 가해지는 plasma로 인해 형성되는 deep trap sites들에 의해 안정적인 메모리 거동을 보이게 되는데, 해당 영역에 Au nanodots을 삽입함으로써 전계 집중 효과를 통하여 안정적인 메모리 거동을 보임을 확인하였다. Au nanodots이 삽입되지 않은 소자와 비교하였을 때 동작 산포가 극적으로 개선되는 결과를 확인하였으며, Au nanodots이 삽입되지 않은 소자는 ~200번 가량의 반복 동작이 가능한 반면, Au nanodots이 삽입된 소자의 경우 1000번 이상의 반복 동작에서도 동일하고 안정적인 메모리 거동을 보임을 확인하였다. 또한 해당 소자를 동작 시키는 과정에서, 컴플라이언스 전류(compliance current)를 조절함으로써 trap sites에 포획되는 전자의 양을 조절하고 이를 통하여 off 상태를 제외한 8개의 서로 겹치지 않는 전류 레벨을 확보함으로써 multi-level 동작 또한 가능함을 확인하였다.

본 논문의 두 번째 파트에서는, 삽입하는 Au nanodots의 위치에 따라 나타나는 소자의 전기적 동작 특성을 확인하고, COMSOL 시뮬레이션을 통해 전계집중 양상을 확인하였다. 기존 HfO_2 박막 내 존재하는 다수의 trap sites에 의해 계면에서 스위칭이 일어난다고 알려져 있는 소자에 Au nanodots의 삽입 위치를 HfO2 박막과 Ta_2O_5 박막 내 삽입하였다. 단원자 증착법으로 HfO_2 박막을 일정 두께 증착하고 Au nanodots을 형성하여 준 후 다시 HfO_2 박막을 증착하는 방법으로 HfO_2 박막 내 Au nanodots을 삽입하였고 Ta_2O_5 박막 내에도 동일한 방법으로 Au nanodots을 삽입하였다.

Ta_2O_5 의 경우 해당 소자에서 스위칭에는 관여를 하지 않으며 상부 전극으로 사용된 높은 일함수를 갖는 Pt 와 Schottky barrier를 형성하여 다이오드와 같은 특성을 보여주는 자가정류 특성에 기여한다고 알려져 있다. 따라서 Ta_2O_5 박막 내 Au nanodots이 삽입되었을 땐, 스위칭에는 영향을 주지 않을거라 예상되지만 이 또한 동작 반복성이 크게 향상되는 결과를 보여주었고, COMSOL 시뮬레이션을 통해 Au nanodots의 삽입 위치가 계면으로부터 멀어지게 되면 전계 집중 효과가 사라지게 되고 그와 동시에 동작 반복성의 개선 효과 또한 사라지는 것을 확인하였다. 이 결과를 통해 전계 집중 효과로 인해 동작 반복성이 개선되며, 계면에서 스위칭이 일어난다는 것을 실험적으로 증명할 수 있는 연구 결과이다.

본 논문의 세 번째 파트에서, Au nanodots 의 형성 과정을 기존 전면에 형성 하던 방법에서 전자빔 노광 방식을 통하여 국부적인 영역에 형성하는 연구를 진행하였다. nanodots을 형성하는 방법에는 다양한 방법들이 존재하는데 널리 알려져 있는 AAO, 구 형태의 나노 구조물들을 이용하는 방법들은 nanodots의 크기나 분포를 원하는 크기로 제작할 수 없다는 단점이 있다. 이러한 nanodots의 분포의 차이는 차후 소자 제작을 하였을 때 소자와 소자 간 사이 산포를 야기하는 요인으로 작용할 수 있으며 그 정도가 심해지게 되면 nanodots이 삽입되지 않는 소자도 존재하게 될 수 있다. 이러한 문제를 해결하기 위하여 본 연구에서는 전자빔 노광 방식을 통하여 원하는 위치에 원하는 크기로 Au nanodots을 형성하고자 하였다.

전자빔 노광을 진행한 후 Au 박막을 증착하고 lift-off 방식을 통하여 Au nanodots을 형성할 수 있었으며, 최소 50nm 크기로 형성할 수 있었으며 노광하는 과정에서 감광물질의 측면 기울기를 조절하기 위하여 서로 다른 분자량을 갖는 PMMA를 두 층으로 증착하여 분자량에 따른 민감성의 차이를 이용하여 확실한 undercut을 형성함으로써 lift-off 과정에서 Au 박막에 가해지는 물리적인 힘을 최소화 함으로써 작은 크기의 nanodots 또한 형성할 수 있었다. 또한 전자빔 노광 과정에서 가해지는 전자의 방사량을 조절하였다. 너무 적은 방사량은 감광 물질을 모두 반응 시키지 못하기 때문에 원하는 패턴을 형성할 수 없고, 너무 많은 방사량은 패턴을 넓어지게 만드는 요인으로 작용하게 되어 미세한 조절이 필요하게 된다. 이렇게 형성한 Au nanodots을 삽입하여 소자를 제작하고 원자 힘 현미경을 이용하여 표면 분석을 진행하였으며 nanodots이 삽입되어 있는 표면에서 눈에 띄게 높은 전류가 흐르는 것을 확인할 수 있었고, 이는 앞서 확인한 결과와 동일한 것으로 nanodots의 위치에 전계가 집중되는 것을 확실하게 보여주었으며, 이로 인해 동작 특성들이 개선되는 것을 알 수 있었다.

핵심어: 저항변화메모리, 금속점, 전계집중, 자가정류, 동작반복성, HfO_2, Ta_2O_5

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