M.S. THESIS

Reliability Issues of 3D NAND Focused on Program Disturbance & Retention in Tapering Devices

Program Disturbance와

Tapering 소자에서의 Retention을 중심으로 한

3D NAND의 Reliability Issues

BY

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이 논문을 공학석사 학위논문으로 제출함

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전기정보공학부

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이용민의 공학석사 학위논문을 인준함

2020 년 8 월

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Abstract

The transition from 2D NAND to 3D NAND brought many advantages, but it brought also new problems. One of them is the program disturbance by hot carrier injection(HCI). Program disturbance refers to the problem in which electrons unintentionally tunnel into the charge trap layer in the unselected string by the voltage difference of boosting channel potential, resulting in V_{th} changing. In 2D NAND, this problem was solved by adding dummy cells at both ends where drain and source selection line(DSL,SSL) transistor exist. However, in 3D NAND, the problem occurs in selected word lines(WL) because of the unique boosting channel potential characteristic named natural local self-boosting(NLSB), which is different from 2D NAND. In this paper, the mechanisms of the problem are investigated. In 3D NAND, the boosting potential of the selected WL is higher than the boosting channel potential of the unselected WL. As a result, a large electric field is formed near the selected WL and band-to-band tunneling(BTBT) occurs. The electrons generated by BTBT can get large energy by the lateral electric field and finally get enough vertical electric field to be tunneled and can be trapped in the charge trap layer of the selected WL. This can cause unintended V_{th}

changes, resulting in data fail, which can cause reliability problems.

Another problem in 3D NAND is the tapering problem. Tapering problem is a problem that occurs due to difficulty of etching process in 3D NAND that increases bit density by WL stacking. In this paper, retention characteristics due to lateral migration in the tapering device were investigated. As a result, the filler tapering did not affect the lateral migration, but in the case of Si/O/N/O tapering, the retention characteristics were changed considerably. In NPN(Neutral-Programmed-Neutral) mode, the electric field felt by trapped electrons becomes smaller as the tapering becomes severer, resulting in the less reduction of V_{th}. In addition, it was confirmed that the trapped electron in the tapering device through the NPP mode and the PPN mode is easier to move to a thicker side in the nitride. Also, in the EPE(Erased-Programmed-Erased) mode, as the tapering became more severe, the electric field increased as the hole was trapped more due to the decrease of the channel radius, resulting in more V_{th} reduction. Also, when comparing the EPP mode and the PPE mode, it was observed that the V_{th} reduction in the PPE mode occurs more than that of the EPP mode because more holes are trapped in the cells located below. These features show

different retention characteristics with the conventional ideal devices without any tapering. These other features come to be an important reliability issue in the flash memory of multi-level cells with small V_{th} margin.

Keyword: 3D NAND, program disturbance, hot carrier injection, tapering, retention, lateral migration

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CONTENTS

1. Introduction

1.1 Program disturbance in 3D NAND

NAND flash memory continues to evolve for efficiency of data storage and economy. As a result, NAND flash memory has changed from 2D NAND to 3D NAND. The transition from 2D NAND to 3D NAND brought many advantages, but it brought also new problems. One of them is the program disturbance by hot carrier injection(HCI). In this paper, we will discuss the mechanism of the program disturbance caused by the hot carrier injection. NAND flash memory refers to memory that works by trapping electrons in a charge trap layer and changing the value of the data by changing the V_{th} of the device. The act of trapping electrons in a place is called “program”. In NAND, it is essential to distinguish between the string to be programmed and the string not to be programmed. To do this, a boosting potential is used in the unselected string making the vertical electric field small, preventing electrons from tunneling [1, 2, 3]. In conventional 2D NAND, all memory cells have the same boosting channel potential. As a result, strong lateral electric fields are formed only at both ends, where the high voltage difference between the low channel potential of the turned off drain selection line transistor(DSL)

and source selection line transistor(SSL) and the high boosting channel potential of memory cells exists, causing unintentional V_{th} changing problems due to hot carrier injection [4, 5]. This is called program disturbance, and this problem in 2D NAND was solved by adding dummy cells at both ends [6]. However, in 3D NAND, there is different trend of boosting channel potential called natural local self-boosting(NLSB) [7]. This means that the selected word line(WL) to be programmed naturally has a higher boosting channel potential than the boosting channel potential of the unselected WL to be passed. As a result, a strong lateral electric field is generated near the selected WL, which means that this program disturbance problem could occur near the selected WL. In this paper, the mechanisms of the program disturbance in 3D NAND are investigated.

1.2 Retention of tapering devices in 3D NAND

In 3D NAND, electrons trapped in charge trap layer move vertically and laterally by the electric field even if no voltage is applied over time. Due to this vertical loss and lateral loss, the V_{th} of the device and the intended data value changes, causing reliability problems. This is called the retention problem in 3D NAND. Especially, because 3D NAND uses charge trap layer and this nitride layer runs continuously along the memory string, bringing an extra charge loss path for the charge, lateral migration in the nitride is very important issue [8]. Also, NAND flash memory with multilevel cells has the smaller V_{th} margins compared to the NAND flash memory with single-level cells [9].

And over time, 3D NAND is evolving into continuously stacking WL to maximize data storage. The number of WLs has been increased by 30 ~ 50% for each generation, and total mold height was also increased along with the increased number of WL. In the aspect of process, there are many difficulties such as high-aspect ratio channel hole etch, the control of the mechanical stress, and the uniform dielectric layer deposition [10,11]. In this reason, the different etching level of the top cell and bottom cell parts exist,

resulting in tapering problems. There are not many studies about tapering 3D NAND flash memory device, and only published papers are about string current, program speed and so on [12, 13]. In this paper, the retention characteristics of the tapering device will be discussed. In detail, retention characteristics due to lateral migration in the tapering device according to the degree of filler tapering and the degree of Si/O/N/O tapering and various patterns such as NPN mode, NPP mode, PPN mode, EPE mode, EPP mode, PPE mode and memory cell positions such as the top cell and bottom cell are discussed. TCAD simulation confirmed how the ideal device without any tapering and the tapering device have different retention characteristics.

2. Mechanisms of program disturbance in NAND flash memory

2. 1 Boosting channel potential and band-to-band tunneling(BTBT)

NAND flash memory has a structure in which each WL in all strings share each voltages excepting for bit lines(BLs). Therefore, during program operation, regardless of strings, the same program pulse is applied to DSL, SSL and all memory cells as shown in figure 1. And the only bit line voltage is used to distinguish between the string to be programmed and the string not to be programmed. In this case, the channel part of the memory cell separated by turning off the DSL and SSL transistor becomes floating and channel potential of memory cells follows the WL voltage. In doing so, the channel potential rises and is said to be “boosting” [1].

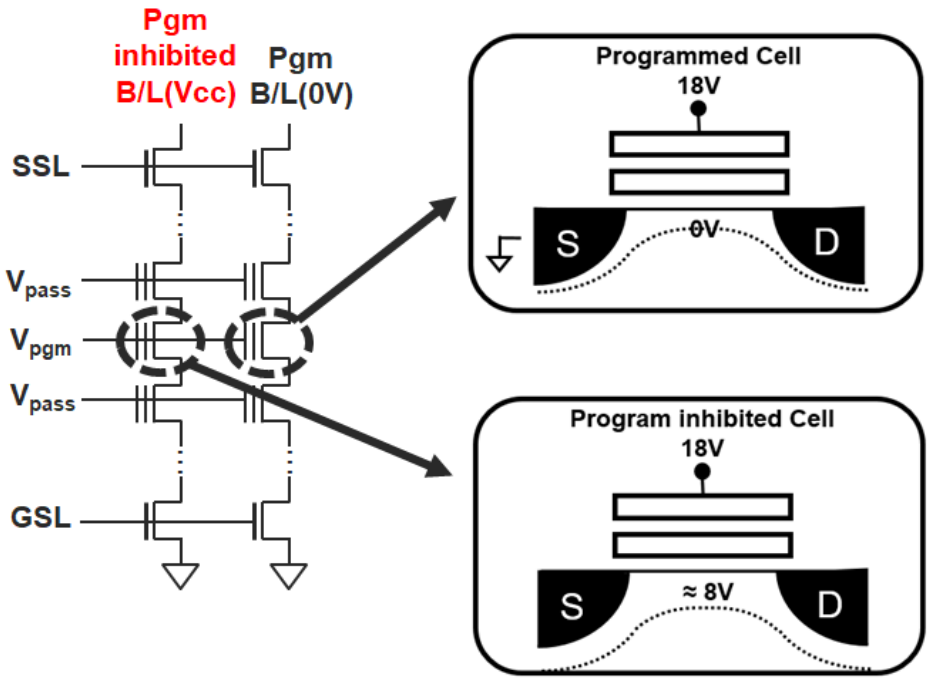


Figure 1. Voltage scheme for the unselected string and selected string, and the channel potential respectively [1]

The boosting channel potential tends to be different in 2D and 3D NAND. In 2D NAND, the substrate is grounded due to the structure of the memory device. As shown in figure 2, 3, the boosting channel potential of the memory cells is formed equally regardless of memory cells. As a result, a high lateral electric field is formed only at both ends by the large voltage difference between the low voltage of the channel potential of the turned off DSL and SSL and the high boosting channel potential of the memory cells.

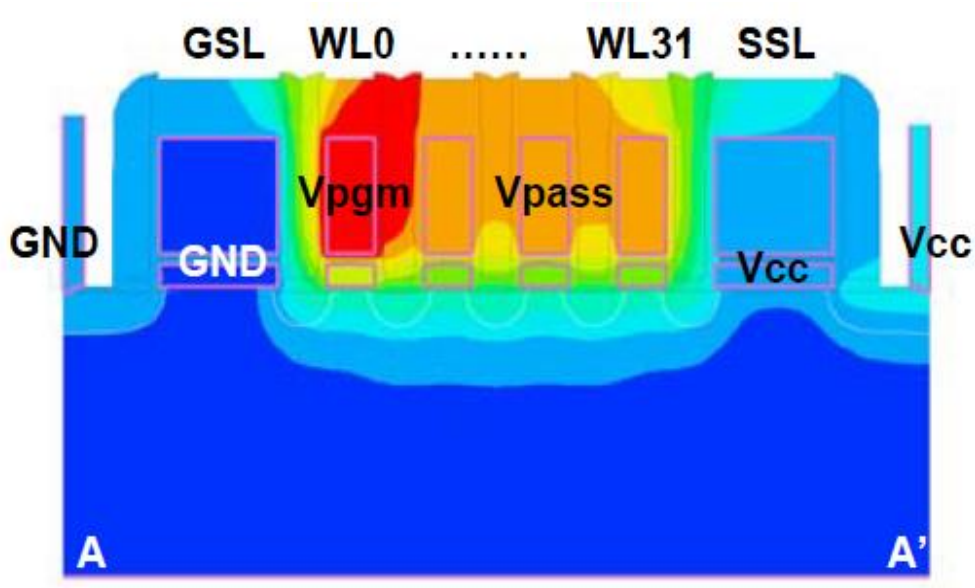


Figure 2. Channel potential contour in 2D NAND [4]

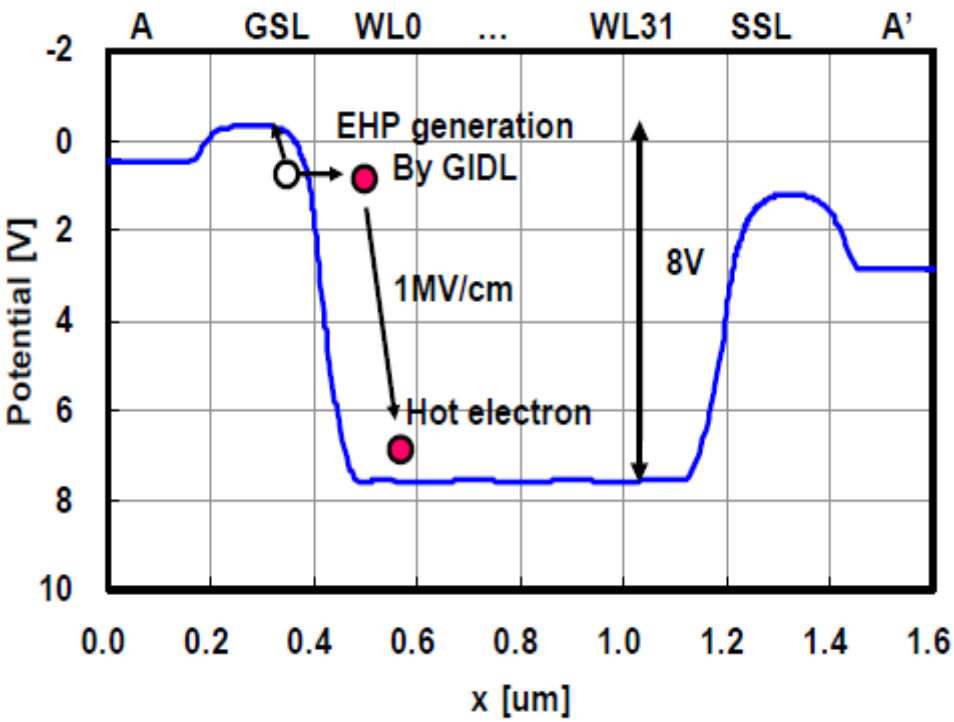


Figure 3. Channel potential in the position of the device of 2D NAND [4]

On the other hand, the boosting channel potential of 3D NAND tends to be different from the boosting channel potential of 2D NAND. As can be seen in figure 4, 5, 3D NAND exhibits a boosting channel potential characteristic named NLSB [7]. This means that the channel potential of the programming cell(selected WL) is naturally higher than that of other pass cells(unselected WLs) like the local self-boosting scheme of 2D NAND [14]. Due to this, in the 3D NAND, high lateral electric field can occur near the programming cell as well as at both ends where the DSL and SSL are located. As a result, the large lateral electric field allows electrons in the valence band to tunnel into the conduction band and makes electron-hole pairs as shown in figure 6 [15]. This is called band-to-band tunneling(BTBT). These electrons and holes affect the characteristics of the device.

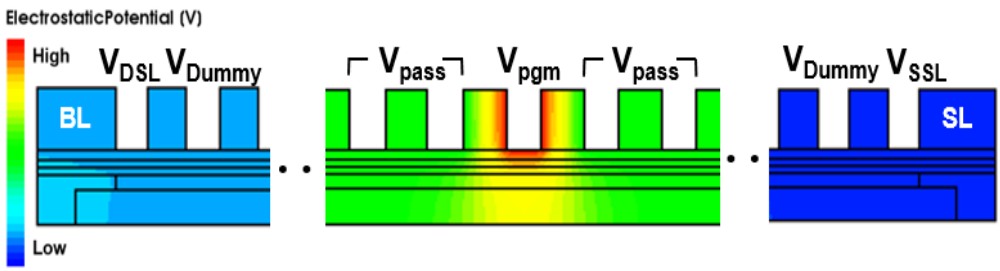


Figure 4. Channel potential contour in 3D NAND

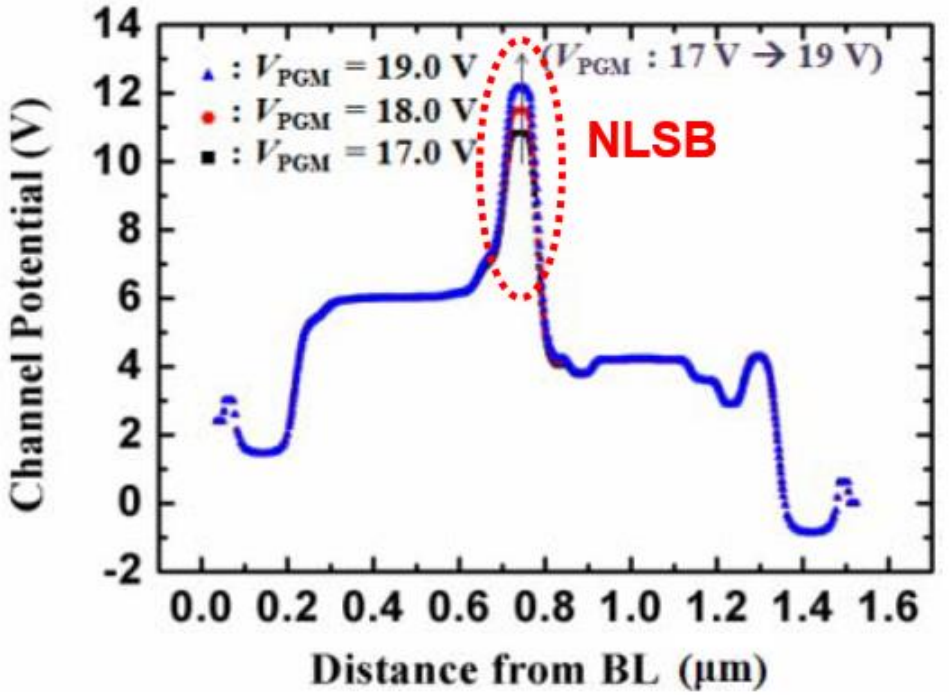


Figure 5. Channel potential in the position of the device of 3D NAND [7]

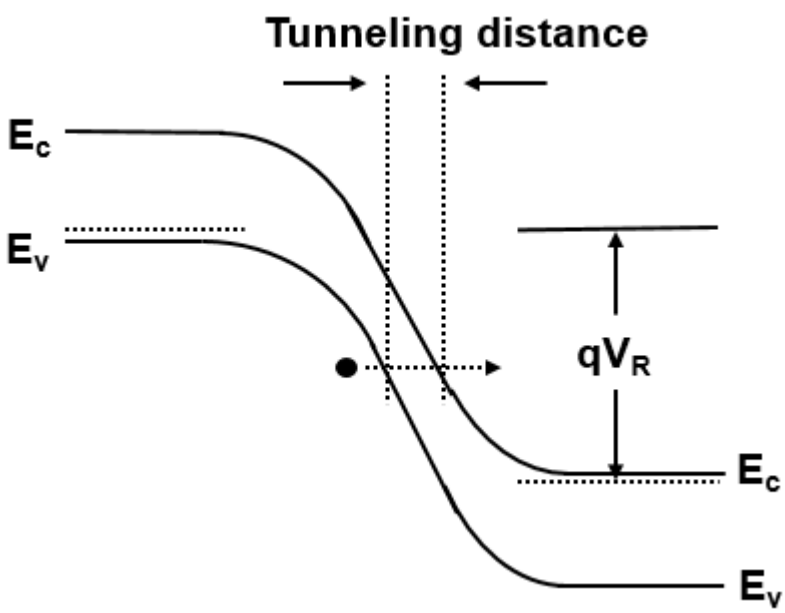


Figure 6. Band-to-band tunneling in a p-n junction [12]

2. 2 Hot carrier injection(HCI) in NAND flash memory

This paper describes the hot carrier injection based on the lucky electron model [16, 17]. Figure 7 shows the movement of electrons inside the semiconductor device. Figure 8 shows the tunneling physics of the electrons in the energy band diagram. The electron generated by BTBT is accelerated by a large lateral electric field in the channel(P_1). This accelerated electron can get a lot of energy, and the electron is said to be “hot". This hot electron gains a force in the direction to tunnel into the oxide once it has a sufficient vertical electric field(P_2). At this point, the less collision there is until the oxide interface is reached, the more likely the probability to tunnel is(P_3). In addition, the energy barrier of the Si-SiO_2 interface felt by the electron is lowered due to the strong vertical electric field(P_4). As a result, considering these probabilities, the electrons that get the big energy can tunnel into the oxide, which is called hot carrier injection.

The logic is represented by equations (1-6). Equation 1 is total lucky electron current from an interface to a gate contact. Equation 2 is the probability that the electron will be redirected. Equation 3 is the probability that the electron will travel a distance y to the interface without losing any

energy. Equation 4 is the probability that the electron has energy between ε and ε + dε. Equation 5 is the probability of scattering in the image force potential well. Equation 6 is the energy barrier of Si-SiO_2, which is a function of F_{ins} and F_{ins} <0 means that the peak point of oxide potential occurs near the Si-SiO_2 interface and corresponds to the program operation. The first term is the zero field barrier height at the semiconductor-insulator interface. The second term represents barrier lowering due to the image potential. The third term is due to the tunneling process. In the programming operation of 3D NAND flash memory, the electrons are tunneled by Fowler-Nordheim(FN) which needs an extremely strong vertical field to trap electrons in the charge trap layer. However, hot carrier injection can occur by lower vertical electric field than that of FN tunneling. In the unselected string, the electrons generated in the region where the strong lateral electric field are accelerated and obtain a large energy. And when a sufficient vertical field is obtained, they can tunnel and trapped in the charge trap layer. Consequently, data can be failed by this hot carrier injection.

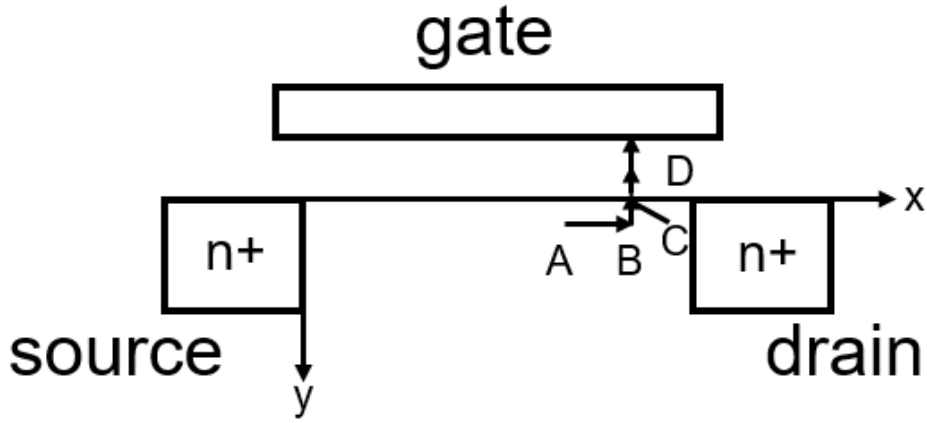


Figure 7. Hot carrier injection mechanism flow in the device [16]

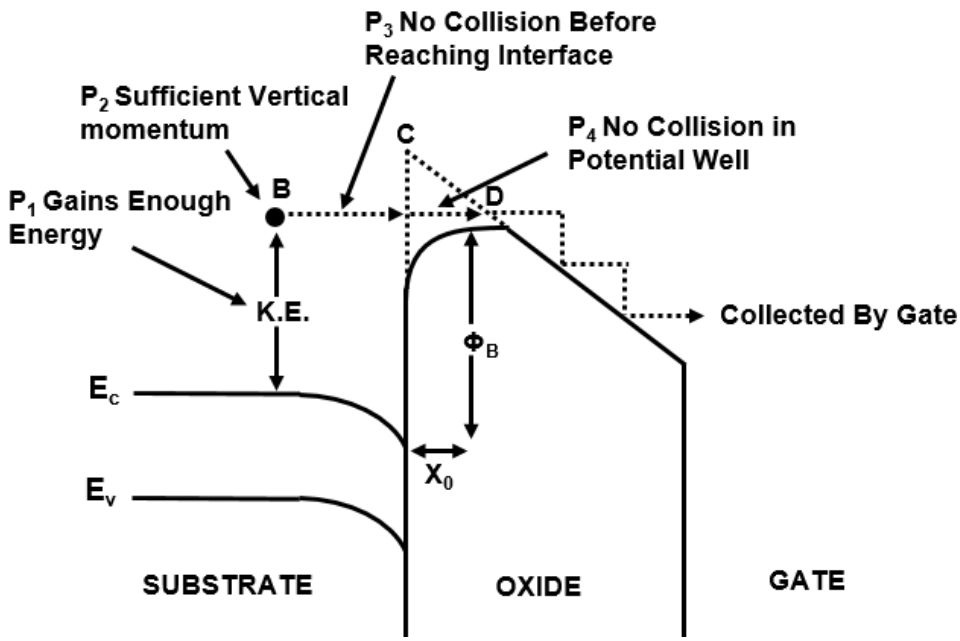


Figure 8. Energy band diagram illustrating probability about hot carrier injection [17]

$$\mathrm{I_g} = \iint J_n(x,y) P_s P_{ins} \left(\int_{E_B}^{\infty} P_\varepsilon P_r d\varepsilon \right) dxdy \qquad (1)$$

$$\mathrm{P_r}(\varepsilon) = \frac{1}{2\lambda_r} \left(1 - \sqrt{\frac{E_B}{\varepsilon}} \right) \qquad (2)$$

$$\mathrm{P_s}(y) = \exp\left(-\frac{y}{\lambda}\right) \qquad (3)$$

$$\mathrm{P_\varepsilon}(\varepsilon) = \frac{1}{\lambda F_{eff}} \exp\left(-\frac{\varepsilon}{\lambda F_{eff}}\right) \qquad (4)$$

$$\mathrm{P_{ins}} = \exp\left(-\frac{x_0}{\lambda_{ins}}\right) \qquad F_{ins} < 0 \qquad (5)$$

$$\mathrm{E_B} = E_{B0} - \alpha q |F_{ins}|^{\frac{1}{2}} - \beta \mathrm{q} |F_{ins}|^{\frac{2}{3}} - V_{sem} \quad F_{ins} < 0 \qquad (6)$$

2. 3 Channel potential lowering phenomenon over time

The electrons generated by BTBT are not only tunneled into the nitride, but also accumulate in the channel under the selected WL due to the high program voltage. Over time, electrons continue to accumulate, which lowers the boosting channel potential of the selected WL. The channel potential of the selected WL continues to be decreased over time. The maximum value of channel potential decreases as electrons continue to accumulate during the duration time after rising time of programming pulse. This is a physical factor that changes the tendency of hot carrier injection over program time, which must be considered for explaining program disturbance.

2. 4 Conclusion

Unlike 2D NAND, in 3D NAND, the NLSB makes the channel potential of the selected WL to be higher than the channel potential of the unselected WL, resulting in a strong lateral electric field near the selected WL. As a result, as can be seen in figure 9, BTBT can occur near the selected WL and electrons are generated by BTBT. These electrons can get large energy by the strong lateral electric field and electrons shows two flows. One of them is channel potential lowering and the other one is hot carrier injection. Channel potential lowering phenomenon can change the channel potential over time. And some electrons can be injected into the charger trap layer by hot carrier injection, resulting in changing V_{th} and data failure.

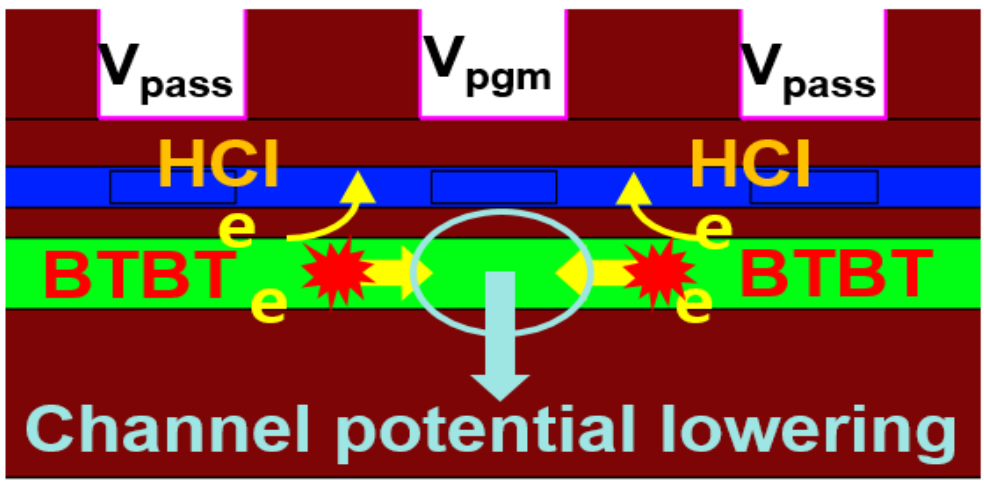


Figure 9. Mechanisms of program disturbance near selected WL

3. Retention in tapering NAND flash memory devices

3. 1 Tapering device structure

Figure 10 shows the tapering device of 3D NAND flash memory. In 3D NAND process, it begins with drilling down through the poly/oxide stack by reactive ion etching (RIE) and then, the tunneling and trapping layers are deposited along the sidewalls of the trenches by using PECVD(Plasma enhanced chemical vapor deposition). Finally, the thin polysilicon channel is deposited, followed by a core filler to form a hollow structure [11]. As like the actual 3D NAND flash memory, the simulated structure is composed of the filler, channel, tunneling oxide, charge trap layer, blocking oxide and DSL, SSL, WLs and spacers. The simulation was conducted with 11 WLs for simulation efficiency. In this paper, filler, channel using Si material, tunneling oxide, charge trap layer using Si_3N_4 material, and blocking oxide were all tapered [13]. The degree of the tapering of filler was split into 0%, 20%, 40%, and 60%, and the degree of the tapering of Si/O/N/O was split into 0%, 10%, 20%, and 30%. WL was counted from the bottom, and the top cell was defined

as 9th WL, and the bottom cell was defined as 3rd WL.

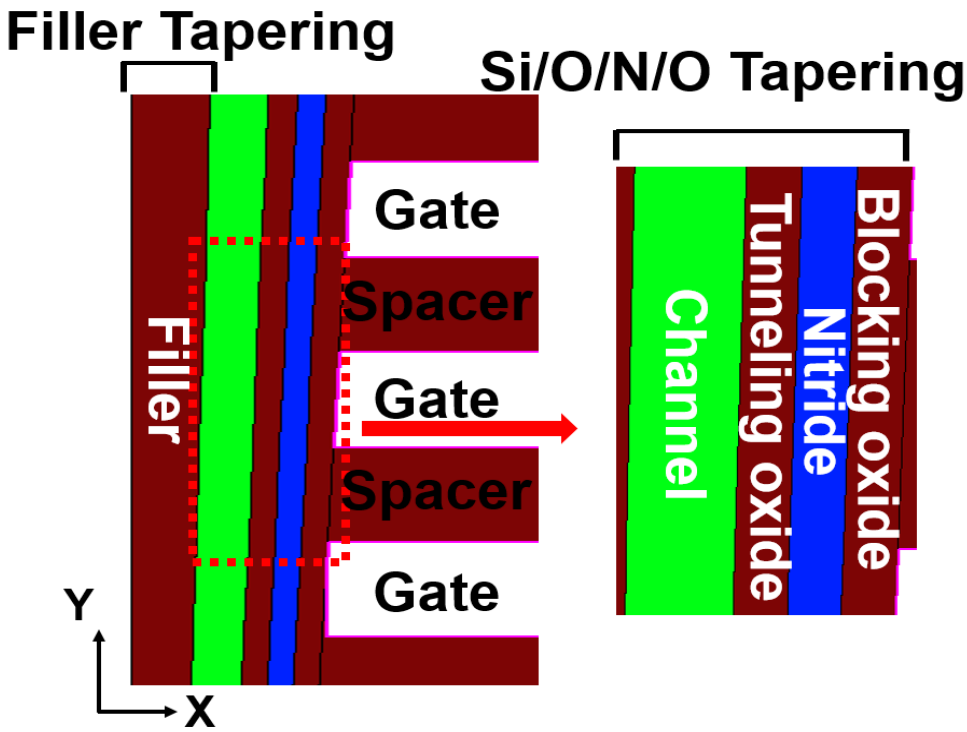


Figure 10. Tapering 3D NAND flash memory cross section in the simulation

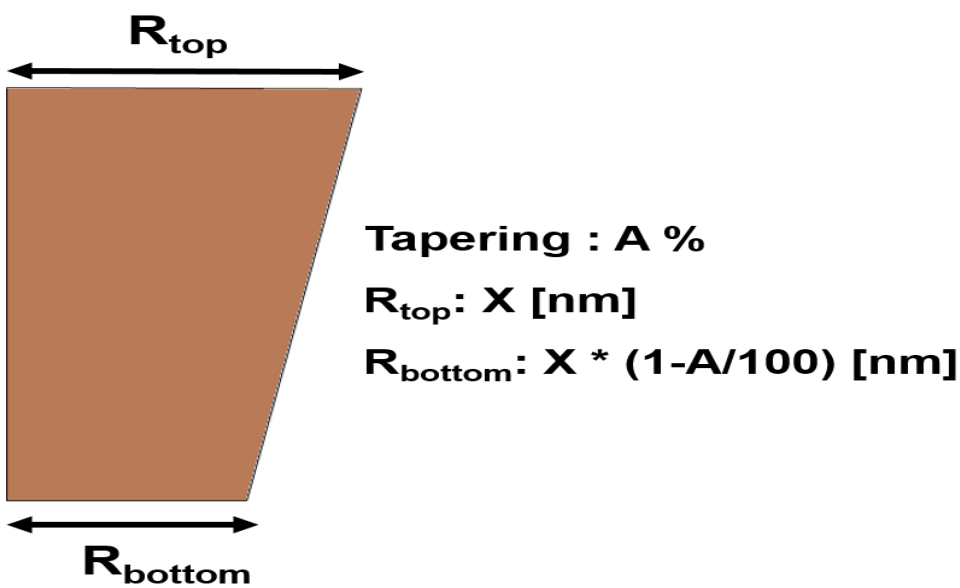


Figure 11. Definition of tapering calculation

Figure 11 shows the definition of tapering calculation. When degree of tapering is A% and the top length is X [nm], the bottom length becomes X * (1-A / 100) [nm] cut by A%. For example, if a filler with a top length of 100 nm is applied with 60% tapering, the bottom length becomes 40 nm. And the table below shows the physical parameters of the structure proceeded in the simulation.

Table 1. Physical parameters of the structure in the simulation

Physical dimensions [nm]	
Gate Length	**28**
Spacer Length	**28**
Selected Tr. Length	**140**
Filler Thickness	**15**
Channel Thickness	**10**
Tunneling oxide Thickness	**5**
Nitride Thickness	**5**
Blocking oxide Thickness	**5**

3. 2 Simulation condition

Sentaurus device simulator was used for the simulation [18]. In this paper, retention characteristics only due to lateral migration except vertical loss were investigated. Figure 12 represents the trapped electron distribution over time by lateral migration. Immediately after the program, electrons were trapped in nitride under the target cell, but electrons moved laterally by electric field in figure 12 (b). In order not to include the vertical loss, the tunneling and the thermionic-related physics were not applied in the simulation. Main physical model used in the simulation includes drift-diffusion transport model. Electron trap energy level is 1.3eV, hole trap energy level is 2.5eV [19, 20]. And simulation is conducted under 363K for checking earlier retention characteristics. And it is assumed that V_{th} of the programmed state is 4V.

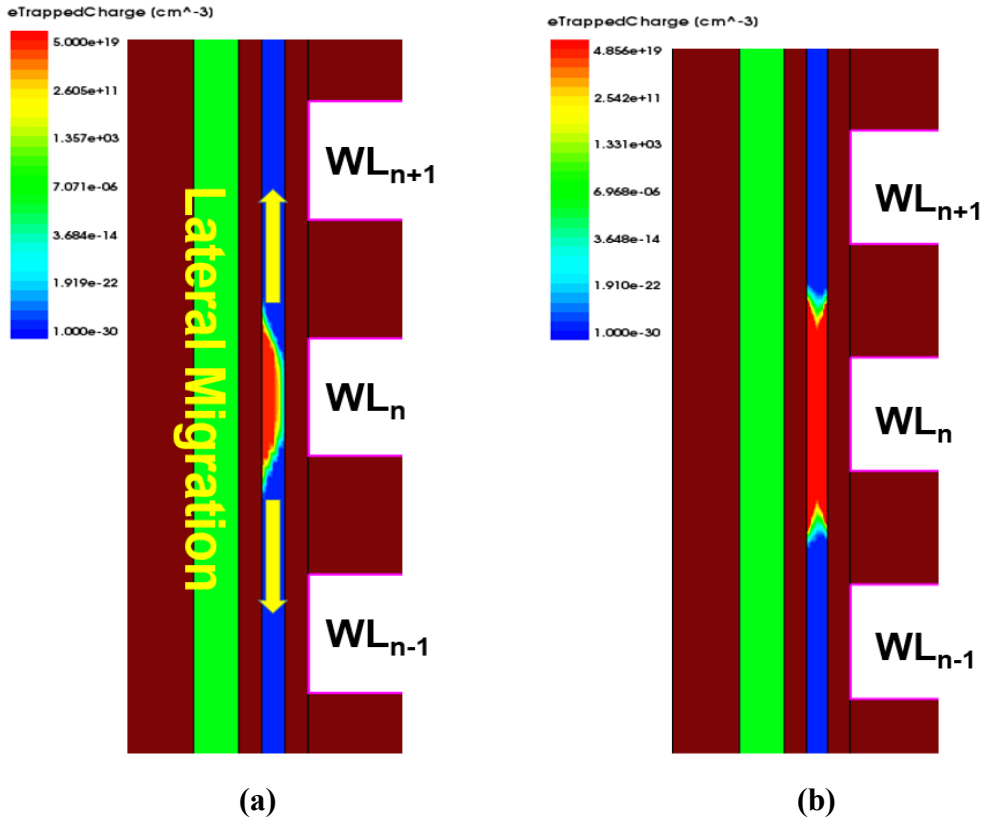
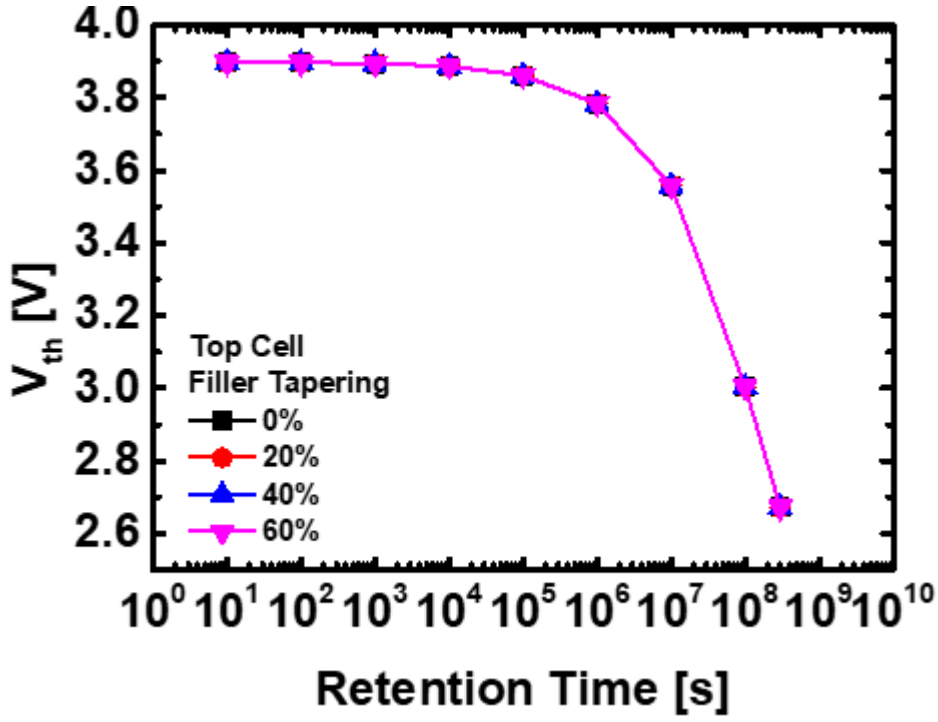


Figure 12. Trapped electron distribution in the charge trap under (a) 0s and (b) 10 years

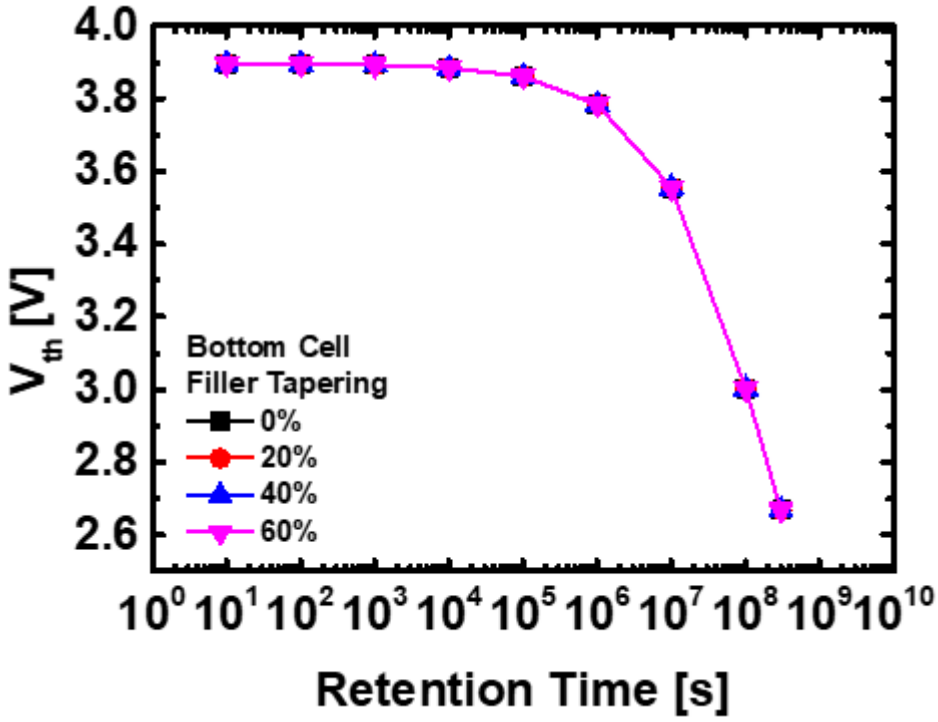
3.3 Retention characteristics of tapering devices

In this chapter, retention characteristics due to lateral migration in the tapering device according to the degree of filler tapering and the Si/O/N/O tapering and various patterns such as NPN mode, NPP mode, PPN mode, EPE mode, EPP mode, PPE mode and memory cell positions such as the top cell and bottom cell are discussed. When the cases of the filler tapering are mentioned, 0% Si/O/N/O tapering is assumed. Also, When the cases of the Si/O/N/O tapering are mentioned, 60% filler tapering is assumed.

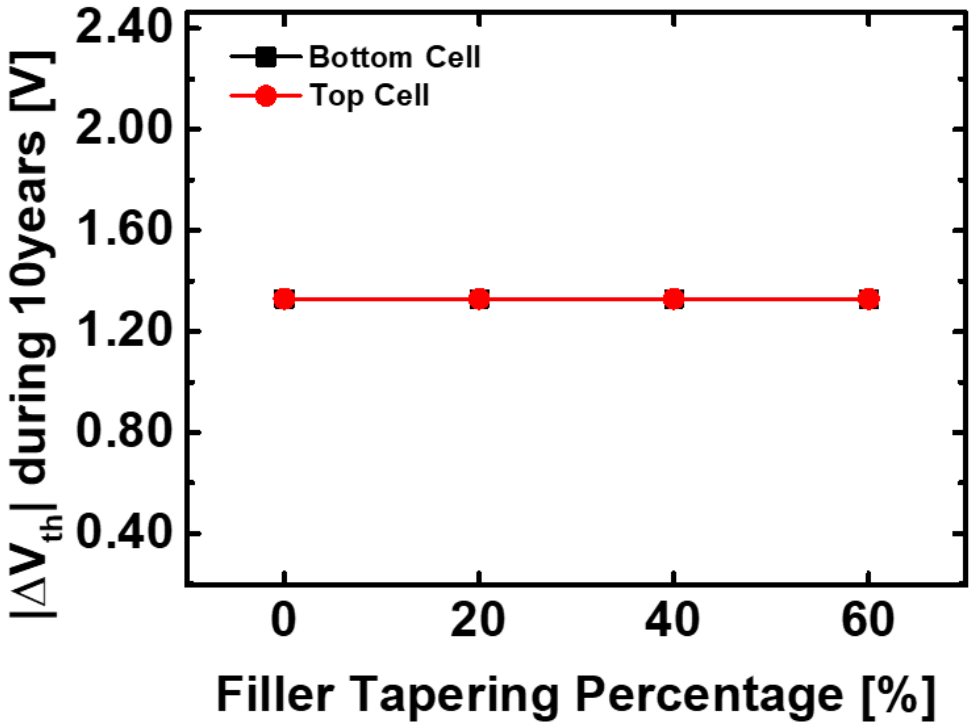
Figure 13 shows the V_{th} shift during retention time according to the degree of the filler tapering. In this case, 0% Si/O/N/O tapering was assumed and NPN mode was assumed. As can be seen, when the degree of the filler tapering was assumed to be 0%, 20%, 40%, and 60% for both the top cell and the bottom cell, no change in retention characteristics was found. Through this, it can be concluded that the degree of the filler tapering does not affect lateral migration in NPN mode.


4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
V_{th} [V]
Top Cell
Filler Tapering
0%
20%
40%
60%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Retention Time [s]

(a)


4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
V_{th} [V]
Bottom Cell
Filler Tapering
0%
20%
40%
60%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Retention Time [s]

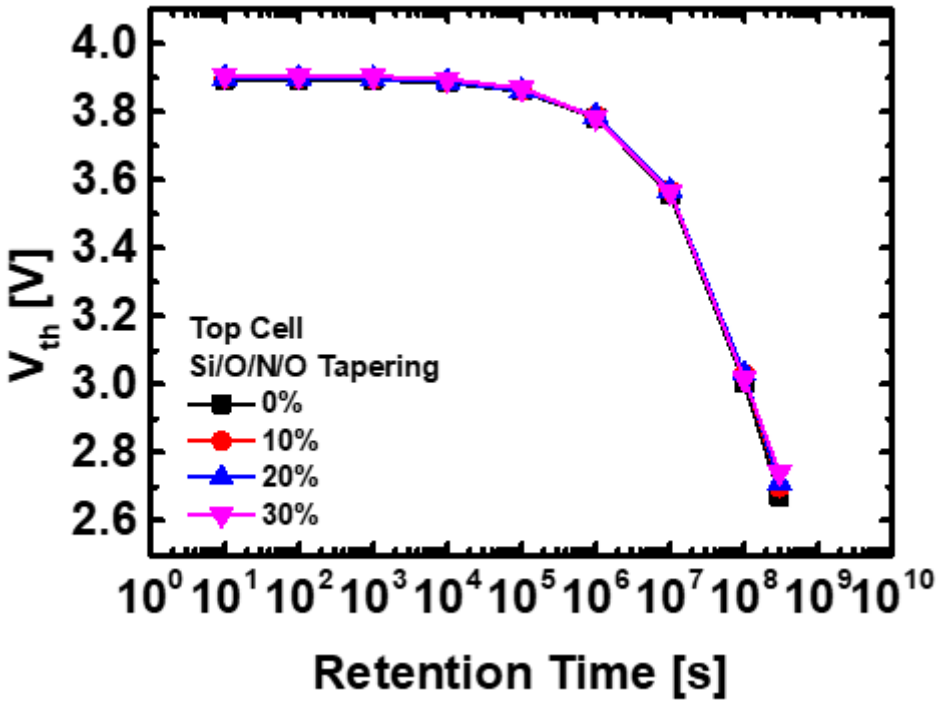
(b)



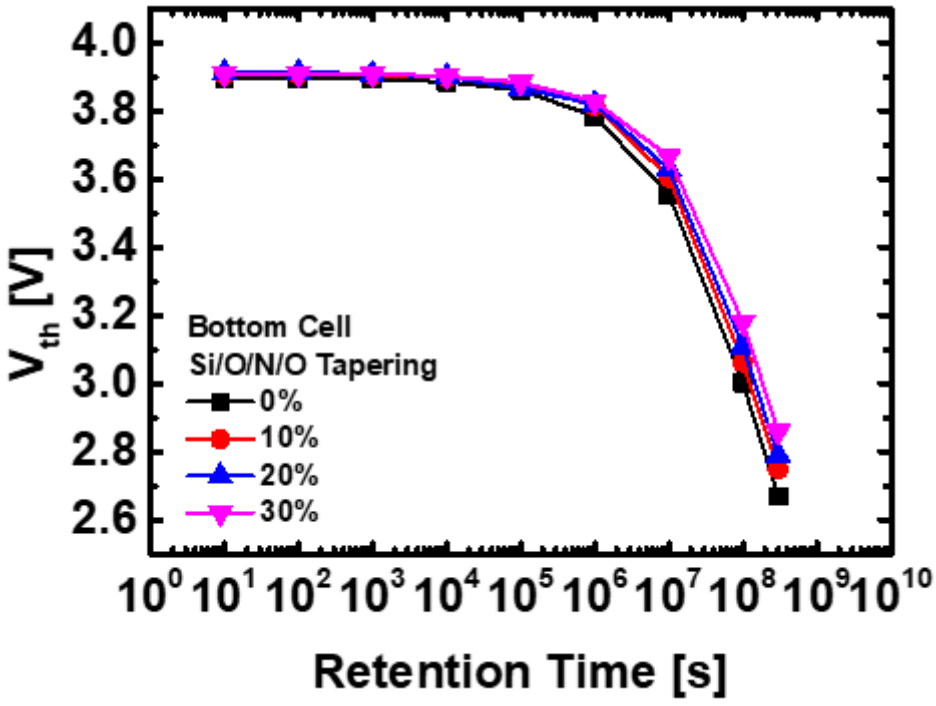
(c)

Figure 13. V_{th} shift during retention time at (a) the top cell and (b) bottom cell, and (c) $|\triangle V_{th}|$ during 10 years according to the filler tapering percentage in NPN mode

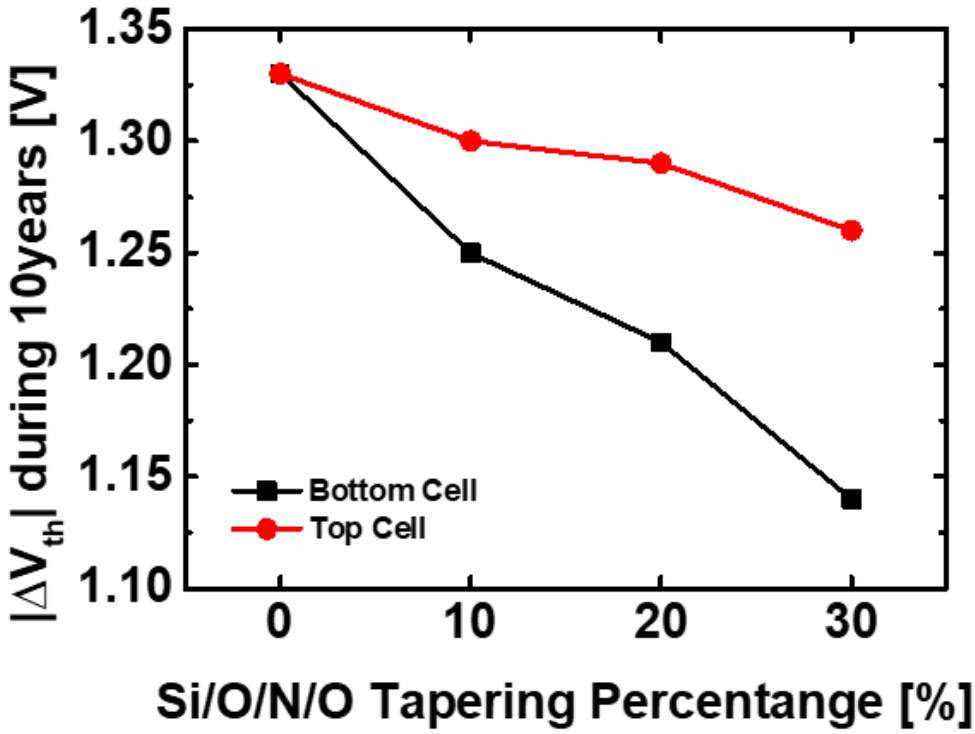
Figure 14 shows the V_{th} shift during retention time according to the degree of the Si/O/N/O tapering. At this time, 60% of filler tapering was assumed and NPN mode was assumed. The reduction of V_{th} became less as the degree of the Si/O/N/O tapering was increased to 0%, 10%, 20%, and 30% in both the top cell and the bottom cell. Especially, these characteristics are more severe in the bottom cell because the thickness of the nitride of the bottom cell is greatly reduced due to tapering effects.


4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
V_{th} [V]
Top Cell
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Retention Time [s]

(a)


4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
V_{th} [V]
Bottom Cell
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Retention Time [s]

(b)



(c)

Figure 14. V_{th} shift during retention time at (a) the top cell and (b) bottom cell, and (c) $|\triangle V_{th}|$ during 10 years according to the Si/O/N/O tapering in NPN mode

Figure 15 plots the bottom cell's electric field in the y-direction right after programming according to y-position at a line 0.15 nm away from the tunneling oxide/nitride interface and the degree of Si/O/N/O tapering. Overall, the trapped electrons of the target cell located in the middle move to both sides, and as the Si/O/N/O tapering increases, the y-direction electric field felt by the trapped electrons decreases, resulting in less reduction of V_{th} for 10 years.

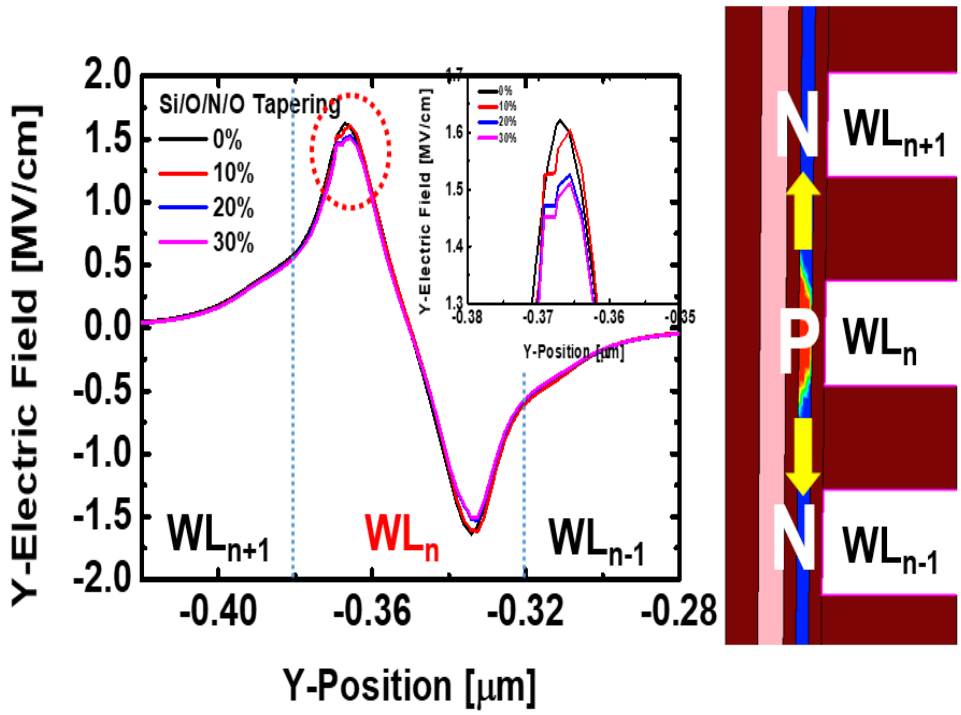
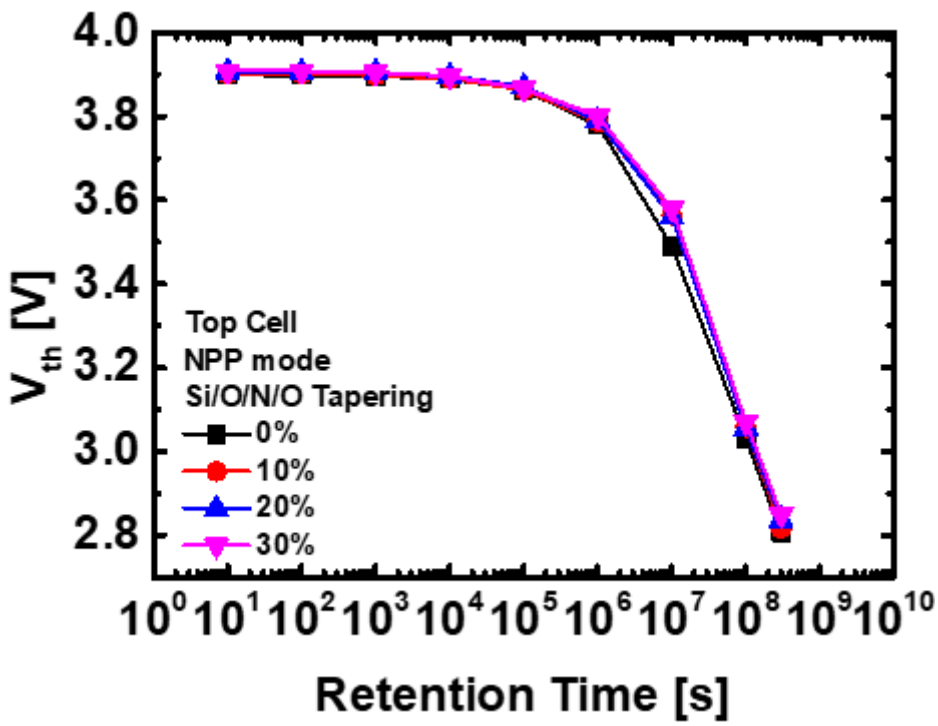


Figure 15. Electric field in y-direction right after programming versus y-position of simulation device according to the Si/O/N/O tapering

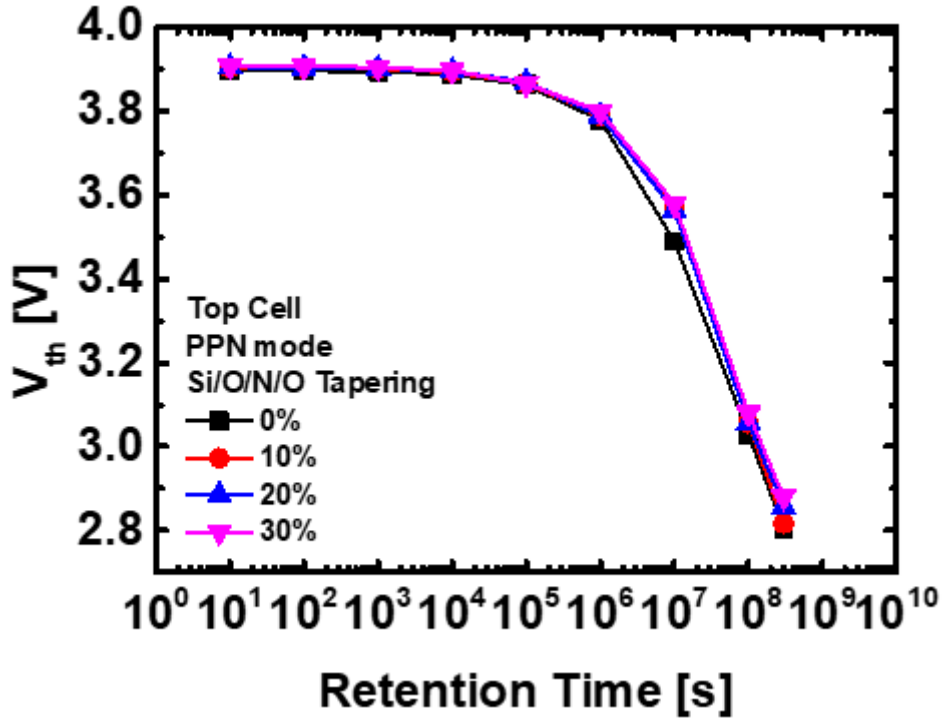
Next, retention characteristics in NPP mode and PPN mode are investigated. In these cases, 60% of filler tapering was assumed. In the case of NPP mode, generally, the trapped electron of the center target cell moves largely upward due to the electric field, and in the case of PPN mode moves largely downward. Figure 16 shows the V_{th} shift of the top cell and the bottom cell in NPP mode and PPN mode during retention time, and the $|\triangle V_{th}|$ for 10 years respectively. In the figure 16 (c), (f), when the degree of the Si/O/N/O

tapering was 0%, the $|\triangle V_{th}|$ in both the top cell and bottom cell are matched. But, as the degree of the Si/O/N/O tapering becomes severe, the $|\triangle V_{th}|$ in NPP mode is larger than that of PPN mode. This confirms that the electron moves upwards easier than downwards when the device is tapered structurally.

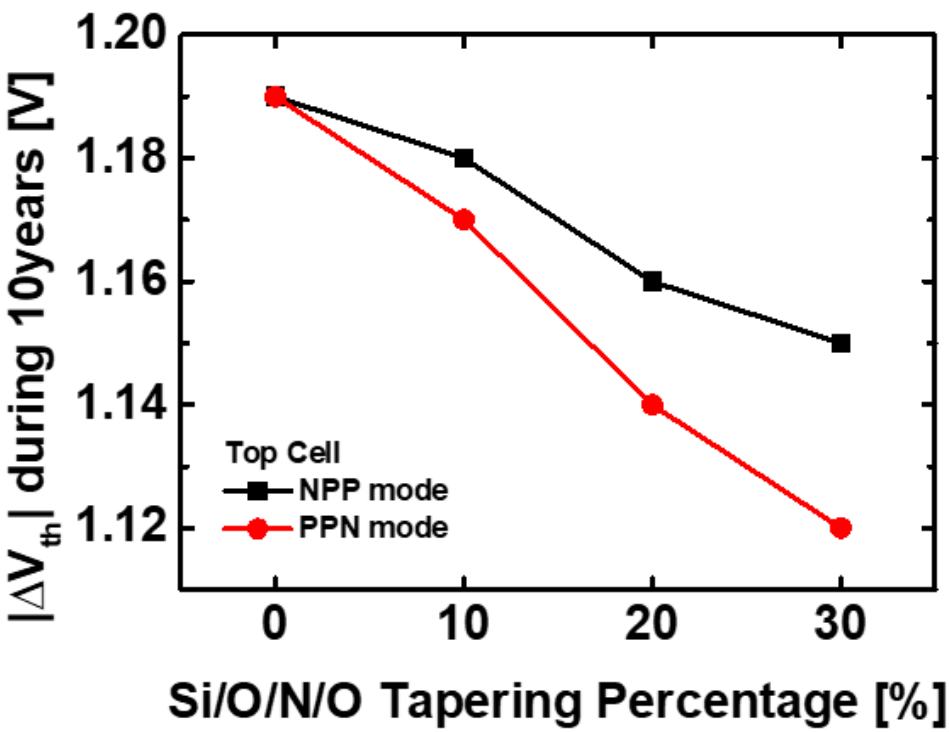


.

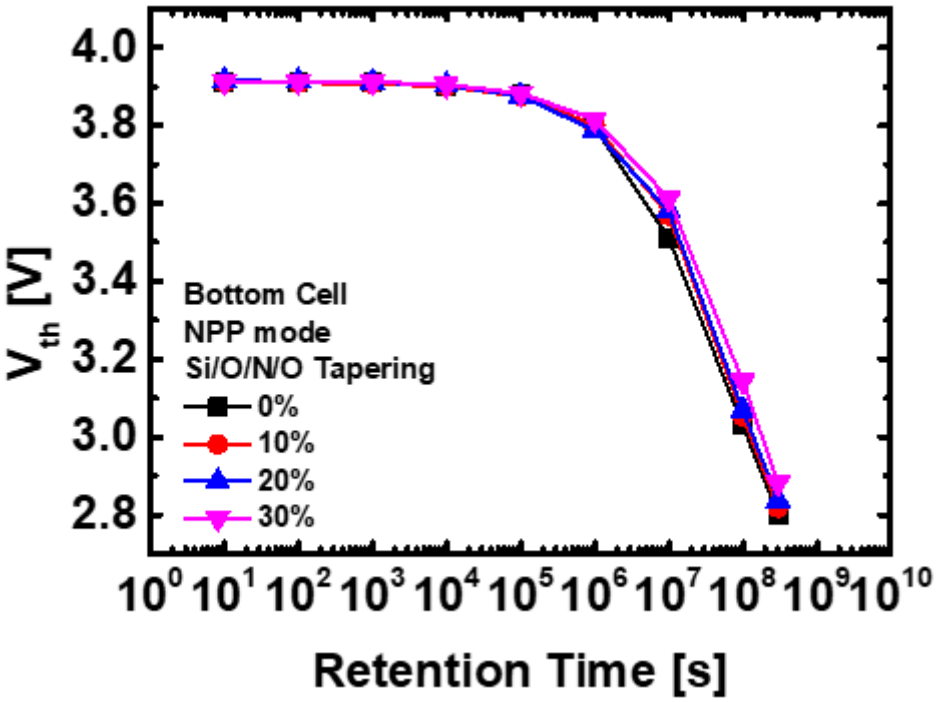
(a)


4.0
3.8
3.6
3.4
3.2
3.0
2.8
V_th [V]
Top Cell
PPN mode
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^10
Retention Time [s]

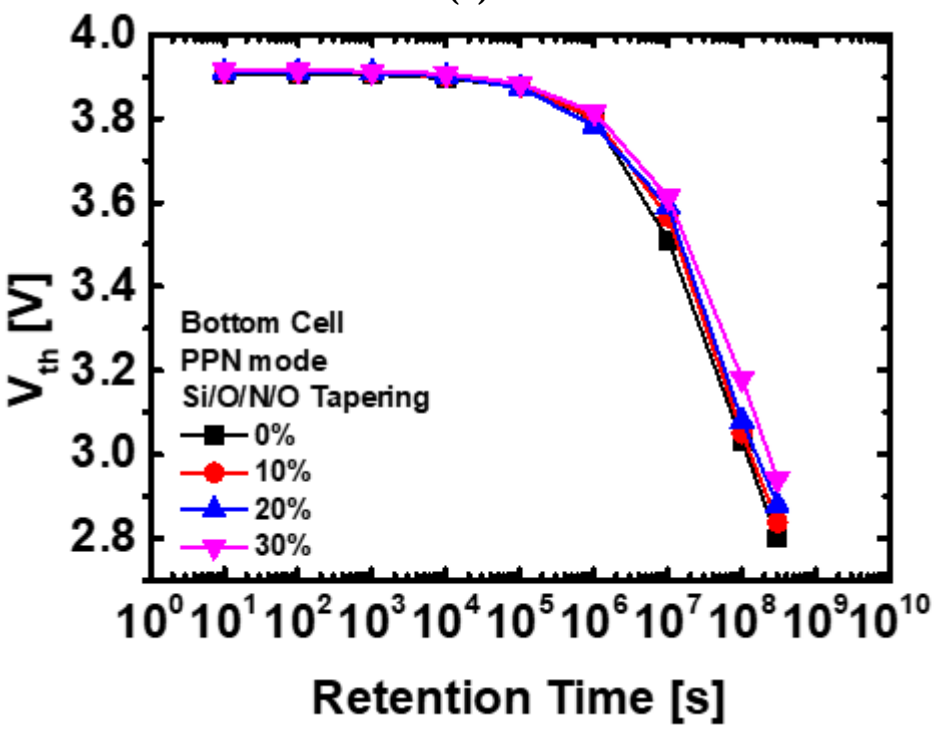
(b)


1.20
1.18
1.16
1.14
1.12
|ΔV_th| during 10years [V]
Top Cell
NPP mode
PPN mode
0
10
20
30
Si/O/N/O Tapering Percentage [%]

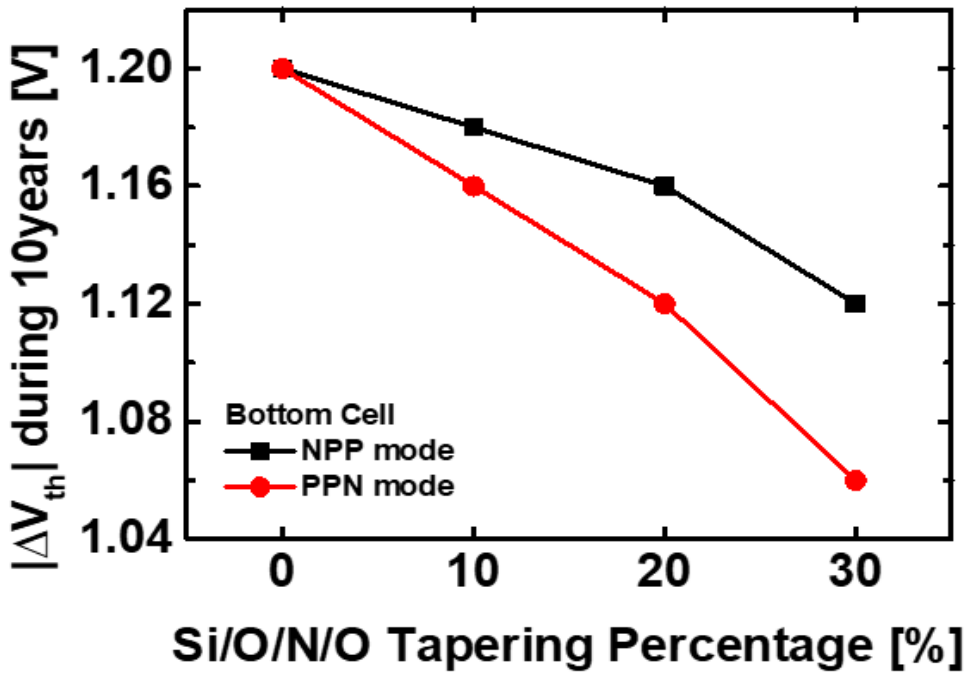
(c)


4.0
3.8
3.6
3.4
3.2
3.0
2.8
V_th [V]
Bottom Cell
NPP mode
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^10
Retention Time [s]

(d)


4.0
3.8
3.6
3.4
3.2
3.0
2.8
V_th [V]
Bottom Cell
PPN mode
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^10
Retention Time [s]

(e)

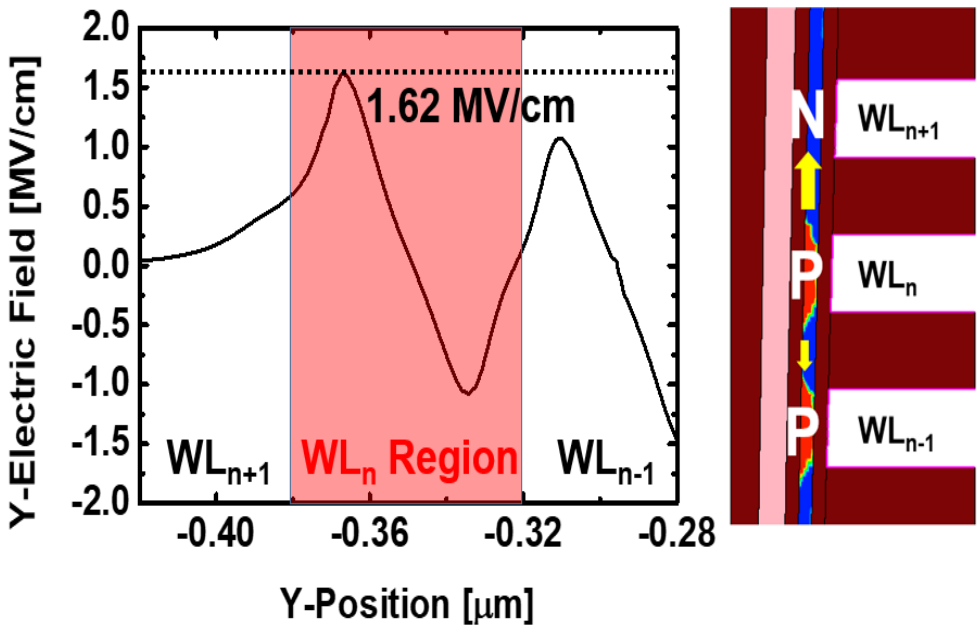


(f)

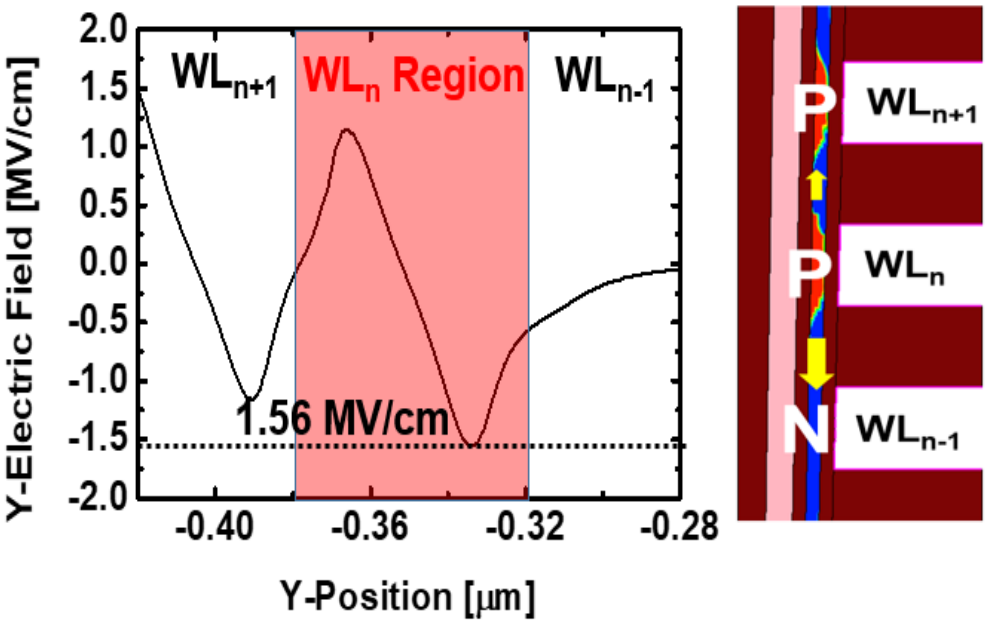
Figure 16. V_{th} shift during retention time in the top cell (a) in NPP mode and (b) PPN mode, (c) $|\triangle V_{th}|$ during 10 years in the both case. And the same thing in the bottom cell (d) in NPP mode and (e) PPN mode, (f) $|\triangle V_{th}|$ during 10 years in the both case.

Figure 17 shows electric field in the y-direction according to the y-position of the simulation device in the NPP mode, PPN mode in case of the bottom cell with 30% Si/O/N/O tapering. As shown in the figure, it can be confirmed that the peak value of the electric field of the NPP mode in the y-direction is greater than that of the PPN mode. In conclusion, because of the electric field in the y-direction felt by the electrons, electrons move upwards

easier in the tapering device.



(a)



(b)

Figure 17. Electric field in y-direction right after programming versus y-position of simulation device (a) in case of the NPP mode and (b) in case of the PPN mode at the bottom cell with 30% Si/O/N/O tapering

The following is to observe the retention characteristics after the erase operation on the tapering device through EPE mode, EPP mode, PPE mode. For the efficiency of the simulation, we proceeded the simulation with the string with 3WLs.

First, in the erase operation, 3D NAND conventional GIDL erase was used as can be seen in figure 18 [21]. Conventional GIDL erase is a method of reducing the V_{th} of the device by applying the same high voltage to BL and SL to make a hole with BTBT generation and trapping the hole in nitride.

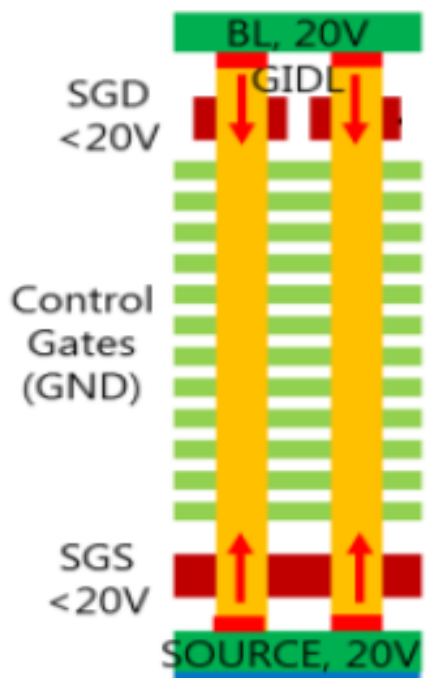
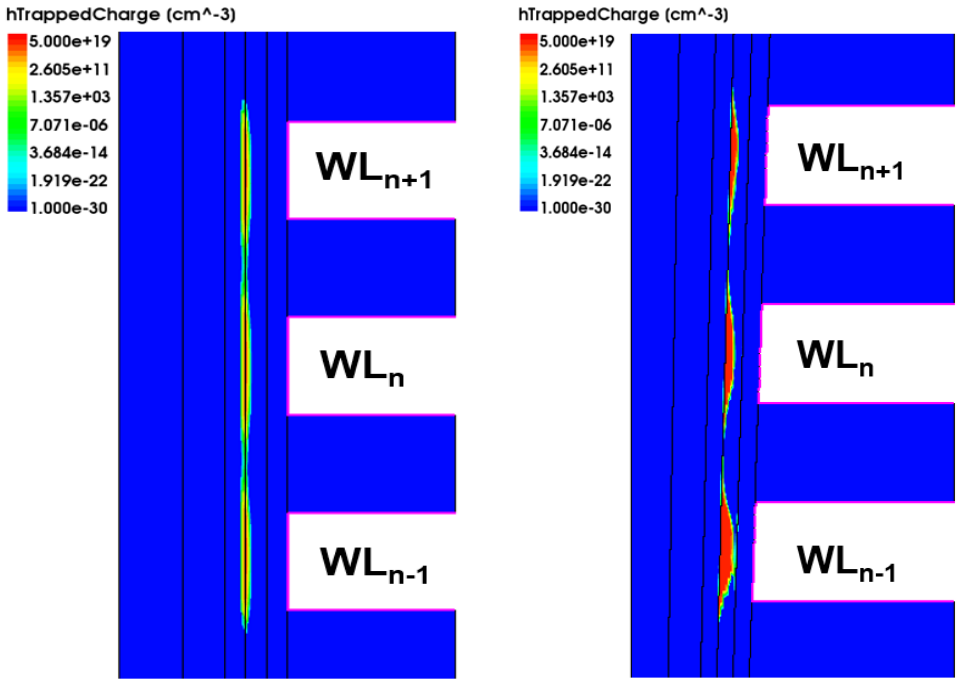
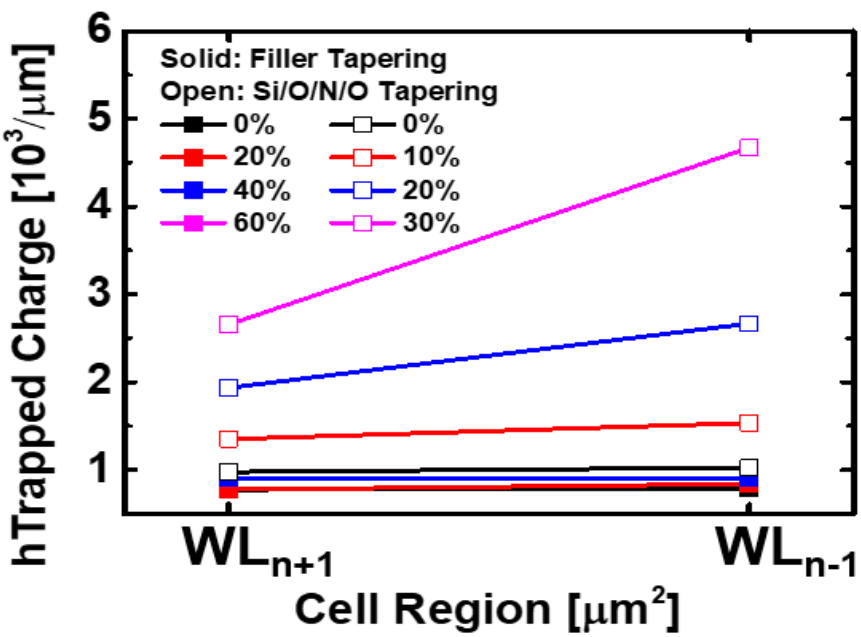


Figure 18. Conventional GIDL erase method [21]

Figure 19 shows the distribution of trapped holes after erase operation. Figure 19 (a) shows a device without any tapering, and as can be seen in the figure, it shows almost same trapped hole distribution in WL_{n+1}, WL_n, and WL_{n-1}. However, in the figure 19 (b) which shows a tapering device with 60% filler tapering, 30% Si/O/N/O tapering, it can be seen that the distribution of trapped holes according to the location is different. Figure 19 (c) is a graph plotting the distribution of trapped hole in WL_{n+1} and WL_{n-1} regions in the cases of filler tapering and Si/O/N/O tapering. As can be seen from the graph, there was almost no change in the case of the filler tapering. But, in the case of Si/O/N/O tapering, the holes in the memory cells located below were trapped more. Also, the amount of the trapped hole increases as the degree of the tapering increases.



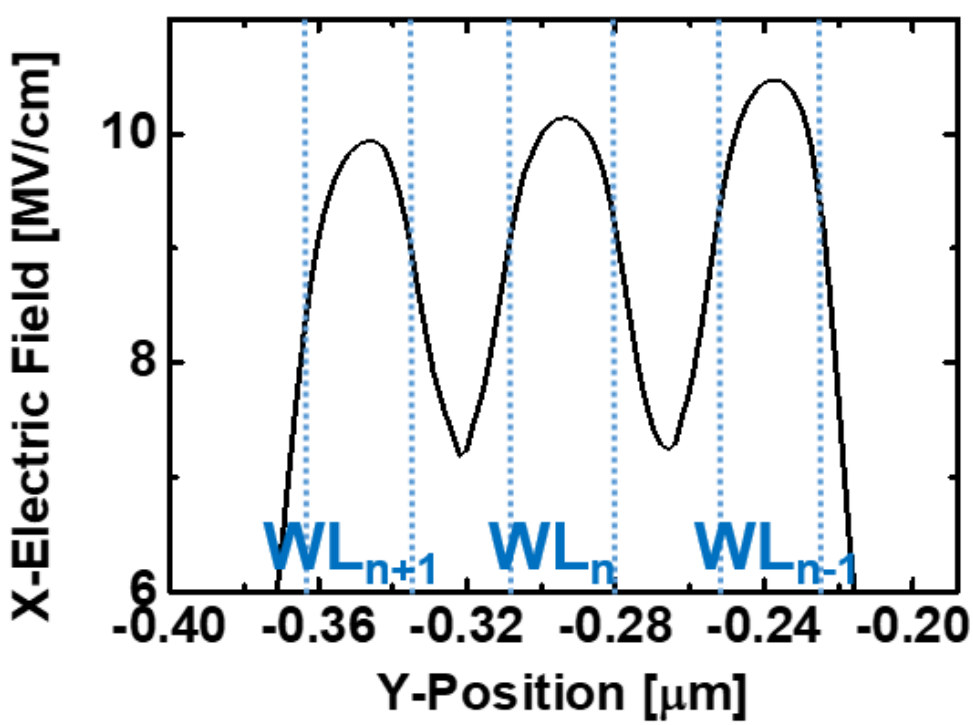
(a) **(b)**



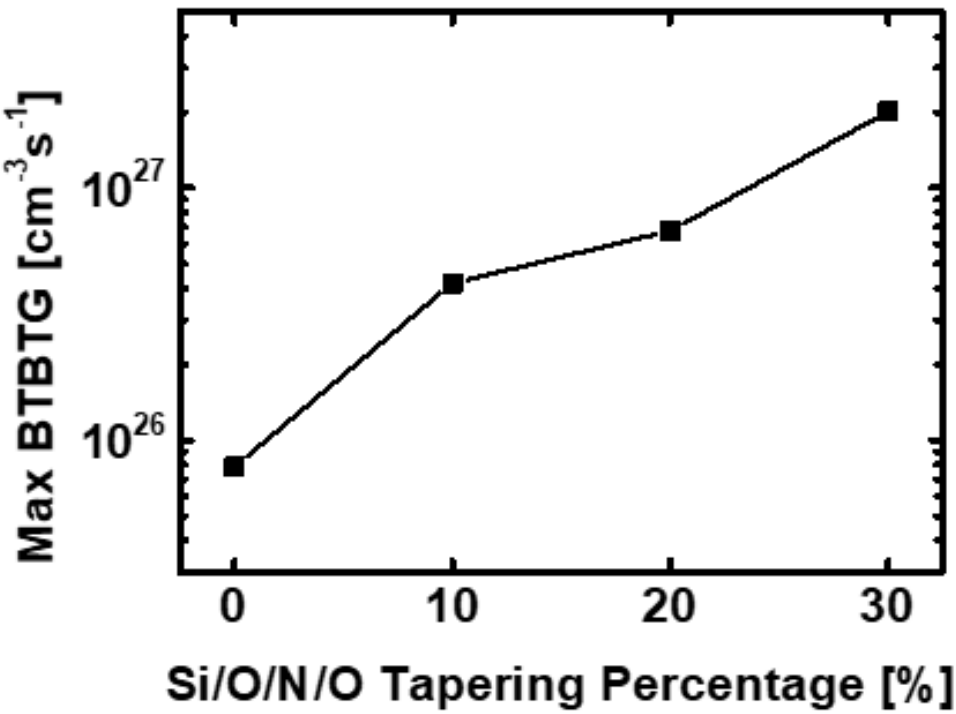
(c)

Figure 19. Trapped hole distribution in the device (a) without any tapering and (b) with 60% filler tapering and 30% Si/O/N/O tapering, and (c) the value of the trapped hole in WL_{n+1} and WL_{n-1} region in both tapering cases.

In the figure 20 (a), the electric field in x-direction increased in the lower cell in the tapering device with 30% Si/O/N/O tapering. This is why the hole was trapped more in the memory cell located below. Also, as shown in figure 20 (b), as the degree of the tapering increases, the radius of the channel decreases, and accordingly, the value of maximum BTBT generation increases, resulting in more hole generation and more hole trapping. As a result, the amount of the trapped hole increases as the degree of the tapering increases.



(a)



(b)

Figure 20. (a) Electric field in x-direction during erase operation at a line 3nm away from the channel/tunneling oxide interface (b) The value of maximum BTBT generation according to the Si/O/N/O tapering

The change in erase operation characteristics caused by this tapering caused a change in retention characteristics. Figure 21 shows the retention characteristics of EPE mode according to the degree of filler tapering. Because the erase property was not changed by filler tapering, the retention property was also not changed.

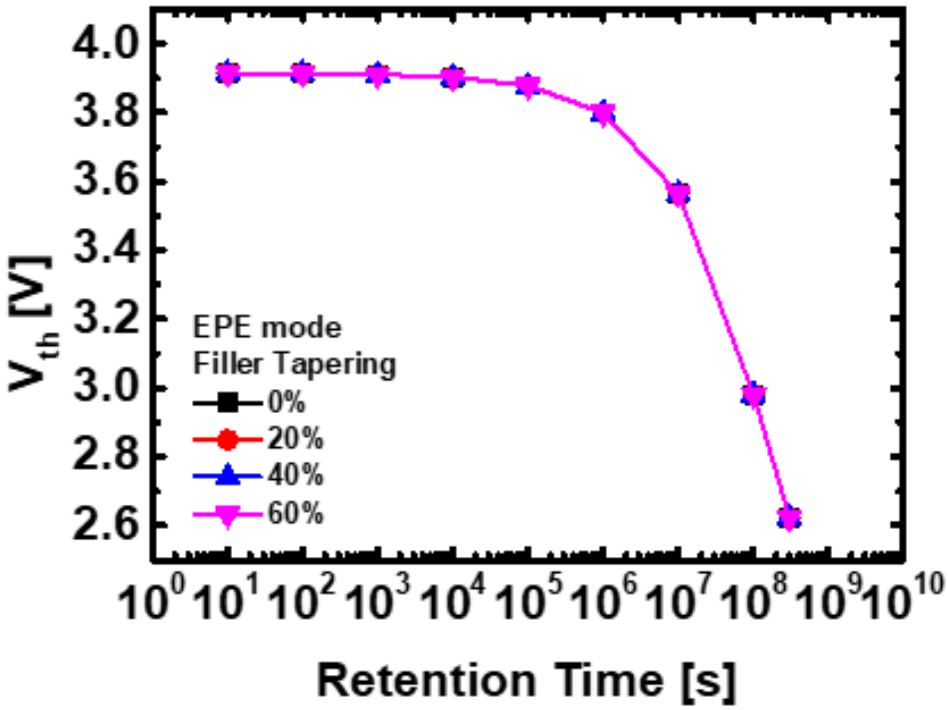
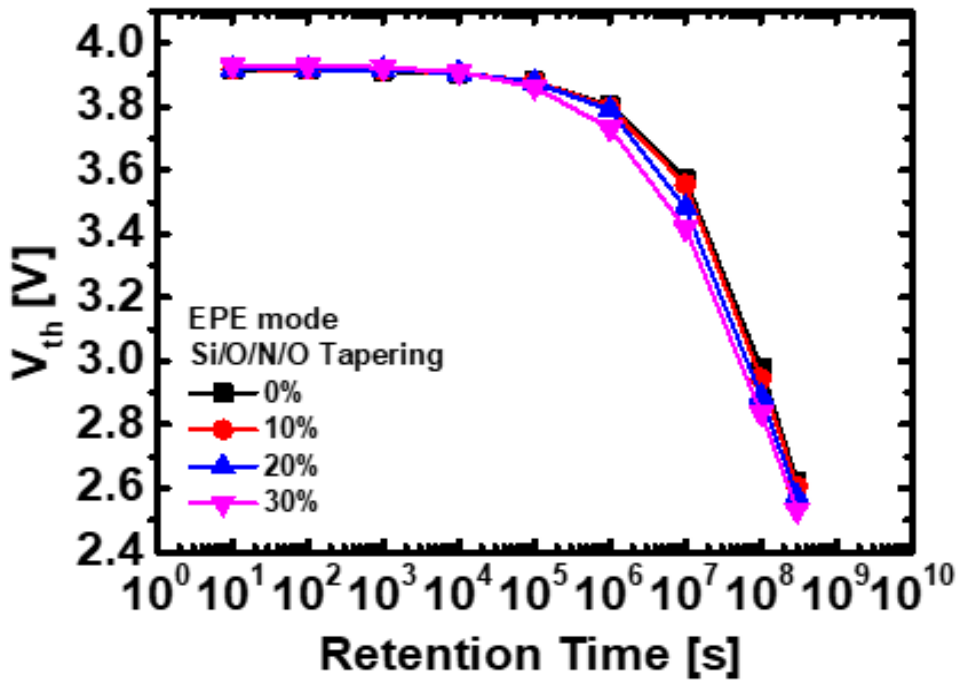
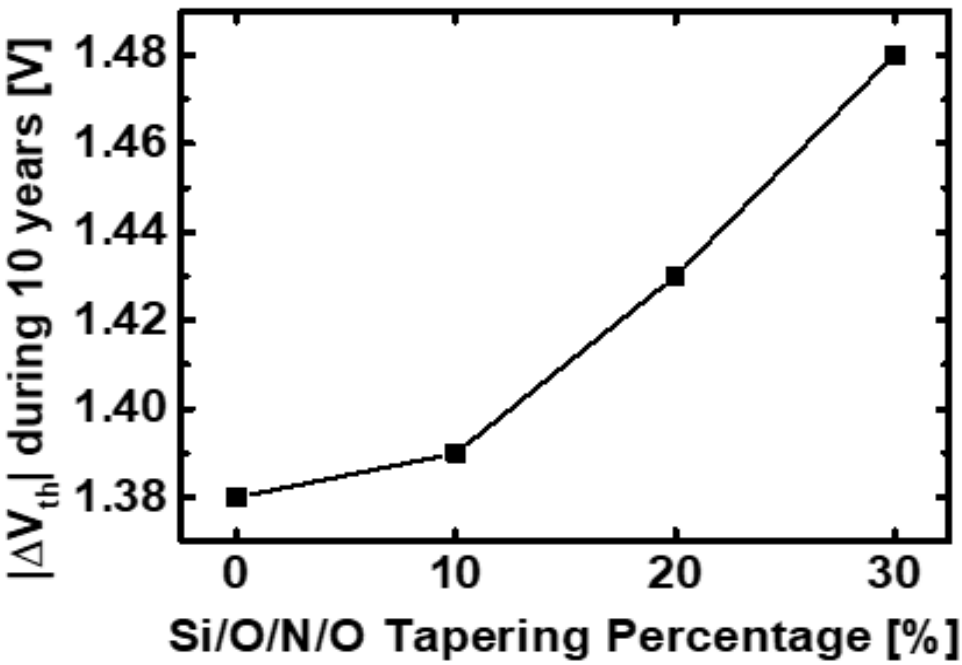


Figure 21. V_{th} shift during retention time in EPE mode according to the degree of filler tapering

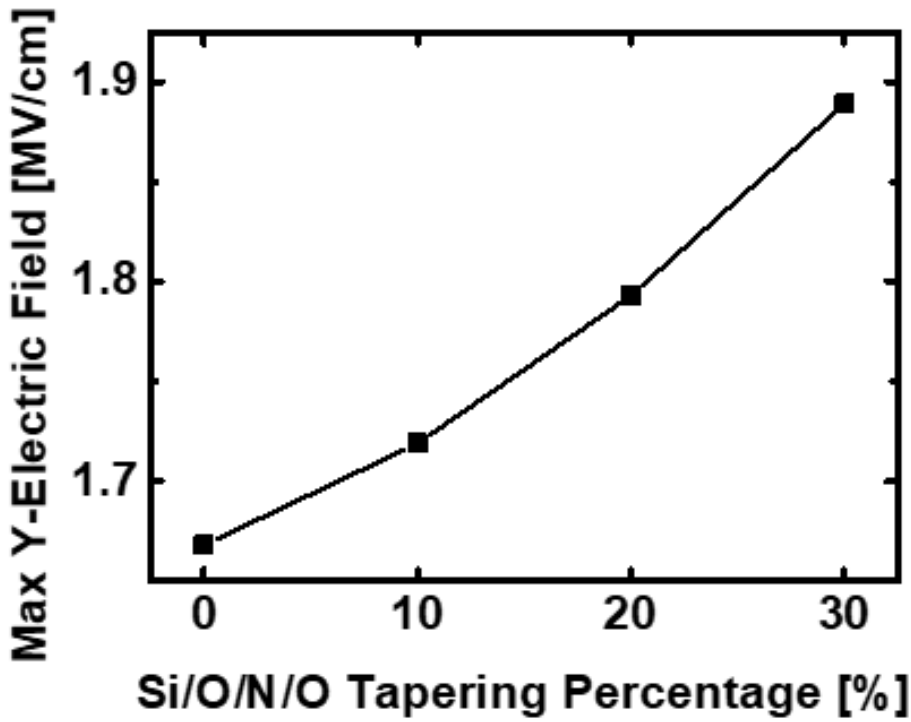
Figure 22 (a), (b), and (c) show retention characteristics and $|\Delta V_{th}|$ during 10 years of EPE mode in case of the Si/O/N/O tapering, and the maximum value of the electric field in y-direction felt by trapped electrons immediately after programming respectively. It can be seen that as the degree of Si/O/N/O tapering increases, the trapped holes increase, and the electric field in y-direction increases resulting in more reduction of the V_{th}.


4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
2.4
V_{th} [V]
EPE mode
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Retention Time [s]

(a)


1.48
1.46
1.44
1.42
1.40
1.38
$|\Delta V_{th}|$ during 10 years [V]
0
10
20
30
Si/O/N/O Tapering Percentage [%]

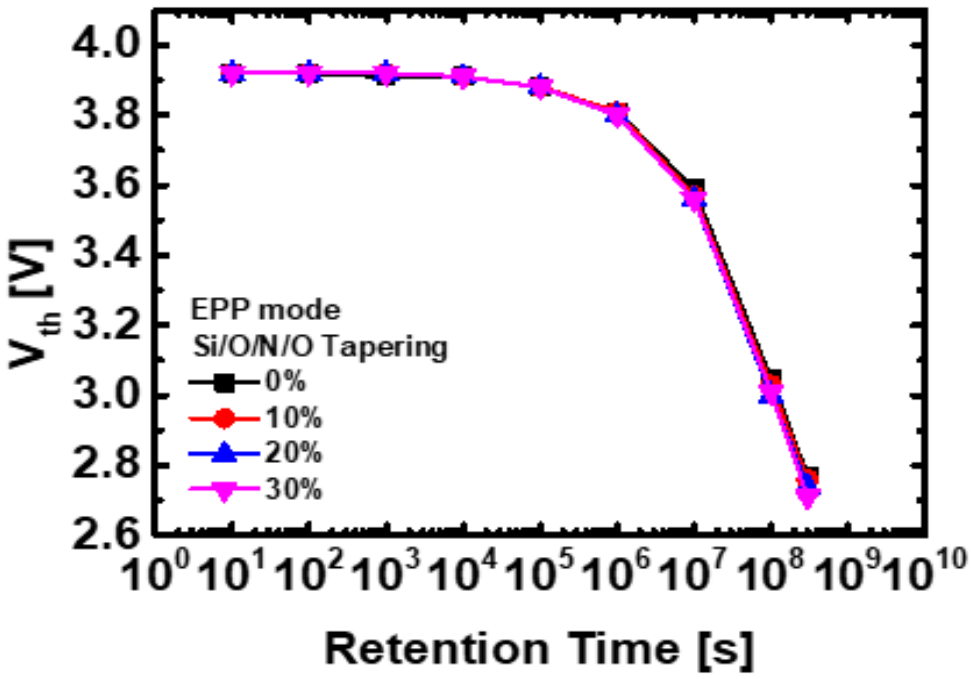
(b)



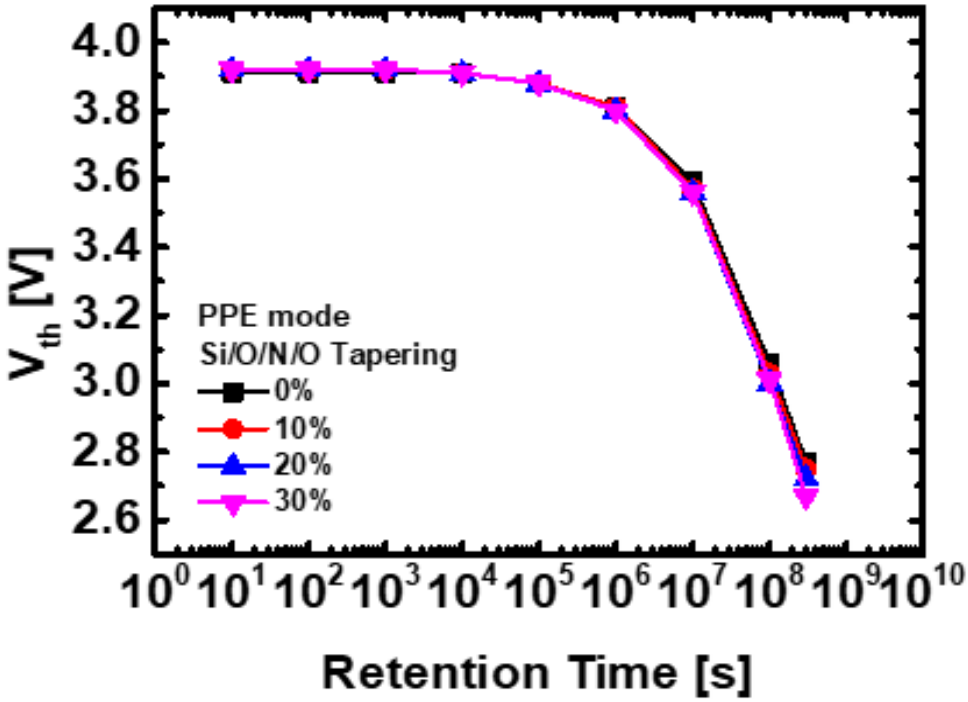
(c)

Figure 22. (a) V_{th} shift during retention time in EPE mode according to the Si/O/N/O tapering, (b) $|\triangle V_{th}|$ during 10 years and (c) the value of maximum electric field in y-direction right after programming

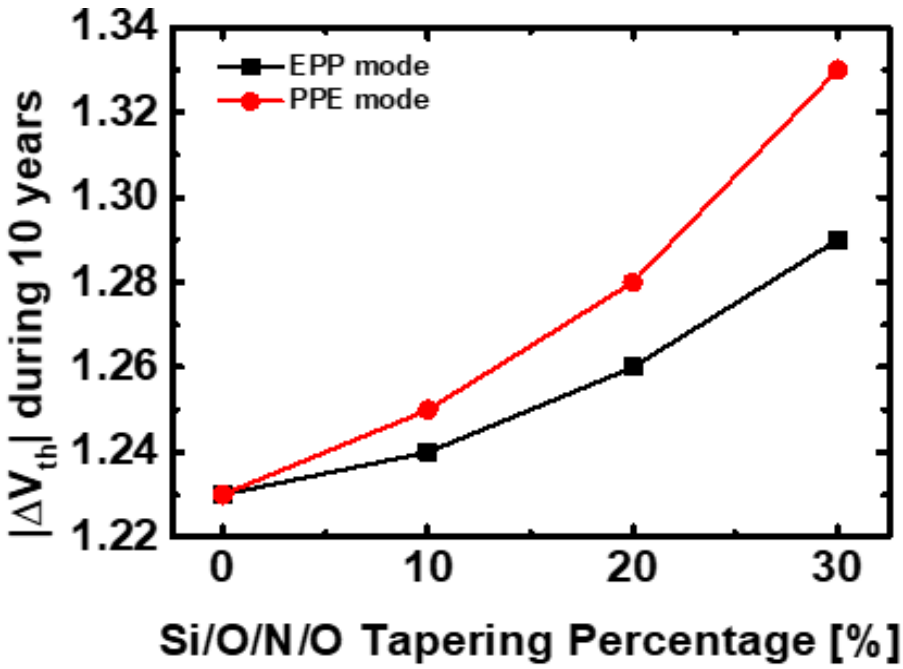
Figure 23 (a), (b), and (c) show the retention characteristics of EPP mode and PPE mode, and $|\triangle V_{th}|$ during 10 years in EPP mode and PPE mode respectively.


4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
V_{th} [V]
EPP mode
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Retention Time [s]

(a)


4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
V_{th} [V]
PPE mode
Si/O/N/O Tapering
0%
10%
20%
30%
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Retention Time [s]

(b)

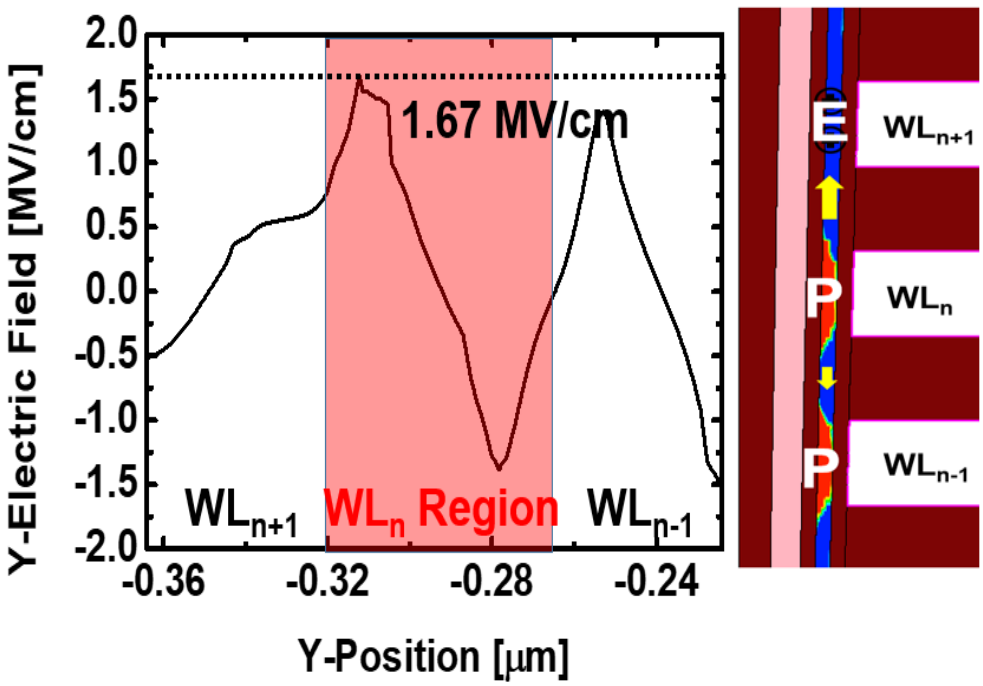


(c)

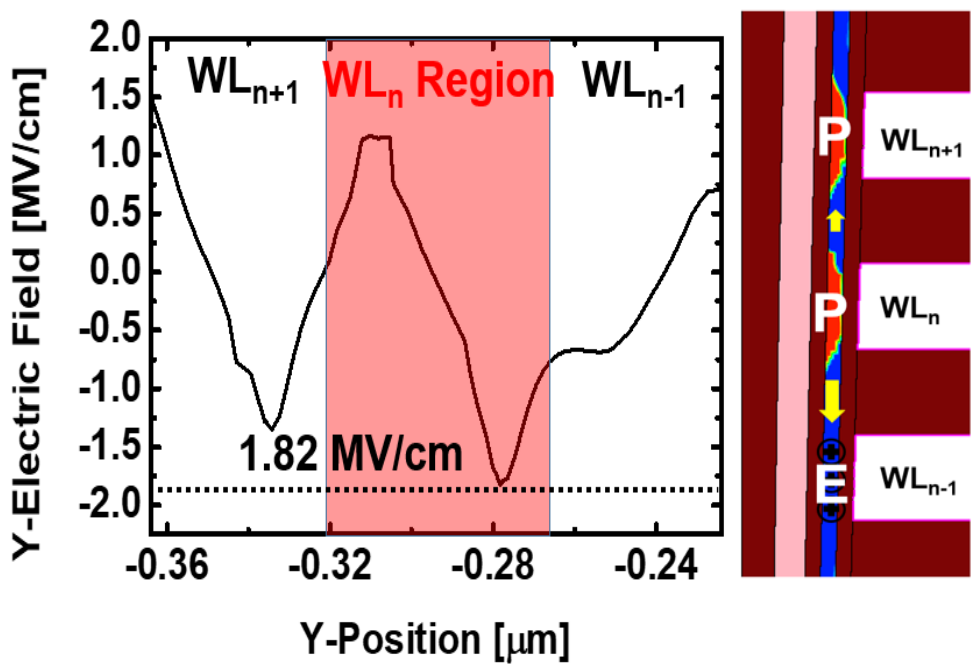
Figure 23. V_{th} shift during retention time according to the Si/O/N/O tapering (a) in EPP mode, (b) in PPE mode and (c) $|\triangle V_{th}|$ during 10 years in both cases

As mentioned above, the difference between the trapped hole concentrations of the upper and lower cells occurs, and thus the difference of the reduction of V_{th} between the EPP mode and the PPE mode occurs. As a result, the PPE mode showed more V_{th} reduction than that of the EPP mode. This is because as shown in figure 24 (a) and (b), the concentration of trapped holes resulted in a difference in electric field in y-direction immediately after programming. Previously, electrons tended to move upwards more easily structurally in neutral mode, but it was analyzed to show the following

characteristics after the erase operation as a result of much dominant to the formation of electric fields due to the concentration of trapped holes.



(a)



(b)

Figure 24. Electric field in y-direction right after programming versus y-position of simulation device with 30% Si/O/N/O tapering (a) in case of the EPP mode and (b) in case of the PPE mode

3.4 Conclusion

The electron trapped in the charge trap layer moves inside the nitride due to lateral electric field. This results in a charge loss and finally a data fail. In this paper, retention characteristics in the tapering device are investigated. Filler tapering did not affect the lateral movement of trapped electrons. However, in the case of Si/O/N/O tapering, as the tapering became more and more severe, the movement of electrons became less as the electric field felt structurally by the electron weakened, leading to a decrease in the reduction of V_{th} in NPN mode. In addition, when comparing the NPP mode and the PPN mode, the NPP mode has more V_{th} reduction than the PPN mode as the degree of the Si/O/N/O tapering becomes more severe. This confirmed that the trapped electrons were easier to move to the thicker side of the nitride because the electric field of the thicker side in the y-direction is larger structurally. Also, EPE mode, PPE mode, and EEP mode have been studied. When the

conventional GIDL erase was used in the tapering device, it was confirmed that as the degree of the Si/O/N/O tapering increases, the holes are trapped more. Also, the holes are trapped more in the memory cell located below. This resulted in a further decrease in V_{th} in EPE mode as the degree of tapering increased, and it was also confirmed that the reduction of V_{th} in PPE mode decreased more than that of the EPP mode. These are because the effect of the trapped holes is much dominant to form the electric field than the effect of the structure. In this way, the fluctuation of the retention characteristics, which is different from the existing ones without any tapering, comes as a reliability problem to be solved in 3D NAND.

4. Conclusion

The transition from 2D NAND to 3D NAND has many advantages, but it also has many disadvantages. Program disturbance and tapering issues are examples. Program disturbance in 2D NAND was solved by adding dummy WL because it occurred only at both ends of DSL and SSL. But in 3D NAND, the problem occurred in selected WL due to the unique channel potential characteristic named NLSB. This causes electrons to be generated due to BTBT inside the channel, and is unintentionally trapped in the charge trap layer due to hot carrier injection, changing V_{th} and causing data failure.

In addition, 3D NAND increases bit density by WL stacking. At the time, 3D NAND faces tapering problems as it becomes difficult to etch evenly. This shows a different retention characteristic from the conventional one without any tapering. In this paper, retention characteristics were identified by focusing on lateral migration. In the case of filler tapering, it did not affect lateral migration. However, in the case of Si/O/N/O tapering, the retention characteristics are quite changed. In NPN mode, the reduction of V_{th} decreased as the degree of the tapering increased. Also, when comparing the

NPP mode and the PPN mode, the NPP mode has more V_{th} reduction than the PPN mode. It was found that trapped electrons were easier to move toward thicker nitride. This is because of the larger electric field in the direction of the thicker side. Also, in EPE mode, the more holes are trapped as the degree of the tapering increases. As a result, the reduction of V_{th} increases as the degree of the tapering increases. Also, in EPP mode and PPE mode, the PPE mode has more V_{th} reduction than the EPP mode. It was because holes are more trapped in the memory cells below. These reliability issues which are different from the conventional flash memory without any tapering are problems that need to be solved in 3D NAND.

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초 록

2D NAND에서 **3D NAND**의 변화는 여러가지 장점을 가져왔지만 새로운 문제점들 또한 발생하였다. 그 중에 하나가 **hot carrier injection**에 대한 **program disturbance**였다. **Program disturbance**는 **boosting channel potential**의 전압 차이에 의해 **unselected string**에서 의도치 않게 전자가 **charge trap layer**로 **trap**되어 V_{th} 변화를 일으키는 문제를 의미한다. **2D NAND**에서는 이러한 문제가 **drain selection line(DSL), source selection line(SSL)**이 존재하는 양끝 부분에 **dummy cell**을 추가함으로써 해결하였다. 그러나 **3D NAND**에서는 **2D NAND**와는 다른 **natural local self-boosting(NLSB)**이란 독특한 **boosting channel potential** 특성 때문에 선택된 **word line(WL)**에서도 문제가 발생한다. 이 논문에서는 이러한 문제의 **mechanism**을 연구하였다. **3D NAND**에서는 선택된 **WL**의 **boosting potential**이 선택되지 않은 **WL**의 **boosting channel potential**보다 높게 형성된다. 그 결과 큰 전기장이 **selected WL** 근처에서 형성되고 **band-to-band tunneling(BTBT)**가 발생한다. **BTBT**로 생성된 전자가 수평 전기장으

로 큰 에너지를 얻을 수 있게 되고 마침내 tunneling될 충분한 수직 전기장을 얻게 되면 선택된 WL의 charge trap layer안으로 trap될 수 있게 된다. 이는 의도치 않은 Vth 변화를 일으켜 결과적으로 data fail을 일으켜 신뢰성 문제를 일으킬 수 있다. 3D NAND의 또 다른 문제는 Tapering에 관한 문제이다. Tapering이란 WL stacking으로 bit density를 높이는 3D NAND에서 etching을 고르게 하는데 어려움을 겪어서 생기는 문제이다. 이 논문에서는 tapering 소자에서의 lateral migration에 의한 retention 특성을 관찰하였다. 결과적으로 filler tapering은 lateral migration에 영향을 주지 않았지만, Si/O/N/O tapering의 경우, retention 특성에 꽤 많은 변화를 주었다. NPN mode의 경우, trap된 electron이 느끼는 전기장이 tapering이 심해지면 심해질수록 작아져 결과적으로 V_{th}가 더 적게 감소되었다. 또, NPP mode, PPN mode를 통해 tapering 소자에서 trap된 전자는 nitride의 두께가 더 두꺼운 부분으로 움직이기 더 수월하다는 것을 확인하였다. 또, EPE mode의 경우, tapering이 심해지면 심해질수록 channel 반지름 감소로 인해 hole이 더 많이 trap됨에 따라 전기장

이 증가하여 결과적으로 V_{th} 감소가 더 많이 일어났다. **EPP mode**와 **PPE mode**를 비교하였을 때에는, 아래에 위치한 셀일수록 **hole**이 더 많이 **trap**됨에 따라 **PPE mode**에서의 V_{th} 감소가 **EPP mode**보다 더 많이 일어나는 것으로 관찰되었다. 이 같은 특징들은 기존의 **tapering**이 없는 **device**와는 다른 **retention** 특성을 보여준다. 이러한 다른 특징들은 작은 V_{th} **margin**을 가지고 있는 **multi-level cell**의 **flash memory**에 있어서 중요한 신뢰성 문제로 다가온다.

Keyword: 3D NAND, program disturbance, hot carrier injection, tapering, retention, lateral migration

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