공학박사 학위논문

Electrohydrodynamic Jet-Printed Transistors and Applications with Single-Walled Carbon Nanotubes

정전기수력학 인쇄를 활용한 단일벽 탄소나노튜브 기반 트랜지스터 및 응용

2020 년 8 월

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Abstract

Electrohydrodynamic Jet-Printed Transistors and Applications with Single-Walled Carbon Nanotubes

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As the demand and research for electronic devices on flexible and stretchable substrates gradually continues comparable to the conventional rigid silicon-based electronic devices, interest in new semiconducting materials capable of low-temperature processes and large-area processes is increasing. Single-walled carbon nanotube (SWCNT) is one of the representative materials satisfying the new interests thanks to its excellent electrical and mechanical properties. SWCNT can be advantageous for non-vacuum, low-temperature, and large-area processes in response to various solution processes such as dipping, inkjet printing, and gravure printing. For high-

performance devices with low power consumption based on next-generation electronics, the demand for ultra-fine patterning technology based on the solution process is also increasing.

In this thesis, SWCNT-based all electrohydrodynamic-jet (E-jet) printing system was established, a SWCNT-based thin-film transistor (SWCNT-TFT) with a channel length of 5 microns was implemented through the system. In addition, by developing and grafting technology to control the threshold voltage of SWCNT-TFTs based on the solution process, we have demonstrated highly integrated and high-resolution SWCNT-based applications including logic gate, pixel circuits for image detector and display. In addition to the micrometer scale fine pattern technology by the E-jet printing system, a new solution process-based vertical stacking technology is also introduced to further improve the transistor density, enabling high-resolution, highly integrated electronic applications in a continuous environment without any vacuum or high temperature process. The technology introduced in this thesis for high performance, high resolution, and high integration of SWCNT-based devices makes it possible to fabricate a 250 pixel per inch active matrix backplane utilizing only the solution process.

Keyword: single-walled carbon nanotube (SWCNT), thin-film transistor (TFT), electrohydrodynamic jet printing, active pixel

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Chapter 1

Introduction

1.1 Single-Walled Carbon Nanotubes

Semiconducting single-walled carbon nanotubes (SWCNTs) made of a single layer of the carbon nanotube have attracted a great deal of attention as semiconducting materials of future nanoelectronics devices thanks to their unique mechanical, chemical, optical, and electrical characteristics. Figure 1.1 introduces the key features of SWCNTs used in various fields. Carbon nanotubes have a unique structure in which carbon atoms are combined into a one-dimensional cylindrical shape. Unlike graphene with two-dimensional form or fullerene with three-dimensional form of carbon, the carbon nanotube is rolled in a specific direction, called a chiral vector, and the diameter of the cylinder and the arrangement of the carbon atoms change depending on the length and direction of the vector. Especially, it is important to determine whether SWCNT has metallic or semiconducting properties according to the chiral vector. More details are described in Section 1.2.

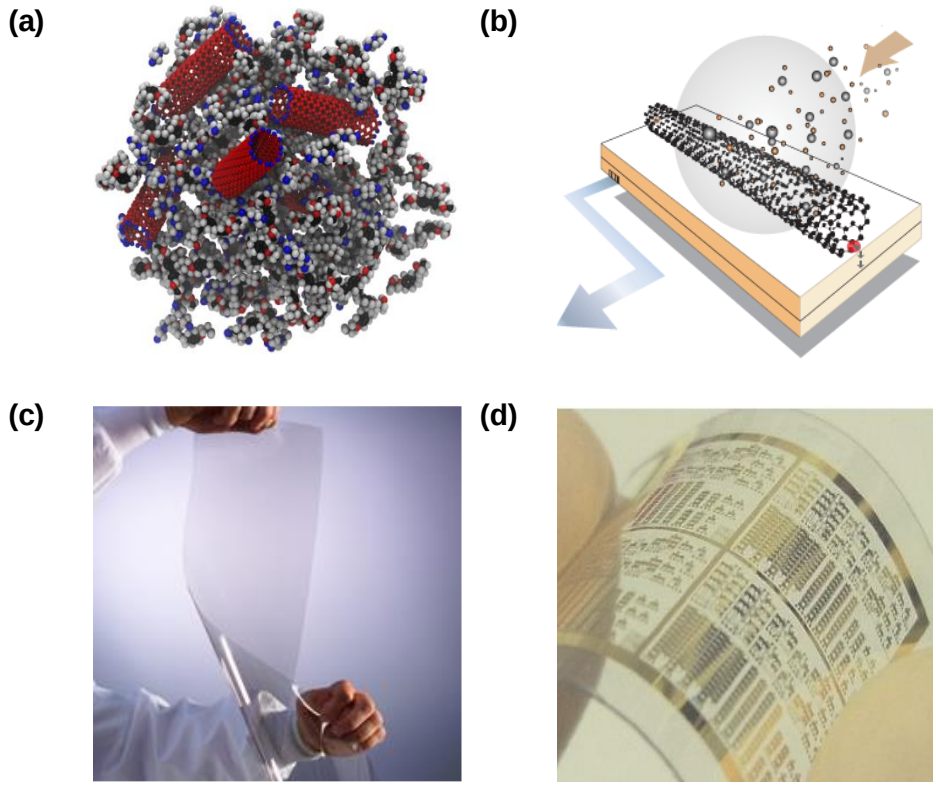

Figure 1.1 Applications in various fields with SWCNTs. (a) Nanocomposite with enhanced mechanical properties by mixing SWCNTs [1]. (b) SWCNT-based chemical sensor that detects changes in electrical properties in response to external chemicals [2]. (c) SWCNT-based transparent electrode film [3]. (d) Integrated circuits using SWCNT-based transistors [4].

Mechanical features SWCNTs have outstanding tensile strength because of their tight nanostructure and binding force among carbon atoms composed of only sp^2 bonds. Young's modulus of SWCNT is a very high value above 100 GPa, indicating that SWCNT is one of the strongest materials in terms of tensile strength in the

axial direction [5]. On the other hand, SWCNT is relatively of elasticity in the radial direction of the nanotubes. Using these unique mechanical properties, many studies have been reported to increase elasticity or strength in combination with epoxy polymers or other nanomaterials as shown in Figure 1.2 (a) and (b) [6]. Applications such as flexible pressure sensors that combine the unique mechanical properties of CNT with the electrical properties of SWCNT to be described later are also reported, as shown in Figure1.2 (c) [7].

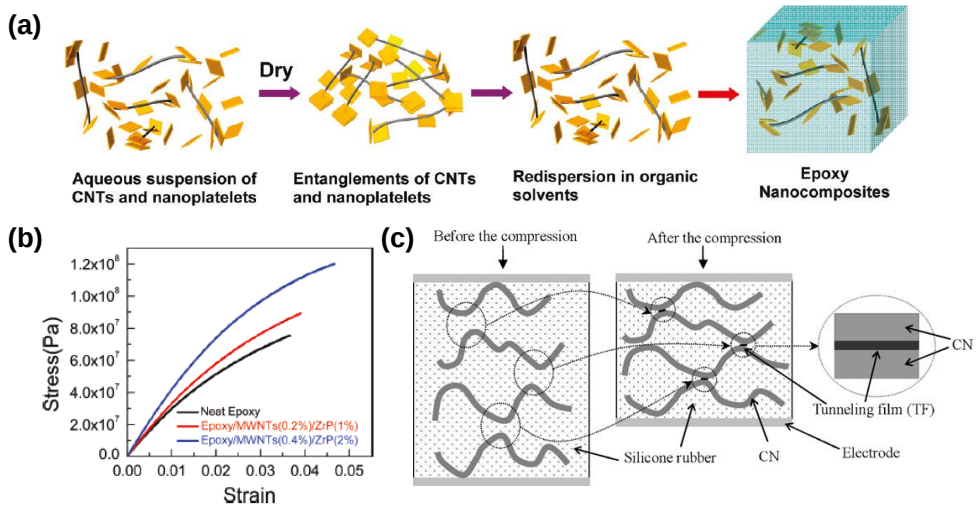

Figure 1.2 (a) Epoxy nanocomposite fabrication process with enhanced tensile properties through CNT addition and (b) its stress–strain curve [6]. (c) Pressure sensor utilizing mechanical and electrical properties of CNTs [7].

Chemical sensing properties SWCNT changes the electrical characteristics depending on the type of attachment of various chemicals on the surface of the nanotubes. In this regard, research

on chemical modification of nanotubes has also been conducted [8]. For example, research into CNT grafting in various chemical sensing devices has been actively studied, including bio-chemicals such as glucose [9], DNA [10] and environmental chemicals including humidity [11], hydrogen sulfide [12], carbon monoxide [13], and acidity [14] (see Figure 1.3). Thanks to the sensitive nature of SWCNT's conductance which changes even at very low concentrations of tens of ppm, it can be used in next-generation wearable skin-attached glucose detection sensors and human body mimicking chemical sensor.

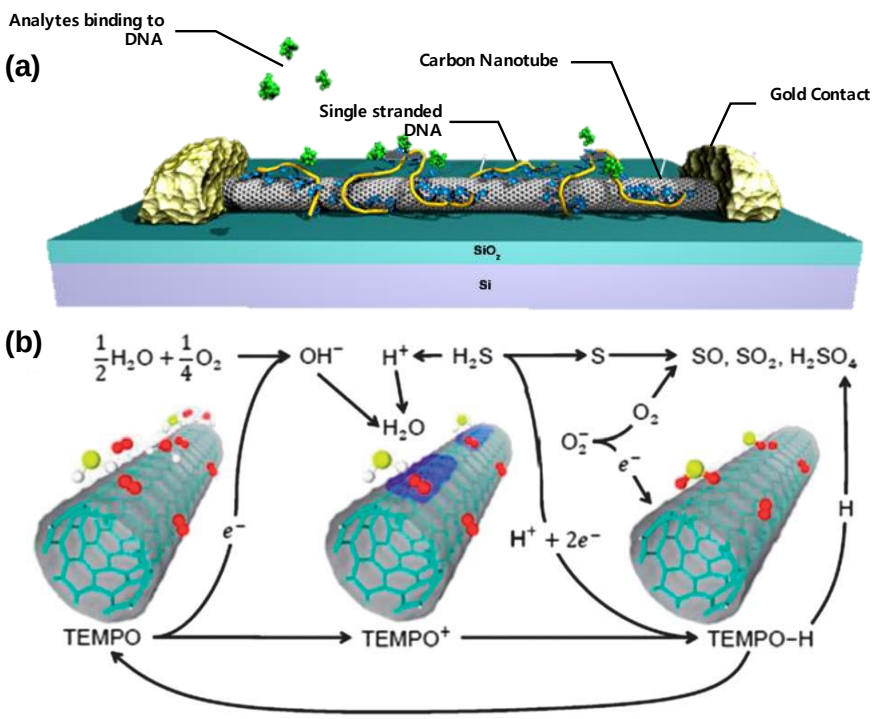

Figure 1.3 (a) DNA detecting device based on SWCNT [10]. (b) Chemical Reaction Mechanism between hydrogen sulfide (H_2S) and CNT [12].

Optical properties In terms of optical characteristics, SWCNT has a unique optical feature that is suitable for transparent electronic devices. In visible light areas at 400 to 700 nm wavelengths, the light absorption rate of the SWCNT is very low, and the photoresponse is slightly shown in some infrared (IR) regions as shown in Figure 1.4 (a) [15]. Using these characteristics, some studies and applications have been conducted and reported about IR sensors based on SWCNT [15], [104], [105]. Also, the diameter of nanotubes is very thin with several nanometers, and the thickness of the film is also stacked on a nanometer scale, resulting in a transmittance of more than 80 percent in the general visible light area (see Figure 1.4 (b)) [16]. Therefore, studies on transparent electrodes using metallic SWCNTs or transparent transistors using semiconducting SWCNTs having little reactivity to light have been reported [17].

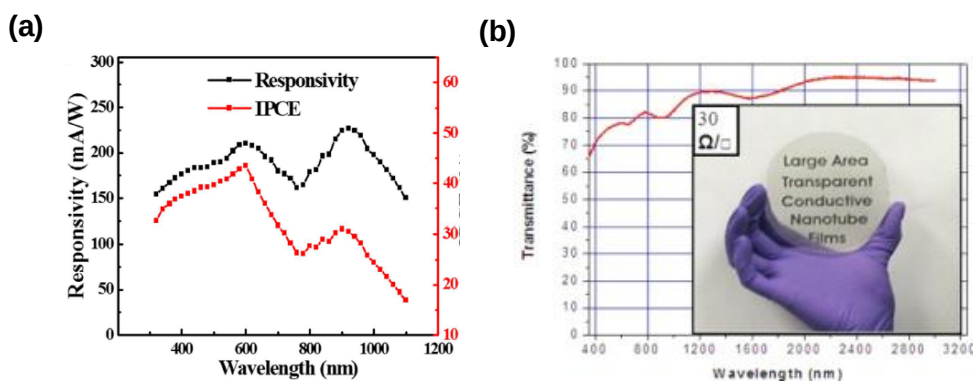

Figure 1.4 (a) photoresponsivity of SWCNT. It shows weak reactivity in some infra-red regions (630 nm & 980 nm) [15]. (b) CNT-based transparent conductive film [16].

Electrical features Above all, a single SWCNT exhibits excellent electrical properties such that the theoretical carrier mobility can reach about 100,000 $cm^2/V \cdot s$ [18]. Generally, solution-process based SWCNT consists of a random network structure that is woven into several strands rather than a single nanotube. In this case, the mobility is reduced to 1 to 100 $cm^2/V \cdot s$ because the contact resistance at the junctions between the nanotubes works greatly [4]. Nevertheless, with comparing mobility in various semiconductor materials shown in Figure 1.5, this mobility is comparable to that of oxide materials such as indium-gallium-zinc oxide, which exhibit higher electrical characteristics than conventional amorphous silicon or organic semiconductor materials. Moreover, recently reported SWCNT-based transistors show high on-off current ratio of over 100,000 as well as high mobility [19]. Thus, solution processed SWCNT has the advantage of being able to take both high electrical performance and process benefits because it is easily deposited in the solution process at room temperature.

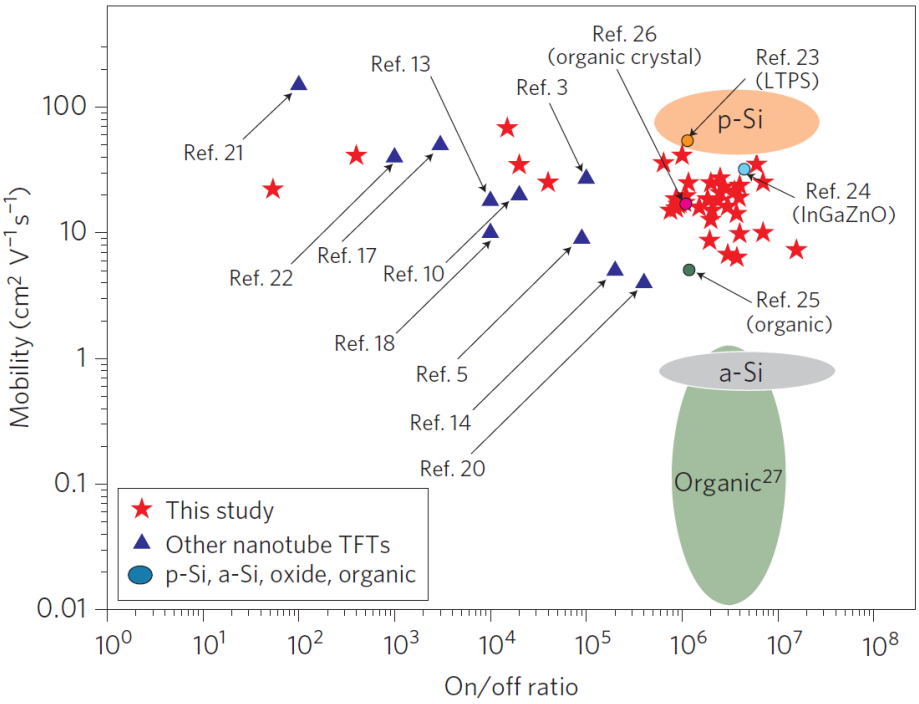

Figure 1.5 A diagram comparing the mobility and on/off current ratio of Silicon, organic, oxide, and SWCNT [4].

Consequently, SWCNT has attractive features as a next-generation flexible electronic material in mechanical, chemical, optical, and electrical properties. There are some issues to be explained later, but thanks to its excellent electrical properties and easy processability at room temperature, SWCNT has been noted as much as polymer-based organic semiconducting materials or oxide semiconducting materials that have been widely used as materials for next-generation flexible transistors. This dissertation covers the entire production of high-resolution and highly integrated solution-processed SWCNT-based circuits including logic circuit and active pixel circuit incorporating electrohydrodynamic jet-printing (E-jet

printing), one of the printing technologies capable of ultrafine patterns, from the manufacture and analysis of solution processed SWCNT thin film transistors (SWCNT-TFTs). The technologies necessary for the fabrication of SWCNT-TFT based on the low-temperature solution process are covered in Chapter 2 and SWCNT-TFT incorporating E-jet printing and the technologies for high-intensity circuits are described in Chapters 3 and Chapter 4. Specifically, to find out the issues arising from the solution process-based SWCNT-TFT, it is necessary to understand the specific electrical properties of SWCNT, and the contents are described in the next sections.

1.2 Band structure of SWCNTs

1.2.1 Energy bandgap of SWCNTs

As mentioned above, carbon nanotube is a form in which a sheet of graphene is rolled in the direction of a specific vector called a chiral vector, as shown in Figure 1.6. A so-called (n,m) carbon nanotube has the below chiral vector $\vec{C}$.

$$\vec{C} = n\overrightarrow{a_1} + m\overrightarrow{a_2} \tag{1.1}$$

$\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ are graphite primitive lattice vectors with $|\overrightarrow{a_1}| = |\overrightarrow{a_2}| = a$. When n and m are equal, SWCNT has an armchair-type symmetric structure, and when m is zero, it is called as zigzag nanotube.

For energy band diagram analysis of SWCNTs, E−k diagrams can be obtained by applying the tight−binding Schrödinger equation to SWCNT [20], and in case of armchair type SWCNT, the dispersion relation is shown in Equation 1.2.

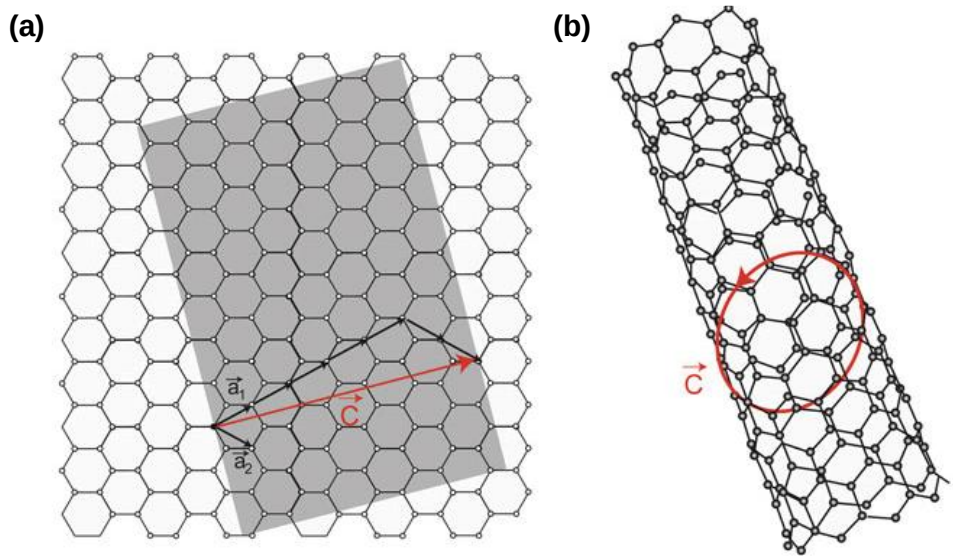

Figure 1.6 (a) The unrolled two−dimensional graphene sheet lattice of a (5,2) tube. Carbon atoms in the shaded region are rolled in the direction of the chiral vector, forming the nanotube structure in (b).

$$E = \pm\gamma_1(1 + 4t\cos\frac{\mu\pi}{n}\cos\frac{ka}{2} + 4t^2\cos^2\frac{ka}{2})^{1/2} \qquad (1.2)$$

μ is quantum number, and $\gamma_i\ (i = 1,2,3)$ is a hopping parameter between three carbon atoms adjacent to one carbon atom. For the above armchair nanotube, γ_1 represents the hopping integral among the two carbon atoms in the direction of the chiral vector, and t is the ratio between the hopping integral γ_1 and γ_2 (or γ_3) which means hopping integral in other direction ($t = \gamma_2/\gamma_1$). Due to the

curvature effect, γ_1 is less than γ_2 or γ_3, so t is greater than 1. From Equation 1.2, continuous energy levels are shown in the Brillouin zone edge, so a zero-energy bandgap can be directly obtained, which means that armchair-type SWCNTs are metallic nanotubes.

On the other hand, in the case of a (n, 0) or zigzag nanotube, energy is expressed as Equation 1.3.

$$E = \pm\gamma_2(1 + 4t\cos\frac{\mu\pi}{n}\cos\frac{\sqrt{3}ka}{2} + 4t^2\cos^2\frac{\mu\pi}{n})^{1/2} \quad (1.3)$$

In Equation 1.3, t is γ_1/γ_2, γ_2 is a hopping parameter in a direction perpendicular to the chiral vector direction, and γ_1, γ_3 are hopping parameters in other directions. Like the armchair nanotube, due to the curvature effect, γ_2 is greater than γ_1 or γ_3, so t is less than 1. From Equation 1.3, the energy gap is accurately derived given by

$$E_g = 2\gamma_2\left|1 - 2t\cos(\frac{\pi}{3} - \frac{qa}{3d})\right|, \quad (1.4)$$

where d is the diameter of the tube and $q = 0, \pm 1$ is the remainder of n divided by 3. When q is 0, the energy band gap has a value of 0 or very small depending on the value of t.

In the case of SWCNTs with general random chiral vectors, not the above two special nanotubes, the ratio of hopping integral (t) can be approximated to 1. Through an appropriate approximation of Equation 1.4, the energy bandgap when q is not 0 can be obtained as in Equation 1.5.

$$E_g = \frac{2\gamma a_{cc}}{d} \quad (1.5)$$

a_{cc} is the distance between two adjacent carbon bonds, and d is the

diameter of the nanotube. Generally, the a_{cc} and γ within SWCNTs are measured at about 0.14 nm and 3 eV. The energy bandgap of the semiconducting SWCNT shows an inversely proportional property to the diameter of the nanotube, for example, SWCNT having a diameter of about 1.4 nm shows an energy bandgap of about 0.6 eV. Consequently, in natural SWCNTs, the ratio between the metallic species and semiconducting species is 1:2.

1.2.2 Density of states for SWCNTs

SWCNT is a cylindrical tube structure, but since the length of the tube is overwhelmingly different from the diameter, it can be generally classified as a semiconductor of one-dimensional nanostructure [21]. The density of states (DOS) in a one-dimensional type of semiconductor material shows a characteristic of gradually decreasing with energy after showing a discontinuous value of density of states at a specific energy point like an edge of conduction band or valence band. As shown in Figure 1.7, in density of states, these kinks are called van Hove singularities (vHs), and the energy bandgap of SWCNTs derived in Section 1.2.1 can be seen as the difference (E_{11}) between the first vHs of valence band (V_1) and the first vHs of conduction band (C_1). As shown in the graph, it can be observed that even after the first vHs, as energy increases, there are other vHs with higher DOS. This is because SWCNT is not just a one-dimensional material but a three-dimensional nanotube structure, and therefore quantized vHs exist inside the conduction

and balance band. In the case of metallic species of SWCNTs, there are slightly constant density of states even in the first energy bandgap, E_{11}, and in the case of semiconducting species of SWCNTs, there is almost no DOS inside E_{11}.

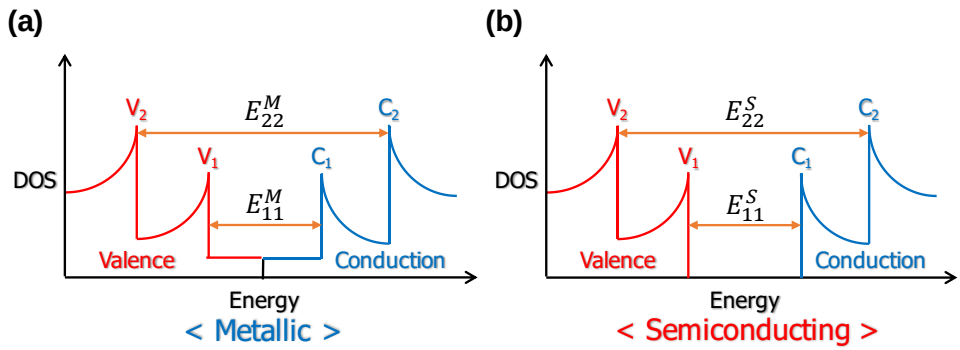

Figure 1.7 Density of states for (a) metallic and (b) semiconducting SWCNTs.

As derived from Equation 1.5, the energy bandgap of SWCNT is inversely proportional to the diameter of the nanotube. It can also be applied to the several energy bandgaps shown in the DOS diagram above. A graph relating the energy bandgaps in SWCNTs and their diameter is Kataura plot as shown in Figure 1.8 [22]. In the following graph, the energy bandgaps in metallic SWCNT are represented as M_{11}, M_{22}, M_{33} marked in black, whereas the energy bandgaps in semiconducting SWCNT are expressed as S_{11}, S_{22}, S_{33} marked in red. The energy bandgaps represent a quantumized distribution in nanotubes with similar diameters. Also, depending on the energy, semiconducting and metallic species in SWCNTs can be

clearly separated. Based on the understanding of SWCNT's unique energy bandgap distribution shown in the Kataura plot, it is possible to estimate how much semiconducting and metallic species are distributed in the deposited SWCNT networks.

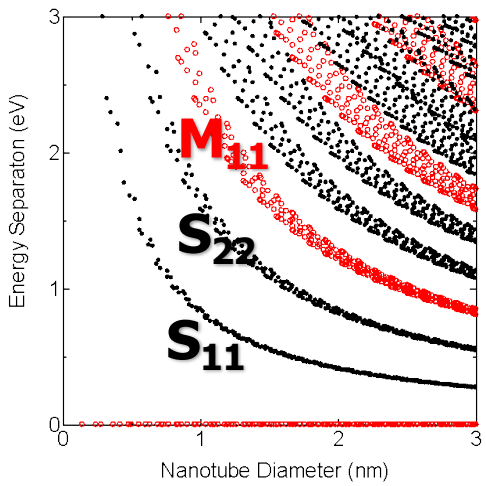

Figure 1.8 Kataura plot showing the relationship between the diameter and energy bandgaps of SWCNTs [22].

1.2.3 Detection for classifying species of SWCNTs

In general, both semiconducting nanotubes and metallic nanotubes exist in any deposited SWCNT network. Resonance Raman spectroscopy measurement is mainly used to confirm the quantitative ratio between semiconducting CNT and metallic CNT inside the SWCNT film. When a photon with a specific energy that causes electronic transition is injected into SWCNTs, resonance and scattering are generated within the nanotubes, and then the photon is

released again. and the energy difference is simultaneously observed. At this time, the frequency difference of the photon before and after the incident is measured, and this is called a Raman shift (see Figure 1.9 (a)).

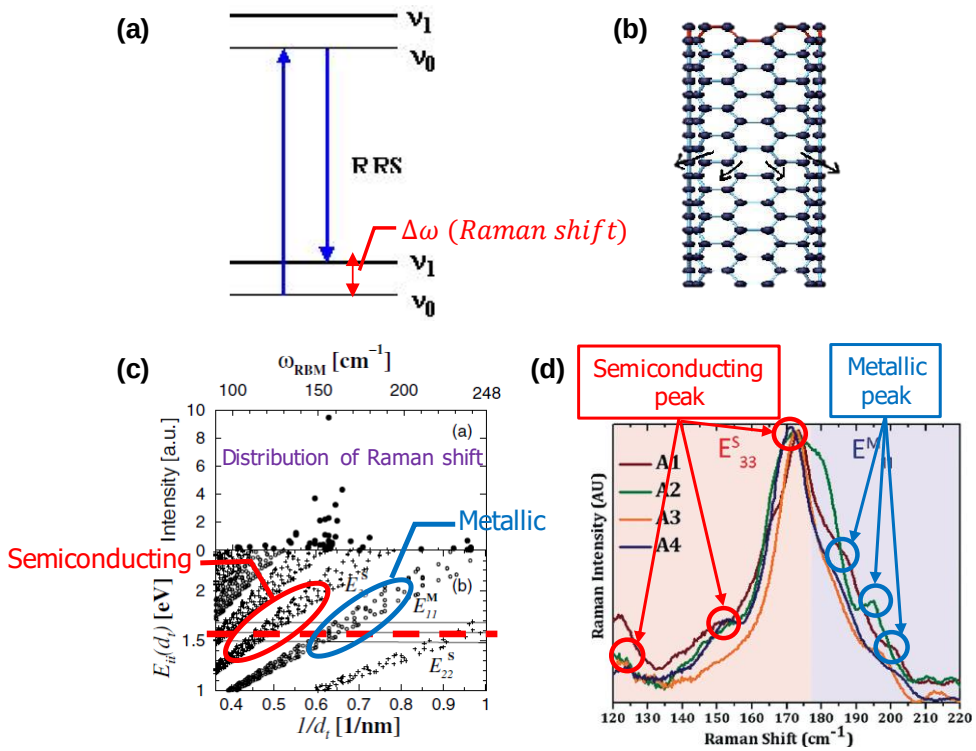

Figure 1.9 (a) resonance Raman spectroscopy to detect the energy difference of a photon between before and after incident. (b) SWCNT resonating in the radial direction of the nanotube. (radial breathing mode; RBM) (c) The relationship between the Raman shift in RBM of SWCNTs and the diameter and energy bandgaps of nanotubes [23]. (d) The peaks of the Raman shift can be detected in the SWCNT film deposited through resonance Raman spectroscopy measurement, and the ratio of the semiconducting species and metallic species can be estimated by referring to (c) [24].

In the resonance Raman spectroscopy measurement of SWCNT, Raman scattering resonating in the radial direction of the nanotube called radial breathing mode (RBM) is mainly observed as shown in Figure 1.9 (b), and the Raman shift at this time shows a property inversely proportional to the diameter of the nanotube [23]. In Section 1.2.2, the relationship between the diameter of nanotubes and the energy bandgaps can be identified through the Kataura plot, combining which can lead to the relationship between energy bandgaps of the nanotubes and the difference in frequency of Raman shift detected in resonance Raman spectroscopy measurements as shown in Figure 1.9 (c). The energy bandgaps of SWCNTs are proportional to the reciprocal of the diameter of the nanotube and the frequency of the RBM, and the energy distribution is clearly classified according to the type of the nanotube species. As a result, using the resonance Raman spectroscopy measurement, it is possible to detect the peaks of the Raman shift in the RBM region in any deposited SWCNT film, and by classifying the frequency region where each peak is located, semiconducting and metallic species inside the network of the SWCNTs can be detected and compared more quantitatively (see Figure 1.9 (d)) [24].

1.3 Sorting out semiconducting SWCNTs

SWCNTs produced by arc-discharge, laser-ablation, or catalytic chemical vapor deposition are generally unsorted, with 33% of metallic species and about 67% of semiconducting species. In order to utilize SWCNTs as electronic applications, it is necessary to separately classify metallic or semiconducting species, not unsorted nanotubes. There are two main ways to sort out semiconducting nanotubes from unsorted SWCNTs. The first method is to form an unsorted SWCNT network first, and then leave only semiconducting species, and the second method is to separate only semiconducting nanotubes before deposition and then form the networks of the semiconducting SWCNTs. This section describes how to separate only semiconducting nanotubes from unsorted SWCNTs.

1.3.1 Pre-deposition of the nanotubes and sorting later

Using the electrical characteristics of SWCNTs that the electrical conductivity of metallic nanotubes is much higher than that of semiconducting nanotubes, it is possible to burn out only metallic nanotubes by passing a high current through an as-grown SWCNT network [25]. The advantage of this method is that it can be applied to an array composed of long nanotubes larger than 100 ㎛. In addition, a pre-aligned SWCNT network can be secured when CNT initially grows by CVD, etc., and then a classification process can be

followed to secure a well-aligned SWCNT array that shows high electrical performance. If such an aligned semiconducting SWCNT array is used, it is easy to implement a SWCNT-based transistor array with high mobility and high on/off current ratio. This well-aligned semiconducting SWCNT array helps to realize a SWCNT based transistor array with high mobility, high on/off current ratio, and high reliability.

A thermo-capillary flow method is also used to obtain a higher quality sorted semiconducting SWCNT array [26]. After coating a photoresist on an unsorted SWCNT array, applying a current in the SWCNT networks generates Joule heat in the SWCNTs. A fine thermo-capillary flow flows along the metallic nanotubes, and the photoresist around the nanotubes melts to expose the metallic nanotubes as shown in Figure 1.10. Subsequently, a high-purity semiconducting SWCNT array is obtained through an etching process of a metallic species and a development of the photoresist.

However, in the post-separation method, uniformity due to residual metallic nanotubes or debris during the purification process becomes an issue. In addition, since it is a method applied to as-grown SWCNT array, the complexity of the overall process is increased since a separate classification process is performed. For example, a transfer process may be required to apply on various substrates such as glass, plastic, metal foil, elastomer, and paper.

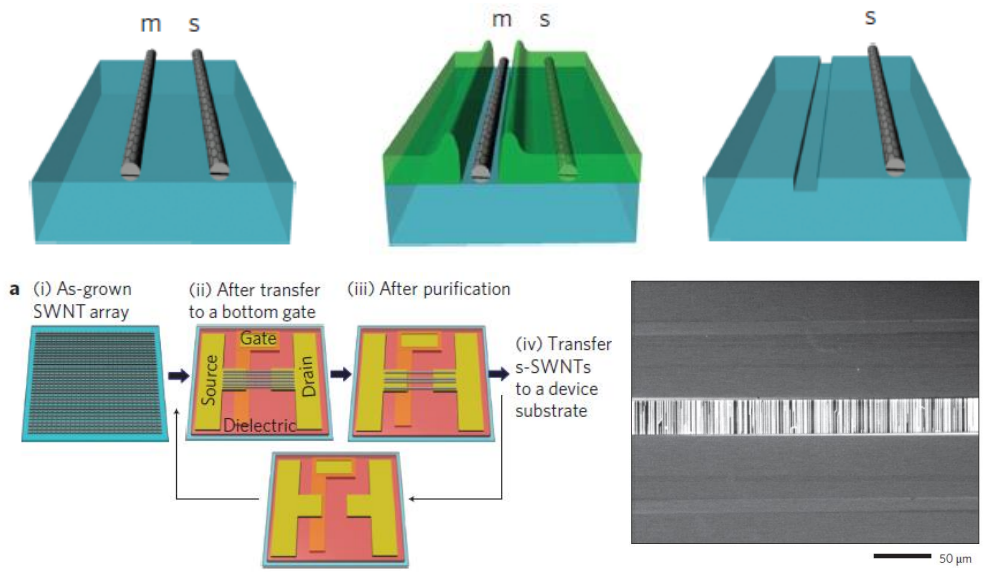

Figure 1.10 Acquisition process and result image of aligned semiconducting SWCNT array using thermo-capillary flow method. 'm' and 's' indicate metallic and semiconducting nanotubes, respectively [26].

1.3.2 First sorting out SWCNTs and deposition later

To obtain a SWCNT film composed of only metallic or semiconducting species, the method of obtaining pre-separated SWCNTs and then depositing them, rather than the post-separation method introduced in Section 1.3.1, is widely used. After dispersing the bulky SWCNT obtained through SWCNT production technology such as a CVD process into a solution, an un-sorted SWCNT dispersion can be obtained with the aid of polymers or surfactants. Subsequently, when a centrifugal separator using a strong centrifugal force of 200,000 g or more is applied, a buoyancy difference occurs according to the

diameter of each CNT in the dispersion, so the layers according to the thickness of the CNTs are generated. As shown in Figure 1.11 (a), this separation method is called a density gradient ultracentrifugation (DGU) method [27].

In addition, there is a method of separating SWCNTs by wrapping DNA or polymer on the outside of SWCNTs as shown in Figure 1.11 (b). Through the $\pi - \pi$ interaction between the polymer and SWCNT, the polymer wraps around the nanotubes, and the binding strength varies depending on the chirality of the SWCNT [28]. Then, after column chromatography and checking the absorption spectra, the spectrum is clearly separated according to the chirality of the nanotubes, and a separated SWCNT solution can be obtained. A high purity isolated SWCNT dispersion through polymer assisted sorting method can be obtained [29]. However, it is more expensive than the DGU method and has difficulty in mass production.

The solution process-based technologies for separating SWCNTs introduced above provide process flexibility by lowering the overall complexity of the SWCNT-based device fabrication process compared to the post-separation method in Section 1.3.1. Since it is possible to supply the separated SWCNTs in solution, it is also advantageous for mass production and commercialization. Currently, high-purity separated SWCNT dispersions are sold by NanoIntegris corporation. Using the separated semiconducting SWCNT dispersion, SWCNT-based transistors can be fabricated on various substrates at low temperatures, and many related studies have been reported to date.

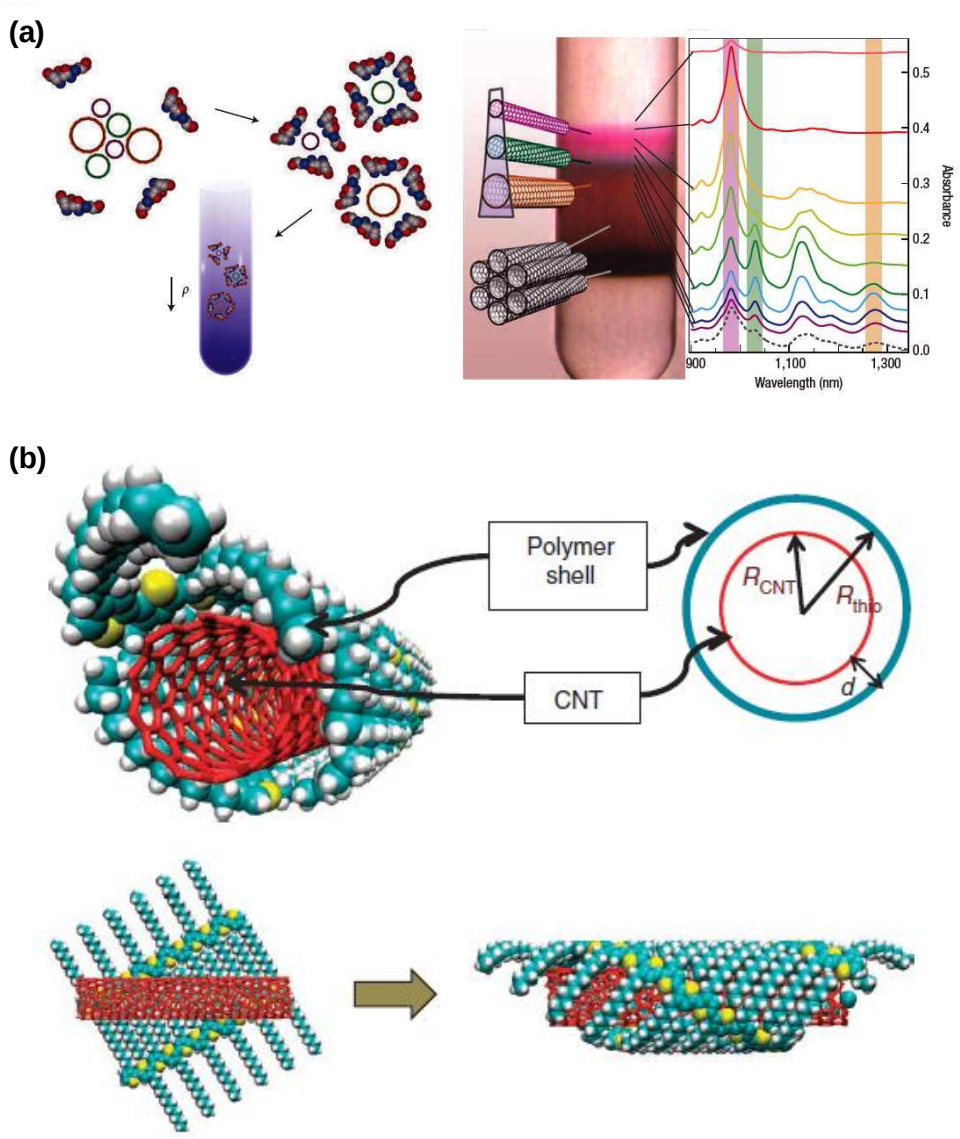

Figure 1.11 (a) Separation of SWCNTs by density gradient ultracentrifugation method. Layers are divided according to the diameter of nanotubes [27]. (b) Separation of SWCNTs through Polymer assisted sorting method [29].

However, when the SWCNT network is formed through the separated SWCNT dispersion, nanotubes are usually distributed in a random direction without specific orientation. This randomly arranged nanotube network is a factor that significantly degrades the electrical performance of SWCNTs-based devices. In addition, external elements, such as surfactant, present in the dispersion may remain on the film, causing a hysteresis of the transistor or impeding electrical stability, which could interfere with normal operation. To compensate for these issues, methods of aligning SWCNTs in the solution process may be necessary, and the rinsing process to reliably remove residual nanotubes and surfactants in the deposited SWCNT film is also important.

1.4 Operation of SWCNT-TFTs

In this section, the electronic transport properties of single-walled carbon nanotubes-thin film transistors (SWCNT-TFTs) will be discussed. Unlike conventional TFTs, such as amorphous silicon or poly silicon based TFTs, the source and drain electrodes located at both ends of the channel through which a charge travels are in direct contact with the nanotube when fabricating SWCNT-based transistors. In case of fabricating the transistor using the semiconducting SWCNT dispersion mentioned in Section 1.3.2, there are numerous nanotubes in the channel, and thus plenty of junctions

between the nanotubes are present in the channel region. Therefore, due to these features, the operation of SWCNT-TFT is different from that of conventional TFTs.

1.4.1 SWCNT-TFTs as Schottky-barrier FETs

The process of fabricating a field effect transistor (FET) having a simple structure using semiconducting SWCNTs is as follows. After depositing the semiconducting SWCNT on an oxidized heavily doped silicon substrate using a transfer process or a solution process, depositing a source and drain metal electrode results in constituting of the transistor of the bottom gate-top contact structure as shown in Figure 1.12 (a). At the metal-nanotube contact a Schottky-contact can be expected with a Schottky-barrier of height Φ_{SB} which means the difference between the Fermi energy level of the metal electrode and the valence band boundary of the semiconducting SWCNT as illustrated in Figure 1.12 (b) [30]. Intrinsically, SWCNT-TFTs exhibit ambipolar characteristics in vacuum or at low temperatures. In addition, this ambipolar characteristic is further emphasized when the work function of the source / drain electrodes is located near the center of the bandgap of the SWCNT. Figure 1.12 (c) is a diagram showing the situation when the current of the ambipolar transistor becomes minimum, and the transfer characteristics according to the drain voltage are illustrated in Figure 1.12 (d). When the height and width of the Schottky-barrier at the contact region between the source/drain electrodes and the SWCNT

is maximized, the transistor enters off-state and a minimum current flow in the channel. As shown in the graph, the off-state leakage current increases rapidly with the drain voltage, which is attributed to the size of the energy bandgap of the nanotube. The above tendency is alleviated in SWCNT-TFTs with a larger energy bandgap.

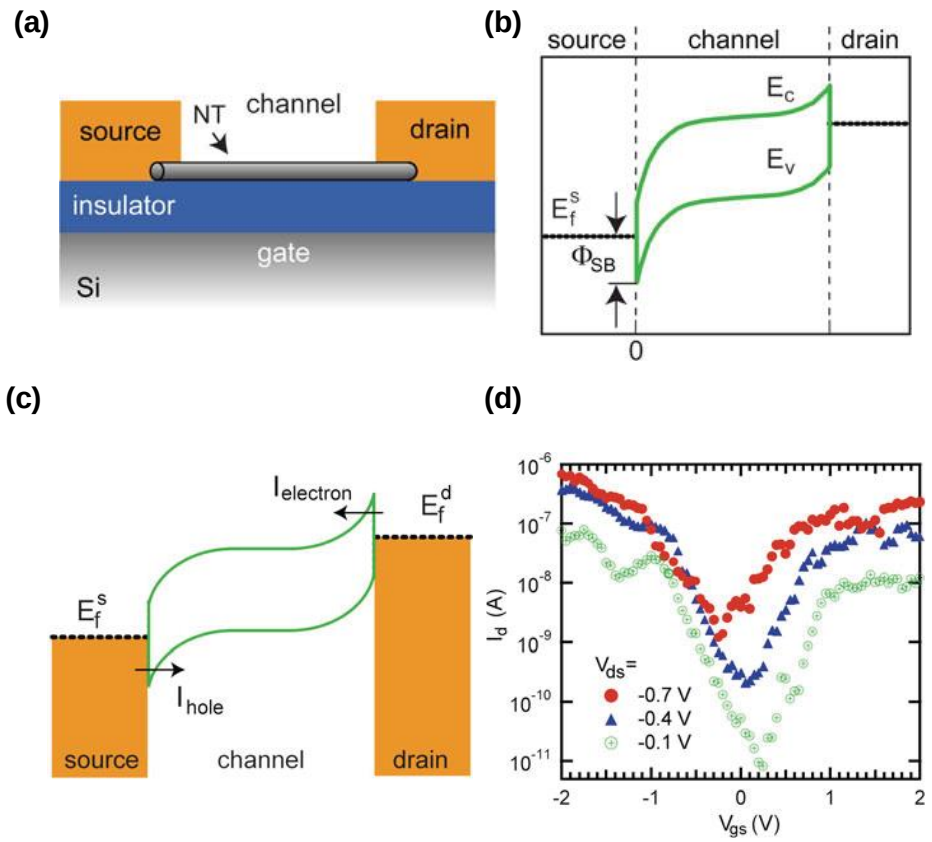

Figure 1.12 (a) A Schottky-barrier field-effect transistor with bottom gate-top contact structure including a channel composed of semiconducting SWCNT and (b) its energy band diagram in the channel. (c) Energy band diagram and (d) transfer characteristics of SWCNT-based transistors with ambipolar characteristics [30].

However, SWCNT-TFTs driven at room temperature and normal pressure exhibit hole transport characteristics rather than ambipolar transport characteristics, so operate like p-type transistors [31]. Oxygen and water molecules around the nanotube greatly inhibit the movement of electrons in the nanotube, and the concentration and movement of the hole are relatively enhanced [32]. Due to these effects, a phenomenon occurs in which the work function of the source / drain electrodes and the valence band of the nanotubes are aligned (see Figure 1.13 (a)). Differences in the work function in the source metal-nanotube contact region result in developing on a local polarization layer on the electrode-nanotube interface. The formed local polarization layer acts as the screening layer, so that the modulation effect according to the gate voltage is hardly observed. The barrier in the contact region is suppressed and the hole is injected into the channel according to the application of the gate bias as shown in Figure 1.13 (b).

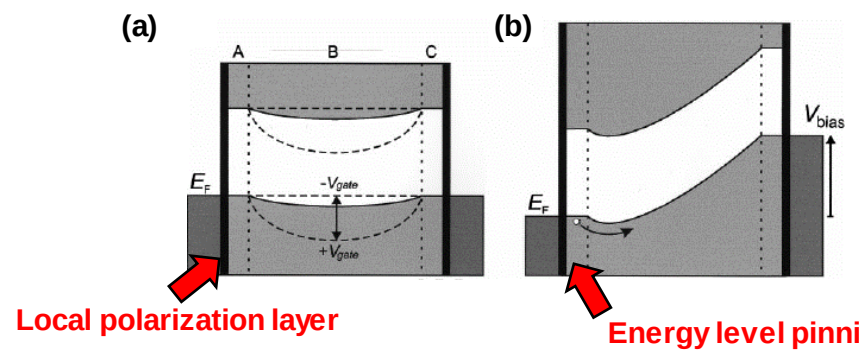

Figure 1.13 (a) Energy band diagram of SWCNT-based FET with a local polarization layer formed on the interface of the contact. (b) A gate bias suppresses of the barrier [31].

Due to the oxygen and moisture around the nanotubes and chemical functional groups such as hydroxy and silanol at the interface between the nanotubes and the gate dielectric, SWCNT-TFTs act as p-type FETs with the turn-on voltage is shifted in the positive bias. Therefore, large hysteresis occurs in the SWCNT-based transistor due to the trapping of electrons around the nanotubes (see Figure 1.14 (a)). This hysteresis can be prevented by passivation of the CNT channel with a polymer such as poly(methyl methacrylate) or polytetrafluoroethylene as illustrated in Figure 1.14 (b) [33]. The passivation layer blocks oxygen and moisture to alleviate the hysteresis phenomenon in transfer characteristics of the SWCNT-TFTs.

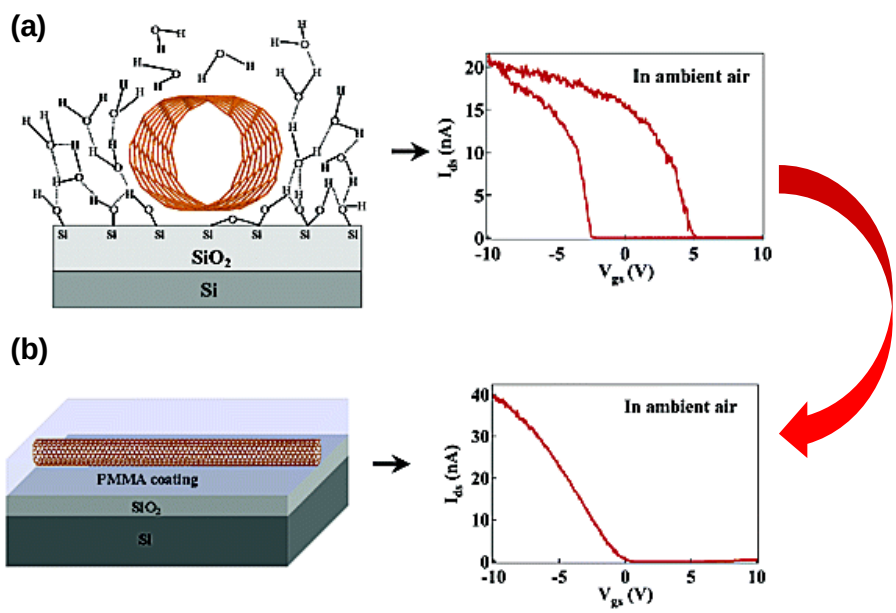

Figure 1.14 (a) Oxygen, water molecules and chemical functional groups around the nanotubes and interface. (b) Passivation layer surrounding SWCNTs in the channel [33].

1.4.2 Random network of SWCNTs

In the case of transistors composed of multiple strands of SWCNTs, not FETs composed of one strand of SWCNTs, numerous nanotubes are deposited in each direction in the channel region. The nanotubes covered in the channel region act as a kind of thin film semiconductor layer. Charge carriers pass through junctions between nanotubes in the channel region, and these junctions are elements that interfere with the movement of charges, which is like grain boundaries inside polycrystalline semiconducting materials such as single-molecule organic semiconductors or polysilicon. According to the method of generating SWCNT, the distribution pattern of SWCNT in the channel varies, and Figure 1.15 (a) illustrates the SWCNT network according to the process method. Images obtained by scanning electron microscopy (SEM) of the SWCNT network by the electrostatic precipitation (ESP), thermal precipitation (TP), press transfer from the filter (PTF), and dissolving the filter (DF) processes in [34] are shown in Figure 1.15 (a), respectively. The degree of alignment of the nanotubes in the SWCNT network varies according to each process method, and the TP-deposited SWCNTs have the highest alignment, followed by DF, PTF, and ESP. Accordingly, the number of the junctions between nanotubes in the channel is the lowest in TP-deposited SWCNTs and the mobility of TP-deposited SWCNTs-TFTs is the highest, followed by DF, PTF, and ESP (see Figure 1.15 (c)).

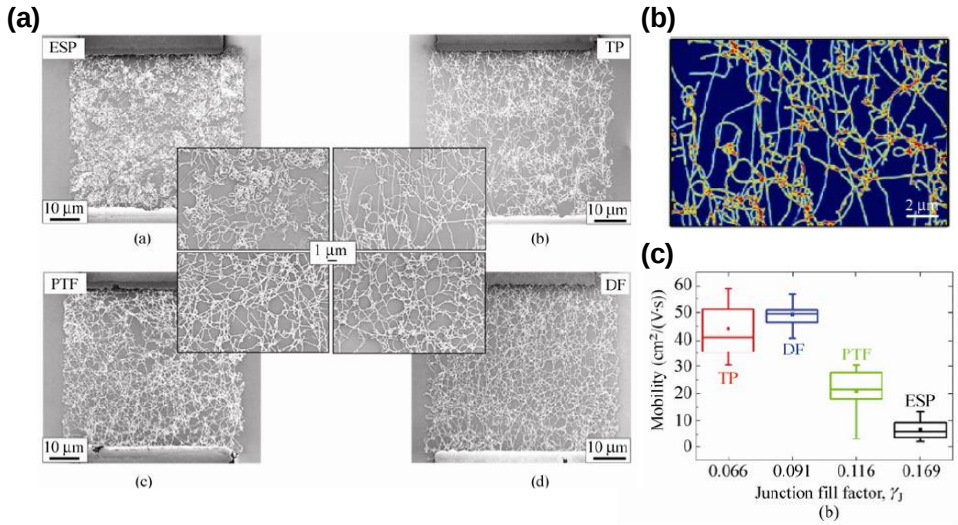

Figure 1.15 (a) SEM image of SWCNT network according to the process method. (b) Junctions between CNTs inside the channel highlighted in red. (c) Correlation between the number of junctions and mobility [34].

Figure 1.16 summarizes the electrical performance of the SWCNT-TFTs according to the generating process of SWCNTs [35]. The CVD-grown or aligned SWCNT network exhibits higher mobility than the random network. Even in a random network structure, it shows a mobility of 1 $cm^2/V \cdot s$ or more, and a high mobility of about 100 $cm^2/V \cdot s$ in a CVD-grown SWCNT network. However, for the samples with very high mobility, the on-off current ratio tends to decrease, which is attributed to the leakage current flowing to the metallic CNT due to the high density of CNTs and alignment in the channel.

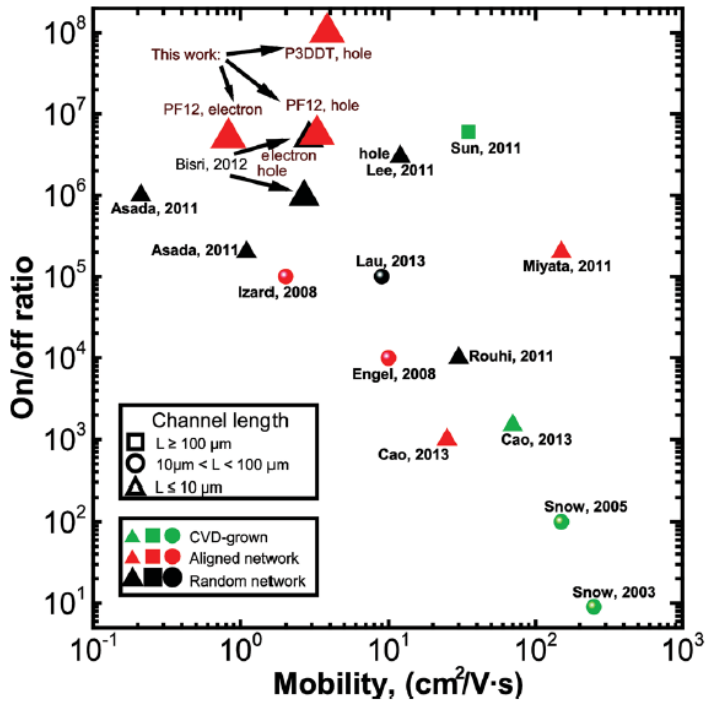

Figure 1.16 Mobility and on/off current ratio of the SWCNT-TFTs according to SWCNT formation method [35].

1.5 Reported SWCNT-TFTs and applications

Semiconducting SWCNTs are suitable for use as active materials for transistors fabricated on flexible or stretchable substrates with high electrical performance and excellent mechanical advantages [36], [37] (see Figure 1.17). In addition, since the absorption rate of SWCNTs in the visible light region is almost non-existent, the SWCNTs can be utilized as an active channel material for a transparent transistor. As a semiconducting SWCNTs ink capable of

solution processing, many electronic devices based on solution processing in low temperature and normal pressure environments have been reported. Micrometer-scale SWCNT-TFTs are manufactured using semiconducting SWCNT ink by spin-coding, dipping, and inkjet printing [38]. Meanwhile, utilizing the ambipolar transport characteristics of the semiconducting SWCNT, solution-processed electrical devices such as ambipolar SWCNT-TFTs and inverters with improved hysteresis and improved electrical stability have been reported by applying a fluorine-based polymer passivation layer to SWCNT-TFTs exposed to normal temperature and pressure [39], [40]. The manufactured SWCNT-TFTs have an advantage in that the electrical properties are not significantly changed even in external physical deformation, and even on soft substrates, logic circuits based on high mobility can be implemented using SWCNTs [37].

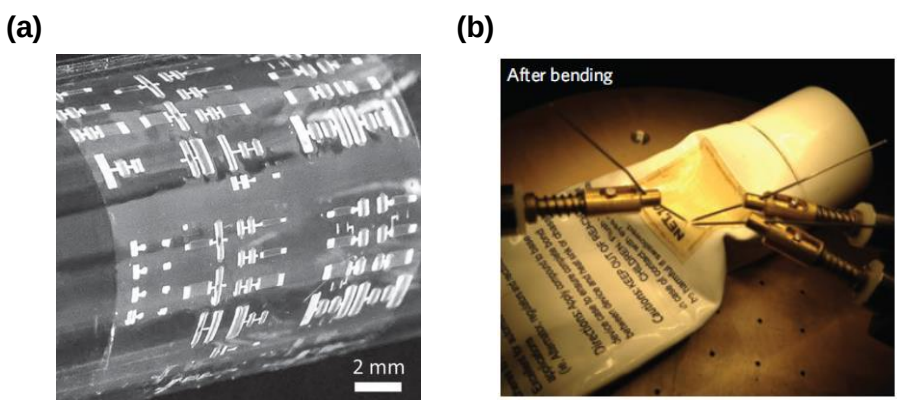

Figure 1.17 (a) Fully printed logic gates on polyimide with SWCNTs [36]. (b) SWCNT-TFTs that operate on physical deformation of the substrate [37].

Electrical devices manufactured by utilizing the high electrical characteristics of semiconducting SWCNTs have been reported from small units of logic gates to large-scale digital integrated circuits such as CNT-based microprocessor [41]. Especially for energy-efficient complementary metal-oxide-semiconductor (CMOS) digital logic, n-type transistors are required in addition to p-type transistors shown by the solution-processed SWCNTs. There are several methods to obtain n-type SWCNT-based transistors. Typically, there is a method of processing a doping material in the channel or coating a separate insulating layer [42], [43]. In the CNT-based microprocessor [41], SWCNT-TFTs of complementary polarities were implemented by depositing different insulator materials on the CNT channel as illustrated in Figure 1.18 (a). About 14,000 SWCNT-TFTs in the microprocessor were implemented by using photolithography process, which is mainly used for existing silicon-based high-integration circuits and using semiconducting SWCNT ink only for active channel materials (see Figure 1.18 (d)). If all processes other than the active formation process such as fine electrode pattern and insulating film deposition are capable of low temperature and normal pressure processes, it is expected to implement a CNT-based microprocessor on a flexible substrate rather than on a rigid silicon wafer. However, the fine pattern technology of the solution process is still insufficient compared to the photolithography process.

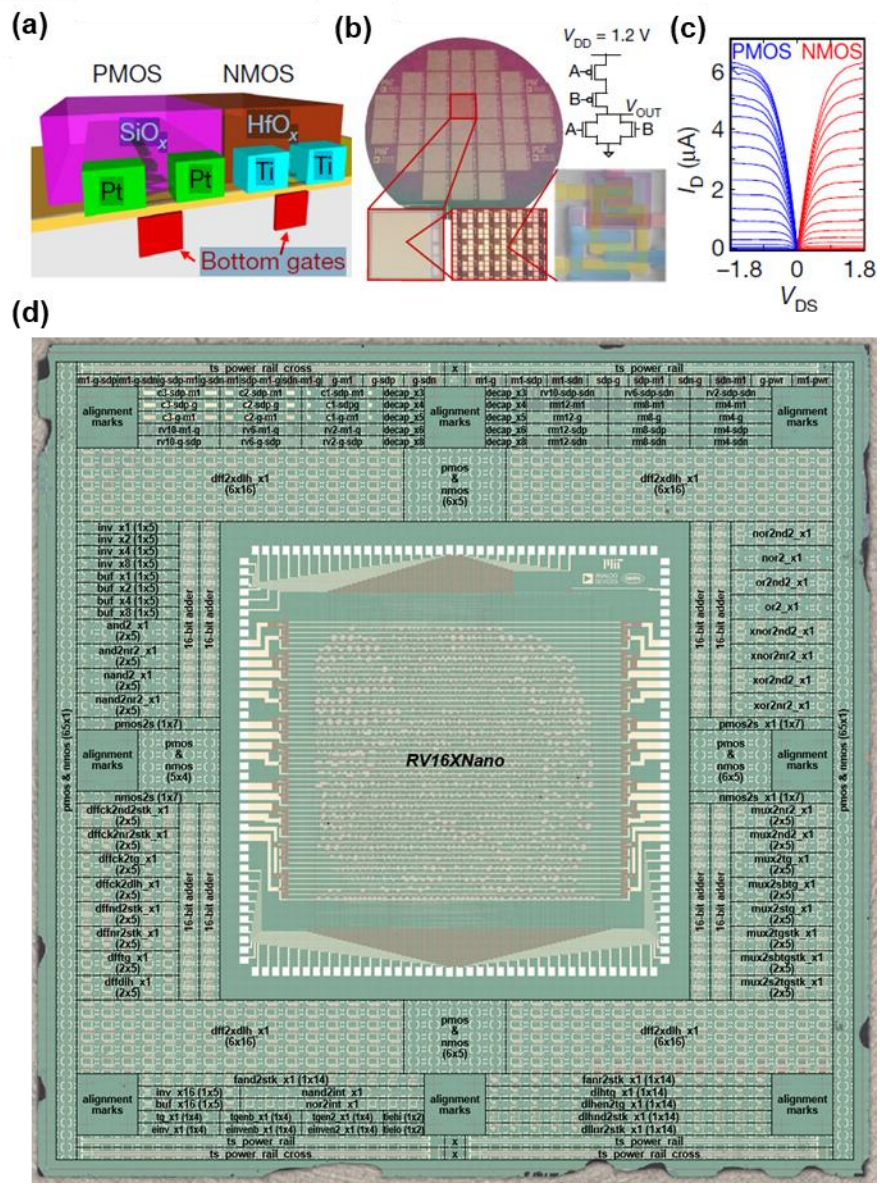

Figure 1.18 (a) CMOS-type SWCNT-TFTs, and (b) CMOS NOR gate. (c) Transfer characteristics for p- and n- type SWCNT-TFTs. (d) Microprocessor made of over 14,000 SWCNT-based transistors on silicon wafers [41].

1.6 Technical points for microelectronics based on SWCNT-TFTs

There are two main points of research in major directions for practical use of microelectronics based on SWCNT-TFT. The first technical point is to control environmental effects in SWCNT-TFTs. In ambient condition, SWCNT-TFTs have p-type unipolar transport characteristics and large positively shifted turn-on and threshold voltage. In other words, the on-off state of the transistor is not converted at the gate bias near zero voltage, and the SWCNT-TFTs operate in the depletion mode in which the transition occurs at a positive gate bias. This phenomenon tends to become more prominent in SWCNT-TFTs based on solution process. Therefore, a technique for reduction and control of the threshold voltages of SWCNT TFTs is required. It is also important to study n-type SWCNT-TFTs for complementary polarities, as used in the CNT-based microprocessors introduced in Section 1.5. In addition, securing reliability against electrical stress or research on long-term stability is also important in the future fabrication of SWCNTs-based electronic devices.

The second technical point for implementation of next-generation electronic applications based on CNT is a research on the fabrication process for highly integrated and miniaturized CNT-based electronics. The high resolution and high integration of transistors are indispensable factors for high performance, efficient

energy use and space efficiency of future electrical applications including display, image sensor array, logic circuits, biosensor, portable and wearable electronics. When scaling down the size of a TFT, the gate oxide thickness and channel layer thickness as well as the channel length must be scaled down. In this respect, one of the major advantages of CNTs is the nano-scaled small diameter of the tubes, which is making CNTs ideally suited for ultra-thin-film transistors. The need for low temperature and non-vacuum processes to realize electrical devices on flexible and stretchable substrates is increasing. The solution process satisfies this point and has the effect of reducing process cost thanks to the relatively simple process rather than photolithography. Currently, tens to hundreds of micrometer-scale transistors and circuits can be manufactured using solution processes such as inkjet printing, but for more high-performance devices, in-depth study is required on solution process methods that enable several micrometers or sub-micrometer scales such as electrohydrodynamic jet-printing and nanoimprint. Additionally, research on a methodology for selectively patterning and aligning CNTs in the fine channel region of the SWNCT-TFTs to reduce leakage current and improve carrier mobility is also important.

1.7 Organization

The thesis is organized as follows. Chapter 2 introduces the simple technique for threshold voltage control in SWCNT-TFTs manufactured by solution process. Through this technique, the turn-on voltage and the threshold voltage shifted significantly in the positive bias direction can be compensated to some extent in the opposite direction, and conversely, the degree of the shift can be deepened, which assists in the robust design of CNT-based circuits. Chapter 3 establishes the all E-jet printing system for SWCNT-TFTs. It includes optimization for e-jet printing of materials such as metals, insulators and semiconductors that make up transistors. Through this printing system, it is possible to bring down the scaling effect of the overall device. Chapter 4 covers the applications such as inverters and active matrix pixel circuits in which two or more TFTs are integrated. In addition, it is possible to pursue a more highly integrated circuit design by introducing a vertically stacked structure implemented by E-jet printing. In Chapter 5, we conclude this thesis with a summary of the fabricated SWCNT-based electronic devices and discuss directions for future SWCNT-based electronics.

Chapter 2

Tunable Threshold Voltage in Single-walled Carbon Nanotube Thin-film Transistors

2.1 Introduction

Single-walled carbon nanotubes (SWCNTs) have great potential for various nanoelectronics from simple logic circuits to CNT-based computer thanks to excellent mechanical and electrical properties. Significantly, random networks of SWCNTs by solution-process at low deposition temperature can enable us to realize large-area flexible electronics. Since the coexistence of metallic and semiconducting SWCNTs leads to low on/off current ratio and poor reliability in thin-film transistors (TFTs), various methods for separation of metallic and semiconducting SWCNTs have been investigated (see Section 1.3). By using density gradient ultracentrifugation method well-known for sorting mixtures of SWCNTs, as introduced in Section 1.3.2, solution-processed SWCNT-TFTs possess a large on/off current ratio (~10^5) with a high field-effect mobility (~30 $cm^2/V \cdot s$) in the linear region [44], [45]. However, large positive threshold voltage (V_T) resulting in a depletion mode of operation, normally observed in solution-

processed SWCNT-TFTs, can be still a big challenge to realize high performance CNT-based nanoelectronics [46], [47]. Furthermore, it is a critical factor to develop molecular-scaled devices requiring low power consumption. In section 1.4, more detailed description of the operation of SWCNT-TFTs can be consulted. In order to control the V_T of SWCNT-TFTs with p-type transport characteristics, several methods have been reported for depositing a passivation layer [43], using a dual gate structure [48], or applying an n-type doping material [42].

In this Chapter, we demonstrate a simple and reproducible technology to favorably tune V_T in solution-processed SWCNT-TFTs employing chemical encapsulation with ammonium hydroxide (NH_4OH) and nitric acid (HNO_3). In addition, inverter circuits using SWCNT-TFTs with tuned V_T was constructed to secure more stable inverter characteristics. We believe that this work presents an important approach toward further control of electrical characteristics in SWCNT TFTs which are adaptable to all-solution process.

2.2 Experimental details

2.2.1 Fabrication process for solution-processed SWCNT-TFTs

The overall device configuration of a solution-processed SWCNT-TFT is shown in Figure 2.1. Bottom gate and top contact structure were adopted. A heavily doped p-type Si wafer and a 200 nm thick thermally grown SiO_2 layer were used as a gate electrode and gate dielectric, respectively. The substrates were cleaned with acetone and isopropyl alcohol in ultrasonic bath, dried with nitrogen gas, and baked in an oven at 100 ℃ for 1 hour in order to remove organic contaminants from the surface. After cleaning processes, the substrates were exposed by an ultraviolet lamp in the ozone chamber for 3 mins by drop-casting of poly-L-lysine (Sigma-Aldrich; 0.1% (w/v) in H_2O) solution onto the surface of the SiO_2 for 5 mins, and a rinse with deionized (DI) water. An as-supplied 95% semiconducting single-walled CNT suspension (NanoIntegris Inc.) was drop-casted for 2 mins, and the samples were rinsed with DI water. This surface functionalization promotes the attachment of semiconducting species of SWCNTs with dense and uniform assembly of nanotube random networks on the SiO_2 surface [49], [50], [51]. A 100 nm thick gold (Au) as source/drain (S/D) electrodes was deposited by thermally evaporation under a vacuum of ~10^{-6} Torr. The dimension of fabricated SWCNT-TFTs possesses a channel width of 1000 ㎛ and

a channel length of 150 ㎛, respectively.

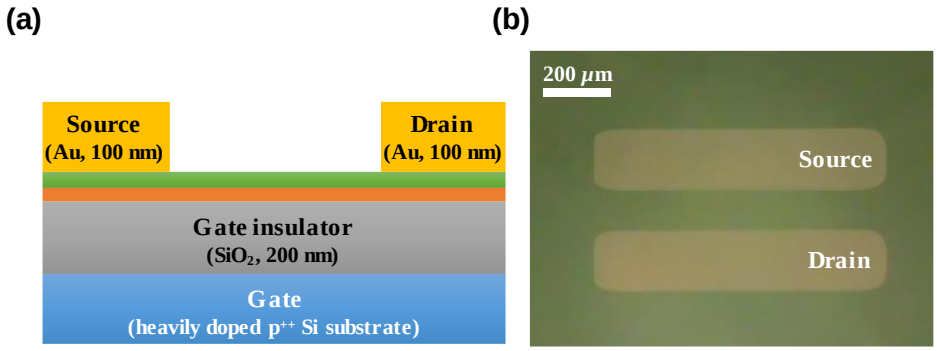

Figure 2.1 (a) The schematic cross-section of a solution-processed SWCNT-TFT and (b) an optical image of a SWCNT-TFT with thermally evaporated gold as S/D electrodes.

2.2.2 Post-treatments for tunable threshold voltage in solution-processed SWCNT-TFTs and measurement of their electrical properties

NH_4OH and HNO_3 were purchased from Sigma-Aldrich, and molar concentration used in this work was 1 M. The acid/base solutions were drop-casted onto SWCNT-TFT samples for 30 seconds, followed by removing the solution by nitrogen gas. The samples were baked on a 70 ℃ hot plate for 5 mins to minimize residual solvent.

Electrical characteristics for all samples were measured with a Hewlett-Packard (HP) 4145B analyzer in ambient air. The applied voltages of the drain and source electrodes in the fabricated SWCNT-TFTs were −50 mV and 0 V, respectively, resulting in the linear mode of the transfer characteristics.

2.3 Results and discussion

2.3.1 Post-chemical encapsulation for tunable threshold voltage

Figure 2.2 (a) shows transfer characteristics of solution-processed SWCNT-TFTs with and without post-treatments by NH_4OH and HNO_3. The measurements of transfer curves were performed by sweeping the gate bias voltage from +5 to −5 V. As-deposited sample clearly exhibits p-type carrier transport characteristics, and a large positive turn-on voltage and V_T of about +2 V as previously reported papers of solution-processed SWCNT TFTs [38], [40], [52]. On the other hands, after post-treatments with NH_4OH, on-current decreased compared to the pristine sample but the turn-on voltage and V_T were shifted toward 0 V for the same gate bias voltage sweep range. Also in the case of post-treatment with HNO_3, the turn-on voltage and V_T were shifted in the positive direction with the magnitude of over 1 V. Figure 2.2 (c), (d), and Table 2.1 summarize the mobility, V_T and on/off current ratio of the samples. By measuring 25 different TFTs for each experiment with NH_4OH or HNO_3, the statistical data and standard deviations were obtained. On the other hand, when post-treatment with Di-water, there is little change in device characteristics (See Section A.1).

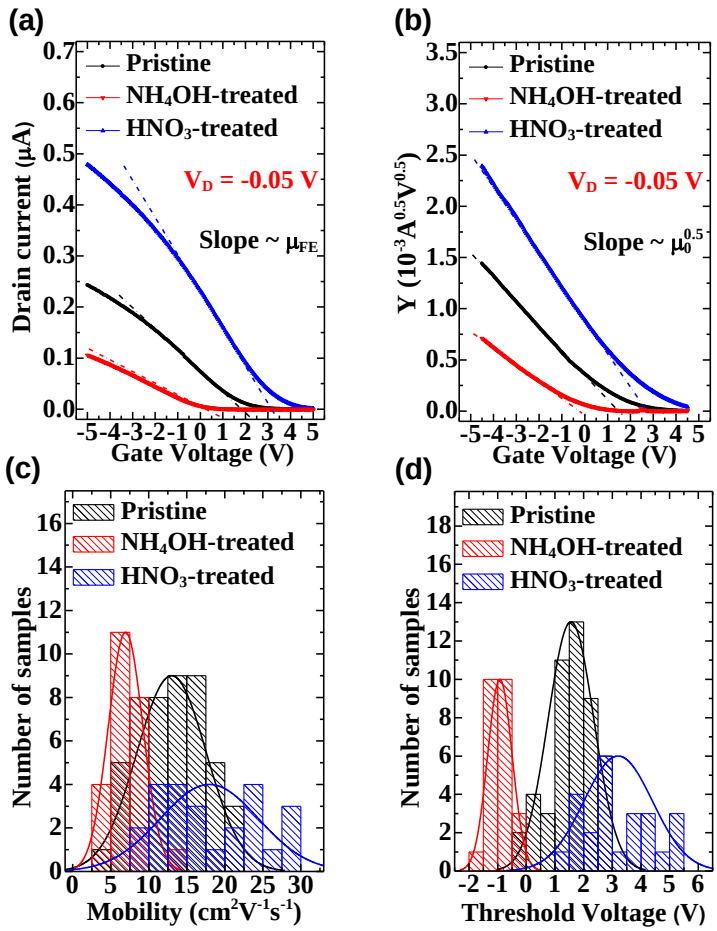

Figure 2.2 (a) and (b) Transfer curves and calculated Y-function of NH_4OH- and HNO_3-treated samples, respectively. (c) and (d) Distribution charts of the low field mobility and V_T for each group.

Table 2.1 Electrical parameters of the solution-processed SWCNT-TFTs with and without post-treatments by NH_4OH and HNO_3.

	Pristine	**NH_4OH**	**HNO_3**
μ_0	13.0 ± 4.57 $cm^2/V{\cdot}s$	6.95 ± 2.28 $cm^2/V{\cdot}s$	18.0 ± 6.46 $cm^2/V{\cdot}s$
μ_{FE}	7.76 ± 2.84 $cm^2/V{\cdot}s$	4.56 ± 1.34 $cm^2/V{\cdot}s$	11.4 ± 3.78 $cm^2/V{\cdot}s$
V_T	1.6 ± 0.80 V	-0.92 ± 0.43 V	3.2 ± 1.2 V
I_{on}/I_{off}	10^4 ~ 10^5	10^4 ~ 10^5	< 10^4

2.3.2 Contact resistance analysis by the Y-function method in SWCNT-TFTs employing chemical encapsulation

The Y-function method was used in this work, which is useful for extracting the mobility, V_T, and contact resistance between the S/D electrodes and the active layer, discussed in this paper, the SWCNT network [53], [54], [55], [56]. Compared to the field effect mobility (μ_{FE}) resulted from the maximum transconductance ($g_m = \mu_{FE} C_{ox} V_D W/L$), the extracted mobility from the Y-function method is called the low field mobility which is less affected by the contact resistance and/or gate voltage. The Y-function is defined as [53]

$$Y = \frac{I_D}{\sqrt{g_m}}, \tag{2.1}$$

where g_m is the transconductance defined as dI_D/dV_G. Considering the contact resistance at the S/D electrodes and assuming that the drain voltage is much smaller than $V_G - V_T$, the drain current equation can be expressed as [54]

$$I_D \cong \mu_0 C_{ox} \frac{W}{L} (V_G - V_T)(V_D - I_D R_C), \tag{2.2}$$

where W and L are the channel width and length, C_{ox} is the gate oxide capacitance per unit area, μ_0 is the low field mobility, V_G and V_D are the gate and drain voltage, and R_C is the contact resistance at the S/D electrodes. Combining the Equation 2.1 and 2.2, the Y-function can be simplified as

$$Y = \sqrt{\mu_0 C_{ox} V_D \frac{W}{L}} (V_G - V_T). \tag{2.3}$$

By plotting the above Y-function with respect to V_G as shown in Figure 2.2 (b) and extracting the slope and x-intercept from the linear fitting, the low field mobility and V_T could be extracted. The contact resistance can be calculated from the following equations [55].

$$R_{total} = R_{Ch} + R_C \tag{2.4}$$

$$R_C = \left|\frac{V_D}{I_D}\right| - \left|\frac{1}{\mu_0 C_{ox}\frac{W}{L}(V_G - V_T)}\right| \tag{2.5}$$

R_{total} is the total resistance (V_D/I_D), R_{Ch} is the channel resistance. The contact resistance (R_C) can be acquired by substituting the mobility and V_T from the Y-function method in the Equation 2.5.

Figure 2.3 (a) and (b) show contact resistance at S/D electrodes in SWCNT-TFTs with and without the chemical encapsulation. There is no significant change of contact resistance for the HNO_3-treated samples, but for the NH_4OH-treated samples, the contact resistance increased by more than 50%, which is consistent with the reduced field effect mobility (μ_{FE}) of the NH_4OH-treated SWCNT-TFTs.

2.3.3 Shift of energy band in SWCNT-TFTs

In SWCNT TFTs, a Schottky barrier at the source electrode is the dominant factor for charge injection in the channel region, and one of the primary metrics in a Schottky barrier is the Schottky barrier height, denoted by Φ_{SB} which depends on the Fermi level (E_F) of the

metal electrode and the valence band edge (E_V) of the active layer [30], [32], [57], [58] (see Section 1.4.1). After considering all the factors, we assumed that the shifts of the energy band could be responsible for the shifts in the V_T of the SWCNT−TFTs when post−treatments with NH_4OH or HNO_3 are employed. Schematic diagrams of the energy band between the source electrode and the SWCNT are depicted in Figure 2.4.

When SWCNTs are exposed by ammonia, the valence band of the nanotube shifts away from the E_F [59], [60]. Thus, holes are depleted, and conductance of the nanotube is reduced, which is one of the reasons for the reduced low field mobility (μ_0) compared to the pristine one. Accordingly, the V_T of the NH_4OH−treated SWCNT TFTs moves in the negative direction. Simultaneously with the shifts in the V_T, the Schottky barrier height at the interface between the source electrode and the nanotubes would also increase ($\Delta\Phi_{SB}$), resulting in increase of contact resistance.

For the HNO_3−treated samples, due to the doping effect of HNO_3, the E_F of the nanotube shifts closer to the valence band, which causes that the SWCNTs possess excessive holes and exhibit more metallic properties [59], [61], [62], [63]. Therefore, the V_T shifts in the positive direction in contrast with the V_T of NH_4OH−treated TFTs. It must be noted that the contact resistance of the HNO_3−treated samples is similar to that of the pristine one, we speculate that the shift of the E_F of the nanotube caused by chemical encapsulation dominantly affects the shift of the V_T in SWCNT−TFTs, while the Schottky barrier height is nearly unvaried.

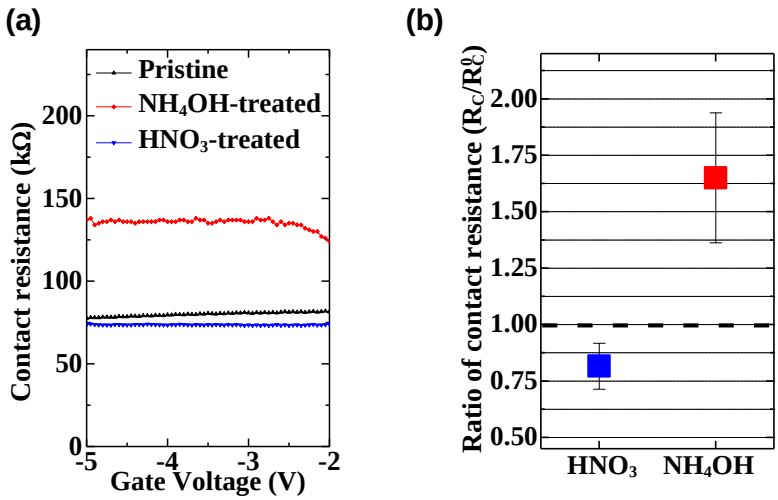

Figure 2.3 (a) Contact resistance of SWCNT-TFTs before and after the post-treatments. (b) Variation in contact resistance for treated SWCNT-TFTs with respect to that of pristine one (R_C^0).

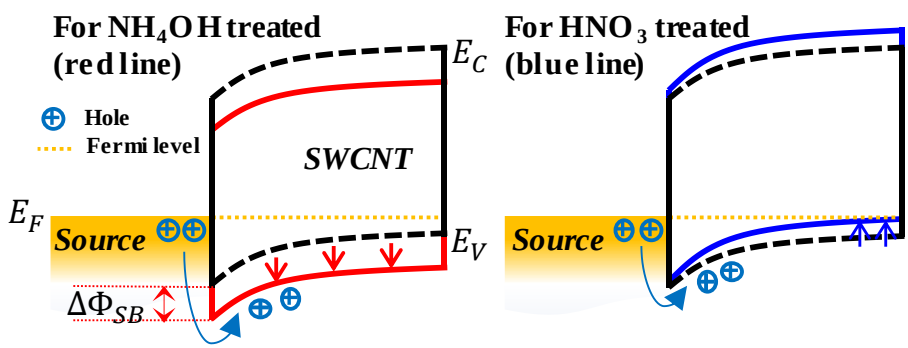

Figure 2.4 Schematic energy band diagrams for the samples after post-treatments (black dot-line means the energy level of the pristine SWCNT)

2.3.4 Cycling tests for post-treatments

Figure 2.5 (a) shows transfer characteristics of SWCNT-TFTs employing sequential chemical encapsulation processes with HNO_3 and NH_4OH. As shown in the transfer curves, it is clearly noted that the turn-on voltage and V_T are sequentially changed for each treatment as previous data. Accordingly, the low field mobility was also modulated by HNO_3 and NH_4OH treatments shown in Figure 2.5 (b). Overall, the mobility increased as progress of sequential treatments, it can be explained that the E_F of the nanotubes shifts much closer to the valence band edge due to the doping effect of HNO_3. Furthermore, based on increase in the contact resistance for the sequences of NH_4OH, we can say that the Schottky barrier at the interface between the source electrodes and the nanotubes are reinforced by NH_4OH treatment, and the increased contact resistance is partially recovered by additional HNO_3 encapsulation. On the other hand, when the treatment time is extended without repeating the NH_4OH treatment, the change in V_T and mobility seem saturated (See Section A.2).

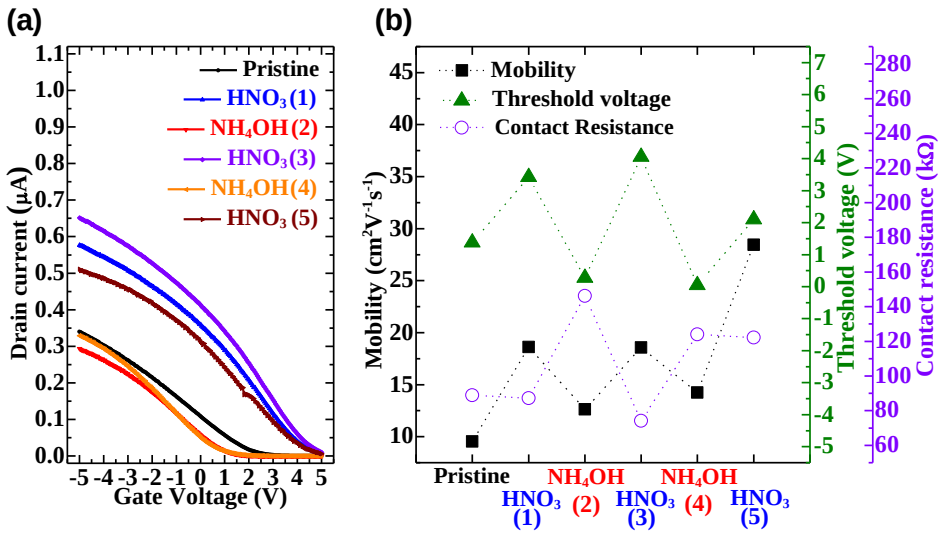

Figure 2.5 (a) Transfer characteristics of sequentially treated SWCNT-TFTs with HNO_3 and NH_4OH. (b) The low field mobility, V_T, and contact resistance of SWCNT-TFTs for each sequence.

2.3.5 SWCNTs-based p-type only inverter

If V_T correction technique by NH_4OH is applied to inverters or memory logic circuits based on SWCNT-TFTs, overall improved performance of the devices can be expected. In the same research group as the author, this V_T tuning technique was applied to SWCNT-TFTs based inverter and memory devices [64]. Using an inkjet printer equipped with piezoelectric print heads, the silver electrodes and semiconducting SWCNTs were patterned to fabricate the SWCNTs-based logic circuits. For detailed process methods, see [64]. Unlike CMOS-based logic gates, when the logic gates are composed only of the p-type TFTs in the enhancement mode, the

diode-connected load is formed by connecting the gate and drain electrode of the TFT, and in the case of a depletion mode p-type TFT, the depletion-mode load is constructed to connect the gate and the source electrode. The inverter logic circuit is composed of the above load TFT and drive TFT (see Figure 2.6 (a)). The switching characteristics of the inverter change significantly depending on the configuration of the TFTs. The V_T tuning technique is useful for adjusting the switching threshold voltage in the voltage transfer characteristics of the inverter. In particular, when implementing a full-swing inverter using a single p-type transistor, the drive TFT should be operated in an enhancement mode rather than a depletion mode to produce an inverter that obtains high voltage gain while maintaining good switching balance [65].

However, solution-processed SWCNT-TFTs usually exhibit depletion-mode characteristics. An energy efficient and high-performance inverter circuit could be constructed by converting the operating mode of the SWCNT-TFT using the V_T adjustment technique presented in this Chapter. As shown in Figure 2.6 (b), pristine SWCNT-TFTs show the operation of depletion mode with large positive V_T (black line), while NH_4OH-treated SWCNT-TFTs operate in enhancement mode (blue line) with shifted V_T and turn-on voltage near 0 V. The voltage transfer characteristics of the inverters with and without V_T tuning technology are depicted in Figure 2.6 (c) and (d). The inverter without V_T tuning technology has a low voltage gain of less than 1 V/V and a small noise margin. On the other hand, the inverter with V_T tuning technology show a high

voltage gain of about 5 V/V and a larger noise margin.

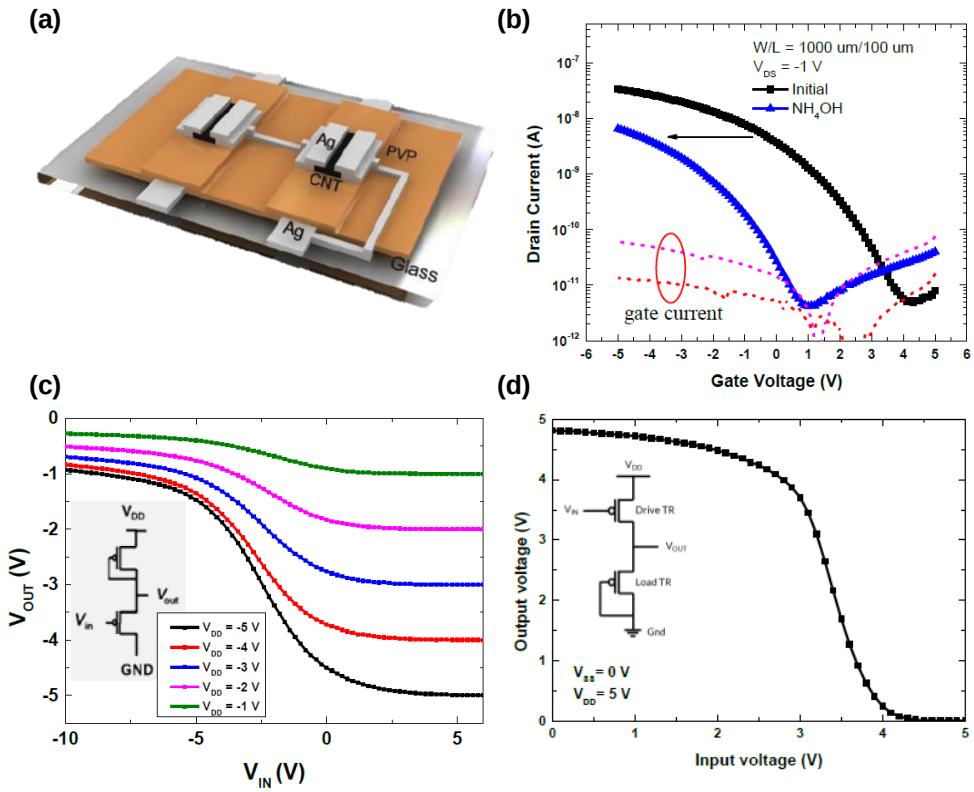

Figure 2.6 (a) SWCNT-TFTs based p-type only inverter circuit. (b) Transfer characteristics of SWCNT-TFTs with and without V_T tuning technology. (c) and (d) Voltage transfer characteristics of SWCNT-TFT based inverters with and without V_T tuning technology. Images are reproduced from [64].

2.4 Conclusion

In summary, we have demonstrated solution-processed SWCNT-TFTs with tunable threshold voltages by the post-encapsulation process with NH_4OH or HNO_3. By optimizing fabrication conditions, we observed the shift in the V_T with the magnitude of up to 2 V in the negative or positive direction for the NH_4OH- or HNO_3-treated SWCNT-TFTs, respectively. The shift of the V_T in SWCNT-TFTs can be explained by modifying the energy band of the nanotubes during the post-treatments. In addition, when the V_T tuning technology was applied to an inverter logic circuit, it was noted that the inverter shows a good switching balance, high voltage gain and large noise margin, and through this, SWCNT-TFT's V_T adjustment is an important factor in circuit design. Consequently, the technique would act as convenient approach which is helpful for design of CNT-based electrical circuits with future advanced fabrications, such as inkjet-printing and roll-to-roll process.

Chapter 3

All Electrohydrodynamic-jet Printing System for Single-walled Carbon Nanotube Thin-film Transistors

3.1 Introduction

Future-oriented and feasible soft electronics including foldable display, E-skin, and bio-electronic sensor inevitably require a low-temperature and relatively uncomplicated process to easily implement large-area devices [66], [67]. In this regards, single-walled carbon nanotubes (SWCNTs) are one of the suitable candidates for the next-generation applications thanks to their high electrical properties such as high intrinsic carrier mobility of SWCNT and remarkable mechanical properties such as high stiffness at external stress in the axial direction and flexibility based on the network of the carbon nanotubes [51], [68], [69]. In addition, since the semiconducting SWCNTs can be easily deposited with a various solution processes such as dipping , dispenser, and inkjet-printing, which ultimately represents simple and low-temperature processability, various electronic devices including logic circuits, large-area display and sensor arrays based on the solution-processed SWCNT thin-film transistors (SWCNT-TFTs) have been

widely studied [19], [39], [49]. Among various solution processing methods, the process using inkjet printing has a merit of simple and low-cost process, easy patterning of any pattern, efficient use of materials, and high throughput, so various researches and applications utilizing it have been reported [70], [71], [72], [73], [74].

SWCNTs-based electronic devices utilizing conventional inkjet printing process, however, exhibit relatively large feature sizes including pixel dimension, electrode width, and channel length in a transistor, resulting in disadvantages for implementing high-speed, high-performance electronic devices. Therefore, in order to overcome the above limitation, many patterning technologies such as photolithography, patterning by laser sintering, screen printing, patterning by transfer-type process, and nanoimprint lithography have been used to realize much finer pattern size [75], [76], [77], [78]. However, some process steps of these methods could be not suitable to the implementation of flexible and stretchable electronics from a fabrication process point, which is contrary to the advantages of the solution-process. Therefore, it is necessary to apply an alternative printing technology that can take advantages of the solution process with simultaneously implementing a finer feature size. Table 3.1 summarizes some technical characteristics of solution process-based printing techniques [79].

Table 3.1 Comparison between solution printing technologies

Printing method	**Ink viscosity [mN/m]**	**Feature size [μm]**	**Film thickness [μm]**	**Yield [m/min]**	**Additional notes**
Piezoelectric-type inkjet	1 ~ 100	30 ~ 50	0.1 ~ 1	1 ~ 500	Multi-nozzle cartridge
Dispenser	10^3 ~ 10^6	10 ~ 1000	50 ~ 100	-	Micro-pattern for large area
Gravure-offset printing	10^4	5 ~ 20	1 ~ 3	1 ~ 10	Roll-to-roll process
Nanoimprint lithography	-	0.01	0.1	Low	Super-fine patterning
Electrohydro-dynamic jet printing	1 ~ 10^4	1	0.001 ~ 0.1	< 1	Stacking for high aspect ratio

Herein, we introduce an electrohydrodynamic-jet (E-jet) printing to fabricate all solution-processed highly integrated and high-resolution devices. When an electric field is applied between a very thin nozzle filled with ink and a substrate, a meniscus deformation of ink called a Taylor cone occurs at the tip of the nozzle (see Figure 3.1 (a)) [80]. Stable E-jet printing is based on the controlling of AC electric field between the nozzle and the substrate to affect the meniscus of the ink at the end of the nozzle, and fine pattern can be deposited to the substrate [81]. One of the main advantages of E-jet printing is that it allows fine patterning down to sub-micro level through femto-liter level ink jetting. In addition, when compared with other printing techniques, the viscous conditions of the ink used are very wide, so it can eject various ink materials. Through this, it is possible to print a very high-viscosity material and create an electrode with a very large aspect ratio or a pattern of a three-dimensional structure, as shown in Figure 3.1 (b) [82]. With the optimization of various conditions for E-jet printing, fine patterns and highly integrated circuits with low-temperature can be easily implemented based on the all-EHD-printed process without additional patterning process, and the feature size is 10 times or more smaller than that implemented by piezoelectric-type inkjet printing.

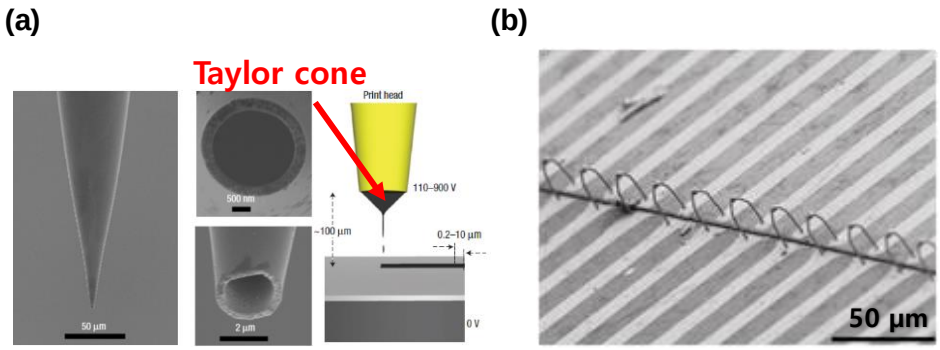

Figure 3.1 (a) Taylor cone formation and ejection of an ink due to electric field between the nozzle with 2 micrometer hole and the substrate [77]. (b) 3D structure electrode pattern via E-jet printing [78].

In this Chapter, we established all E-jet printing system for SWCNT-TFTs with short channel length less than 5 ㎛. In order to fabricate the all E-jet printed high-performance SWCNT-TFTs, all jetting parameters and related design parameters for the E-jet printing were fully optimized. In case of our fully optimized conditions, each layer of the SWCNT-TFT, including metal, insulator, and active materials, and device itself exhibited high quality and performance.

3.2 Experimental details

3.2.1 Ink manufacturing for E-jet printed metal, dielectric, and active layers

We utilized a silver nanoparticle-type ink with a diameter of about 50 nm (DGP 40LT-15C from Advanced Nano Products Corp.) as an electrode material for E-jet printing. In printing of the metal layer, temperature of the substrate was set to 30 ℃ for improving the waviness at the edge of the printed layer, and the it was repeatedly printed 3 ~ 4 times for obtaining the desirable thickness and conductivity of it. After printing the metal layer, it was annealed at 160 ℃ for 1 hour.

As the dielectric and insulating layer, poly(4-vinylpheol) (PVP) was adopted. To manufacture the dielectric ink for E-jet printing, PVP was dissolved in organic solvent mixed with propylene glycol methyl ether acetate (PGMEA) and ethyl alcohol, and added poly(melamine-co-formaldehyde) (PMF) as a cross-liking agent which enhances insulation characteristics through rigidly coupled PVP molecules in the deposited film. In order to optimize the surface distortion or roughness due to the coffee-ring effect generated by the film formed by the inkjet-printing process, two solvents system, which consisted of PGMEA and ethanol, were used in a 1:1 ratio as a dispersion solvents for the ink. For smoothly discharging the PVP ink, the concentration of PVP was set to 1 wt.% with the weight ratio

between PVP and PMF of 1:2. As with the same reason for the silver printing, the substrate temperature during printing of the PVP ink was fixed at 30 ℃. After printing the PVP layer, it was sequentially sintered at 100 ℃ for 20 mins to eliminate residual solvents, and at 160 ℃ for 40 mins to fully cross-link the PVP molecules.

We used a commercialized 95% semiconducting SWCNTs suspension (NanoIntergris Inc.) as an active material. To promote the attachment of semiconducting species of SWCNTs with dense random networks on the substrates, surface functionalization with poly-L-lysine (PLL, 0.01wt.% in H_2O) was followed [49], [50], [51]. Instead of printing semiconducting SWCNT ink directly, the PLL was selectively printed to pattern the active material, and then the substrate was immersed in the SWCNT dispersion to form SWCNT random networks [96]. This indirect printing method helps to deposit a uniform network of SWCNTs when forming an active pattern over a large area. The PLL printing was performed at room temperature. Furthermore, to rapidly and effectively deposit the network of semiconducting SWCNTs, our previously reported multi-dipping technique was utilized [83].

3.2.2 Optimized E-jet printing conditions and fabrication process for all E-jet printed SWCNT-TFTs

550 ㎛ thick glass substrates (Eagle XG, Freemteck Corp.) were selected as the main substrate for the E-jet printed SWCNT-TFTs. Prior to the experiments, the substrate was cleaned by SPM cleaning (sulfuric-peroxide mixture, H_2SO_4:H_2O_2 = 4:1, temperature of 120 ℃), and sequentially rinsed with deionized water (DI-water), acetone, and isopropyl alcohol (IPA) in ultrasonic bath.

We used the sub-femtoliter inkjet processing unit, SIJ-S050 model from SIJ company as E-jet printing equipment, and the nozzle was a Super Fine Nozzle (SIJ-SFN from SIJ) with a target line width of about 1 to 3 ㎛. For each Ag, PVP, and PLL ink, the waveform, amplitude, bias level, and frequency of the AC voltage applied to the end of the nozzle were optimized, and specific values including above the parameters and printing speed are summarized in Table 3.2. The distance between the substrate and the ends of the Ag and PLL nozzles was about 15 ㎛, and in the case of the PVP nozzle, about 30 ㎛ were maintained.

Table 3.2 Optimized jetting conditions for the E-jet printed inks

Ink type	Waveform	Amplitude [V]	Bias [V]	Frequency [Hz]	Printing speed [mm/s]
Ag	Triangular	230	0	200	0.40
PVP	Square (25% duty)	250	0	1000	0.35
PLL	Square (75% duty)	400	0	200	0.40

For an E-jet printed single SWCNT-based transistor, a bottom-gate and bottom-contact configuration is adopted. The gate electrode was printed on the cleaned glass substrate by E-jet printing, sintering on a 160 ℃ hot plate, and then the 300-nm-thick gate insulating film was formed by E-jet printing twice using a nozzle filled with the engineered PVP ink, introduced in Section 3.2.1. Before printing the source and drain electrodes, it is necessary to perform surface treatment to lower the surface energy in order to improve the wetting properties of the E-jet printed PVP surface. So, hexamethyldisilazane (HMDS) was spin-coated onto the PVP film at 3,000 rpm and the substrate was heat-treated at 150 ℃ for 1 hour. After lowering the surface energy of the printed PVP layer by HMDS, the source and drain electrodes were printed in a circular shape with a width of about 10 ㎛. For patterning the active channel region between the source and drain electrodes, the PLL was selectively

printed on the channel region and rinsed with DI-water. After drying the PLL-treated substrates, a network of semiconducting-SWCNTs were deposited on the channel area using the previously reported our multi-dipping technique that repeats the immersing and rinsing process. Average dipping time for immersing the substrate into SWCNTs dispersion was 5 to 10 mins, and then dried on a 150 ℃ hot plate for 1 hour. Detailed process techniques are given in the paper we have previously reported [83].

In addition, to negatively shift the turn-on voltage and threshold voltage (V_T) of the SWCNTs-based transistors, chemical encapsulation with ammonium hydroxide (NH_4OH), as introduced in Chapter 3, was applied on the network of semiconducting SWCNTs. The 1 M NH_4OH solution was drop-casted onto the SWCNT-TFTs for 20 seconds, followed by removing the solution by nitrogen gas. The samples were baked on a 100 ℃ hot plate for 3 mins to evaporate the residual solvent.

After the fabrication process of all E-jet printed SWCNT-TFTs is completed, electrical characteristics for the SWCNT-TFTs were measured with an Agilent 4155C semiconducting parameter analyzer in ambient air, and the optical images of the samples were obtained with an optical microscope (DSX510, Olympus Corp.). Morphology of the printed layers and the channel region was analyzed with FE-SEM (S-4800, Hitachi Corp.) and AFM (XE-100, Parks' System Corp.) equipment. Line profile of the films were measured by AFM or surface profiler (Alpha-Step® D-600, KLA Corp.).

3.3 Results and discussion

3.3.1 Constituting of all E-jet printing system

Figure 3.2 (a) depicts the principle and related parameters of E-jet printing system, and the chamber where the nozzle and stage are located, the high voltage unit and the nozzle camera are shown in Figure 3.2 (b) and (c). When deforming the meniscus of the ink at the nozzle tip by properly controlling the electric field between the nozzle and the substrate, it starts to form the continuous and stable jetting of the prepared ink while the meniscus of the ink keeps Taylor-cone shape. After that, we could fabricate the high quality and high performance thin-films with controlling the parameters in design and process such as line-pitch, substrate temperature, and the number of stacks in printing.

Specifically, material selection and process optimization for the metal electrode, gate insulating film, and active materials constituting the TFT should be required to construct the all E-jet printing system. Nanoparticle-type silver ink and PVP were used as metal electrodes and insulating films, respectively, and adsorption of SWCNTs was induced by printing PLL, a pre-surface treatment material, to deposit semiconducting SWCNTs, as active materials. For more information on each substance, see Section 3.2.1.

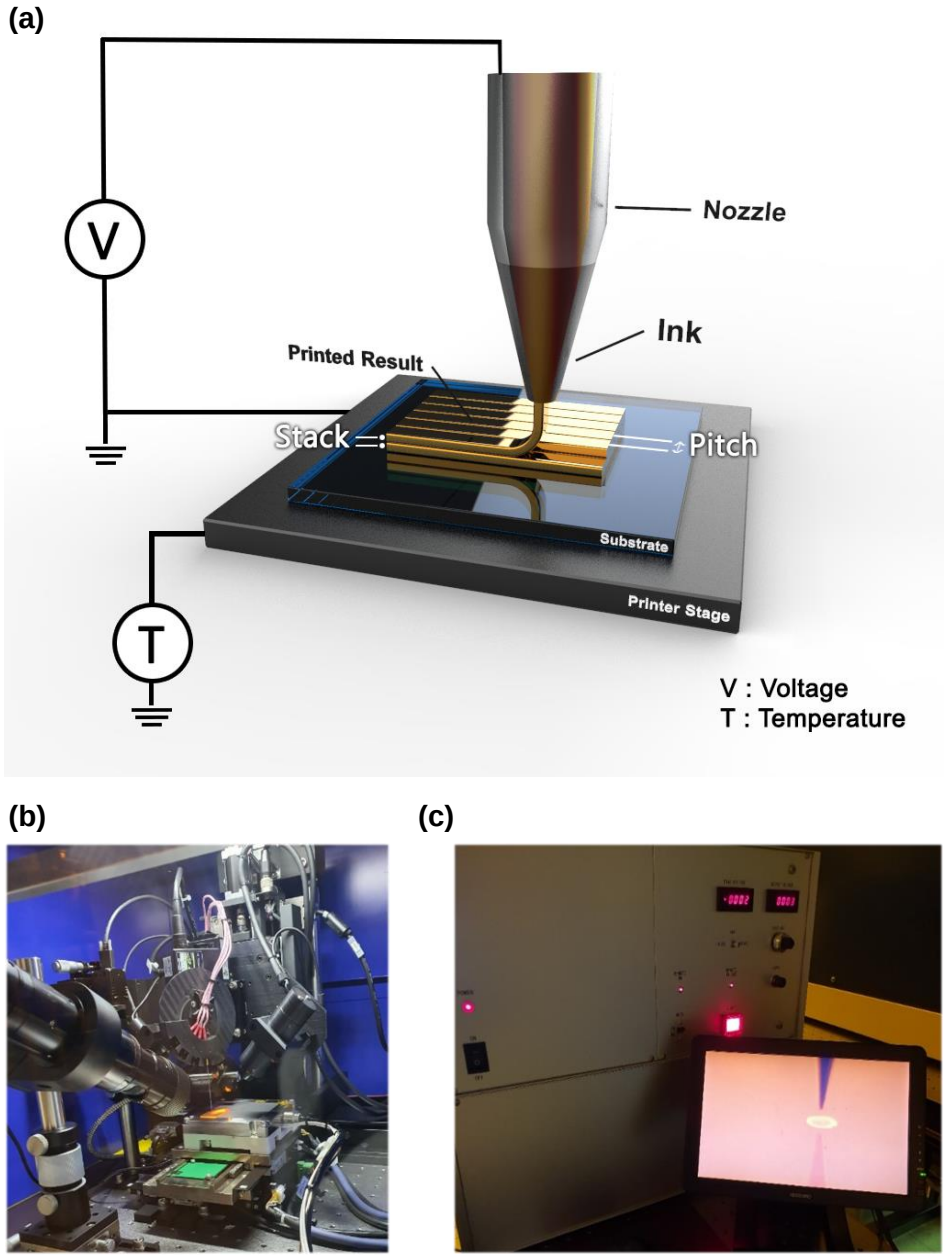

Figure 3.2 (a) Schematic diagram of E-jet printing system. (b) Printing chamber in E-jet printing equipment. (c) High voltage unit and nozzle camera of E-jet printer.

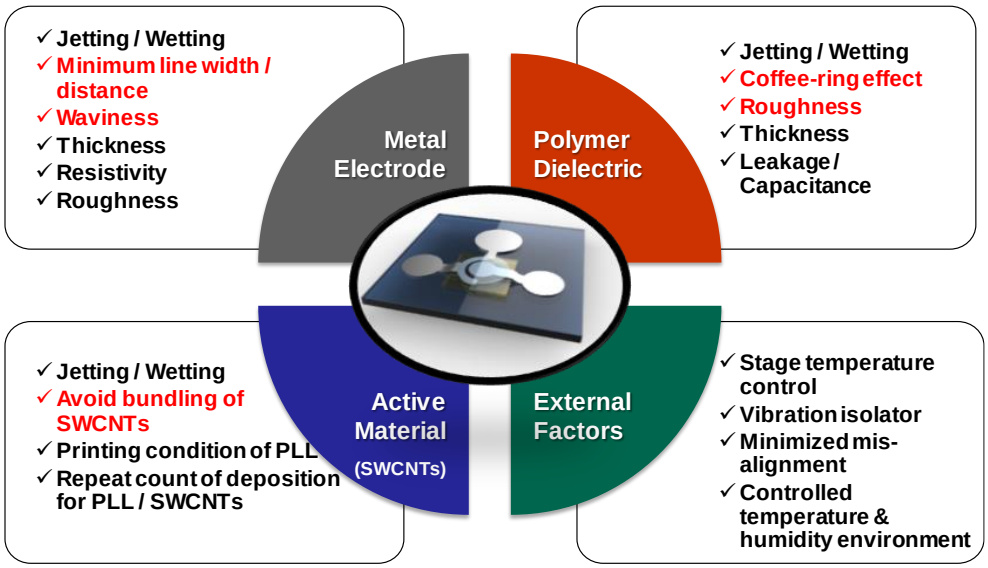

Figure 3.3 Diagram for technical points in constituting of all E-jet printing system

In addition, external factors such as temperature control of the printing stage, isolation from external vibration, and control of ambient temperature and humidity are also important factors when constructing an all e-jet printing system. Temperature and humidity are one of the most important factors in any solution process, and in forming a pattern on a micrometer scale, the misalignment of printed patterns and layers must be minimized. Therefore, the E-jet printing equipment was set up on an anti-vibration table in a separate space where the temperature and humidity were controlled. Figure 3.3 summarizes the technical points in constituting of all E-jet printing systems. The parameters highlighted in red indicate that it is a more important element in the printing of each layer, and a detailed analysis of each printed layer is covered in the subsequent sections.

3.3.2 Optimized E-jet printed metal electrode

The major issues that can occur in E-jet printed metal electrodes are as follows. First, the waviness at the edge of the electrode line is an important point for the electrodes in a TFT. In particular, when the channel region between the source and drain electrodes is formed, a uniform electric field is not applied to the channel if the waviness of the electrode exists. In severe cases, the source and drain electrodes stick together, hindering the normal operation of the TFT. Besides, if the process is not optimized, sprayed ink is present around the electrode, and bulging parts at both ends of the electrode appear as shown in Figure 3.4 (a) and (b). From a different point of view than the printed line shape, it is also important to print a low-resistance electrode while keeping the overall size of the electrode as small as possible.

There are several key process parameters to alleviate the above issues. By adjusting the profile of voltage between the nozzle and the substrate, the overall appearance of the printed metal line can be improved. With setting the appropriate frequency of the AC voltage and changing the waveform from square wave to triangular wave, sprayed ink existing around the electrode can be effectively suppressed (see Figure 3.4 (b)). In addition, the speed, acceleration, and temperature of the printing stage can be controlled to further minimize the bulging part at both ends of the metal line that occurs when printing starts and ends.

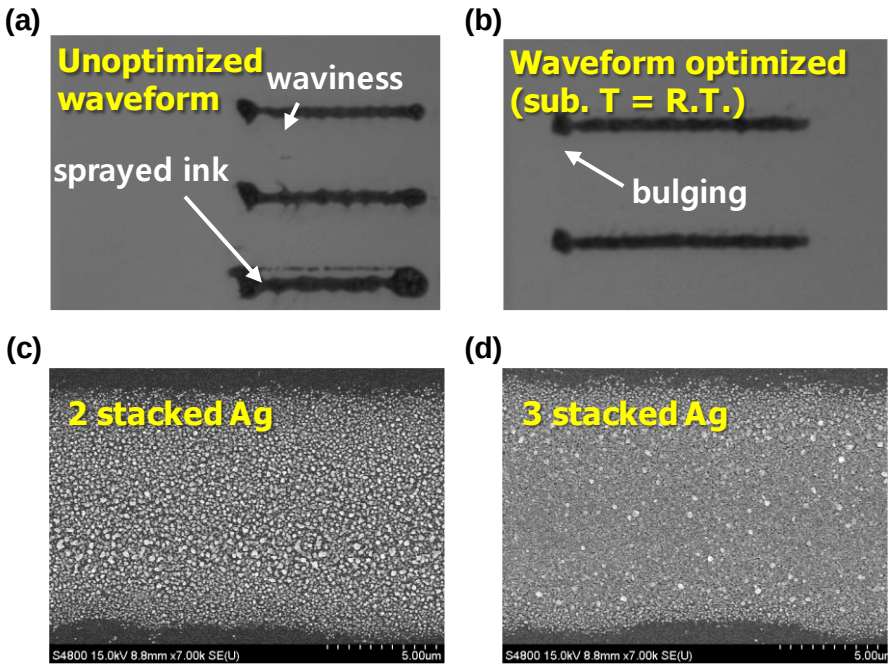

Figure 3.4 (a) and (b) Optical image of printed metal line without and with optimization of waveform. (c) and (d) Images obtained by FE-SEM for 2 stacked and 3 stacked printed line with nanoparticle-type Ag ink, respectively.

On the other hand, in order to improve the electrical properties of the printed metal electrodes, by increasing the number of printing stack or shortening the line pitch, the reduced resistance of the metal line could be obtained. Figure 3.4 (c) and (d) are images, obtained by field emission scanning electron microscope (FE-SEM), of E-jet printed silver line according to the number of printing. Ag nanoparticles of about 50 nm are tightly packed in the 3 stacked line rather than the 2 stacked line, which means high electrical conductivity. However, it is necessary to be careful that excessively

superimposed printing would destroy the geometry of the printed electrodes.

Figure 3.5 (a) and (b) show images of E-jet printed well-defined silver electrodes, fabricated with fully optimized printing condition in Table 3.3, obtained by optical microscope and FE-SEM, respectively. In E-jet printed single metal line, continuous and non-waviness Ag lines were demonstrated with stable jetting of the Ag ink with optimized process parameters. We utilized 4 lines with 3 ㎛ spacing for single printing and repeated the printing 4 times for stacking, resulting in the line width of 11 ㎛, the resistance of 30 Ω and the extracted resistivity of 1.71×10^{-7} Ω · m. For reference, the resistivity of silver in bulk is 1.59×10^{-8} Ω · m [84], and the resistivity value of the E-jet printed silver is about 10 times larger. However, considering that the resistivity of inkjet-printed Ag thin film is about 1×10^{-7} Ω · m or more [85], it can be considered that the E-jet printed silver is of good quality in terms of electrical properties. As the number of printing stacks decreases for the same pitch, the electrical conductance of electrode is degraded because printed thin film of Ag exhibits sparse network of nanoparticle. When comparing the I-V characteristics of the printed silver line according to the number of stacks shown in Figure 3.5 (c), it exhibits good resistance characteristics at 4 times or more printing stacks. Through the line profile analysis across the printed line using the atomic force microscope (AFM) equipment, the thickness of the center portion of the printed line was measured to be about 120 nm, and the average thickness is 98 nm (see Figure 3.5 (d)).

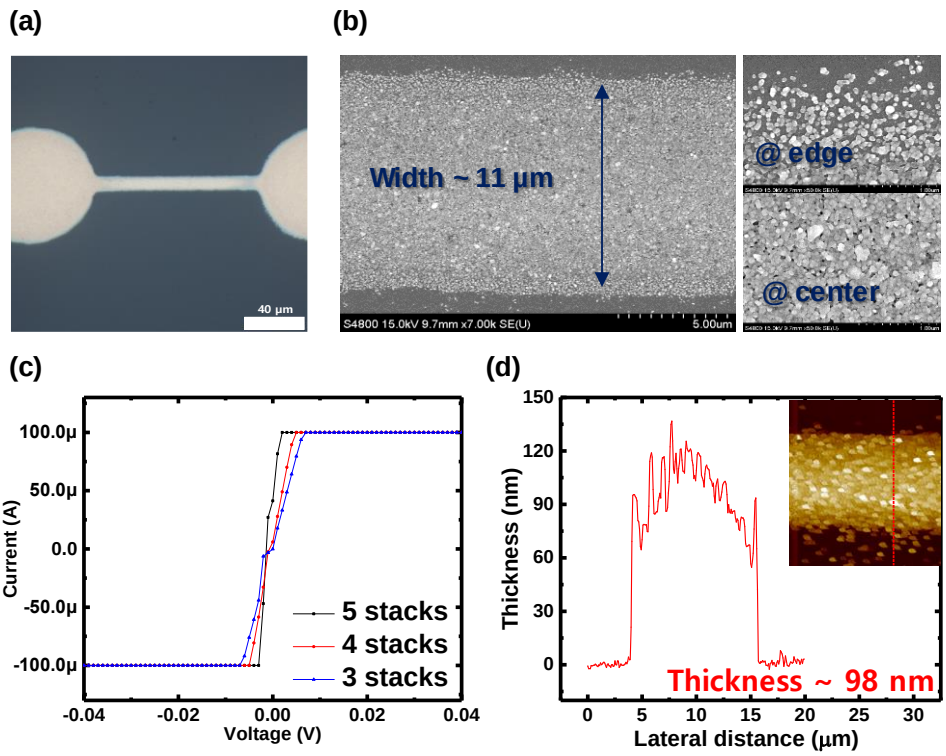

Figure 3.5 (a) and (b) Optical and FE-SEM images for E-jet printed Ag line. (c) Current-voltage graph of E-jet printed Ag line according to the number of printing stacks. (d) Line profile obtained by AFM of Ag line stacked 4 times. The top right inset is the image of the printed line obtained by AFM.

Table 3.3 Optimized parameters for fabrication of E-jet printed silver electrode

Nozzle distance	15 μm
Waveform	Triangular wave
Applying voltage amplitude	230 V (Bias 0 V)
Frequency	200 Hz
Printing pitch	3 μm
Printing speed	0.4 mm/s
# of Printing stacks	4
Substrate temperature	30 °C

3.3.3 Optimized E-jet printed polymer dielectric

The PVP ink, as insulating material, previously used in our research group [86] should be newly engineered for E-jet printing due to the following issues. For information on the newly engineered PVP ink for E-jet printing, see Section 3.2.1. When directly applying the previously reported PVP ink to the E-jet printing, there are three major issues. The first is that the nozzle is easily clogged when the PVP solution is used for E-jet printing, and the second is that the surface energy on the surface of the PVP layer is high, so that the

smear of silver ink is largely generated during the subsequent electrode printing process. The last issue is that it is difficult to obtain a flat morphology on the PVP layer due to the coffee-ring effect that refers to the phenomenon that solutes gather outside the droplets and leave a ring-shaped residue.

First, in order to solve the clogging issue, the concentration of the PVP solution was greatly reduced from 10 wt.% to 1 wt.%. This ensured smooth jetting of the PVP ink at lower voltages during E-jet printing. In addition, in order to lower the surface energy of the PVP layer, the ratio between PVP and PMF, which are cross-liking agents, was changed from 5:1 to 1:2, and simultaneously it was noted that the viscosity of the solution increased significantly. See Section A.3 for surface energy change according to the ratio between PVP and PMF. By increasing a ratio of cross-liking agent, we were able to control the wetting properties of PVP, and as shown in Figure 3.6, the blurring of the subsequent silver lines was significantly alleviated.

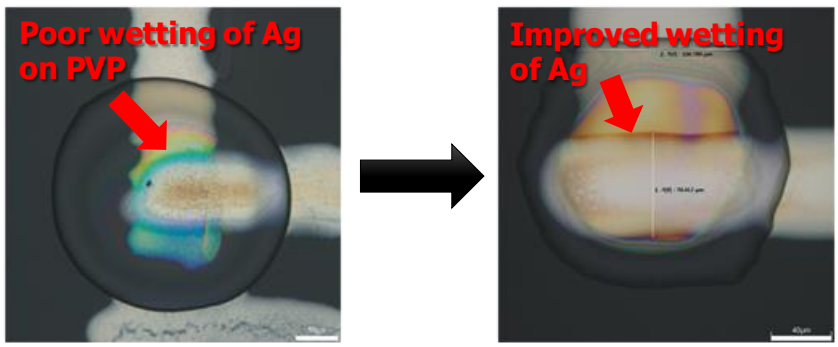

Figure 3.6 Improved wetting properties of the E-jet printed PVP layer by increasing a ratio of cross-liking agent.

For minimized coffee-ring effect at the edge of the PVP layer, a mixed-solvent system of the PVP solution [87] was assembled by additionally supplying an ethanol solvent to the previously reported PVP ink based on a single solvent of PGMEA. Since the boiling point and vapor pressure of ethanol are significantly lower and higher than that of PGMEA (See Table 3.4), when the droplet of the PVP ink with the mixed-solvent system is formed on the substrate, the evaporation rate is accelerated to reduce the amount of PVP solute to be deposited toward the outside of the droplet. In addition, the Marangoni flow is developed due to the difference in the surface tension of the two solvents, which weakens the strong capillary flow inside the droplet. Therefore, when E-jet printing a PVP layer using the mixed solvent-based PVP ink, the coffee-ring effect on the edge of the printed PVP layer is greatly mitigated as shown in Figure 3.7. For quantitative analysis of the coffee ring effect, after printing PVP layers with the two PVP inks based on the single solvent and the mixed solvent, a line profile analysis was performed for each printed PVP layer. As a result, in the case of the PGMEA-based single solvent ink, the peak-to-valley ratio, which is the ratio of the thickness of the central portion and the edge portion of the printed PVP layer, was 0.2, and the coffee ringing effect was very severe, resulting in the silver line breaking near the edge of the PVP layer in subsequent silver printing process. On the other hand, in the case of the PVP ink based on a mixed solvent added with ethanol, the peak-to-valley ratio is about 0.9, so that the coffee ring effect is greatly mitigated and does not interfere with subsequent processes.

Table 3.4 The boiling point, vapor pressure, and surface tension for ethanol and PGMEA

	PGMEA	Ethanol
Boiling point [℃]	146	78.4
Vapor pressure [mmHg]	3.8	43
Surface tension [mN/m]	28.5	22.4

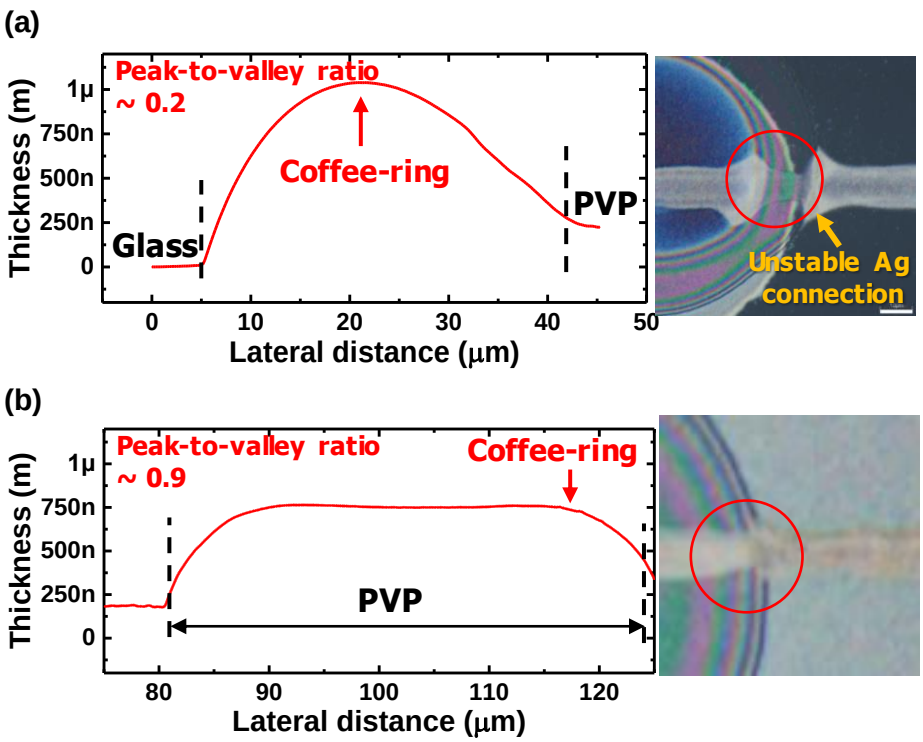

Figure 3.7 (a) and (b) Line profile of E-jet printed PVP films with the single solvent and the mixed solvent based-PVP ink, respectively. The subsequent silver line shows an unstable connection at the edge of the PVP film in (a).

To optimize the surface roughness characteristics and the thickness of E-jet printed PVP films with the engineered ink, the printing speed and line pitch should be optimized. We investigated the effect of the parameters by analyzing the surface roughness parameters consisting of root mean square (RMS), skewness, and kurtosis value extracted from the roughness distribution measured by surface profiler [88]. The engineered PVP ink was printed while changing the line pitch from 1 to 2 ㎛ and the printing speed from 0.3 to 0.6 mm/s, and the surface roughness parameters of the printed PVP films are shown in Figure 3.8. Refer to Section A.4 for detailed description of surface roughness parameters and optical image and line profile of the E-jet printed PVP films.

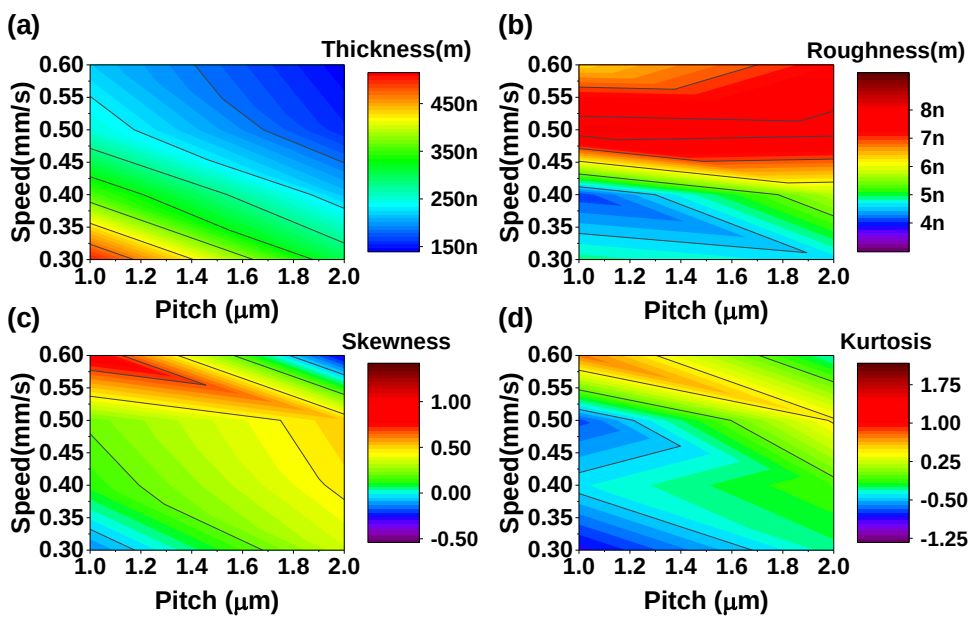

Figure 3.8 (a) Thickness, (b) RMS, (c) skewness, and (d) kurtosis of E-jet printed PVP films according to line pitch and printing speed.

As the RMS roughness is low, and the skewness and the kurtosis approach zero, the better the surface roughness properties can be expected. Through the analysis in Figure 3.8, a good quality surface morphology could be expect during E-jet printing of the PVP ink with the line pitch of 2 ㎛ and the printing speed of 0.35 mm/s. Figure 3.9 (a) shows optical images of E-jet printed PVP film with the engineered ink and the optimized process parameters. In addition, when the PVP film was printed twice in a row and stacked in 2 layers, the line profile characteristics and roughness parameters of the 2 stacked PVP film are further improved with the thickness of about 300 nm, as shown in Figure 3.9 (b) and Table 3.5. The insulation properties of the printed PVP film stacked twice is 5.1 nA/cm^2 at 1 MV/cm, which is remarkable insulation characteristic compared to the insulation properties of the previously reported PVP film or other dielectrics [86], [89], [90]. For fully-optimized printed PVP film, a capacitance in unit area is 8.2 nF/cm^2, and relative permittivity is 2.8 (See Figure 3.10 (b)). Table 3.6 summarizes the optimized process parameters for E-jet printed PVP thin films.

Table 3.5 Roughness parameters for E-jet printed PVP films

# of Printing stacks	Thickness	RMS	Skewness	Kurtosis
1 stack	142 nm	5.63 nm	-0.582	0.232
2 stacks	297 nm	2.53 nm	0.374	-0.545

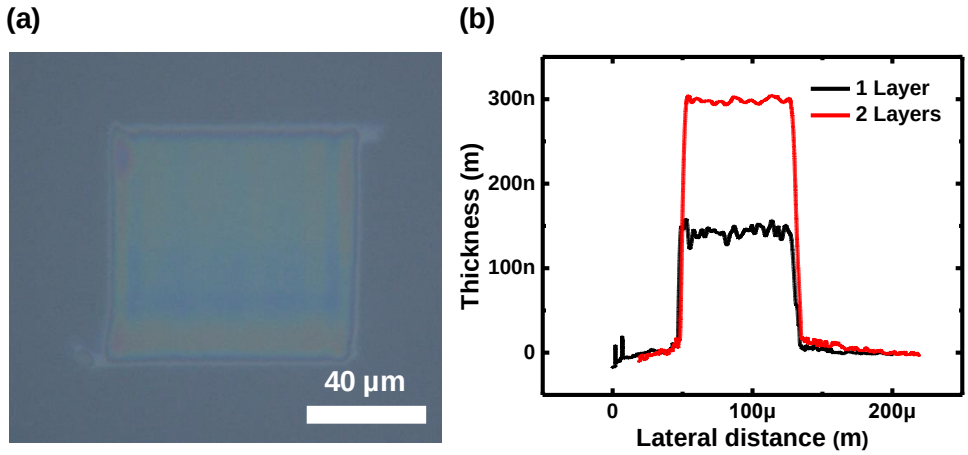

Figure 3.9 (a) Optical image of a PVP thin film printed once with optimized process parameters. (b) Line profile of the PVP thin films printed once (black line) or twice (red line).

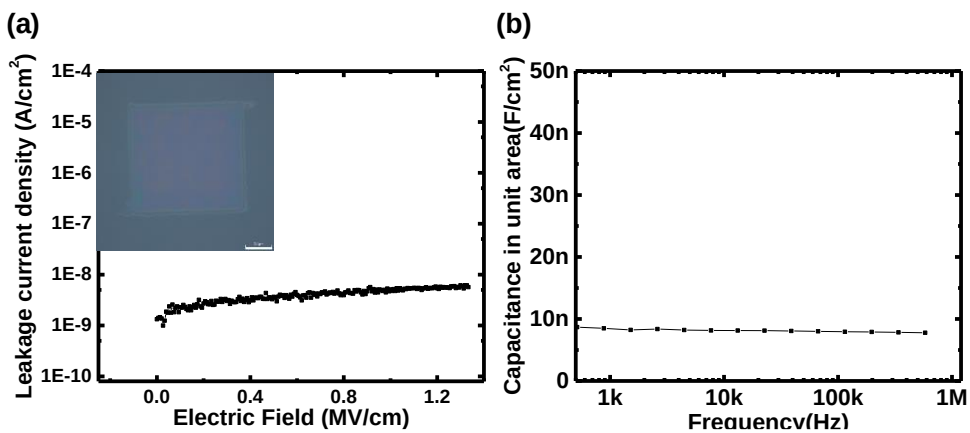

Figure 3.10 (a) Leakage current vs applied field and (b) areal capacitance vs frequency for E-jet printed PVP stacked twice. The inset in (a) is the optical image of PVP printed twice.

Table 3.6 Optimized parameters for fabrication of E-jet printed PVP

Nozzle distance	30 μm
Waveform	Square wave (duty 25%)
Applying voltage amplitude	260 V (Bias 0 V)
Frequency	1,000 Hz
Printing pitch	2 μm
Printing speed	0.35 mm/s
# of Printing stacks	2
Substrate temperature	30 °C

3.3.4 E-jet printing of S/D electrodes with short channel length

The smearing of silver ink on PVP film was alleviated using the engineered PVP ink introduced in Section 3.3.3. In order to fabricate TFTs with short channel length of less than 10 ㎛, the source and drain (S/D) electrodes must be printed at intervals of several micrometers. However, with the engineered ink alone, it is difficult to form the fine S/D electrodes in which the silver ink does not penetrate into the channel area. One way to solve this issue is to increase the temperature of the substrate while printing the silver

electrodes. However, if the temperature of substrate exceeds over 30 ℃, the silver nozzle was rapidly clogged during the printing, resulting in unstable jetting of Ag ink. Therefore, it is necessary to further reduce the surface energy of the printed PVP layer to prevent the smearing of the silver ink.

To drastically reduce the surface energy of the lower layer, HMDS was spin-coated onto the printed PVP layer before the printing the S/D electrodes. Detailed surface treatment method with HMDS is introduced in Section 3.2.2. HMDS treatment makes the target surface more hydrophobic with replacing the functionalized groups such as hydroxyl (-OH) on the surface [91]. In addition, it greatly reduces the electron trap states present on the PVP surface, which helps in more stable transistor operation [92]. As a result, by employing the HMDS treatment, the S/D electrode pattern with a short channel length of about 5 ㎛ was successfully implemented as shown in Figure 3.11.

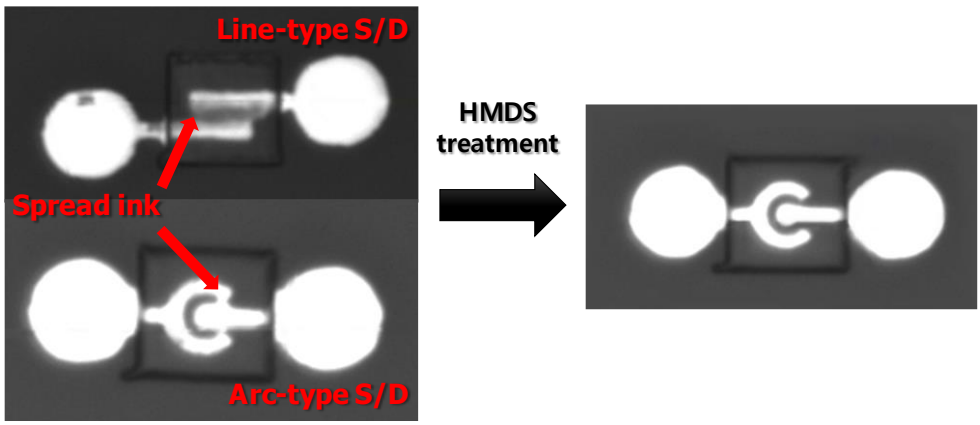

Figure 3.11 Optical image of S/D electrodes before and after HMDS treatment on the surface of E-jet printed PVP layer

In this thesis, for fabrication of all E-jet printed SWCNT-TFT with short channel length, arc type electrodes were adopted instead of conventional rectangular electrodes. This S/D geometry is called a Corbino structure. The main difference is that it exhibits asymmetric electrical characteristics under different drain bias conditions. Although the Corbino-type transistors have unique electrical characteristics [93], [94], [95], we adopt the Corbino structure from the viewpoint of fabrication process, not from the viewpoint of its exclusive electrical properties. The major difference, seen in E-jet printed SWCNTs for line-type and arc-type S/D electrodes, is that the leakage current is much larger for the SWCNT-TFTs with line-type electrodes. For detailed comparative analysis according to the shape of the S/D electrodes, see Section A.5.

3.3.5 Formation of SWCNT networks in E-jet printing system

When the SWCNT dispersion is directly discharged, nanotubes are aggregated together, and bundled tubes with metallic characteristics exist in the channel region and cause high leakage current. In addition, the nozzle filled with the SWCNT dispersion is easily clogged and the nozzle cannot be used for a long time. In addition, when SWCNT dispersion is e-jet printed, it is necessary to repeat printing at least 5 times to ensure a certain level of performance. In this case, the

uniformity between TFTs on a large area substrate is greatly reduced and the overall yield is not high. Therefore, instead of directly printing the separated semiconducting SWCNT dispersion, a method of indirect deposition was adopted.

For effectively depositing the semiconducting SWCNT layer onto the substrate, multi-dipping technique and in-situ printing the surface treatment material were utilized, which were previous reported in our group [83], [96]. After printing the PLL in all channel regions, the SWCNT network with good uniformity can be quickly deposited in the channel region of all devices through a multi-dipping technique. In addition, when printing the PLL directly to the channel region, it is possible to form a lot of attachment sites for SWCNTs in a short time intensively around the channel region and the S/D electrodes. Relatively small amounts of SWCNTs are present in the channel region when the substrate is immersed in the PLL and coated as a whole, rather than selectively printing the PLL in the channel region. It can be assumed that this is caused by the difference in wetting properties of the electrodes, PVP, and glass substrate. As shown in Figure 3.12, it was confirmed by SEM analysis that much more SWCNTs were present around the channel region and the S/D electrode when the PLL was directly printed on the channel region. The jetting conditions of the PLL are shown in Table 3.2, and the PLL was E-jet printed once with a line pitch of 2.5 ㎛ to cover the entire channel area.

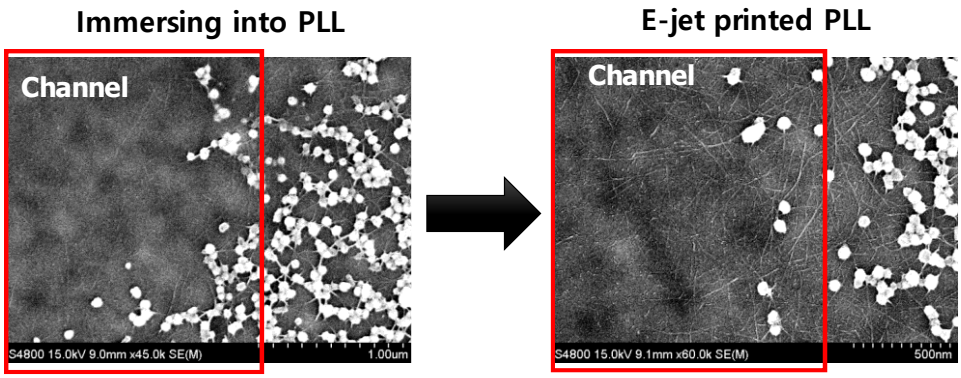

Figure 3.12 SEM image showing the difference in density of adsorbed SWCNTs in the channel region in red square border when the substrate was immersed in the PLL and the PLL was directly printed.

3.3.6 Overall process for all E-jet printing and electrical characteristics of all E-jet printed SWCNT-TFTs

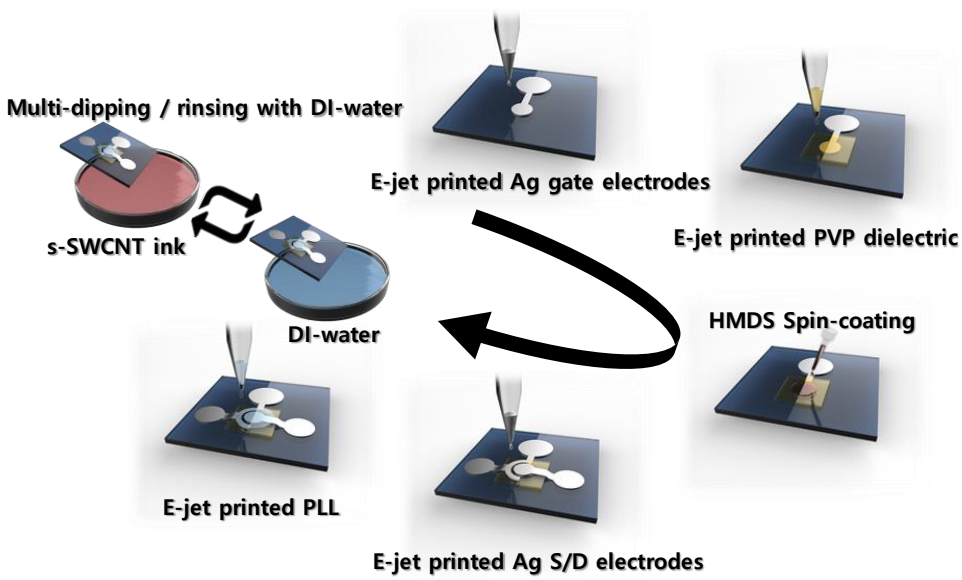

Figure 3.13 Overall fabrication process for all E-jet printed SWCNT-TFTs

After all the optimized processes from Section 3.3.2 to Section 3.3.4, we have succeeded in realizing all E-jet printed SWCNT-TFT. Figure 3.13 shows a schematic diagram depicting the entire E-jet printing process. Figure 3.14 (a) shows optical image of fabricated all E-jet printed SWCNT-TFT. We defined the channel dimension by the Corbino-shape electrode with the designed value of angle, and in our fabricated device, the channel width (W) and length (L) are 24.7 ㎛ and 5 ㎛, respectively. It can be seen that the silver of the S/D electrode does not penetrate into the desired channel region and the channel region is clearly distinguished.

Figure 3.14 (b) and (c) exhibit the transfer characteristics, and output characteristic of representative unit-device of fabricated SWCNT-TFTs. Gate voltage (V_G) was swept by forward direction from 5 V to −5 V and again swept back from −5 V to 5 V for hysteresis analysis. The currents at the drain and gate electrodes were measured at the drain voltage (V_{DS}) of −1 V. Electrical characteristics of the all E-jet printed SWCNT-TFTs, such as field-effect mobility, threshold voltage, were extracted from measured the transfer characteristic. With the measured gate capacitance of 8.2 nF/cm^2, the mobility is about 6.5 cm^2/V · s, and threshold voltage is about 2.4 V. In particular, it is noted that the on/off current ratio of our fabricated device is about 10^6, and especially the off-leakage current level exhibits under 2 pA, which is attributed to not only the insulation property of our highly-engineered PVP dielectric but also the minimized pattern size of PLL.

We cannot observe noticeable issue about contact resistance between the active region and S/D electrodes deposited on the printed PVP layer while considering the output characteristic. Therefore, we can strongly insist that our fully-engineered materials, fabrication processers, and the geometric structure of the TFT are suitable for the implementation of high-performance all E-jet printed SWCNT-TFTs.

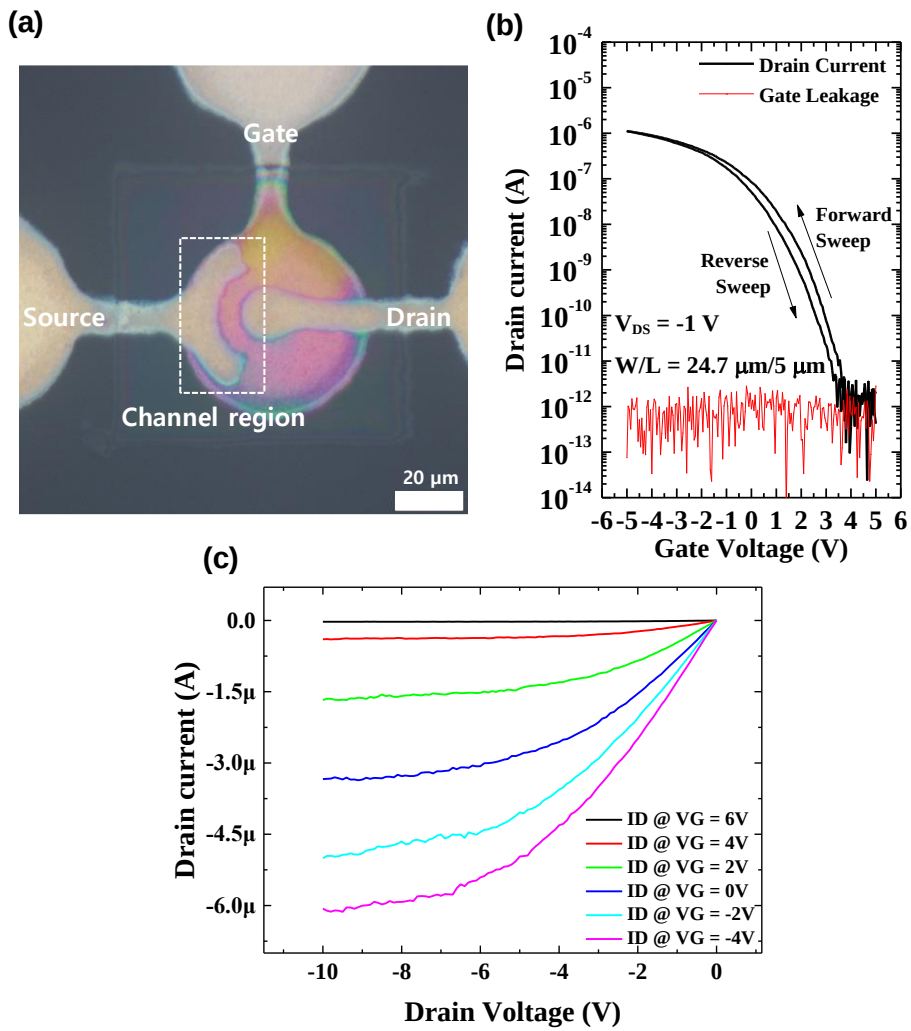

Figure 3.14 (a) Optical image, (b) transfer characteristics, and (c) output characteristics for all E-jet printed SWCNT-TFT

Meanwhile, the turn-on voltage of the SWCNT-TFT manufactured through the all EHD-printing process above is about 4 V, and the V_T tuning technology introduced in Chapter 2 was employed to compensate it in the 0 V direction. After finishing the SWCNT adsorption process by multi-dipping technology, chemical encapsulation was applied by drop-casting the NH_4OH solution on the TFT region.

The electrical properties including transfer characteristics and output characteristics of NH4OH-treated all E-jet printed SWCNT-TFT are shown in Figure 3.15. Through the chemical encapsulation by NH_4OH, the turn-on voltage was adjusted from 4 V to 2.4 V. However, it can be inferred that the contact resistance between the SWCNT and the S/D electrodes increases and the interfacial traps sites between the gate insulator and the SWCNT increase as the mobility and the sub-threshold slope (S.S) decrease and increase, respectively. Nevertheless, hysteresis rarely exists from 0.4 V to 0.04 V, as the electronic suppression effect on the surfaces of nanotubes due to the oxygen and moisture around CNTs has been fairly nullified through NH_4OH treatment.

After ammonia treatment, the gate leakage current or off-state current was maintained, but the on-off current ratio was reduced to around 10^5 due to the decrease in the overall conductivity of the device. In the output characteristic, it can be seen that the slope which was quite steep before the treatment was slightly smoother after the ammonia treatment.

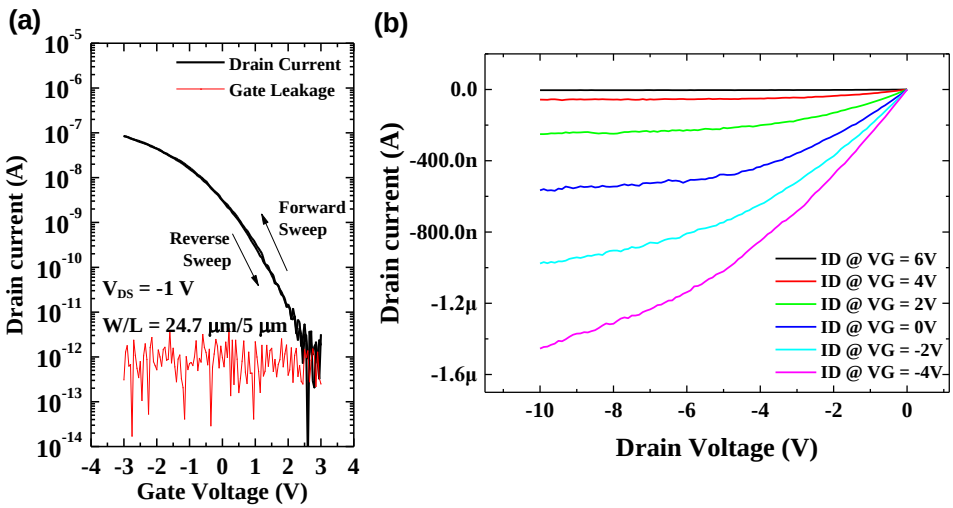

Figure 3.15 (a) Transfer characteristics and (b) output characteristics for NH_4OH-treated all E-jet printed SWCNT-TFTs.

Table 3.7 Comparison of electrical parameters for the pristine and NH_4OH-treated all E-jet printed SWCNT-TFTs

	Pristine	**NH_4OH-treated**
Mobility [$cm^2/V \cdot s$]	6.5	2.1
Turn-on voltage [V]	4.0	2.4
Threshold voltage [V]	2.4	0.50
S.S [V/dec]	0.33	0.71
On/off ratio	~ 10^6	~ 10^5
Hysteresis [V]	0.4	0.04

3.4 Conclusion

In summary, we have demonstrated all E-jet printing system for SWCNT-TFTs by optimized E-jet printed materials including nanoparticle-type silver as the metal, PVP as the gate dielectric, and PLL as the enhancer to efficiently adsorb SWCNTs to a target substrate. By optimizing the silver ink and related process parameters, we succeeded in patterning the silver electrode with a greatly low resistivity of 1.7×10^{-7} Ω · m without any bending or smearing. About insulating film, with newly engineered PVP ink for E-jet printing system, the insulation properties of the E-jet printed PVP layer are much better than those of previously reported printed or solution-based insulating layers. Furthermore, overcoming the coffee ring effect and the roughness of the printed surface, one of the major difficulties in the solution process, a PVP thin film with very small RMS roughness of 5 mm or less was implemented by E-jet printing. In addition, a method using HMDS surface treatment was proposed to enable electrode patterning at the level of 5 ㎛ even on a PVP surface that is relatively hydrophilic compared to the substrate. In order to improve the uniformity and yield of the entire device, PLL ink was printed only in the necessary area, and SWCNT networks were derived that self-assembled at once on all devices on the substrate.

After all the optimization of each individual material was completed, each layer was combined in an environment where

temperature and humidity and external vibration were completely controlled, and finally SWCNT-based all E-jet printed transistor was efficiently implemented. When printing each layer, the misalignment occurring in each layer is very small, within 1 to 2 ㎛. The all E-jet printed SWCNT-TFTs with short channel length of 5 ㎛ exhibit high on-current and low off-state leakage current, resulting in good mobility of 6 $cm^2/V \cdot s$ and high on-off current ratio of 10^6. In addition, the adjustment of threshold voltage technology presented in Chapter 2 can be applied to this E-jet printed devices, and it is expected that it would be useful for robust circuit design using two or more TFTs to be introduced in Chapter 4. The maximum process temperature required for all E-jet printing systems presented in this Chapter is 160 ℃, so it can be applied not only to glass substrates, but also to plastic, fiber, elastomer substrates.

Chapter 4

All Electrohydrodynamic-jet Printing system-based Circuit Design for High-resolution and Highly Integrated Applications

4.1 Introduction

Efforts for minimizing the overall dimensions of transistors and overall integrated circuits have been made as one of the most important technical goals in all electronic applications from the moment Moore's Law came to this day [103]. The benefits of miniaturization and high integration of transistors are high performance, fast operation, and low-power operation, which is key role in high-performance logic devices such as microprocessors, high capacity memory device, portability of electronic devices such as smartphones, and high-resolution displays. In particular, in order to improve the degree of integration of transistors, a vertically stacked structure that is extended in three dimensions from an arrangement of two-dimensional transistors has been applied to further increase the degree of integration.

For high-resolution and high integration of electronic devices in the next generation flexible, stretchable and wearable electronics as well as conventional silicon wafer-based microelectronics, many

research groups have previously reported the three dimensional stacking structure for the circuit including two or three transistors to effectively utilize the pixel area for the high-resolution applications with organic and oxide semiconducting materials instead of silicon based semiconductor or adopting new fabrication process such as inkjet-printing [97], [98], [99]. Also, a high-resolution fingerprint sensor has been reported using the vertically stacked structure composed of oxide TFTs and capacitors [100]. The cross-sectional structure of the inverter circuit using vertically stacked organic TFTs [97] and the vertically stacked capacitive finger sensor based on oxide TFT [100] is shown in Figure 4.1.

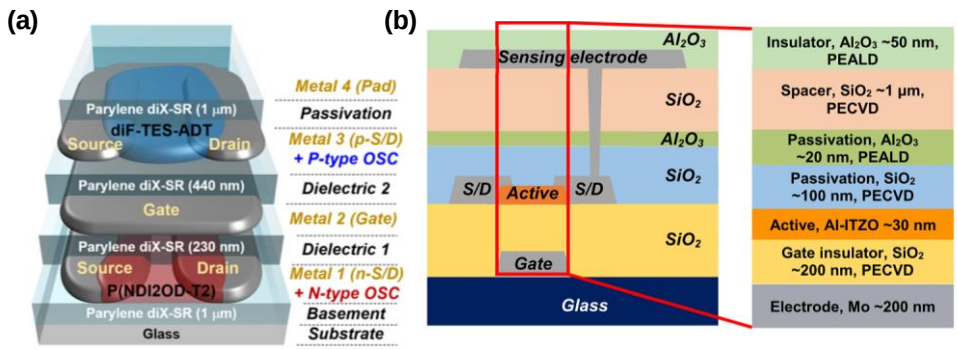

Figure 4.1 Vertical structure for (a) Inkjet-printed inverter with organic semiconducting materials [97] and (b) capacitive fingerprint sensor with oxide semiconductor [100].

In the vertically stacked structure, it is important to form an interconnect for connecting electrodes in each layer, and in order to generate such interconnections, a process of drilling via-holes in an insulating layer that separates each layer is essential. Most of the via-hole forming processes utilized photolithography method, but some methods of direct drilling through laser and patterned shadow mask have been reported, but many of these processes are non-solution processes. Non solution-processed fabrications of via-hole interfere with the ongoing process of the solution process-based devices and increase the complexity of the overall process, which can lead to an increase in the cost of the entire process. A method of forming a via-hole through inkjet printing based on a solution process has recently been reported. A via-hole of 200 ㎛ diameter was implemented by discharging a solution by inkjet printing to partially dissolve the underlying insulating layer, which allows continuous manufacturing of all solution-processed devices in the same environment [101]. However, in the fabrication of via-holes based on the solution process, there is a limitation in forming a via-hole with a smaller diameter comparable to the non-solution process.

In this Chapter, we introduced a high-resolution and highly integrated circuit design for applications such as diode-connected transistor, inverter logic gate, active pixel sensor (APS) for image detector, and active matrix pixel circuit for polymer light-emitting diode (PLED), containing two or more transistors per single pixel by utilizing all E-jet printed SWCNT-based transistors covered in Chapter 3 and adoption of vertically stacked structure. In order to

maximize the density of pixels in our 3D stacking structure, in-situ formation technology of via-hole structure based on the E-jet printing system was developed and vertically connected circuits including diode-connect load-based logic inverter and pixel circuits for APS and active matrix PLED with the developed via-hole structure were introduced without separate via-hole patterning processes. By using in-situ formation technology of via-holes, via-holes of several micrometer scale can be formed, and the overall device size can be significantly reduced. With utilizing the fully engineered E-jet printing technology and optimization of integrated circuit design, we suggest that a matrix array of novel design with active pixel circuits of up to 250 pixels per inch (ppi) level is expected to be feasible at a process temperature of up to 160 ℃ by the solution process alone, which suggests that all-printed high-resolution image display or sensor array can be fully implemented on flexible and stretchable substrate-based platforms in the near future.

4.2 Experimental details

4.2.1 In-situ fabrication of via-hole and diode-connected SWCNTs-TFTs in all E-jet printing system

To form an interconnect between metal layers placed above and below the PVP layer, the insulating film of PVP was E-jet printed except for the via-hole region with a diameter of 10 ㎛ or less, which was practicable by forming an arbitrary pattern of several micrometer scale through E-jet printing. We define this via-hole fabrication process as 'in-situ via-hole printing'. To confirm that the via-hole was properly fabricated, an E-jet printing-based metal-insulator-metal structured device was manufactured. The resistance characteristics for the interconnect were measured by probing each of the upper and lower electrodes. Additionally, line profile analysis was performed to check the surface roughness of the PVP layer including via-hole with surface profiler.

Based on the manufacturing process of all E-jet printed SWCNT-TFT in Section 3.2.2, the PVP ink was selectively printed on the rest of the area except for the central portion so that the via-hole was naturally located at the center of the gate electrode without additional process for via-hole. When the S/D electrodes are printed on the PVP layer containing the via-hole, the inner circle electrode and the bottom gate electrode are connected to each other through the via-hole to form a diode-connected structure.

4.2.2 Fabrication process of all E-jet printed inverter with vertically stacked SWCNT-TFTs

The circuit configuration and schematic diagram of the vertically stacked p-type only inverter consisting of driving transistor (drive TR) and depletion load transistor (load TR) based on all E-jet printed SWCNT-TFT are shown in Figure 4.2. Each condition of printing process corresponding to the electrode, insulating film, and active layer is the same as the method described in Section 3.2. After printing the circular electrode (input, V_{in}) having a diameter of 72 ㎛ on the glass substrate, the first PVP layer having a thickness of about 300 nm is printed in a square form of 100 ㎛. The circle-shape electrode with a diameter of 36 ㎛ and the full circle-type outer electrode with inner diameter of 54 ㎛ and outer diameter of 72 ㎛ were printed to form the output electrode (V_{out}) and the voltage supply electrode (V_{DD}), respectively. After forming the active channel of the drive TFT through the deposition method of SWCNTs introduced in Section 3.2.2, the NH_4OH chemical encapsulation suggested in Chapter 2 was employed to control the threshold voltage (V_T) of the drive TR for operating in the enhancement mode. The second PVP insulating layer was E-jet formed on the fabricated drive TFT except for the via-hole region of 10 ㎛ diameter. Finally, after E-jet printing the S/D electrodes of quarter circle-type Corbino structure with an inner diameter of 20 ㎛, an outer diameter of 40 ㎛, and a 10 ㎛-width of outer electrode, SWCNTs were deposited in

the channel region in the same way as the driving TR except for NH_4OH treatment. The inner electrode of the load TR is connected to the V_{out} electrode through the via-hole, and the outer electrode was connected to ground (GND), resulting in the all E-jet printed vertically stacked inverter based on SWCNT-TFTs. The overall fabrication steps for all E-jet printed SWCNT-based inverter with vertically stacked structure are summarized in Figure 4.3.

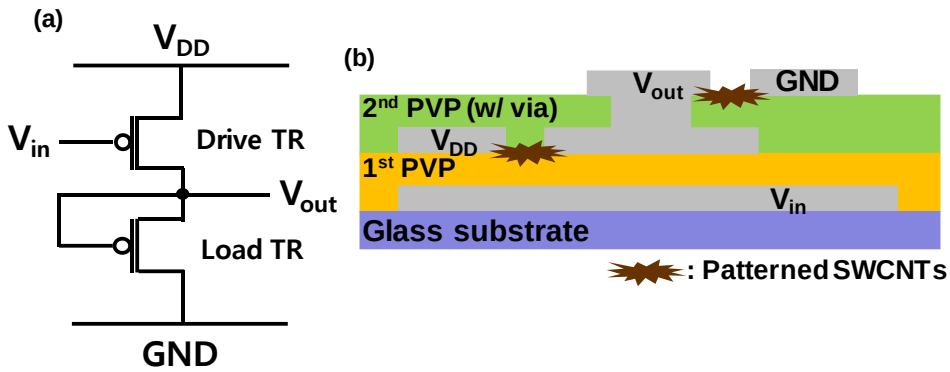

Figure 4.2 (a) Circuit configuration and (b) schematic diagram of the vertically stacked p-type only inverter based on all E-jet printed SWCNT-TFTs.

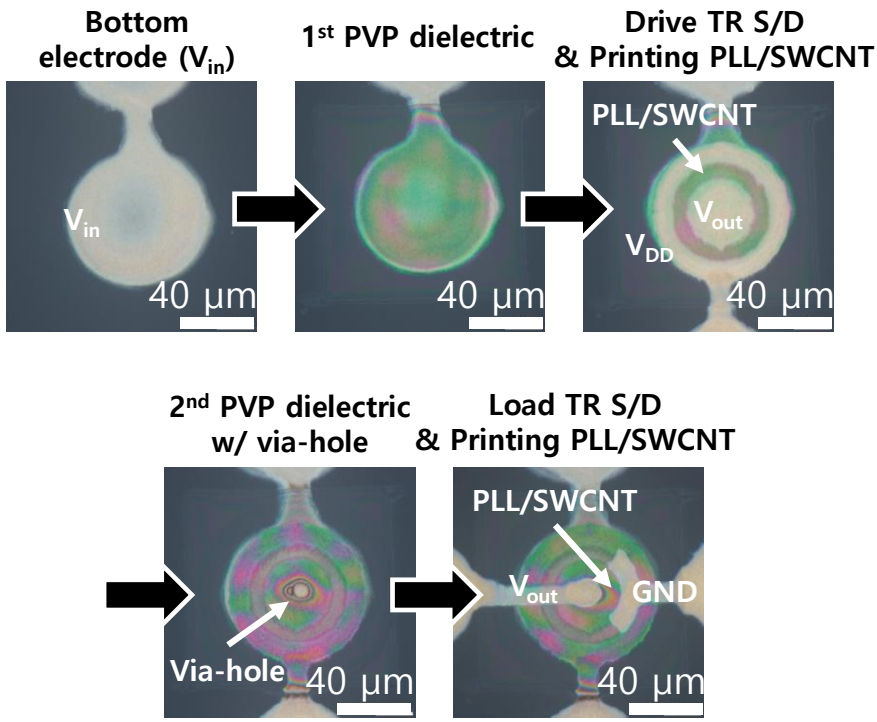

Figure 4.3 The overall fabrication steps for all E-jet printed SWCNT-based inverter with vertically stacked structure.

4.2.3 Fabrication process of all E-jet printed active pixel sensor for image sensor with vertical stacking structure

The active pixel sensor (APS) covered in the thesis consists of one photodiode and three transistors, and the part of photodiode is replaced by a diode-connected SWCNT-TFT. The circuit of the APS and the cross-section structure of the E-jet printed APS are shown in Figure 4.4. All printing conditions for the Ag, PVP, PLL and SWCNTs are the same as previously mentioned conditions. After

printing the electrodes of the Corbino structure with an inner diameter of 13 ㎛, an outer diameter of 28 ㎛ and a 10 ㎛-width of outer electrode, SWCNTs are deposited in the same manner as before. After printing the first PVP layer containing 10 micro-diameter via-hole through in-situ via-hole printing, the circular electrode with a diameter of 60 micrometers was printed, followed by printing the second PVP including the via-hole same as the first PVP layer. In printing the third silver electrodes, the diameter of the center electrode is 20 ㎛, the width of the other three electrodes is 10 ㎛ each, and each electrode is 5 ㎛ apart, which consists of the channel for the three transistor in APS. After depositing as in the previously mentioned method, the last PVP was printed without a via-hole pattern, followed by printing the two Ag electrodes 10 ㎛. Each printed electrode was connected to the corresponding node shown in Figure 4.4 (b). The overall fabrication steps with optical images are summarized in Figure 4.5.

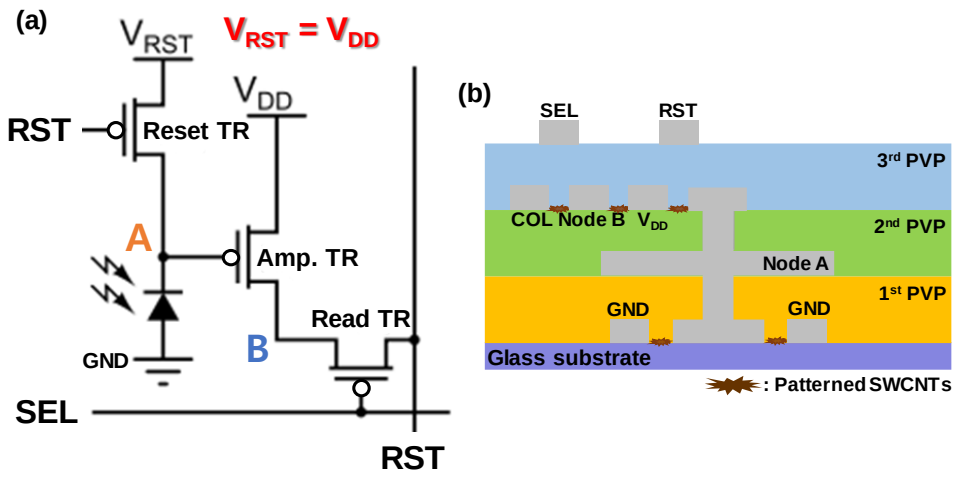

Figure 4.4 (a) Circuit and (b) schematic diagram of the vertically stacked APS based on all E-jet printed SWCNT-TFTs.

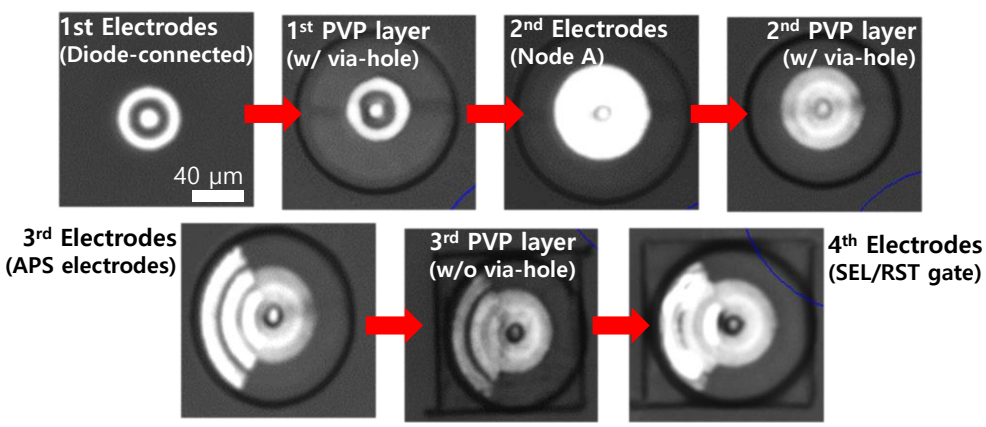

Figure 4.5 The overall fabrication steps for all E-jet printed SWCNT-based APS with vertically stacked structure.

4.2.4 Fabrication process of all E-jet printed pixel circuit for active matrix polymer light-emitting diode with vertical stacking structure

The pixel circuit for active matrix polymer light-emitting diode (PLED) and schematic of the device is illustrated in Figure 4.6. It is divided into the E-jet printed backplane part, consisting of two SWCNT-TFTs and one capacitor, and the spin-coated PLED part, of which the PLED part was implemented using the fabrication process reported by the our group [73], [102].

The configuration of the E-jet printed backplane is as shown in the lower part of Figure 4.6 (b). The bottom Corbino S/D electrodes with an inner diameter of 60 ㎛, an outer diameter of 76 ㎛ and a width of 10 ㎛ were printed on the glass substrate. The outer electrode was printed in an arc-shape with a center angle of 150 degrees. The SWCNT was deposited on the channel of switching transistor by previously mentioned method, followed by NH_4OH-based chemical encapsulation for adjusting the threshold voltage of the switching transistor. After printing the first PVP insulating film, a second electrode layer composed of one central circular electrode and two arc-shape electrodes having a central angle of 120 degrees was printed. The diameter of the central electrode is 42 ㎛, the inner diameter and the outer diameter for each outer electrode is 58 ㎛ and 76 ㎛, respectively. The SWCNT-based channel for driving transistor was also deposited in the similar way to the switching

transistor excluding NH_4OH treatment. For the clear separation of the backplane part and the PLED part, the previously mentioned printing method of the PVP ink was repeated twice to make an interlayer insulating layer (IIL) with a thickness of 660 nm and the via-hole pattern of 8 ㎛-diameter, followed by E-jet printing circle-shape Ag cathode of 80 ㎛-diameter. The overall fabrication steps for vertically stacked pixel circuit are summarized in Figure 4.7.

In the part of PLED, the functional layers including zinc oxide (ZnO), polyethyleneimine (PEI), super yellow solution (PDY-132, Merck), and less conductive poly(3,4-ethylenedioxythiophene):-poly(styrenesulfonate)(PEDOT:PSS) as hole injection layer (HIL) were spin-coated on the E-jet printed Ag bottom cathode sequentially, and then the highly conductive PEDOT:PSS electrode (top anode) were spin-coated last on the HIL. Detailed information of the materials and fabrication process is described in [73], [102].

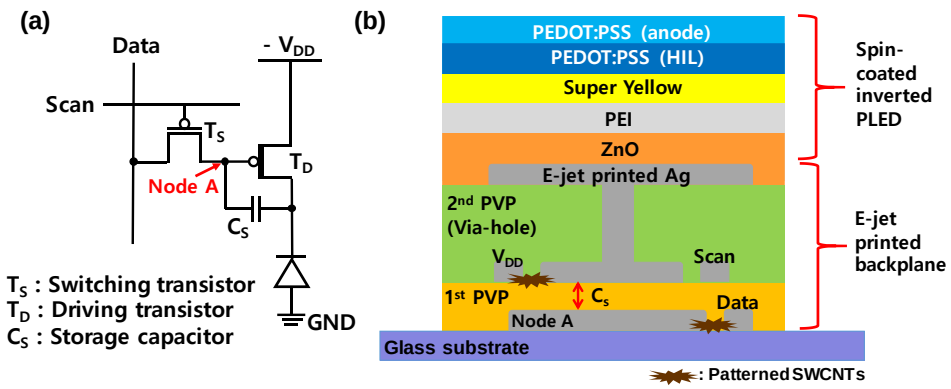

Figure 4.6 (a) Circuit and (b) schematic diagram of the vertically stacked pixel circuit for active matrix PLED based on all E-jet printed SWCNT-TFTs.

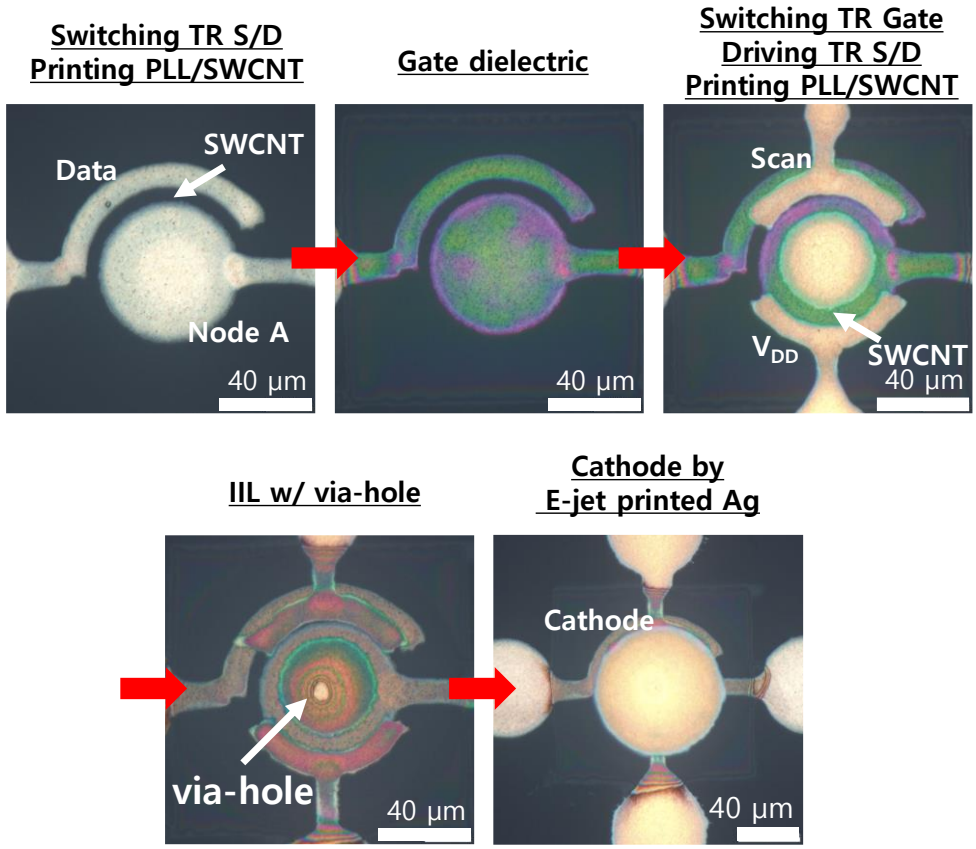

Figure 4.7 The overall fabrication steps of all E-jet printed SWCNT-based pixel circuit for active matrix PLED with vertically stacked structure.

4.3 Results and discussion

4.3.1 In-situ via-hole formation technology based on all E-jet printing system

As described in Section 4.2.1, with simply non-printing on the target area for via-hole and filling the un-printed hole region with the Ag ink, we can easily in-situ fabricate the interconnection part of the vertically stacked circuit as well as the insulation part of other regions. Figure 4.8 show the optical image and surface profile of the PVP including the via-hole. The via hole was clearly defined at the center of the E-jet printed PVP film and formed in a desired shape and size. Since the coffee-ring effect of the E-jet printed PVP thin film was minimized in Section 3.3.3, the line profile characteristic shows that the coffee ring effect is significantly suppressed in the vicinity of the via-hole and the edge of the PVP film. The RMS roughness of the rest of the via-hole is 3.2 nm, which means that the E-jet printed PVP films maintain the flat surface morphology characteristic regardless of fabrication of the via-hole.

Moreover, the resistance of the interconnect at the via-hole was extracted by measuring current-voltage (I-V) characteristics of the electrodes connected to each other through the via-hole (See Figure 4.8 (c) and the inset of (d)), resulting in the resistance of 32 Ω. Considering the resistance of E-jet printed silver line in Figure 3.5 (c), the resistance of the interconnect is negligible.

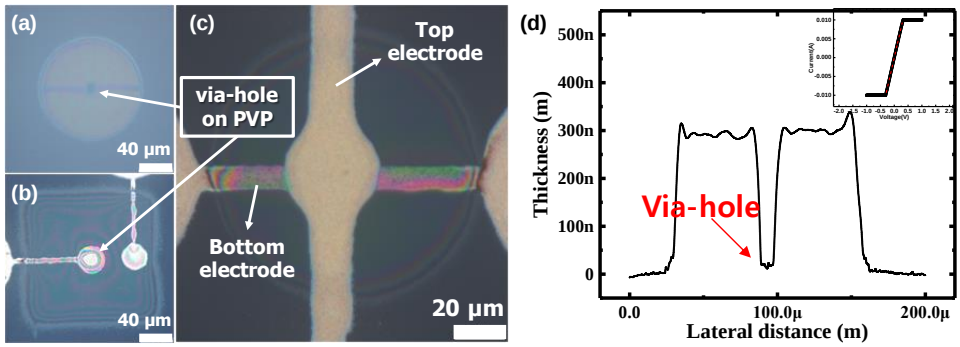

Figure 4.8 (a) and (b) Optical images for the E-jet printed PVP films containing the via-hole and (c) metal-insulator-metal structure with in-situ printed via-hole. (d) Line profile of the via-hole with the diameter of 10 ㎛. I-V characteristics for the interconnect are shown in the inset of (d).

4.3.2 Additional E-jet printing of PVP layer on the SWCNT-TFTs

Before implementing a circuit in which a vertically stacked structure is grafted, an additional PVP layer is printed on a single SWCNT-TFT manufactured in Chapter 3 to predict the situation when another TFT is stacked on top, and the change in electrical characteristics of the TFT is measured. Figure 4.9 (a) shows the change in the transfer characteristics after printing the upper PVP layer onto the all E-jet printed SWCNT-TFT without any chemical encapsulation. The most notable changes are that the turn-on voltage is very close to zero voltage with the ambipolar transport characteristics. As detailed in

Section 1.4, SWCNTs intrinsically have the ambipolar carrier transport. It is presumed that SWCNT exhibits intrinsic properties as the additional PVP layer acts as a passivation. The NH_4OH-treated samples also exhibit a similar pattern as shown in Figure 4.9 (b). When comparing the transfer characteristics of PVP-passivated SWCNT-TFTs with or without NH_4OH treatment, the NH_4OH-treated sample generated the wider off-region as shown in Figure 4.9 (c), which is attributed to the effect of chemical encapsulation by NH_4OH as described in Chapter 2. In common, there is a feature that mobility is greatly reduced when printing the upper PVP, which means that the transport of holes is limited by the added PVP layer. The presumed reason is that the oxygen around the CNT is blocked after the process, resulting in intrinsic CNT. At the same time, the presence of a fixed positive charge in the E-jet printed PVP layer bends the energy band of the SWCNT downward, limiting the movement of the hole and conversely increasing the conduction of electrons. The reduction of hole mobility and the expression of ambipolar characteristics are similar to the phenomena when the passivation of insulating films such as Al_2O_3 and HfO_2 over the network of SWCNTs is applied [43].

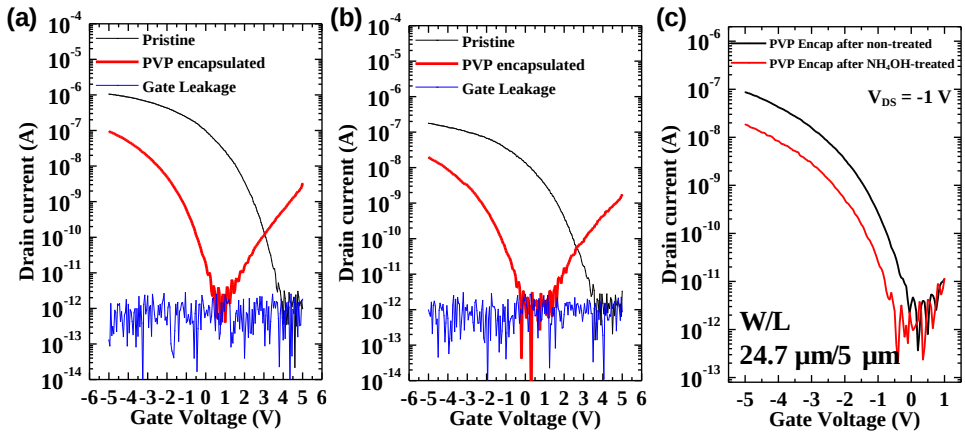

Figure 4.9 Change in the transfer characteristics by printing the upper PVP film on (a) pristine SWCNT-TFT and (b) NH_4OH-treated SWCNT-TFT. (c) Comparison of the transfer characteristics of PVP-passivated SWCNT-TFTs with or without NH_4OH treatment.

4.3.3 Electrical characteristics for all E-jet printed diode-connected SWCNT-TFTs

When the via-hole structure is inserted in the center of the gate dielectric in the structure of the fully E-jet printed SWCNT-TFT fabricated in Section 3.3.6, the gate electrode and the inner electrode in the Corbino S/D electrodes are naturally connected to each other, resulting in the diode-connected SWCNT-TFTs, as shown in Figure 4.10. The fabricated device has a channel length of 5 ㎛ and an effective channel width of 88 ㎛, and the change in the transfer characteristics after printing the additional PVP layer onto the device was also measured and shown in Figure 4.11.

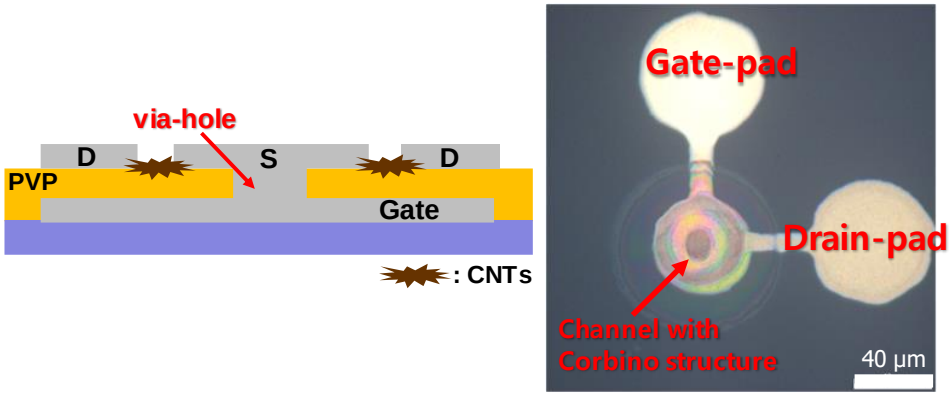

Figure 4.10 Schematic diagram and optical image of all E-jet printed diode-connected SWCNT-TFT.

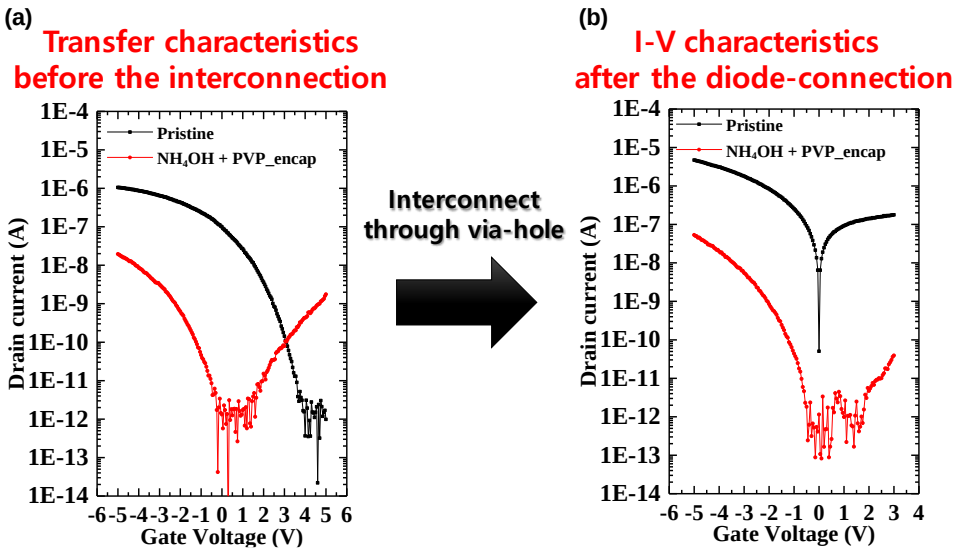

Figure 4.11 Transfer characteristics of (a) the conventional TFT without via-hole and (b) the diode-connect TFT through the via-hole located at the center of the PVP gate insulating layer. The black line is the data of the sample where the SWCNT is exposed to the air as it is, and the red line is the data of the sample with the additional PVP layer printed on the SWCNT.

In the case of the diode-connected SWCNT-TFT through the via-hole, it exists as off-state in positive gate bias and the current in off-state is called reverse bias current similar to photo-diode. It can be seen that the reverse bias current is very large (above 100 nA) due to the large positively shifted V_T of the SWCNT-TFT in the air. On the other hand, in the case of the sample with the NH_4OH post-treatment and the additional upper PVP insulating layer through printing of the PVP ink (red line in Figure 4.11), it shows a reverse bias current as low as 1 pA, which is attributed to nearly zero turn-on voltage for the NH_4OH-treated SWCNT-TFT with the passivation layer by the upper PVP layer. Diode-connected TFTs with very low reverse bias currents are useful in applications that detect very small changes in current, such as photodetectors. In Section 4.3.5, based on the diode-connected SWCNT-TFT with the low reverse bias current, we have implemented the fabrication of an active pixel sensor with vertically stacked structure for the image sensor.

4.3.4 Electrical characteristics for all E-jet printed inverter with vertically stacked SWCNT-TFTs

SWCNT-based p-type only inverter is composed of a driving transistor that regulates the current according to the input voltage and a diode-connected load transistor that operates in depletion mode. To realize the improved switching characteristic, voltage gain,

and full-swing inverter, the recommended operating mode of the driving transistor (drive TR) is the enhancement mode, so the turn-on voltage of the driving TFT needs to be close to 0V. Through the threshold voltage (V_T) adjustment technology by chemical encapsulation presented in Chapter 2, the V_T of the driving TFT was shifted in the negative direction as much as possible, and the channel width of the driving TFT was increased by more than 5 times compared to the channel width of the load TFT in order to offset the decrease in mobility of more than 75% due to the effect of the encapsulation by PVP and chemical encapsulation by NH_4OH, as described in Section 4.3.2.

The optical image of the SWCNT-based inverter with vertically stacked structure produced through the all E-jet printing system is shown in Figure 4.12 (a). As shown in the optical image, the full-circle type Corbino S/D electrodes were applied to the driving TFT to match the current of the driving transistor to the current level of the load transistor. The channel width and length of the driving TFT located at the bottom layer of the vertically stacked inverter are 142 ㎛ and 6.2 ㎛, respectively, and the linear field effect mobility is 0.24 ± 0.059 $cm^2/V \cdot s$, and the turn-on voltage is about +2 V. On the other hand, the S/D structure of the load TFT located on the top of the vertically stacked inverter has an arc shape of 90 degrees, the channel width and length are 23.4 ㎛, 10 ㎛, the mobility is 1.8 ± 0.84 $^2/V \cdot s$, and the turn-on voltage is measured to be about 4V. The transfer characteristics of the driving TFTs and load TFTs are depicted in Figure 4.12 (b) and (c), respectively.

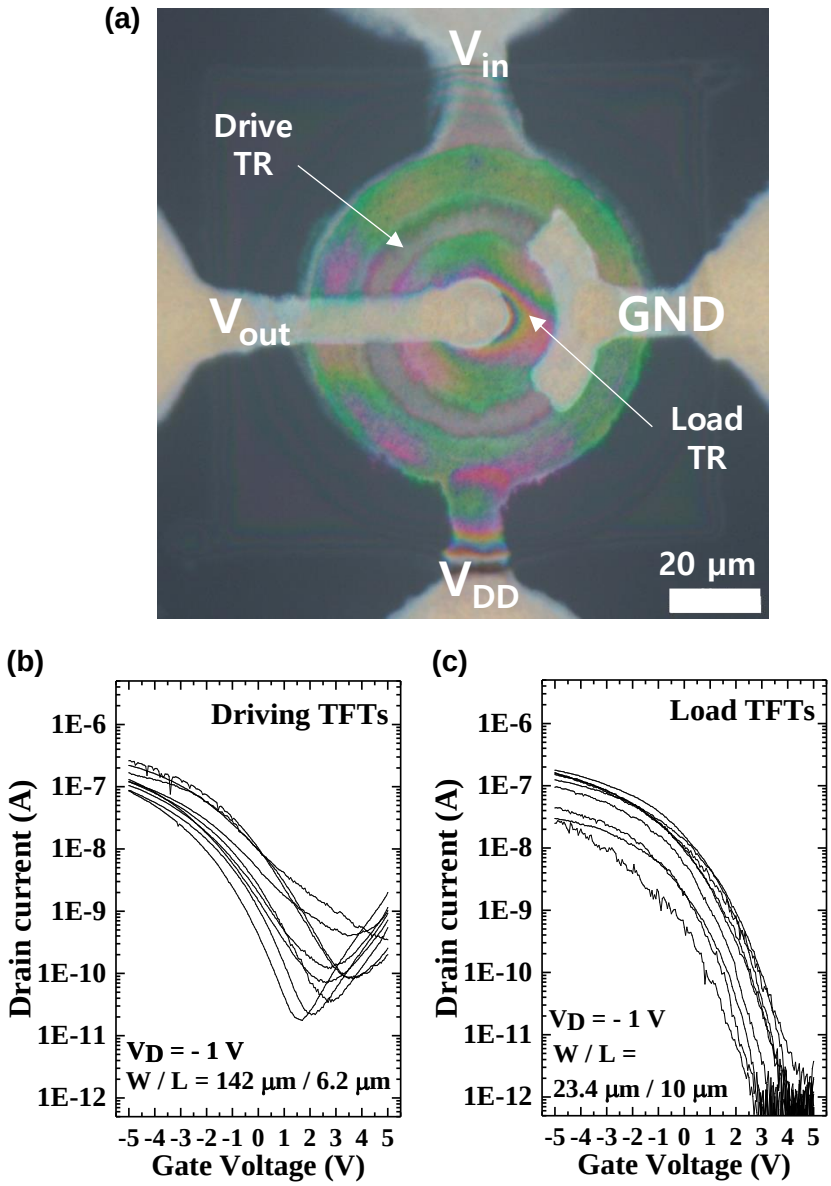

Figure 4.12 (a) Optical image of all E-jet printed p-type only inverter based on vertically stacked SWCNT-TFTs. (b) and (c) Transfer characteristics for driving TFTs and load TFTs in the fabricated inverter, respectively.

The all E-jet printed inverter with vertically stacked structure composed of SWCNT-based driving TFT and diode-connected load TFT exhibits voltage transfer characteristics as shown in Figure 4.13. The output voltage is completely switched from the near-ground to V_{DD} depending on the input voltage, and the voltage gain is around 1.5 V/V. Although the output voltage does not drop completely to 0 V due to the structural limitation of the p-type only inverter, not the CMOS-type inverter, it can be seen that the output voltage is almost completely switched to the V_{DD} when the input voltage is low, which is attributed to the driving TFTs whose the V_T and turn-on voltage are negatively adjusted through the chemical encapsulation by NH_4OH unlike the load TFTs which are operated in the deeply depletion mode. Similar effects above have already been observed in Section 2.3.5.

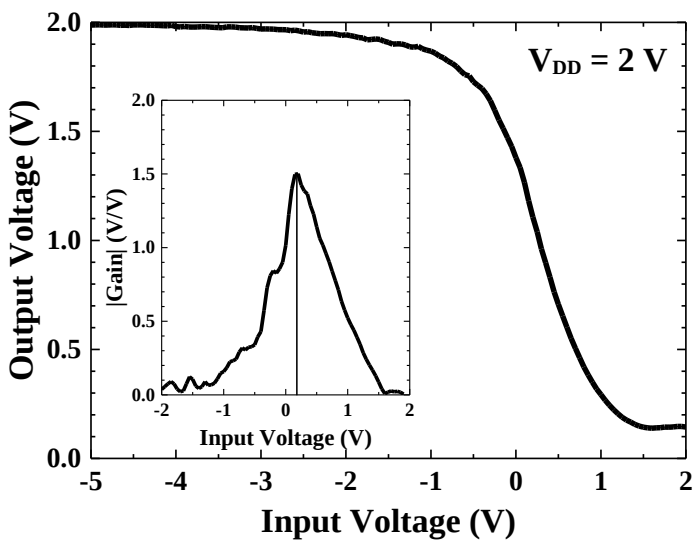

Figure 4.13 Voltage transfer characteristics and voltage gain for all E-jet printed SWCNT-based inverter

4.3.5 Structure design for active pixel sensor based on vertically stacked E-jet printed SWCNT-TFTs

As can be seen from the optical properties of SWCNTs introduced in Section 1.1, SWCNTs show little reactivity to light in the visible region, but weak photo-reactivity in some red and infrared (IR) regions. In general, semiconducting SWCNT-based IR-photodetectors tend to exhibit low responsivity of 10^{-3} A/W [104]. Figure 4.14 (c) shows the variation of reverse bias current according to IR laser (wavelength : 980 nm, intensity : 1 mW/cm^2) for all E-jet printed diode-connected SWCNT-TFT fabricated in Section 4.3.3. SWCNT-based diode-connected TFT can replace the IR-photodetector, and slight change of the reverse bias current and weak tendency were observed with IR laser exposure, but generally this level of response is almost impossible to utilize as a practical IR-image detector.

Several methods have been reported to improve responsivity of SWCNT-based photodetectors by applying an asymmetric electrode structure [105] or by depositing graphene to increase the built-in potential and form a heterojunction inside the active region [15]. Alternatively, there is a method of amplifying a photo-current with the help of an external circuit rather than the above material approach, and a weak signal detection can be amplified and observed by grafting an active pixel sensor (APS) structure composed of three or more transistors. Unlike the passive pixel

sensor (PPS), which contains only one switching TFT, the APS includes a TFT for amplification and a TFT for signal reset. The APS structure has the advantage of showing a faster readout time and a high signal-to-noise ratio compared to the PPS structure, but it has disadvantages in terms of uniformity and fill factor because several transistors are included in the pixel. Therefore, it can be said that realizing a fine and integrated APS structure is one of the technical goals.

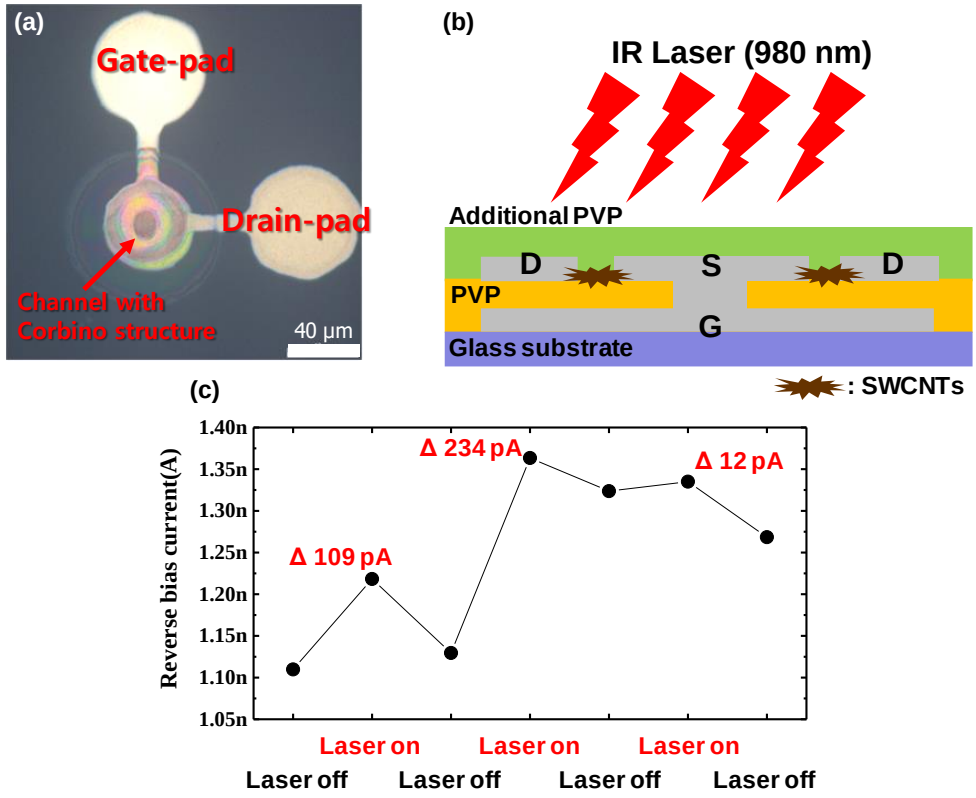

Figure 4.14 (a) and (b) Optical image and schematic diagram for all E-jet printed diode-connected SWCNT-TFT. (c) Change in reverse bias current according to IR exposure.

APS circuit that includes three SWCNT-TFTs and one diode-connected SWCNT-TFT acting as a photodetector was implemented through the all E-jet printing system and the grafting of vertically stacked structure, as shown in Figure 4.15 (a). The size of the implemented APS circuit is 100 ㎛, and it is possible to implement the 250 ppi array of the wavy structure proposed in Figure 4.15 (b). In the APS circuit proposed in this dissertation, light is sensed at the lowest diode-connected TFT part and signal amplification and signal reading are performed from integrated transistors on the top of the pixel. Through the optimized all E-jet printing system, it is possible to confirm with an optical image that integrated S/D electrodes arranged at about 5 ㎛ intervals are well defined. In the structure extended from the pixel to the array structure, the Corbino electrode structure in the pixel can be modified into a wavy bus line structure to implement the image sensor array. The IR detection performance of the diode-connected SWCNT-TFT was too weak and difficult to secure the consistency, so it was not possible to measure the actual signal in the APS structure. Nevertheless, it seems that there is great significance in implementing the 3D structure in which three or more transistors are integrated in a pixel space of less than 100 ㎛ through solution processing alone.

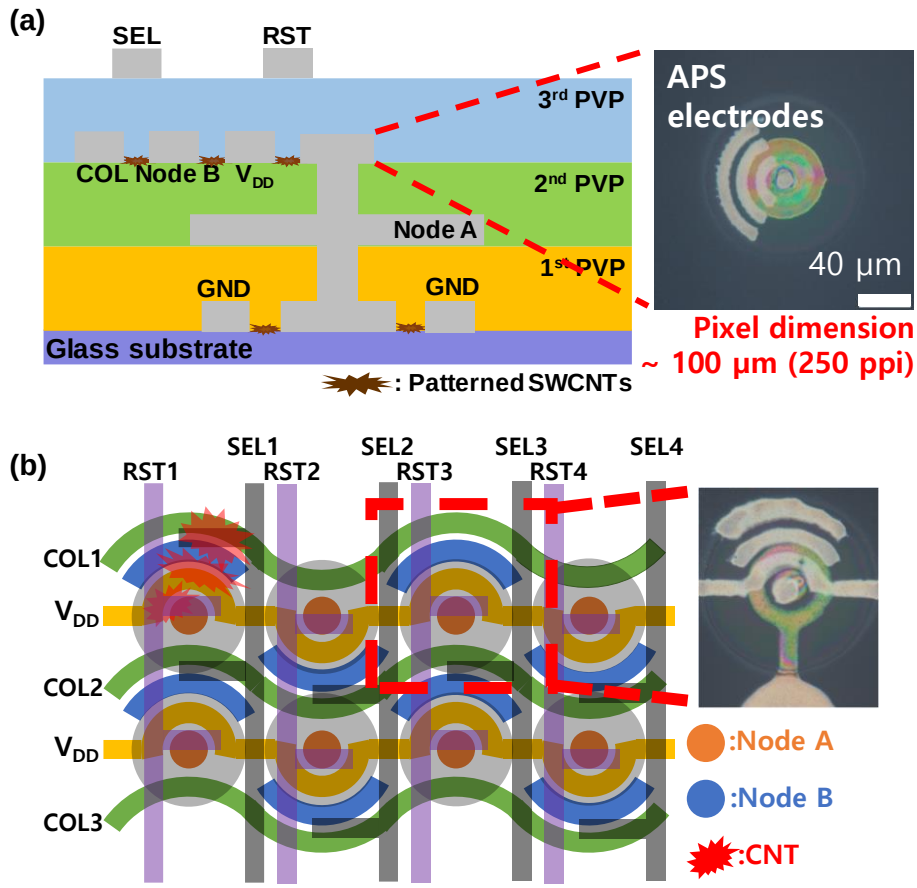

Figure 4.15 (a) Schematic diagram and optical image of all E-jet printed APS with vertically stacked structure. (b) Proposed APS array structure based on E-jet printing system.

4.3.6 All E-jet printed pixel circuit for active matrix polymer light-emitting diode with vertical stacking structure

Based on the fabrication process in Section 4.2.4, pixel circuits for active matrix polymer light-emitting diodes (PLED) were implemented through the all E-jet printing system, and vertically stacked structures as shown in Figure 4.6 (b) were adopted to

improve the degree of integration. The active matrix PLED pixel circuit implemented in this chapter consists of a switching TFT for selecting pixels, a driving TFT for providing current to the PLED, and a capacitor for storing data signals. The capacitance of storage capacitor located at the center of the pixel was measured to be about 250 fF, and the transfer characteristics of the switching TFTs and driving TFTs inside each pixel are shown in Figure 4.16 (c) and (d), respectively. The overall pixel dimension does not exceed 100 ㎛, which is enough to achieve an array of up to 250 pixel per inch, as shown in Figure 4.16 (b).

The channel width and length of the switching TFTs are 91.3 ㎛ and 6.0 ㎛, respectively, and the ammonia-based chemical encapsulation technique proposed in Chapter 2 was applied to realize lower off-current and negatively shifted threshold voltage (V_T). The mobility and V_T of the E-jet printed switching SWCNT-TFTs were measured to be 0.06 ± 0.05 $cm^2/V \cdot s$ and −0.52 ± 0.68 V, respectively, and mobility reduction and threshold voltage shift due to NH_4OH treatment were observed. Meanwhile, the channel width and length of the driving TFTs are 53.0 ㎛ and 6.5 ㎛, respectively, and ammonia-based chemical encapsulation was not applied to the driving TFTs for higher driving current. The mobility and V_T of the E-jet printed driving SWCNT-TFTs were measured to be 0.58 ± 0.21 $cm^2/V \cdot s$ and 0.51 ± 0.41 V, respectively.

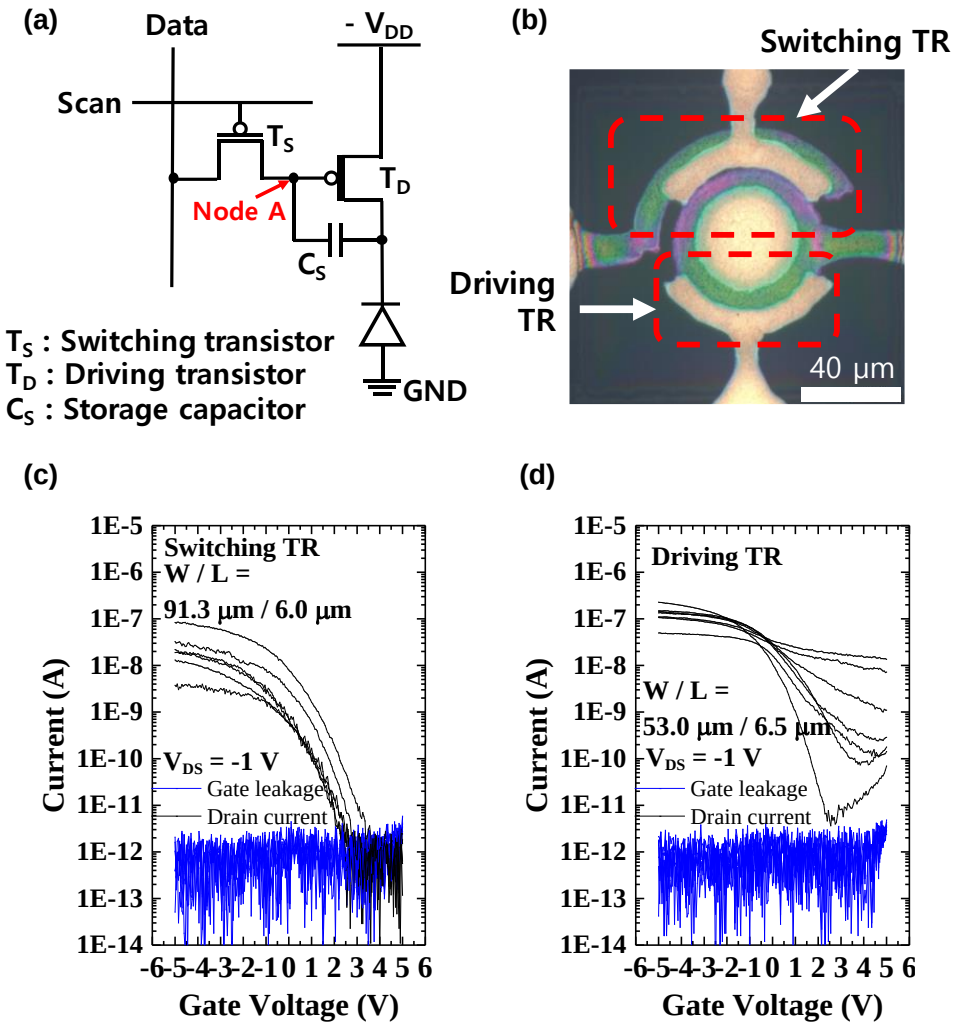

Figure 4.16 (a) Circuit configuration of pixel circuits for active matrix PLED. (b) Optical image of vertically stacked E-jet printed pixel circuits excluding the cathode electrode. (c) and (d) Transfer characteristics for switching and driving transistors in the pixel circuits, respectively.

The transfer characteristics and electrical characteristics including the linear field effect mobility and the V_T corresponding to the samples with the excellent on-current and off-current characteristics among the fabricated pixel circuits sample groups are shown in Figure 4.17 and Table 4.1, respectively. Although the on-current characteristic of the ammonia-treated switching SWCNT-TFT of the corresponding pixel sample is rather low, it shows a good on-off current ratio characteristic to show a very low off-current level under 1 pA. In the case of sub-threshold slope (S.S), switching TFT and driving TFT showed values of 0.25 V/dec and 0.55 V/dec, respectively.

Before coating the PLED layers on the pixel circuit fabricated through the E-jet printing system, the interlayer insulating layer (IIL) with a thickness of about 660 nm was E-jet printed to separate the TFT back-plane and the PLED front-plane using PVP ink. At the same time, a via-hole region with a diameter of about 7 ~ 8 ㎛ was simultaneously formed in the center, and the electrode of driving TFT and the cathode electrode of PLED were connected. ZnO, one of the functional layers of the PLED, which serves to assist the injection of electrons, is positioned directly above the cathode electrode, but without a separate surface treatment, the film quality is reduced due to poor wetting properties. The issue for de-wetting of ZnO can be solved as shown in Figure 4.18 when the sample is immersed in the PLL solution for 20 minutes before spin-coating of the ZnO layer.

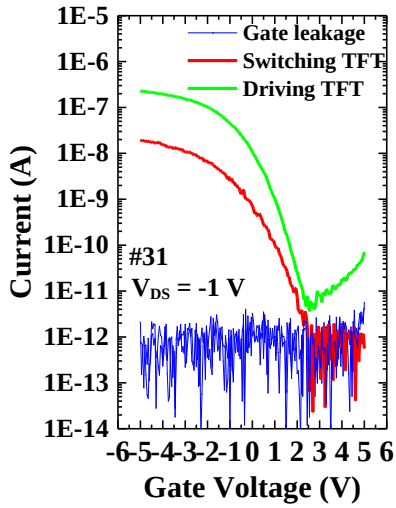

Figure 4.17 Transfer characteristics corresponding to the best sample among the pixel circuits.

Table 4.1 Electrical properties of TFTs in the pixel sample corresponding to Figure 4.17.

TR	Mobility [$cm^2/V \cdot s$]	V_T [V]	S.S [V/dec]	$V_{turn-on}$ [V]	On/Off Ratio
Switching	0.070	-2.2	0.25	2.7	~ 10^5
Driving	0.92	-0.32	0.55	2.4	< 10^5

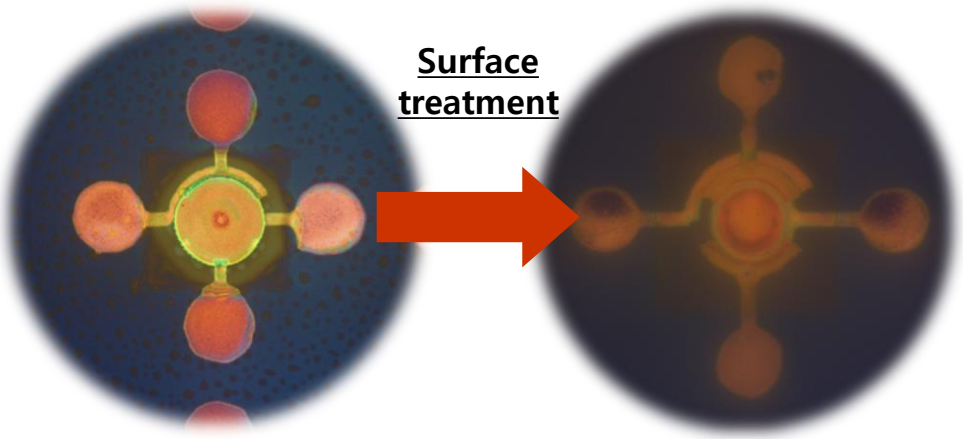

Figure 4.18 Improved wetting properties of ZnO layer on the bottom backplane structure by PLL-based surface treatment.

Figure 4.19 demonstrates the driving operation of the vertically stacked pixel circuit for active matrix PLED based on the all solution process. Based on the pixel circuit diagram composed of the p-type TFTs shown in Figure 4.16 (a), the $-V_{DD}$ electrode maintains −2 V, and when the scan electrode is +5 V and −5 V, the switching TFT turns off and on, respectively. Meanwhile, when +2 V and −2 V are applied to the data electrode, the currents flowing through the driving TFT are 10^{-9} A and 10^{-7} A levels, so this data line signals are defined as a black signal and a light signal, respectively. When the scan line is always maintained at +5 V and a square wave alternating voltage with an amplitude of 2 V and a frequency of 1 Hz is applied to the data electrode, the current flowing through the driving TFT exhibits low driving current under 10^{-9} A and tends to slightly increase from 10^{-10} A, as shown in Figure 4.19 (a), which is attributed to RC leakage current under the off-state of

the switching TFT.

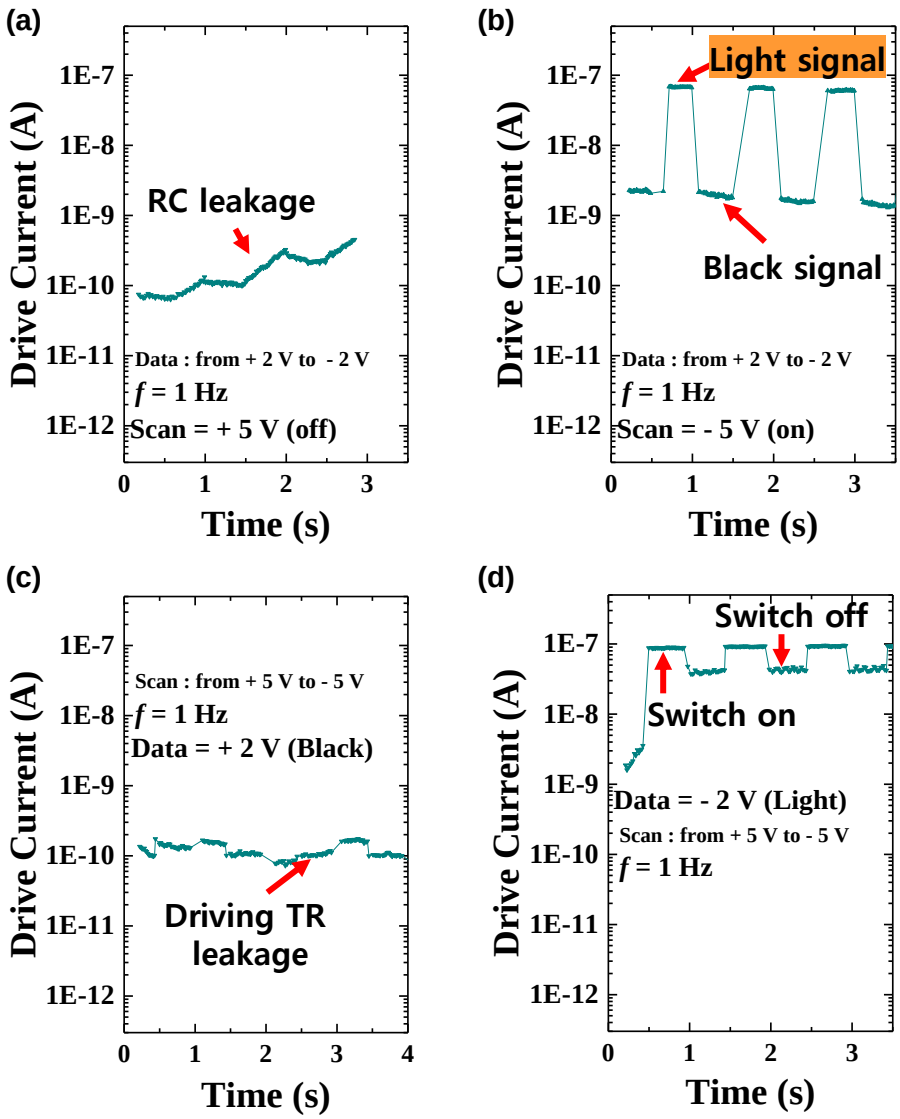

Figure 4.19 Operation of pixel circuit for active matrix PLED. Driving current according to data signal when switching TFT is always (a) off or (b) on. Driving current according to the state of the switching TFT in a fixed data signal ((c) black or (d) light) state.

Meanwhile, when only the scan voltage is changed from +5 V to −5 V when the same AC voltage is applied to the data electrode, the switching TFT remains on−state and the driving current changes according to the black and light signals of the data electrode, as shown in Figure 4.19 (b).

Figure 4.19 (c) and (d) show the current of the driving TFT when the off−state and on−state of the switching TFT are periodically changed under the state with the data electrode fixed to the black or light signal, respectively. When the data electrode keeps +2 V, only the leakage current of the driving TFT flows through the diode regardless of the state of the switching TFT. On the other hand, when a light signal is input to the pixel by keeping −2 V on the data electrode, initially, since the switching TFT is off, it shows a low driving current of 10^{-9}A, but after the switching TFT is turned on, a high current of 10^{-7}A flows through the driving TFT. After that, when the switching TFT is turned from on to off again, it can be seen that the driving current does not completely return to 10^{-9}A but maintains the reduced driving current by only about 40%. This is because the driving TFT continues to flow a high current even when the switching TFT is turned off due to the electric charge stored in the storage capacitor. As a result of analyzing the pixel operation so far, it can be concluded that the E−jet printed active matrix PLED pixel circuit with vertically stacked structure is operating as intended.

4.4 Conclusion

In summary, we have further improved the integration of transistors by introducing the vertically stacked structure in addition to the all E-jet printing system implemented in chapter 3. In addition, by introducing a technology to form in-situ via-hole patterns in a continuous solution process environment without a photolithography or laser drilling process, it is possible to realize devices with more complex structures utilizing E-jet printing system. Vertically stacked SWCNT-TFT-based inverter, active pixel sensor structure with 4 active elements, and active matrix PLED pixel circuit with 2 transistors and 1 capacitor were successfully implemented through the E-jet printing system. The dimensions of the fabricated devices do not exceed 100 ㎛, which shows a greatly high level of integration among the printing-based devices reported so far. If additional studies to improve the uniformity and reliability of SWCNT-TFT based on E-jet printing are performed, we expect to be able to implement SWCNT-based high-performance, highly integrated logic devices, various sensing arrays and image panels using only low-temperature solution processing onto flexible or stretchable substrates.

Chapter 5

Conclusion

Semiconducting single-walled carbon nanotubes (SWCNTs) have been spotlighted as a novel material for next-generation electronic devices on flexible and stretchable substrates because they can be easily utilized as solution processes applicable to low process temperatures, non-vacuum processes, and large areas with excellent electrical and mechanical properties. However, in general, SWCNT-based transistors fabricated by solution process show positively shifted turn-on voltage and threshold voltage, which is one of the factors that interfere with SWCNT-based circuit design. We suggested convenient approach for controllability of electrical characteristics of solution-processed SWCNT-TFTs by chemical encapsulation, which assists SWCNT-based more elaborate circuit design by adjusting turn-on and threshold voltage of SWCNT-based transistor in normal temperature and ambient environment.

Optimized electrohydrodynamic-jet (E-jet) printing system capable of patterning several micrometers was built for high performance, high resolution, and high integration of solution process-based electronic devices. As a results, high-performance

SWCNT-based transistors with a channel length of 5 ㎛ or less were implemented through all E-jet printing systems. Expanded from the single E-jet printed SWCNT-based transistor, we succeeded in implementing inverter logic circuit, active pixel sensor for image detector, and pixel circuit for active matrix light-emitting diode by E-jet printing within a size of less than 100 ㎛ under process temperatures up to 160 ℃, which is attributed to the in-situ via-hole printing technology and grafting of the vertically stacked structure. In addition to all E-jet printing systems presented in this dissertation, if further research is conducted to secure reliability in device manufacturing, it would be possible to fabricate a 250 pixel per inch active matrix backplane utilizing only the solution process on flexible substrates.

Appendix

A.1 Post-treatment with DI-water on SWCNT-TFT

Unlike post-treatments by NH_4OH or HNO_3, when SWCNT-TFT samples are immersed in deionized water (DI-water), electrical properties such as field effect mobility and threshold voltage do not change significantly with time compared to the initial state. (See Figure A.1 and Table A.1) Therefore, it is possible to exclude the case where device performance changes in the rinsing process using DI-water, which is an important factor when depositing SWCNT with the multi-dipping technique [83].

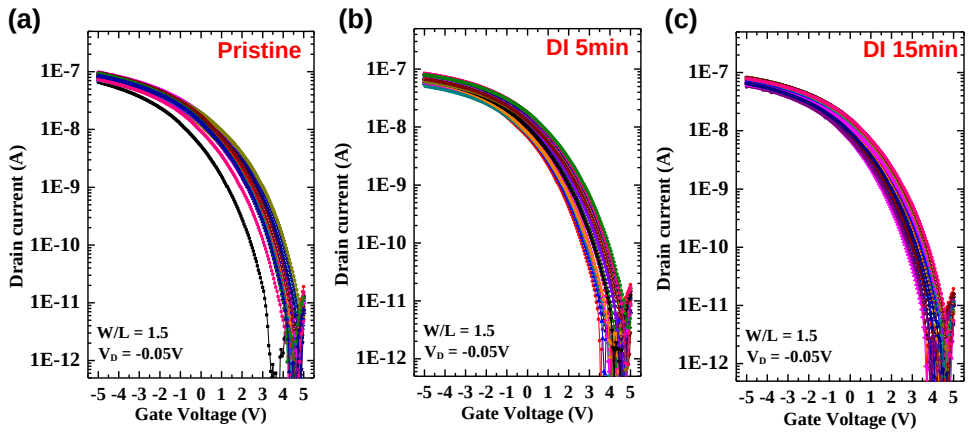

Figure A.1 Effects of post-treatment with DI-water on SWCNT-TFTs. (a) Pristine samples. Immersed into DI-water for (b) 5 minutes and (c) 15 minutes.

Table A.1 Electrical characteristics for SWCNT-TFT samples corresponding to Figure A.1.

	Pristine	**DI 5 min**	**DI 15 min**
Mobility [$cm^2/V \cdot s$]	11.3 ± 1.08	9.84 ± 1.00	10.3 ± 0.78
Threshold Voltage [V]	0.76 ± 0.37	0.77 ± 0.28	0.60 ± 0.28

A.2 Variation of characteristics of SWCNT-TFTs by post-treatment time with NH_4OH

The transfer characteristics and electrical characteristics of SWCNT-TFT according to the treatment time of the post-treatment by NH_4OH are shown in Figure A.2 and Table A.2. As a result, longer processing time does not shift the threshold voltage further in the negative direction, meaning that the bending effect of the SWCNT's energy band by ammonia is limited.

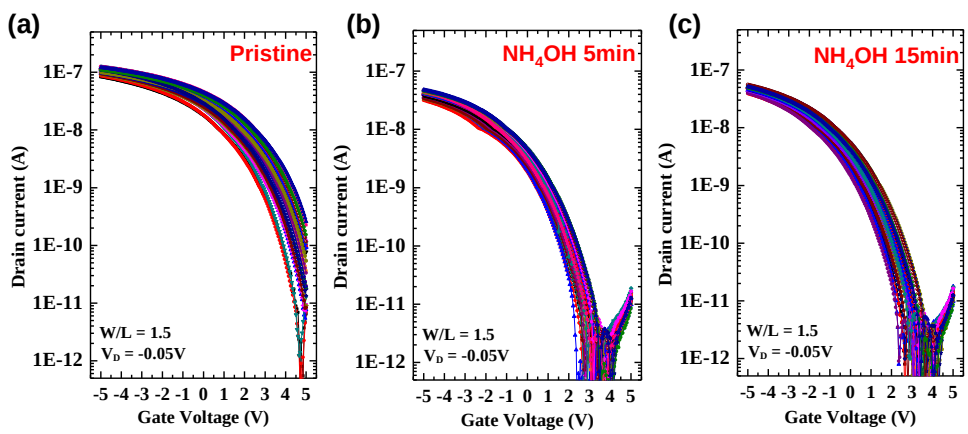

Figure A.2 Changes in transfer characteristics of SWCNT-TFTs with NH_4OH post-treatment time. (a) Pristine samples. NH_4OH treatment for (b) 5 minutes and (c) 15 minutes.

Table A.2 Electrical characteristics for SWCNT-TFT samples corresponding to Figure A.2.

	Pristine	NH_4OH 5 min	NH_4OH 15 min
Mobility [$cm^2/V \cdot s$]	12.3 ± 0.79	7.38 ± 0.83	8.47 ± 0.52
Threshold Voltage [V]	2.00 ± 0.48	-0.48 ± 0.37	-0.50 ± 0.28

A.3 Surface energy variation by a ratio between cross-liking agent and PVP

By dropping two solvents of different polarity on the surface, measuring the contact angle of droplets, and substituting the value into the Owens-Wendt model, the surface energy of a specific surface can be extracted [106]. Surface energy can be treated as the sum of nonpolar dispersion term and polar term, and Table A.3 shows the surface energy of the PVP thin film according to the ratio of PVP and crosslinking agent (CLA). It can be seen that the polar term of the surface energy decreases as the content of CLA increases, and thus the overall surface energy tends to decrease. This result is due to the gradually decreasing amount of free hydroxyl groups on the PVP surface as CLA increases. As a result, the ratio of CLA can be increased to expect a PVP thin film with a more hydrophobic surface.

Table A.3 Surface energy analysis of PVP:CLA films with Owens–Wendt model

Samples	Contact angle (deg)		Dispersion term (mJ/m^2)	Polar term (mJ/m^2)	Surface energy (mJ/m^2)
	Water	Diiodo methane			
PVP:CLA (5 : 1)	**67.8**	**31.6**	**37.10**	**9.26**	**46.36**
PVP:CLA (5 : 3)	**71.7**	**29.6**	**39.08**	**6.80**	**45.88**
PVP:CLA (5 : 5)	**71.2**	**30.7**	**38.41**	**7.21**	**45.62**
PVP:CLA (5 : 7)	**72.3**	**33.1**	**37.55**	**6.96**	**44.50**

A.4 Analysis for surface roughness parameters

The root mean square (RMS) roughness, a representative parameter of surface roughness analysis, refers to the second momentum of the height distribution of the thin film surface. The third momentum of the height distribution of the thin film surface is defined as skewness, which is a measure of the asymmetry of the roughness distribution. As shown in Figure A.3 (a), when the skewness value is positive, the surface roughness is generally concave, and when the skewness is negative, it is the opposite. Kurtosis is a measure of the tailedness of the roughness distribution as the fourth momentum value of the

height distribution. When the Kurtosis is large, the roughness distribution becomes sharp and there are very rough spikes on the surface. In the opposite case, the roughness distribution is widened, and the surface has a large bend apart from the small roughness. (see Figure A.3 (b))

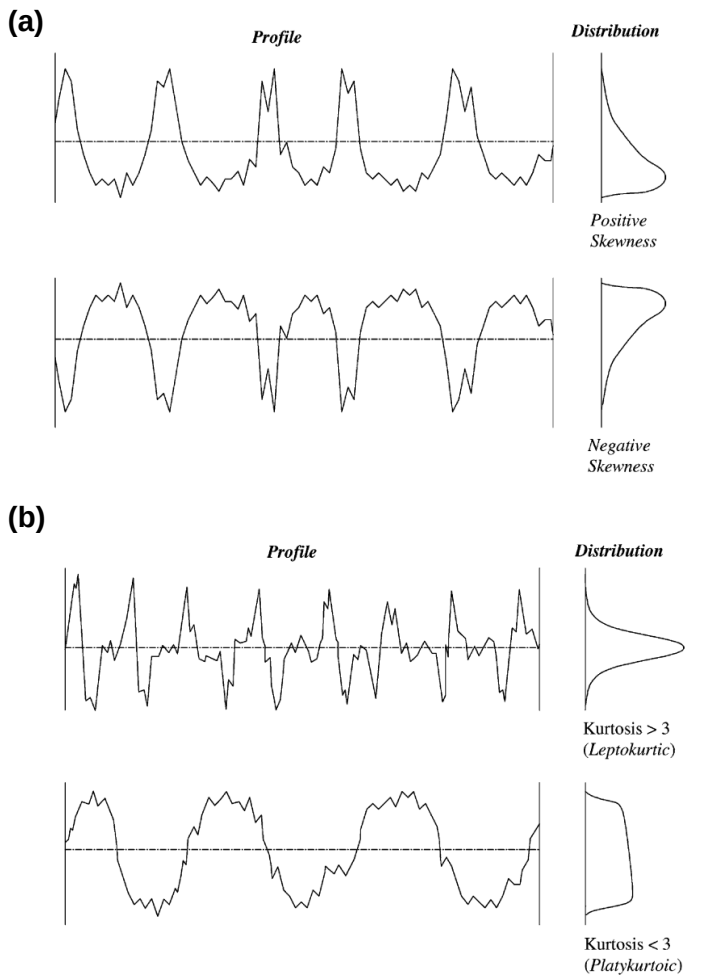

Figure A.3 (a) Distribution of roughness according to the sign of skewness. (b) Distribution of roughness according to the value of Kurtosis [88].

In Section 3.3.3, analysis for surface roughness parameters on the PVP surfaces according to the E-jet printing speed and line pitch was conducted. The corresponding optical images and line profiles are shown in Figure A.4 below, and the extracted roughness parameter analysis is shown in Figure 3.8.

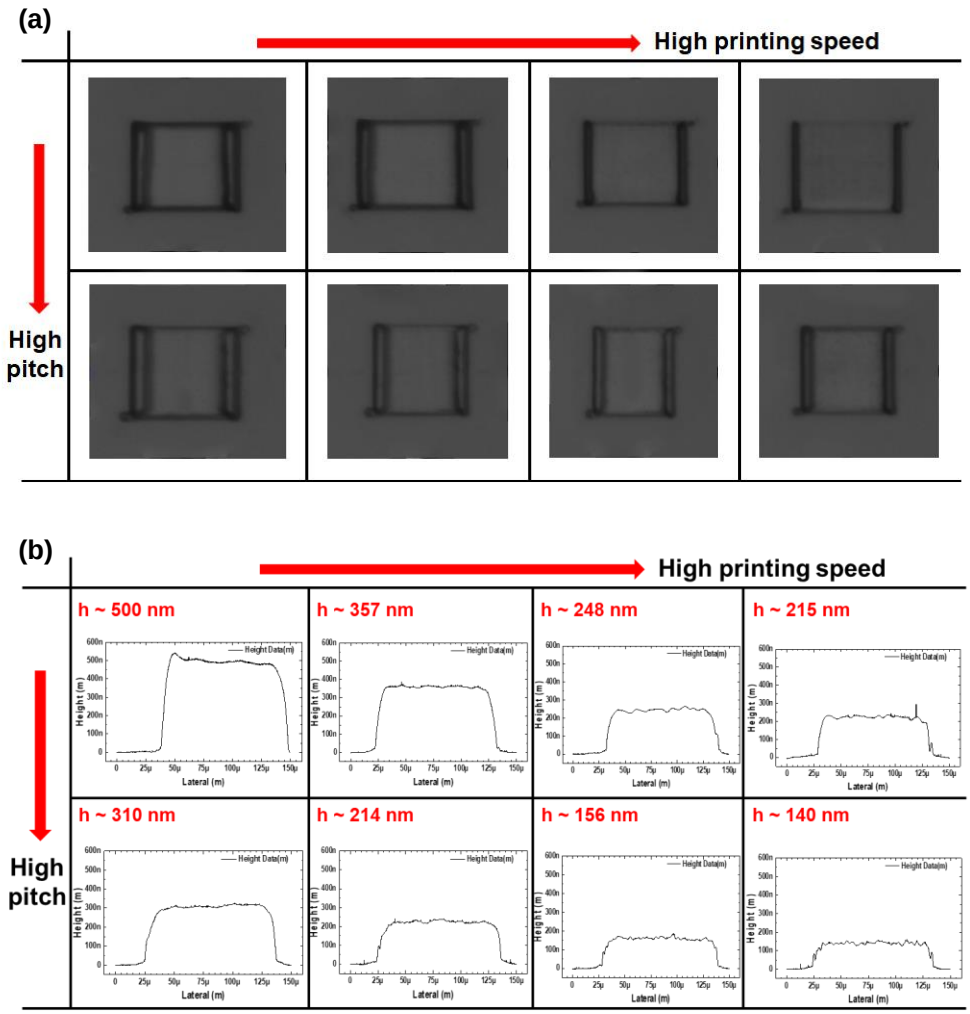

Figure A.4 (a) Optical images and (b) line profiles of E-jet printed PVP surfaces according to printing speed and line pitch.

A.5 Electrical characteristics of E-jet printed SWCNT-TFTs according to channel structure

Figures A.5, A.6 and Table A.4 exhibit the optical image, transfer characteristics, output characteristics, and electrical properties of the E-jet printed SWCNT-TFT with rectangular type S/D and Corbino type S/D, respectively. In the case of rectangular type S/D, bundling of SWCNTs tends to be accelerated at the end of the line, thereby significantly increasing leakage current and deteriorating sub-threshold slope characteristics.

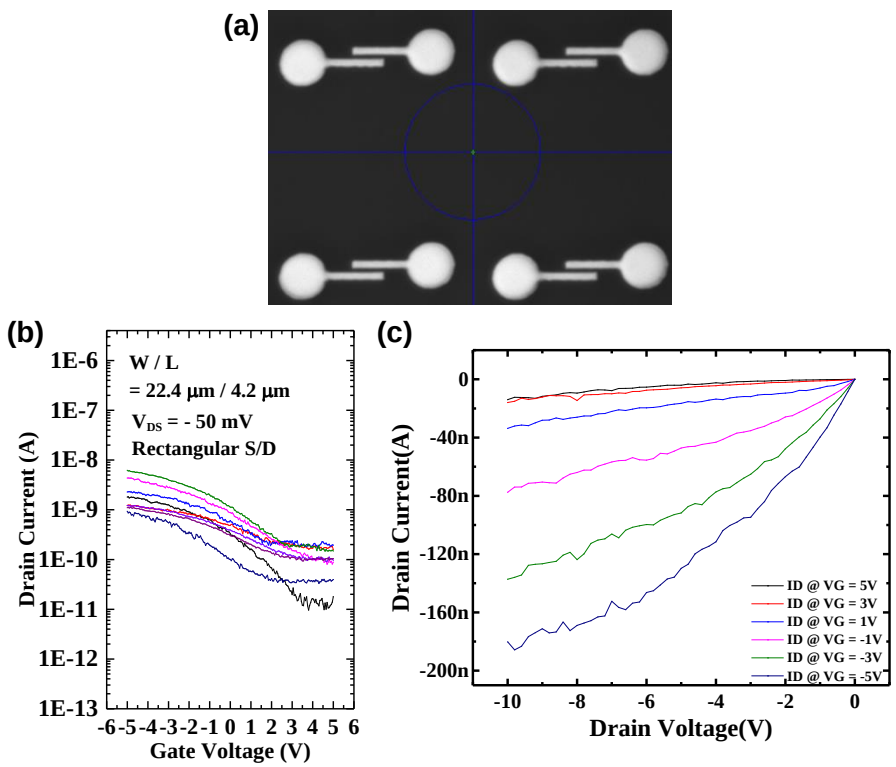

Figure A.5 (a) Optical image, (b) transfer characteristics and (c) output characteristics of E-jet printed SWCNT-TFTs with rectangular type S/D.

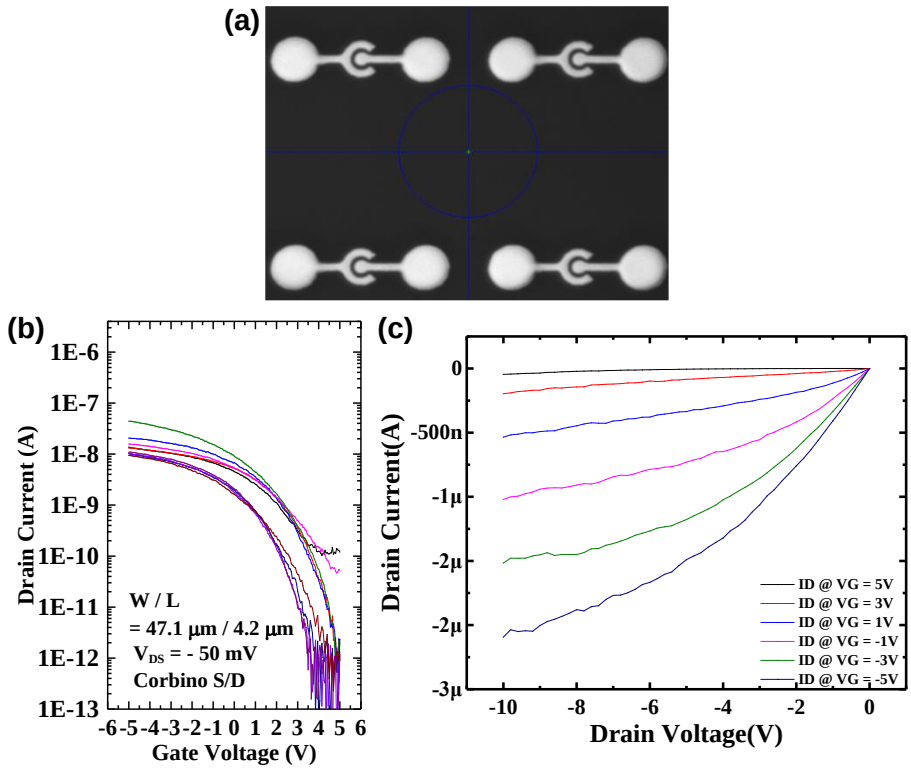

Figure A.6 (a) Optical image, (b) transfer characteristics and (c) output characteristics of E-jet printed SWCNT-TFTs with Corbino type S/D.

Table A.4 Electrical properties for E-jet printed SWCNT-TFTs with the rectangular S/D and the Corbino type S/D electrodes.

	Mobility [cm^2/V·s]	**Threshold Voltage [V]**	**Log (on/off current ratio)**
Rectangular S/D	0.15 ± 0.11	1.77 ± 0.99	0.89 ± 0.44
Corbino S/D	0.69 ± 0.47	4.32 ± 0.54	4.61 ± 0.67

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국문초록

유연 기판 및 신축성 기판상의 전자 소자에 대한 수요 및 연구가 종래의 단단한 실리콘 기반의 전자 기술만큼이나 많은 관심을 받고 있어, 이를 위한 저온 공정 및 대면적 공정이 가능한 새로운 반도체 물질 연구에 대한 관심이 증가하고 있다. 단일벽 탄소나노튜브는 뛰어난 전기적 및 기계적 특성 뿐만 아니라 비 진공, 저온, 그리고 대면적 공정이 가능한 담금 공정, 잉크젯 프린팅, 그리고 그라비아 인쇄법과 같은 용액공정에 대응하기에 이러한 요구를 충분히 충족시킨다. 마찬가지로 용액 공정 기반 소자의 고성능 및 저전력화를 위한 용액 공정기반의 초 미세 패터닝 기술에 대한 필요성도 증가하고 있다.

본 학위 논문에서는 단일벽 탄소나노튜브 기반의 전 정전기수력학 인쇄 시스템을 구축하여 5마이크론의 채널 길이를 갖는 단일벽 탄소나노튜브 기반 박막트랜지스터를 구현하였다. 또한 용액 공정기반의 단일벽 탄소나노튜브 기반 박막트랜지스터의 문턱 전압을 조절하는 기술을 개발하고 이를 접목시켜 논리소자와 영상센서 및 디스플레이를 위한 픽셀 회로를 포함한 단일벽 탄소나노튜브 기반의 고해상도, 고집적화된 응용소자를 개발하였다. 정전기수력학 인쇄 시스템을 통한 마이크론 수준의 미세 패터닝 기술 뿐만 아니라 집적도를 더욱 향상시키기 위한 용액 공정기반의 새로운 수직 적층형 기술을 도입하여 고해상도 및 고집적화된 단일벽 탄소나노튜브 기반의 전자 소자를 어떠한 진공 공정이나 고온공정 없이 연속된 환경에서 구현하였다. 본

학위논문에서 제시한 단일벽 탄소나노튜브 기반 소자의 고성능, 고해상도, 고집적화를 위한 기술은 250 ppi급의 능동형 매트릭스 백플레인의 제작을 순수 용액공정만으로 실현 가능하게 한다.

주요어 : 단일벽 탄소나노튜브, 박막 트랜지스터, 정전기수력학 인쇄, 능동형 픽셀

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