이학박사 학위논문

Electrical Characteristics of TMDC Field-Effect Transistor with defects and charged impurities

전이금속칼코겐 전계효과 트랜지스터의

불순물에 의한 전기적 특성 변화에 대한 연구

2021 년 2 월

서울대학교 대학원

물리·천문학부

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Abstract

Electrical Characteristics of TMDC Field Effect Transistor with defects and charged impurities

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Two-dimensional (2D) materials, such as graphene and transition metal dichalcogenides (TMDCs), have been attracted remarkable attention due to their novel electronic features coming from their thin nature. While graphene is hard to utilize as a semiconductor due to its zero electrical bandgap nature, TMDCs have been considered as a promising candidate for the next-generation electronic device due to their thickness dependent tunable bandgap. In particular, semiconducting TMDCs have shown desirable field effect transistor (FET) properties, such as the high on-off ratio, high mobility and low subthreshold voltage swing voltage. In this regard, numerous studies have been reported for the application of TMDCs in various field, such as electronics, optoelectronics and thermoelectrics. However, due to a large number of intrinsic defects of TMDCs ($\sim 10^{12}\,\text{cm}^{-2}$) comparing to graphene ($\sim 10^{10}\ \text{cm}^{-2}$), the performance of TMDCs devices has been far behind to the theoretically predicted device performance. Furthermore, due to the 2D nature of TMDCs, interface absorbents also can act as impurities. Therefore, understanding the effect of defects to the charge transport of TMDCs is essential to fully realize the potential of TMDCs devices.

In this manner, first, I investigated the noise generation and electric conduction at grain boundaries in CVD-grown MoS_2 field effect transistor. For application of MoS_2 as

various devices, understanding the effect of grain boundaries which are unavoidable structure defect is essential. Through electrical characteristics and noise measurements, I confirmed that the grain boundary hinders the charge transport of CVD-grown MoS_2, which can be considered as a dominant noise source. The noise characteristics showed that the noise generation mechanism of CVD-grown MoS_2 at grain boundary is different from the single grain regions of MoS_2. Also, I observed that the noise generated at the grain boundary concealed the percolative noise characteristics of the single grain regions of MoS_2.

Secondly, I investigated the molecular dopant dependent charged impurity scattering in WSe_2 field effect transistor. In general, dopants counterions which are generated by charge transfer process can decrease the mobility of the materials. After doping, the mobility of WSe_2 was decreased at low temperature, which means that dopant counterions can act as Coulomb scattering center. Using theoretical model and density functional theory calculation, I investigate the dopant dependent Coulomb scattering of dopant counterions and the microscopic origin of charge transfer process between molecular dopants and WSe_2.

Additionally, I conducted research on the trap mediated charge transport of pentacene/MoS_2 heterojunction p-n device. I confirmed that charge transport of the pentacene/MoS_2 heterojunction devices is explained by space-charge-limited conduction. Also, as the temperature goes higher, the variable range hopping transport of the pentacene/MoS_2 heterojunction device was transformed to thermally activated transport.

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This work is dedicated to my loving Eunkee and our family.

Chapter 1. Introduction

1.1. Brief introduction of TMDCs

Recently, atomically thin two-dimensional (2D) materials have been attracted much attention for electronic, optoelectronic applications and their unique physical properties, such as topologically protected states, valley effect, moiré structure and exciton dynamics [1-8]. Among them, transition metal dichalcogenides (TMDCs), such as molybdenum disulfides (MoS_2) and tungsten diselenides (WSe_2), have been widely studied due to their thickness-dependent bandgap and semiconducting nature [9,10]. From these unique properties, TMDCs have been extensively studied for exploring new physics and applications as various devices [11,12]. Especially, TMDCs are an excellent platform for investigating the excitonic physics due to their large binding energy of exciton. In addition, due to their excellent field-effect transistor (FET) properties and environmental sensitivity, TMDCs have been used as various devices such as memories, complementary logic circuits, sensors, and photodetectors.

1.2. Origin of the disorder in TMDCs

However, the performance and physical properties of devices based on 2D materials are far from the theoretically predicted values and results due to the material disorder [13]. The disorder of 2D materials can be originated from not only the intrinsic defects, such as crystalline imperfections of materials but also the extrinsic defects arising from the environment because 2D materials have a high surface-to-volume ratio and hence highly sensitive to the environment, such as substrate and surface absorbents, as shown in Figure 1.1. Especially, the intrinsic defect density of TMDCs (~10^{12} cm^{-2}) much higher

compared to that of the graphene ($\sim 10^{10}$ cm^{-2}), which is reasonable considering that the formation energy for defects in TMDCs (e.g. 2.1 eV for sulfur vacancy in MoS_2) is much smaller than for defects in graphene (e.g. 7~8 eV for a graphene vacancy) [14]. In this manner, understanding the role of both intrinsic and extrinsic defects on the charge transport of TMDC materials is essential for fully realize the potential of TMDC materials.
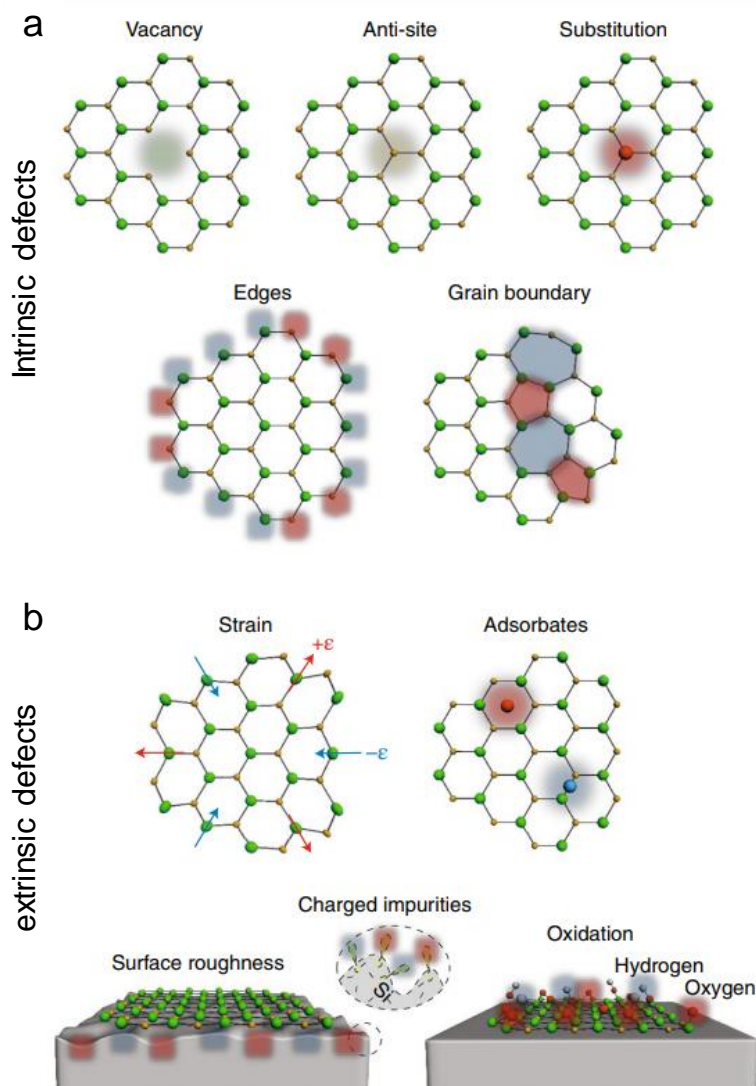
Figure 1.1. Schematics of origin of disorder in 2D materials. Reproduced from ref [14].

1.3. The effect of defects in electrical characteristics of TMDCs

As previously mentioned, the electrical transport of TMDCs is still significantly limited by material disorder arising from intrinsic and extrinsic defects. For example, even though the theoretically predicted mobility of monolayer MoS_2 and WSe_2 at room temperature is ~410 cm^2 V^{-1} s^{-1} and ~1100 cm^2 V^{-1} s^{-1}, the experimental record is far from this value (MoS_2: ~150 cm^2 V^{-1} s^{-1}, WS_2: ~80 cm^2 V^{-1} s^{-1}) [13]. To reduce the disorder of TMDCs, encapsulation within hexagonal boron nitride (h-BN) has been utilized. Using encapsulation with h-BN approach can reduce the extrinsic defects of TMDCs and h-BN encapsulated MoS_2 exhibits the quantum transport properties, which prove the excellent sample quality (See Figure 1.2) [15,16]. For example, h-BN encapsulated MoS_2 and WSe_2 were shown Shubnikov-de Hass oscillations. The measured data shows even-odd behavior, which is clear evidence of Zeeman splitting. However, a fully formed quantum hall state (with zero longitudinal resistance and clear plateaus in Hall resistance) has not been observed. Thus, the reduction in impurity density with h-BN encapsulation is still far from that in graphene, indicating that reducing an intrinsic defect is essential for utilizing TMDCs in exploring quantum physics.
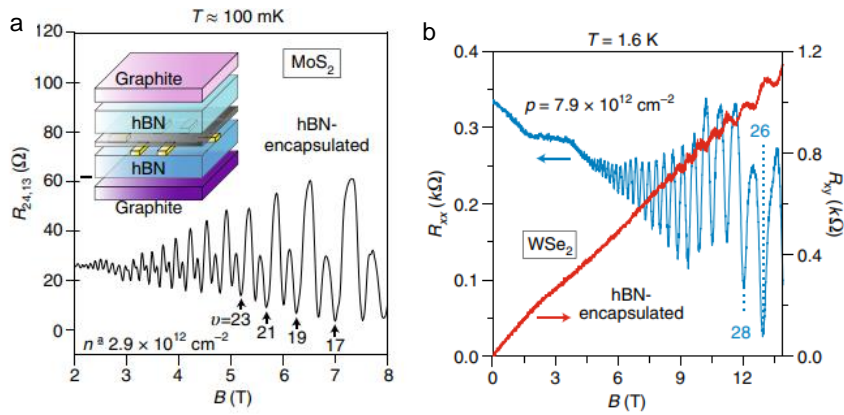
Figure 1.2 Shubnikov-de Hass oscillations of h-BN encapsulated (a) MoS_2 and (b) WSe_2. Reproduced from ref [15], [16].

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1.4. Outline of This Thesis

In this point of view, I have been focused on the investigation of the role of the defects in charge transport of TMDCs during my doctorate course. In chapter 2, I discuss the electrical noise generation and conduction at the grain boundaries of chemical vapor deposition (CVD) grown MoS_2. Using *1/f* noise and electrical measurements of MoS_2 FET, I demonstrate the role of grain boundaries in charge transport of the CVD-grown MoS_2. In chapter 3, I discuss the dopant dependent charged impurity scattering in surface-charge-transfer doped WSe_2. Through the theoretical model and the density functional theory analysis, I demonstrate the relation between the amount of charge transfer at the interface of WSe_2/dopant and the intrinsic mobility of WSe_2. In chapter 4, I discuss the trap-mediated transport in pentacene/MoS_2 p-n junction device. Although the pentacene/MoS_2 p-n junction device is a very different system compared to TMDCs, it is similar to TMDCs in that disorder originating from the defects can affect the transport of the device. Using the temperature varying measurements, I confirmed that the space-charge-limited conduction and variable range hopping transport is the dominant transport mechanism in the pentacene/MoS_2 p-n junction devices. Finally, chapter 5 summarizes this thesis and suggests some future directions.

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Monolayer and Bilayer WSe$_2$: Landau Level Degeneracy, Effective Mass, and Negative Compressibility. *Phys. Rev. Lett.* **2016,** 116, (8), 086601.

Chapter 2. Analysis of noise generation and electric conduction at grain boundaries in CVD-grown MoS₂ field effect transistors

In this chapter, we will discuss abo ut the electrical noise generation and conduction at grain boundaries in CVD-grown MoS₂ field effect transistors. Grain boundaries in a chemical vapor deposition (CVD)-grown monolayer of MoS₂ induce significant effects on the electrical and low frequency noise characteristics of the MoS₂. Here, we investigated the electrical properties and noise characteristics of MoS₂ field effect transistors (FETs) made with CVD-grown monolayer MoS₂. The electrical and noise characteristics of MoS2 FETs were analysed and compared for the MoS₂ channel layers with and without grain boundaries. The grain boundary in the CVD-grown MoS₂ FETs can be the dominant noise source, and dependence of the extracted Hooge parameters on the gate voltage indicated the domination of the correlated number-mobility fluctuation at the grain boundaries. The percolative noise characteristics of the single grain regions of MoS₂ were concealed by the noise generated at the grain boundary. This study can enhance understanding of the electrical transport hindrance and significant noise generation by trapped charges at grain boundaries of the CVD-grown MoS₂ devices.

2.1. Introduction

Molybdenum disulfide (MoS₂), a two-dimensional (2D) transition metal dichalcogenide (TMDC), has attracted remarkable attention as a promising semiconductor of next-generation nanoelectronics due to its unique electrical and mechanical properties [1-6]. MoS₂ and other TMDCs are typically prepared by a mechanical exfoliation method in a similar manner to which an atomic film of graphene was first prepared [7-10]. However, to utilize MoS₂ in large-area integrated applications, it is desirable to grow uniform large-area MoS₂ using techniques such as the chemical vapor deposition (CVD) synthesis method

[11-17]. When MoS_2 films are grown using CVD, it is well-known that the electrical performance of CVD-grown MoS_2 is limited by structural defects which are created during the synthesis process [18-22]. Grain boundaries in CVD-grown MoS_2 can be trap sites which must be avoided for low-signal sensors or AC operating applications, as the dimension of MoS_2 devices is scaled down to the sub-µm regime [22]. The effects of grain boundaries on the electrical performance and noise characteristics in CVD-grown MoS_2 require a thorough understanding to increase their potential for future applications. In this regard, the electrical analysis with low frequency *1/f* noise characterization can be an effective approach by providing insights into the determination of the dominant noise source between carrier mobility fluctuation and carrier number fluctuation, as well as the information of conductive paths in the channel layer [22-27]. Recently, Hsieh *et al.* reported that carrier localization length can be significantly reduced at grain boundaries of CVD-grown MoS_2 films from the temperature dependence of the electric transport properties [22]. The strongly localized electronic channel within the grain boundary was reconfirmed by the enhanced low-frequency noise by one to three orders of magnitude [22]. However, the exact noise generation mechanism from the grain boundaries needs to still be addressed.

In this work, we investigated the effect of grain boundaries in CVD-grown monolayer MoS_2 on the electrical characteristics using electrical noise measurements. The electrical and noise characteristics of MoS_2 FETs with and without grain boundaries were analysed and compared. In particular, the relation between the Hooge parameters and gate bias indicated the domination of correlated number-mobility fluctuation at the grain boundaries. A low exponent value in the power-law relation between relative noise and resistance indicated that the noise in MoS_2 with grain boundaries is primarily generated from grain boundary regions. These results support that grain boundaries are the dominant noise

source by acting as trap sites, which affect the current fluctuation in CVD-grown MoS_2 FETs.

2.2. Experiments

2.2.1. Growth of monolayer MoS_2 and device fabrication

The uniform monolayer MoS_2 was grown on a SiO_2/Si substrate using a CVD system (Teraleader Co., Korea). The substrate had a 270 nm-thick SiO_2 layer on heavily doped p++ Si. Boats with MoO_3 and sulfur powder were placed in the middle and upper position of the tube in the CVD system, respectively. The detailed CVD growth process of monolayer MoS_2 has previously been reported [12]. Figure 2.1(a) explains the fabrication process of MoS_2 FETs. To prevent the potential leakage of current through the SiO_2 layer, which might have been damaged during the CVD process, the CVD-grown MoS_2 films were transferred to the other SiO_2/Si substrate using the poly(methyl methacrylate) (PMMA)-assisted transfer method [16]. A thermal tape was attached as a supporting layer, and entire parts (thermal tape, PMMA, MoS_2, SiO_2, and Si) were submerged in a potassium hydroxide solution (~25%) to separate the MoS_2 films from the SiO_2/Si substrate. After the separated MoS_2 film is attached to the other SiO_2/Si substrate, an isolated and large MoS_2 piece (~10 μm size) with grain boundaries was selected to make the MoS_2 FETs with and without grain boundaries. Next, a pattern was designed for the source and drain electrodes by an e-beam lithography system (JSM-6510, JEOL). Finally, Au (50 nm)/Ti (5 nm) layers were deposited by an e-beam evaporator (KVE-2004L, Korea Vacuum Tech.) at a pressure of ~10^{-7} Torr to form the source and drain electrodes. The electrical performance of TMDC
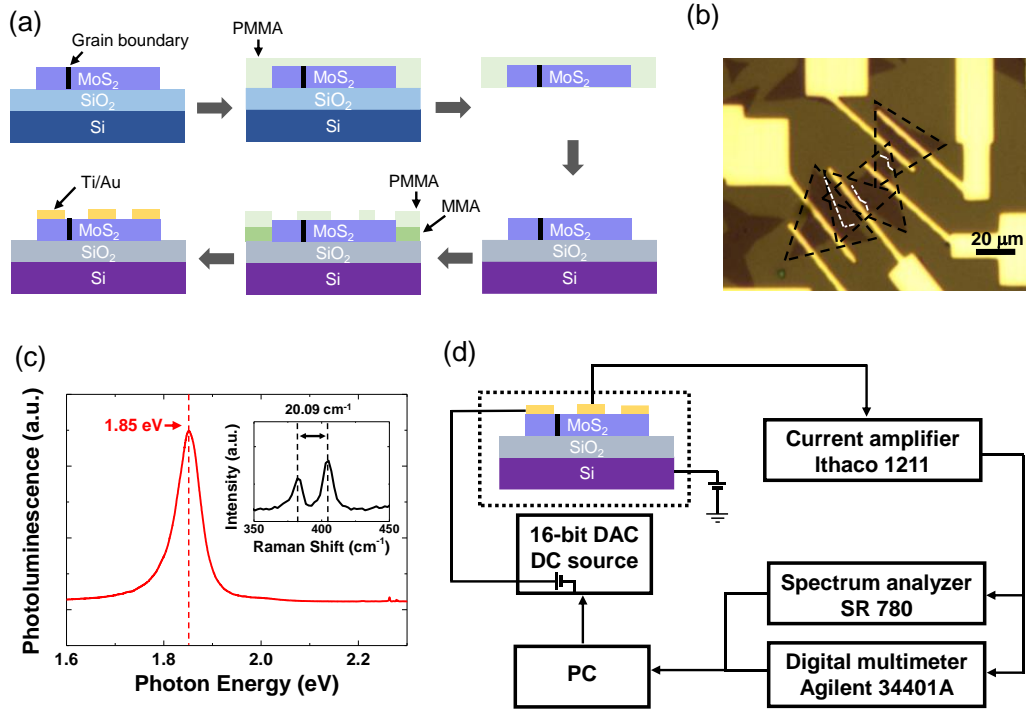
Figure 2.1 (a) Schematic illustration of the fabrication processes for CVD-grown MoS$_2$ FETs with and without grain boundary. (b) Optical image showing CVD-grown MoS$_2$ FETs with and without grain boundary made from a MoS$_2$ flake. (c) Raman and PL spectra of CVD-grown monolayer MoS$_2$. (d) Schematic of the noise measurement setup.

FETs has been limited by contact resistance. In this regard, the contact resistance of the CVD-grown MoS$_2$ FET was extracted by Y-function method. The extracted value of contact resistance was 68.0 kΩ and comparable to the reported value of previous studies .This result indicates that the contact resistance between MoS$_2$ channel and metal contacts did not deteriorate significantly the electrical characteristics of the CVD-grown MoS$_2$ in this work.

When monolayer MoS$_2$ films are grown by CVD, single grains of MoS$_2$ are formed as a triangular shape and grain boundaries exist between the merged MoS$_2$ triangles [11,17-22]. Therefore, we could fabricate both MoS$_2$ FETs with and without grain

boundaries from a large enough piece of MoS$_2$ film. Figure 1(b) shows the optical image of fabricated both MoS$_2$ FETs with and without grain boundaries from a MoS$_2$ flake. In this figure, the grain boundaries are indicated by white dashed lines in a MoS$_2$ flake that is indicated by a black dashed line, and some MoS$_2$ FET devices include a grain boundary, while others do not.

2.2.2. Raman and Photoluminescence characteristics of CVD-grown monolayer MoS$_2$

To confirm the number of layers of the CVD-grown MoS$_2$, Raman and photoluminescence (PL) spectra were measured (Figure 2.1(c)). An A1 peak (~ 1.85 eV) was observed in the PL spectra. The two peaks, which represent the in-plane E_{2g}^1 and the out-of-plane A$_{1g}$ vibration, were shown in the Raman spectra (the inset of Figure 2.1(c)). The difference between two peaks of Raman spectra was 20.09 cm^{-1}. The peak values in PL and Raman spectra are similar to the known values of monolayer of MoS$_2$ [28-30], which supports that our CVD-grown MoS$_2$ films are indeed a monolayer.

2.2.3. Current-voltage (I-V) characteristics

The electrical characteristics of the CVD-grown MoS$_2$ FET devices were measured using a semiconductor parameter analyser (Keithley 4200, USA) in the dark and under a vacuum (~10^{-3} Torr). Before measurement, the CVD-grown MoS$_2$ devices were heated at 400 K under a vacuum for about six hours to eliminate adsorbates from the MoS$_2$ surface, such as water, oxygen molecules, and polymer residue [20]. These adsorbates can work as trap states, which induce electrical noise in the MoS$_2$ FETs. To scrutinize the effect of the grain boundary on the noise characteristics of the CVD-grown MoS$_2$ FET, this

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annealing process can reduce other noise sources from the interface interaction.

2.2.4. Electrical noise characteristics

Figure 2.1(d) shows a schematic of the noise measurement setup. A 16-bit digital-analogue converter (DAC) was used to apply the voltage bias. A battery-powered current amplifier (Ithaco 1221) was used for amplifying the current fluctuation. A spectral analyser (SR760) and a digital multimetre (Agilent 34401A) were used to monitor the frequency domain noise signal (power spectral density) and obtain the average electrical current, respectively. Current fluctuations between the source and drain electrodes were measured, while a back-gate bias was applied.

2.3. Results & Discussions

2.3.1. Electrical characteristics of MoS$_2$ FETs with and without grain boundary

Since the geometries of MoS$_2$ FETs with and without grain boundaries are different from each other, the current level from the characteristic curve was normalized to the channel width (W) and length (L) to compare the electrical conductions. The normalized current, I_{norm}, was defined as $I_{norm} = I_{DS} \times L/W$, where I_{DS} is the source-drain current. The transfer characteristics, i.e., normalized current versus source-gate bias (I_{norm}–V_{GS}), of both MoS$_2$ FETs with and without grain boundaries exhibited a typical n-type semiconductor behaviour (Figures 2.2(a) and 2.2(b)). The output characteristics (I_{DS}–V_{DS})
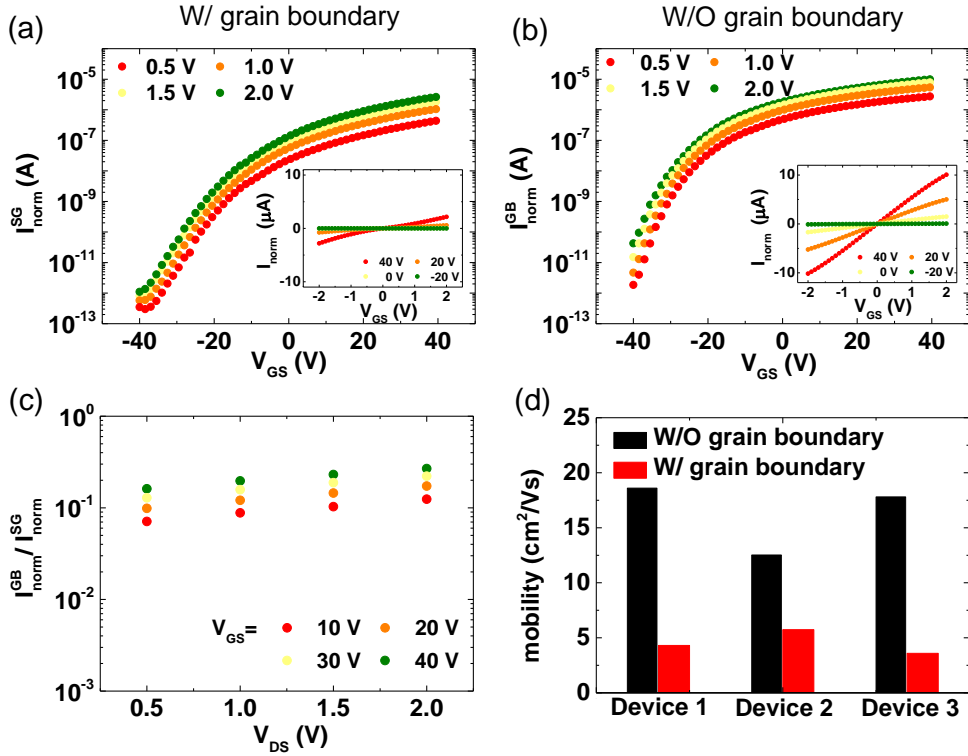
Figure 2.2 $I_{DS}-V_{GS}$ curves of CVD-grown MoS₂ FETs (a) with and (b) without grain boundary for different drain bias. The insets indicate the $I_{DS}-V_{DS}$ curves of the same device for different gate bias. (c) The ratio of I_{norm}^{GB} to I_{norm}^{SG} for different gate and drain bias. (d) A histogram showing the mobility values of three sets of CVD-grown MoS₂ FETs with and without grain boundary.

of both MoS₂ FETs are also shown in the inset of Figures 2.2(a) and 2.2(b). As shown in these figures, the current level of the MoS₂ FET without a grain boundary was higher than that of the MoS₂ FET with a grain boundary. To more explicitly compare the current level between the two MoS₂ devices with and without a grain boundary, the ratio of I_{norm}^{GB} to I_{norm}^{SG} was calculated with V_{GS} varying from 10 V to 40 V with a step of 10 V and V_{DS} varying from 0.5 V to 2.0 V with a step of 0.5 V, where SG and GB denote the sample with a single grain without a grain boundary and the sample with a grain boundary, respectively (Figure 2.2(c)). The ratio values were found to be less than 0.2, which means the current of

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MoS$_2$ FET without a grain boundary is about five times higher than that of MoS$_2$ FET with a grain boundary.

To further investigate the effect of a grain boundary on the electrical characteristics of MoS$_2$ FETs, mobility values of three sets of MoS$_2$ FETs with and without a grain boundary were extracted from the electrical characterization and compared (Figure 2.2(d)). As shown in this figure, the mobility values of the MoS$_2$ FETs with a grain boundary were two to four times lower than those of the devices without a grain boundary. This substantial reduction in the mobility of the MoS$_2$ FETs with a grain boundary implies that the charge carriers at the grain boundary undergo a significant hindrance in the electrical transport. This hindering effect of the grain boundary can be attributed to trap states formed at the grain boundary, which can be electrical noise sources. The restriction of charge transport at the grain boundary in CVD-grown MoS$_2$ has also been observed in previous studies [21,22]. Furthermore, the mobility of the CVD-grown MoS$_2$ was not significantly affected by the misorientation angle ($> 20°$) between two coalescing grains, which is consistent with previous studies [21].

2.3.2. Electrical noise characteristics of CVD-grown MoS$_2$ with and without grain boundary

Figure 2.3(c) shows the relative noise of the MoS$_2$ FETs with and without a grain boundary at $V_G = 40$ V. The grain boundaries in the CVD-grown MoS$_2$ films increase the relative noise of the MoS$_2$ FET more than ten times. For a more correct comparison of the noise levels, an area normalization of the relative noise should be considered. In most transistor devices, the reversely proportional relation between the relative noise amplitude and device area ($f \cdot S_I/I^2 \propto (WL)^{-1}$) has been observed with several models, such as the
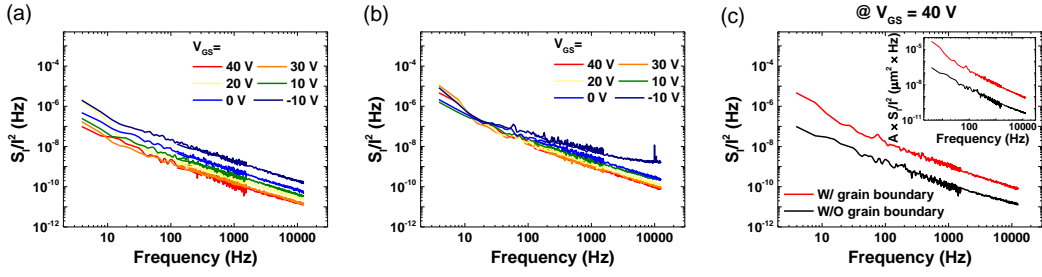
Figure 2.3 The relative noise of CVD-grown MoS_2 FETs (a) with and (b) without grain boundary for different gate bias. (c) The relative noise of CVD-grown MoS_2 with and without grain boundary at a fixed $V_{GS} = 40$ V. The inset indicates the relative noise normalized to device area.

Hooge's empirical relation, the interfacial trapping model, and the variation-range-hopping fluctuation model [31,32]. Therefore, the relative noise, normalized to the device area, was defined as $A \times S_I/I^2$, where A is the device area. $A \times S_I/I^2$ of the MoS_2 FETs with and without a grain boundary is shown in the inset of Figure 2.3(c). As shown in the inset of Figure 2.3(c), $A \times S_I/I^2$ of MoS_2 FET with a grain boundary was still more than ten times higher than that of MoS_2 FET without a grain boundary. These results indicate that grain boundaries can be regarded as a dominant noise source in the CVD-grown MoS_2 films.

2.3.3. Hooge parameter analysis and network properties of CVD-grown MoS_2 FETs

The *1/f* type noise in transistor devices has been explained by several sources of charge carrier fluctuations, such as Hooge mobility fluctuation, McWhorter carrier number fluctuation, and correlated number-mobility fluctuation [31-36]. Through analysing the gate bias dependence of current noise of the MoS_2 FETs with and without a grain boundary using these models, noise sources of MoS_2 FETs with and without a grain boundary can be discriminated. The gate bias dependence of the Hooge parameter can be a useful guideline
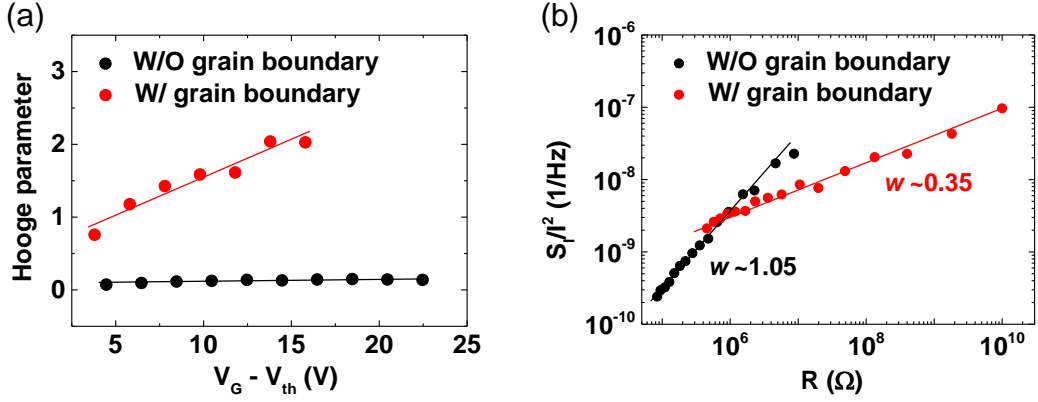
Figure 2.4 (a) The Hooge parameters of CVD-grown MoS$_2$ FETs with and without grain boundary for different $V_{GS} - V_{th}$. (b) Power-law relation between the relative noise and resistance of CVD-grown MoS$_2$ FETs with and without grain boundary.

for determining the dominant noise source. In the case of mobility fluctuation, the Hooge parameter is independent of the total charge carrier number (N) [37-39]. On the other hand, the Hooge parameter is proportional to I/N in case of McWhorter number fluctuation [36,38,40]. The Hooge parameter can be extracted using Hooge's empirical relation, which is expressed as

$$\frac{S_I}{I^2} = \frac{\alpha_H}{N} \frac{1}{f} \quad , \tag{1}$$

where S_I is the current power spectral density, I is the current, α_H is the Hooge parameter, N is the total number of free charge, and f is the frequency [37-40]. In the case of FET devices, the total number of free charge N can be calculated as $N = (V_{GS} - V_{th})AC_i/q$ with the condition of a small V_{DS}, where V_{th} is the threshold voltage, A is the area of the device, C_i is the gate dielectric capacitance of the device, and the q is the elementary charge.

Using Hooge's empirical relation and N, the Hooge parameters of the MoS$_2$ FETs were extracted as the function of $V_{GS} - V_{th}$ (Figure 2.4(a)). With the MoS$_2$ FET without a grain boundary, the Hooge parameters were nearly constant (~ 0.14) with $V_{GS} - V_{th}$, which

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can be explained by the mobility fluctuation model [38,40]. Note that the gate dependence of the relative noise, consistent with the Hooge model, has been reported in mechanically exfoliated monolayer MoS_2 [41]. The linearly increasing behaviour of the Hooge parameters, with increasing $V_{GS} - V_{th}$, can be explained by the correlated number-mobility fluctuations model, where the carrier number fluctuation at traps influences the carrier mobility fluctuation [35]. In the correlated number-mobility fluctuations model, α_H becomes linearly proportional to N under the condition of a sufficiently small drain voltage and large N, which means $\alpha_H \sim (V_{GS} - V_{th})$. The Hooge parameter behaviour, explained by the correlated number-mobility fluctuation model, implies that trapped carriers at the grain boundary can be considered as scattering centres in CVD-grown MoS_2 films, and the number of trapped carriers at the grain boundary can fluctuate. The number fluctuation of trapped carriers can cause the fluctuation of scattering rate; when this occurs at the grain boundary, it can lead to the correlated carrier number-mobility fluctuation.

The CVD grown-MoS_2 can be considered to have a disordered electronic structure, which has randomly distributed charge puddles due to the large trap density originated from structural defects, such as sulfur vacancies, dielectric impurities, and grain boundaries [16]. A disordered conductive system can be regarded as a random resistor network [42]. Hopping of charge carriers between neighbouring charge puddles can be considered, as the current flows through randomly distributed resistors. According to percolation theory, the electrical characteristics of a random resistor network are determined by a conductive phase fraction p. Additionally, a conductive channel is formed when p exceeds the percolation threshold p_c. The relation between the electrical noise and resistance of a random network resistor system obeys the following power-law relation [42-44]

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{\sum_m \tilde{s}(f)_m\ i_m^4}{(\sum_m i_m^2)^2} \propto R^w \quad \text{at} \quad p > p_c, \tag{2}$$

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where S_I is the power spectral density for current signal, S_R is the power spectral density for resistance signal, i_m denotes the current flowing in m-th resister, $\tilde{s}(f)_m$ is the spectral density of factional noise of m-th resistor, and R is the total resistance of percolating network. Higher gate bias lowers the potential barrier between charge puddles, modulating the connection of the conductive network in the MoS_2 layer [45]. Therefore, various S_I/I^2 and R values were obtained by modulating the gate bias. Our CVD-grown MoS_2 FET devices exhibited the power-law behaviour between the relative noise and resistance, which can be considered as percolative behaviour (Figure 4(b)). In the MoS_2 FET without a grain boundary, the power-law exponent w was found to be ~1.05, which is a comparable value of w reported from previous noise study on single grain MoS_2 [20]. On the other hand, the w value of the MoS_2 FET with a grain boundary was found to be ~0.35, which is much smaller than the exponent in the single grain MoS_2. This low value of w has not been expected from the available percolation theories, which could indicate that the percolation is not geometrical [46-48]. This non-geometric property can be attributed to the grain boundary, which has one-dimensional geometry. Therefore, the percolative noise characteristics from single grain MoS_2 regions were concealed by the larger noise generation from the grain boundary. In short, the large noise generation at the grain boundary by the correlated number-mobility fluctuation predominated over the noise generated from the resistor network of the single grain MoS_2.

2.3.4. Schematics of conduction network of CVD-grown MoS$_2$ FETs with and without grain boundary
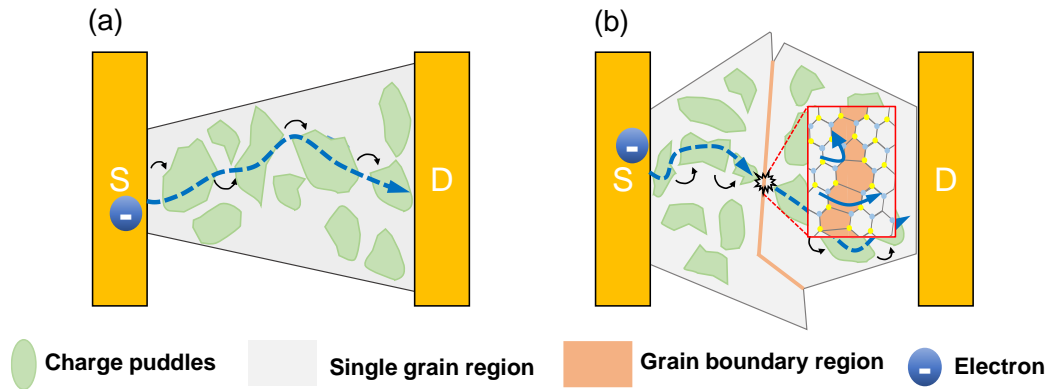
Figure 2.5 Schematic illustration of carrier conduction in CVD-grown MoS$_2$ FETs (a) without and (b) with grain boundary.

Figures 2.5(a) and 2.5(b) illustrate the schematics of conductive network in the CVD-grown MoS$_2$ FETs without and with a grain boundary, respectively. In case of the MoS$_2$ FET without a grain boundary, the charge carriers in one of the charge puddles can hop to the neighbouring charge puddle, which can be regarded as the current flowing in one of the randomly distributed resistors. On the other hand, in case of the MoS$_2$ FET with a grain boundary, the charge carriers can hop to another charge puddle, similar to the carriers in MoS$_2$ FET without a grain boundary. However, charge carriers in MoS$_2$ FET with a grain boundary can be trapped at the grain boundary as energy levels near the Fermi level can be induced by the dislocations in the grain boundary [21]. These trapped carriers can play as scattering centres, undermining the electrical characteristics of the MoS$_2$ devices. Additionally, the scattering at the grain boundary can generate a considerable amount of noise, concealing the noise characteristics of the random resistor network in single grain MoS$_2$. Trapping/de-trapping events of charge carriers can induce fluctuation of the

scattering rate at the grain boundary, which can be observed as the correlated number-mobility fluctuation.

2.4. Conclusion

The electrical and noise characteristics of CVD-grown monolayer MoS_2 FET devices with and without a grain boundary were investigated. The electrical transport in CVD-grown MoS_2 FETs were hampered by the grain boundary, which can be considered as the dominant noise source. According to the gate bias dependence of the Hooge parameters, the correlated number-mobility fluctuation at the grain boundary generates large noise in CVD-grown MoS_2 films. From the relation between the relative noise and resistance values, the noise generated at the grain boundary concealed the percolative noise characteristics of the single grain regions of MoS_2. This work provides insight into how a grain boundary hinders the electrical transport and can be a significant noise source of CVD-grown MoS_2 devices.

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Chapter 3. Molecular Dopant-dependent Charge Transport in Surface-charge-transfer-doped WSe₂ Field Effect Transistor

In this chapter, we discuss about molecular dopant dependent charge transport in surface-charge transfer doped tungsten diselenide (WSe₂) field effect transistors. The controllability of carrier density and major carrier type of transition metal chalcogenides (TMDCs) is critical for electronic and optoelectronic device applications. To utilize TMDCs in the applications, it is important to understand the role of dopants in charge transport properties of TMDCs. However, despite several reports on demonstrations of molecular surface charge-transfer doping (SCTD) in TMDCs, the doping effects on charge transports of TMDCs have not been systematically demonstrated. Here, we investigate the effects of molecular SCTD on the charge transport properties of WSe₂ using three p-type molecular dopants, 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F₄-TCNQ), Tris(4-bromophenyl)ammoniumyl hexachloroantimonate (magic blue), and molybdenum tris(1,2-bis(trifluoromethyl)ethane-1,2-dithiolene) (Mo(tfd-COCF₃)₃). By controlling the degree of doping using different dopants we find that the generated carrier densities are significantly dependent on fundamental properties of molecular dopants. Our temperature-dependent transport measurements show that the dopant counterions on WSe₂ surface can induce Coulomb scattering in WSe₂ channel and the degree of the scattering is significantly dependent on the molecular properties, which can be corroborated by first-principles density functional theory (DFT) calculations. Furthermore, DFT calculations show that an amount of charge transfer between dopants and WSe₂ is determined by the molecular properties. Our systematic investigation the charge transport of doped TMDCs will be directly relevant for pursuing molecular routes for efficient and controllable doping in nanoelectronic devices.

3.1. Introduction

Two-dimensional (2D) layered transition metal dichalcogenides (TMDCs) have attracted remarkable attention due to ultrathin semiconducting features with thickness-dependent tunable bandgap.[1-4] In particular, semiconducting TMDCs, such as molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), have shown desirable field-effect transistor (FET) properties such as the high on-off ratio, high mobility, and low subthreshold swing voltage. Moreover, a possibility for breaking the scaling limit of Si-based electronics makes them a promising candidate for the next-generation electronic devices.[5, 6]

To utilize TMDCs in an integrated circuit for various electronic and optoelectronic device applications, the ability to control conductivity and carrier type becomes essential. In this manner, several studies have been reported for controlling the electrical properties of TMDCs by doping since the free carrier concentration and the majority carrier type can be tuned by dopings.[7-14] One of the approaches is the substitutional doping, which is replacing transition metal elements (Mo, We) in TMDCs to other elements with a different number of valence electron (such as Nb, Re, or Zr). [7-9] Although substitutional doping has an advantage in terms of the stability of doping, the controllability of doping level is comparatively difficult to achieve via a direct synthesis.[7,15] Another route for controlling the electrical characteristics of TMDCs is by surface charge transfer doping (SCTD).[10-14] SCTD involves physisorption of dopants on the surface of TMDCs, which induces a charge transfer across the TMDC/dopant interface. A large surface area to volume ratio of 2D layered TMDCs makes them highly sensitive to the surface-attached dopants. In addition, comparing to substitutional doping, SCTD has an advantage that it is a relatively non-destructive process. Particularly, for SCTD by molecular reductants (oxidants) for

n(p)-type doping, the potential range of material selection for dopants is greatly diverse due to a high degree of freedom in the molecular design.[16] For these reasons, several studies have demonstrated the applicability of molecular SCTD in TMDC devices.[12-14, 17-19] For example, a typically large contact resistance of TMDC devices, which is one of the main challenges for the realization of nanoscale TMDC devices, can be reduced by doping the contact regions. The molecular SCTD was also shown to be effective in complementary logic applications for controlling the majority carrier type.[18, 19]

Considering that SCTD involves the creation of charged dopants which exert the Coulomb force to the free carrier in TMDC, it is natural to consider the scattering originated by the generated charged impurities on the surface of the doped TMDCs by SCTD. In this regard, in graphene, SCTD was shown to induce charged impurity scattering which significantly affected the charge transport, which has even been utilized for gas sensing purposes.[20] Likewise, we can expect that SCTD will induce charged impurity scattering in doped TMDCs. Ideally, molecular SCTD should preserve the high carrier mobility of TMDCs by minimizing the charged impurity scattering. Therefore, in order to fully realize the potential of molecular doping for SCTD, it is essential to understand what fundamental properties of molecular dopants and their interfacial properties with TMDCs determine the degree of charge transfer and their effects on the overall charge transport. Although there have been a few studies on estimating the degree of charged impurity scattering in intrinsic TMDC devices,[21, 22] an understanding of the effects of the additional scattering induced by the counterions created in doped TMDC devices on the charge transport is still lacking. In particular, the contributions of different molecular dopants with the different electron affinities and electronic properties to the charge transport properties of TMDS devices have yet to quantified.

In this study, we systematically studied the electrical properties and impurity scattering in doped WSe_2 by SCTD using three p-type molecular dopants with different electron affinities. Doping strength of each molecular dopant is dependent on intrinsic molecular characteristics such as their relative lowest unoccupied molecular orbital (LUMO) positions to the valence band maximum (VBM) of WSe_2 and extrinsic factors such as density of molecular dopants. Considering this, we investigated the effects of molecular dopings on the charge transport of WSe_2 FETs through the intrinsic mobilities extracted by 4 point-probe measurements. From the intrinsic mobility values, the surface charged impurity densities of doped WSe_2 can be obtained by considering the screening induced by the charged molecular dopants. Additionally, we performed first-principles density functional theory (DFT) calculations to compute the degrees of charge transfers from WSe_2 to molecular dopants. Our DFT calculations show that the electrons generally transfer from WSe_2 to three molecular dopants, and each molecular dopant has its own optimal doping density.

3.2. Experiments

3.2.1. Device fabrication and doping process

WSe_2 was mechanically exfoliated from a bulk WSe_2 crystal and transferred to SiO_2/p++ Si substrate. The suitable WSe_2 flakes were founded using an optical microscope and the thickness of the flakes was measured by an atomic force microscope system (NX 10 AFM, Park Systems). After double electron resist layers, methyl methacrylate (MMA)/poly(methyl methacrylate) (PMMA), were spin-coated, the source-drain electrodes patterns were made by using an electron-beam lithography system (JSM-6510, JEOL). Subsequently, Ti (2 nm)/Pd (40 nm)/Au (20 nm) layers were deposited by using an

electron-beam evaporator (KVE-2004L, Korea Vacuum Tech.). Here, Pd was used to enhance hole injection and p-type conduction of WSe$_2$ FET due to its high work function (~5.6 eV). And, Ti was used for the adhesive layer to SiO$_2$ and Au was used for compatibility with wire bonding. The fabricated WSe$_2$ FET devices were annealed at 200 °C for 1 hour before the electrical measurement. The electrical characteristics of the WSe$_2$ FETs were measured through a semiconductor parameter analyzer (Keithley 4200-SCS) and a cryostat system (CS204*I-FMX-12, Advanced Research Systems).

To make a doping solution, F$_4$-TCNQ and Mo(tdf-COCF$_3$)$_3$ were dissolved in butyl acetate and magic blue was dissolved in dichloromethane. About 20 µL of the molecular dopant solution was used in a drop-casting process for each dopant.

3.2.2. Dopant molecules and 4-point probe measurement

As the p-type molecular dopants for SCTD on WSe$_2$, three different molecules were used in this study; 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F$_4$-TCNQ), tris(4-bromophenyl)ammoniumyl hexachloroantimonate (magic blue), molybdenum tris(1,2-bis(trifluoromethyl)ethane-1,2-dithiolene) (Mo(tfd-COCF$_3$)$_3$). The molecular structure of each dopant is shown in Figure 3.1(a). The dopants with different LUMO levels were chosen for investigating different doping strengths according to the LUMO level which correlates with the electron affinity. Figure 3.1(b) shows the energy diagrams for the valence band maximum of WSe$_2$ and LUMO levels of the molecular dopants. Due to similar (F$_4$-TCNQ) or deeper (magic blue and Mo(tfd-COCF$_3$)$_3$) LUMO levels of the dopants relative to the valence band maximum of WSe$_2$ (5.33 eV)[23, 24], all three molecules are expected to act as p-type dopants. Also, it is expected that magic blue (LUMO level: 5.5 eV)[14] and Mo(tfd-COCF$_3$)$_3$ (5.6 eV)[25] generate a higher carrier density in WSe$_2$ FETs
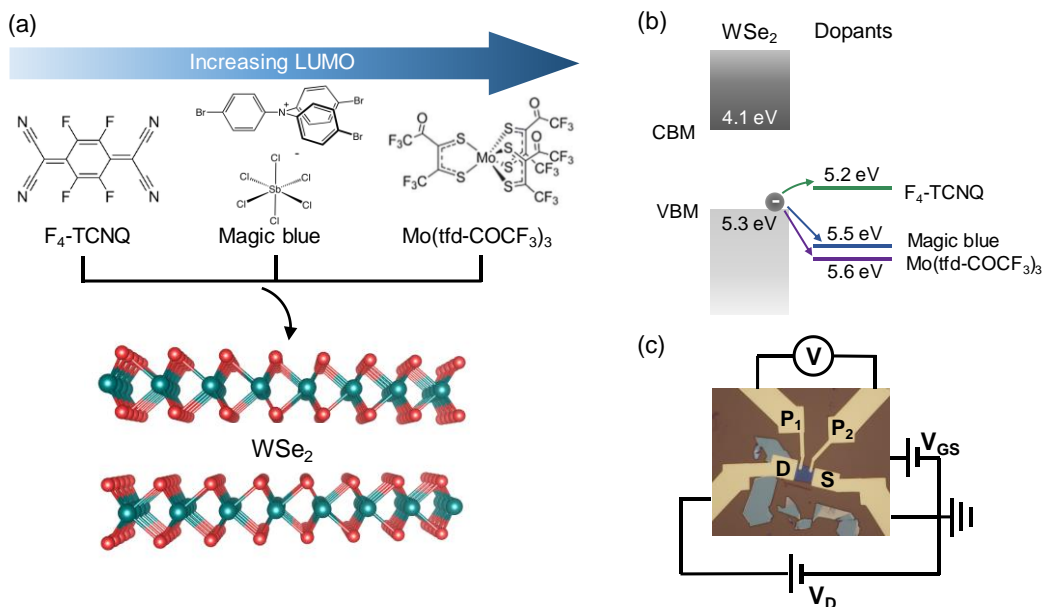
28

Figure 3.1 (a) The lattice structure of WSe$_2$ and the molecular structures of F$_4$-TCNQ, magic blue, Mo(tfd-COCF$_3$)$_3$ molecular dopants. (b) Energy diagram of WSe$_2$ and the LUMO levels of dopant molecules. CBM (VBM) is abbreviation of conduction band minimum (valence band maximum) (c) The schematic of 4-point probe measurement with optical image of WSe$_2$ FET.

than F$_4$-TCNQ (5.2 eV)[26]. Table 1 shows the computed LUMO and HOMO levels of three dopants compared to the experimental values. The computed LUMO levels of magic blue and Mo(tfd-COCF$_3$)$_3$ relatively well agree with the experimental values while DFT significantly overestimates electron affinity of F$_4$-TCNQ. As shown in Table 1, the computed LUMO level of F$_4$-TCNQ (-6.0 eV) is even deeper than the valence band minimum of WSe$_2$ (-5.1 eV), which is an opposite trend of the experiment (see Figure 3.1(b)). Due to the deep LUMO level of F$_4$-TCNQ, the transferred charges per a dopant for F$_4$-TCNQ is larger than the experiment (see Table 3.1). Even though our DFT calculations overestimate the transferred charges for F$_4$-TCNQ, we can still see the p-type dopant behavior of F$_4$-TCNQ in our DFT calculations as shown in Figure 3.6. To measure the

Table 3.1 Computed the lowest unoccupied molecular orbitals (LUMOs) (in eV), the highest occupied molecular orbitals (HOMOs) (in eV), and the transferred charge per a dopant (in e) for WSe$_2$, F4-TCNQ, magic blue, and Mo(tfd-COCF$_3$)$_3$ compared to the experiments. The reference is the vacuum level (=0 eV)

	LUMO		HOMO		Transferred charge	
	DFT	Exp.	DFT	Exp.	DFT	Exp.
WSe$_2$	-3.9		-5.1			
F$_4$-TCNQ	-6.0	-5.2	-7.3	-8.3	0.38	0.20
magic blue	-5.9	-5.5	-6.2		0.24	0.38
Mo(tfd-COCF$_3$)$_3$	-5.8	-5.6	-7.1	-7.8	0.35	0.64

intrinsic channel mobility of WSe$_2$ FETs, we employed a 4-point probe measurement as schematically shown in the optical image of a WSe$_2$ FET device in Figure 3.1(c). In this measurement, the intrinsic conductance of WSe$_2$ channel (i.e. free from contact resistance) can be obtained by measuring the voltage difference between the two inner probes (P$_1$, P$_2$) located in the channel while current was flown between the contacts (S, D) by applying drain (V$_D$) and gate voltages (V$_{GS}$).

In device fabrication, we used WSe$_2$ flakes with a layer thickness from 6 nm to 15 nm, confirmed by atomic force microscopy. In this thickness range, the substrate effect can be minimized ruled out due to a larger thickness relative to the expected screening length of WSe$_2$.[27] Also, it was confirmed that the effect of the thickness of WSe$_2$ on doping is negligible was not dominant in this thickness range.

3.2.3. Thickness effect to doping

The doping effect of surface charge transfer doping (SCTD) is dependent on the thickness of WSe$_2$. We investigated the effect of thickness of WSe$_2$ on the threshold voltage shift of WSe$_2$ FETs by SCTD. We suggested that the threshold voltage shifts of WSe$_2$ have the same tendency for the thickness of WSe$_2$ in all dopant solution concentration cases if

the SCTD effect is affected by the thickness of WSe₂. Figures 3.2 (a)-(c) show the threshold

voltage shift of magic blue doped WSe₂ FETs with 1 mM, 2.5 mM, and 5 mM solution

concentration. As shown in Figure 3.2, the dependency of threshold voltage on the

thickness of WSe₂ FETs was not same in all dopant solution concentration cases. While the

threshold voltage shift of WSe₂ was decreased with increasing the thickness of WSe₂ in the

case of doping with 5 mM doping solution, the threshold voltage shift of WSe₂ was not

significantly changed with respect to the thickness of WSe₂ in case of doping with 1 mM

and 2.5 mM magic blue dopant solution. It seems that the thickness effect was concealed

by the device-to-device variation of the threshold voltage shift of WSe₂ FET coming from

the non-uniformity of the doping method.
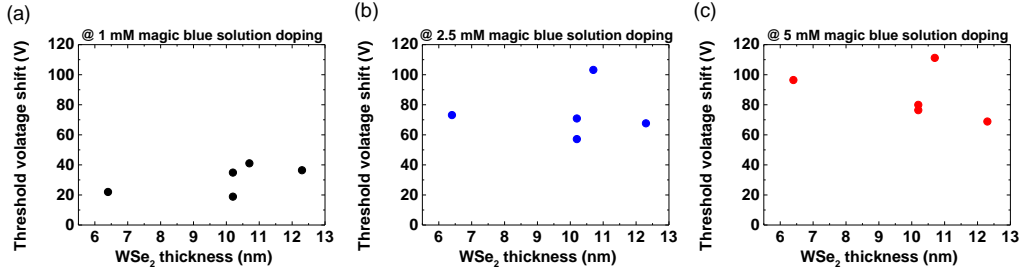
Figure 3.2 The threshold voltage shifts of doped WSe₂ with (a) 1 mM, (b) 2.5 mM, and (c)
5 mM magic blue dopant solution relative to the pristine WSe₂ FETs made with different
thickness of WSe₂ flakes.

3.2.4. Theoretical model for density of charged impurity (n_{imp}) calculation

Ong et al. reported a theoretical model for calculation of the charged impurity

limited mobility of TMDCs encapsulated by different top and bottom dielectric materials

[22]. In this model. TMDC layer was approximated as a zero-thickness 2-dimensional

electron gas (2DEG). The single charged impurity scattering potentials ϕ_q^{scr} is given by

$\phi_q^{scr} = e^2 G_q / \epsilon_{2D}(q, T)$, where q is the wave vector, e is the elementary charge, and G_q is

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Fourier transform of the Green's function solution of the Poisson equation. The G_q includes the electrostatic boundary conditions and is expressed by $G_q = [(\epsilon_{top}+\epsilon_{bottom}\coth(qt_{ox}))\,q]^{-1}$, where ϵ_{top} is the static permittivity of top dielectric, ϵ_{bottom} is the static permittivity of top dielectric, and t_{ox} is the thickness of bottom dielectric. In our case, top dielectric is air and bottom dielectric is SiO_2 which has a 270 nm thickness. So, in our case, the values are $\epsilon_{top} = 1$, $\epsilon_{bottom} = 3.9$, and $t_{ox} = 270$ nm. $\epsilon_{2D}(q,T)$ is the generalized static dielectric function expressed by $\epsilon_{2D}(q,T) = 1 - e^2 G_q \Pi(q,T,E_F)$, where $\Pi(q, T, E_F)$ is the static charge polarizability and E_F is the chemical potential. The static charge polarizability $\Pi(q, T, E_F)$ is expressed by $\Pi(q,T,E_F) =$

$\int_0^\infty d\mu \frac{\Pi(q,0,\mu)}{4k_BT\,\cosh^2(\frac{E_F-\mu}{2k_BT})}$, where $\Pi(q,0,\mu) = \Pi(0,0,\mu)[1 - \Theta(q - 2k_F)\{1 - $

$\left(\frac{2k_F}{q}\right)^2\}^{\frac{1}{2}}]$ with $k_F = \frac{\sqrt{2m_{eff}\mu}}{\hbar}$ and $\Pi(0,0,\mu) = -\frac{gm_{eff}}{(2\pi\hbar^2)}$. We used hole effective mass $0.44m_e$. The scattering rate for the single charged impurity (μ_{imp}) can be given by following equation

$$\Gamma_{imp}(E_k) = \frac{1}{2\pi\hbar}\int d\mathbf{k}' \left|\phi^{scr}_{|k-k'|}\right|^2 \times (1 - \cos\theta_{\mathbf{kk}'})\delta(E_\mathbf{k} - E_\mathbf{k'}),$$

where $\theta_{\mathbf{kk}'}$ is the scattering angle between the $\mathbf{k}$ and $\mathbf{k}$' states. From μ_{imp}, the charged impurity-limited mobility (μ_{imp}) is given by

$$\mu_{imp} = \frac{e}{\pi n \hbar^2 k_B T}\int_0^\infty f(E)[1 - f(E)]\,(n_{imp}\Gamma_{imp}(E))^{-1}EdE,$$

where $f(E)$ is the Fermi-Dirac function, k_B is the Boltzmann constant, and n is the carrier density, and n_{imp} is the charged impurity density. Using this equation, the μ_{imp} of WSe_2 was calculated.

In molecular scale, the amount of charge transfer (denoted as αe) between the

dopant molecule and WSe$_2$ is dependent on the molecule properties such as the dopant's available unoccupied density of states (DOS) and dielectric properties as well as the relative frontier orbital level. Then, the scattering potential between the charged dopant molecule and free carrier in WSe$_2$ FET is proportional to α. The scattering rate for the charged dopant molecule (Γ_{dopant}) is proportional to α^2 because the scattering rate is proportional to the square of the potential magnitude. This means that the larger the amount of charge transferred per dopant molecule, the lager scattering will be. Because it is defined as the scattering rate (Γ_{imp}) for the single charged impurity charged as e, we can regard Γ_{dopant} as $\Gamma_{dopant} = \alpha^2 \Gamma_{imp}$. In order to compare the charged impurity scattering by each dopant, the α^2 dependency of Γ_{dopant} was included in the ΔN_{imp} which is experimentally determined charged impurity density. That is, ΔN_{imp} is defined by $n_{dopant} \Gamma_{dopant} = n_{dopant}(\alpha^2 \Gamma_{imp}) = \Delta N_{imp} \Gamma_{imp}$.

3.3. Results & Discussions

3.3.1. Transfer curves of pristine and doped WSe$_2$ and threshold voltage shifts

To compare the doping strength and doping range achievable with each molecular dopant, we have calculated the amount of generated carrier density by doping using the shift in the threshold voltage for the doped WSe$_2$ FETs relative to the pristine devices. The generated carrier density of WSe$_2$ FETs by doping (Δn) can be estimated from $\Delta n = C_i \Delta V_{th}$, where C_i is the unit-area capacitance of the bottom SiO$_2$ dielectric ($C_i = 1.3 \times 10^{-4}$ F/m^2) and ΔV_{th} is the shift in the threshold voltage of the doped WSe$_2$ FETs relative to the pristine devices. Δn for three molecular dopants cases are summarized in Figure 3.3(d) (top panel). For this figure, several WSe$_2$ FETs (typically four to six devices) were

Figure 3.3 The representative gate-voltage dependent conductance curves of (a) pristine and (b) Mo(tfd-COCF$_3$)$_3$-doped WSe$_2$ devices at various temperatures, respectively. The representative temperature-dependent intrinsic mobility values extracted for the pristine and doped WSe$_2$ devices with (c) F$_4$-TCNQ, (d) magic blue and (e) Mo(tfd-COCF$_3$)$_3$, respectively.

measured to obtain the average ΔV_{th} and standard deviation values shown as error bars. For all the three molecular dopants, the generated carrier densities in WSe$_2$ FETs increase with the concentration of the dopant solutions. For example, for F$_4$-TCNQ, the generated carrier density increases from 2.04×10^{12} cm^{-2} to 2.75×10^{12} cm^{-2} and 3.61×10^{12} cm^{-2} as the dopant solution concentration increased from 1 mM to 2.5 mM and 5 mM, respectively.

It is worth noting that the maximum generated carrier density in the WSe$_2$ FETs doped by F$_4$-TCNQ (3.61×10^{12} cm^{-2}) was lower than that by magic blue (7.03×10^{12} cm^{-2}) and Mo(tfd-COCF$_3$)$_3$ devices (4.15×10^{12} cm^{-2}). Interestingly, although the LUMO levels

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of magic blue and Mo(tfd-COCF$_3$)$_3$ are comparable, the maximum generated carrier density for magic blue is about 1.7 times larger than that for Mo(tfd-COCF$_3$)$_3$. This indicates that the relative LUMO level of the dopant molecules with respect to the VBM of WSe$_2$ is not the sole parameter that determines the doping strength. Therefore we need to consider other factors such as coverage and surface density of the dopant molecules on the surface of TMDCs,[30, 31] which will be discussed in details later.

The conductivity ratio of the doped devices to the pristine devices (extracted at V_{GS} = -90 V) is shown in Figure 3.3(d) (bottom panel) to preliminarily check the effect of doping on the charge transport in the conduction channel. The conductivity increases with different doping levels for the F$_4$-TCNQ and magic blue devices can be associated with either the intrinsic mobility change of the doped channel or the contact resistance change. In this study, we focus on the intrinsic mobility changes of the channel in order to investigate the effect of doping on the charge transport of WSe$_2$ by eliminating the contribution of the contact resistance towards the total resistance of the device.

3.3.2. Temperature dependent conductance and intrinsic mobility of WSe$_2$ FET

Using 4-point probe measurement configuration shown in Figure 3.1(c), we conducted temperature-dependent electrical characterization. The channel conductance, G, which can be obtained by $G = I_{DS}/\Delta V$, where I_{DS} and ΔV denote the current level of WSe$_2$ FET device and the voltage difference between probe P$_1$ and P$_2$ shown in Figure 3.1(c), respectively. Figures 3a and 3b show typical gate-voltage dependent conductance curves of pristine and Mo(tfd-COCF$_3$)$_3$-doped WSe$_2$ devices, respectively, at different temperatures. The channel mobility can be calculated from the conductance curve by $\mu =$
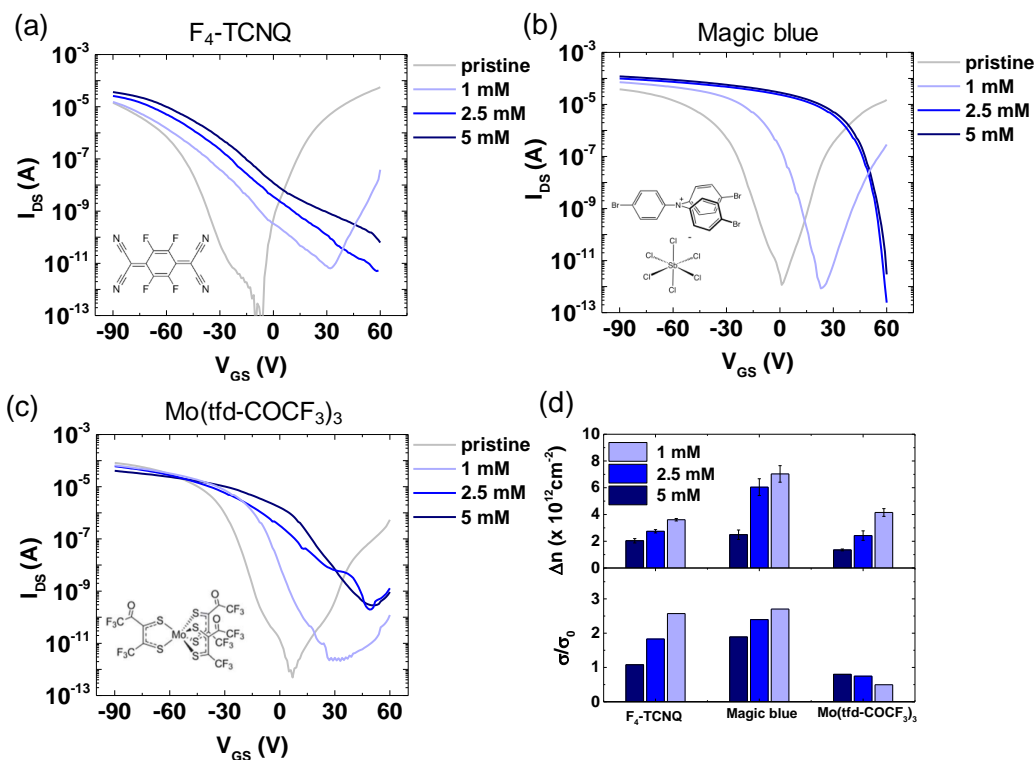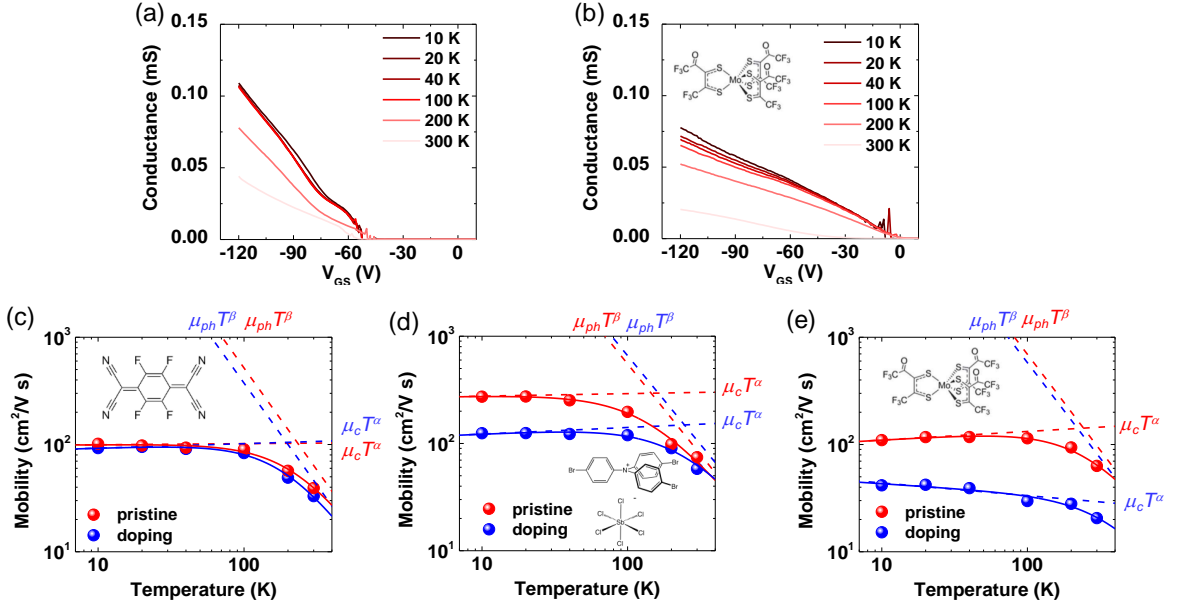
Figure 3.4 The representative gate-voltage dependent conductance curves of (a) pristine and (b) Mo(tfd-COCF$_3$)$_3$-doped WSe$_2$ devices at various temperatures, respectively. The representative temperature-dependent intrinsic mobility values extracted for the pristine and doped WSe$_2$ devices with (c) F$_4$-TCNQ, (d) magic blue and (e) Mo(tfd-COCF$_3$)$_3$, respectively.

$(dG/dV_{GS}) \times (L/WC_i)$, where $C_i = (\varepsilon_0\varepsilon_r)/d = 1.3 \times 10^{-4} F/m^2$ and G, L, and W denote the conductance, the channel length, and the channel width, respectively. Figures 3.4(c)-3.4(e) show the temperature-dependent intrinsic mobility values for the pristine and doped WSe$_2$ devices with 2.5 mM solution. To investigate different scattering mechanisms in the doped WSe$_2$ devices, we decompose the temperature dependence of the mobility by using Matthienssens's rule

$$\mu_{FET}(\mathrm{T}) = (1/\mu_C T^\alpha + 1/\mu_{Ph} T^\beta)^{-1} ,$$

where T, μ_C, μ_{Ph}, α and β denote temperature, charged impurity scattering-limited mobility at the zero temperature, phonon-limited mobility at the zero temperature, and their exponents, respectively. The contribution from each scattering mechanism (i.e. charged

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impurity scattering ($\mu_C T^{\alpha}$) and phonon scattering ($\mu_{Ph} T^{\beta}$)) are shown in Figure 3(c)-3(e) as dashed lines. In this analysis, we assume that the scattering from intrinsic defects in WSe$_2$ (e.g. Se vacancies[32]) and other scattering sources near the substrate were negligible in our multi-layer WSe$_2$ FET devices. [33, 34] The scattering effects of absorbents other than the dopants on the top surface of WSe$_2$ (e.g. residual water, organic contaminants, etc.), which can also act as scattering centers, are assumed to be negligible because they are mostly removed through the annealing process.[35] These are relevant since the charged impurity scattering (i.e. a long-range scattering) and phonon scattering contributions are the most dominant mechanisms in the charge transport of TMDCs. [21, 33]

In the case of multi-layer TMDCs, a homopolar phonon mode can be dominant among the phonon modes to determine the intrinsic mobility of TMDCs. [21] Rai *et al.* reported that the homopolar phonon mode of MoS$_2$ can be suppressed by depositing a high-k amorphous titanium suboxide on top of the MoS$_2$ surface.[36] In this case, β was confirmed to decrease by depositing the dielectric material due to the suppressed phonon scattering by the homopolar phonon mode. However, β value barely changes upon doping in WSe$_2$ devices (see Figures 3.4(c)-3.4(e)). This suggests that the phonon contribution to the charge transport properties of the WSe$_2$ is insensitive to the presence of the dopant molecules. On the contrary, the charged impurity scattering-limited mobilities of WSe$_2$ ($\mu_C T^{\alpha}$ in Figure 3.4(c)-3.4(e)) are generally reduced after doping for all three dopants (i.e. the charged impurity scattering increased upon doping). These results indicate that the dopant counterions created on the WSe$_2$ surface due to the charge transfer doping can act as charged impurity scattering centers for the WSe$_2$ channel. The mobility reduction by the externally introduced charged impurities has been well established for various

semiconductor materials (e.g. Si, GaAs, etc.).[37-39] We note that the magnitude of the reduction in the charged-impurity-scattering-limited mobility (i.e. $\mu_C T^\alpha$) is different for each dopant, indicating that the degree of scattering in the WSe$_2$ channel varies with the dopant molecule.

3.3.3. Dopant dependent charged impurity density

To quantitatively analyze the degree of charged impurity scattering, we have extracted the charged impurity density present in the doped WSe$_2$ by relating to their transport properties. Ong et al. reported a theoretical model for calculating the charged impurity-limited mobility of TMDCs.[22] In this model, the charged impurity-limited mobility of TMDCs is determined by the scattering rate for the charged impurity scattering potential ϕ_q^{scr} for a unit charge, e. The scattering rate for the single charged impurity (Γ_{imp}) can then be given by the following equation

$$\Gamma_{imp}(E_k) = \frac{1}{2\pi\hbar} \int d\mathbf{k}' \left| \phi_{|\mathbf{k}-\mathbf{k}'|}^{scr} \right|^2 \times (1 - cos\theta_{\mathbf{k}\mathbf{k}'})\delta(E_{\mathbf{k}} - E_{\mathbf{k}'}), (1)$$

where $\theta_{\mathbf{k}\mathbf{k}'}$ is the scattering angle between the $\mathbf{k}$ and $\mathbf{k}$' states. From Γ_{imp}, the charged impurity-limited mobility (μ_{imp}) is given by

$$\mu_{imp} = \frac{e}{\pi n \hbar^2 k_B T} \int_0^\infty f(E)[1 - f(E)] \left(n_{imp} \, \Gamma_{imp} \, (E) \right)^{-1} E dE, (2)$$

where $f(E)$ is the Fermi-Dirac function, k_B is the Boltzmann constant, and n is the carrier density, and n_{imp} is the charged impurity density. In our analysis, the mobility and carrier density extracted at 10 K were used to rule out the phonon contribution towards the charge transport. Figure 3.5(a) shows the calculated μ_{imp} as a function of the carrier density in the WSe$_2$ channel, n_{WSe2}, for n$_{imp}$ = 1,2,3,4, and 6×10^{12} cm^{-2}. To extract the charged impurity
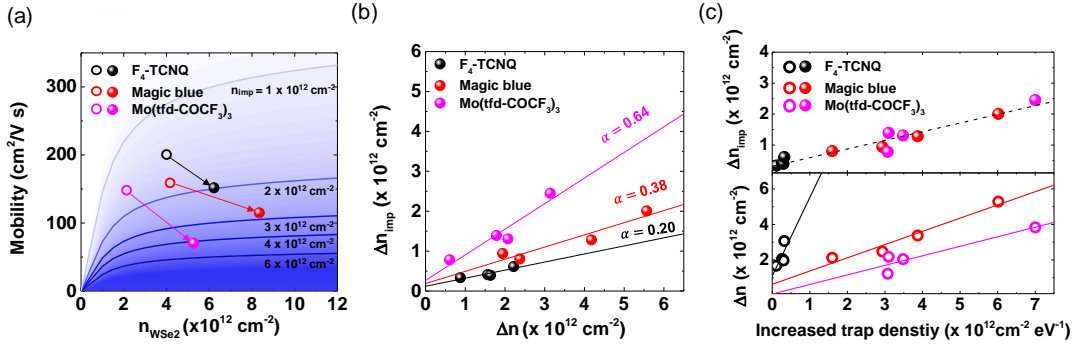
Figure 3.5 (a) The carrier density dependent calculated WSe$_2$ mobility with different n$_{imp}$ (lines) and the experimentally measured intrinsic mobility of pristine and doped WSe$_2$ (circles). (b) The plot of n$_{imp}$ generated in WSe$_2$ FETs by doping (Δn$_{imp}$) with F$_4$-TCNQ, magic blue, and Mo(tfd-COCF$_3$)$_3$ dopants versus generated carrier density by doping (ΔnWSe$_2$). (c) (Top panel) The universal linear relation between increased trap density of WSe$_2$ and Δn$_{imp}$. (Bottom panel) The dopant dependent relation between Δn$_{WSe2}$ and increased trap density of WSe$_2$.

density for each device, the mobility values extracted from each device were compared to the calculated μ_{imp} values shown in Figure 3.5(a). Representative mobility and carrier density (n_{WSe2}) values of the pristine (doped) WSe$_2$ devices extracted at V$_G$ = −120 V are plotted as open (filled) circles in Figure 3.5(a). A set of pristine and doped WSe$_2$ for each molecular dopant is denoted in different colors. As shown in Figure 3.5(a), the mobility reduction upon doping for all three dopants, as indicated by the arrows, is a direct evidence of the Coulomb scattering induced by the dopant counterions in the doped WSe$_2$ devices. Therefore, we can estimate the extra impurity density generated by doping, ΔN_{imp}(= $N_{imp-doped}$ − $N_{imp-pristine}$) for each dopant from the mobility curves for various n_{imp} values as shown in Figure 3.5(a) ,where $N_{imp-doped}$ and $N_{imp-pristine}$ are charged impurity density in doped and pristine WSe$_2$ devices, respectively.

The degree of Coulomb scattering induced by the dopant counterions will depend on the amount of charge transfer between WSe$_2$ and the dopant molecule. In molecular scale, the amount of charge transfer per dopant molecule (denoted as $\Delta Q = \alpha e$, where α is a constant that determines the effective degree of charge transfer) is dependent on the intrinsic molecular properties. In this case, the experimentally determined ΔN_{imp} values should not be treated as the actual charged impurity density (i. e. $\Delta n_{imp} = n_{imp\text{-}doped} - n_{imp\text{-}pristine}$, see Eqn. 2) generated by doping, but should be treated as an effective charged impurity density generated by doping since the scattering potential of each dopant molecule can differ by a factor of α from a unit charge (i.e. $\Delta N_{imp} = \Delta n_{imp}$ when $\alpha = 1$). For comparing the ΔN_{imp} between dopants, we analyzed the relation between ΔN_{imp} and Δn_{WSe2} to obtain the α value of each dopant corresponding to the transferred charge. Considering the dopant concentration and the value of α in combination with the theoretical model, we obtain a simple relation, $\Delta N_{imp} = \alpha \Delta n_{WSe2}$. In other words, the larger the value of α, the larger the contribution of each dopant molecule towards Coulomb scattering. Figure 3.5(b) shows the ΔN_{imp} of each dopant as a function of Δn_{WSe2}, from which we found that ΔN_{imp} for Mo(tfd-COCF$_3$)$_3$ is the largest, followed by magic blue and F$_4$-TCNQ at the same doping level. That is, α value for Mo(tfd-COCF$_3$)$_3$ ($\alpha = 0.64$) is the largest, followed by magic blue (0.38) and F$_4$-TCNQ (0.20).

The doping can additionally influence the subthreshold swing (SS) of WSe$_2$ FET which is related to trap density of WSe$_2$ FET. This is because trap states can be created by the charged impurity.[40] To investigate the relation between the SS value and the charged impurity, the trap density of WSe$_2$ FET was extracted by $D_{it} = \frac{c_i}{q^2}(\frac{qS}{k_B T ln(10)} - 1)$, where D_{it} is trap density and S is SS value. By comparing the trap density of pristine and doped

WSe$_2$ FET, we can calculate the increased trap density by doping. As shown in Figure 3.5(c) (top panel), the increased trap density has a universal linear relation with Δn_{imp} for all dopants showing that there is a correlation between the increased trap density and Δn_{imp}. Considering $\Delta n = \Delta n_{imp}/\alpha$, this monotonic behavior indicates that the increased trap density mainly depends on α of the dopant at the same doping level. In other words, the larger α, the larger trap density will be generated by doping, as shown in Figure 3.5(c) (bottom panel).

3.3.4. DFT Calculation

To understand the microscopic nature of charge transfer process between WSe$_2$ and the dopant molecules, the experimentally determined values of α for each dopant can be viewed against in-depth DFT calculations. In principle, the charge transfer process at the WSe$_2$/molecule interface is a complex problem that depends on multiple variables such as the relative frontier orbital levels, available density of states, and dielectric properties, all of which are considered in our DFT calculations. From the DFT calculations, we obtained the planar-averaged charge density profiles of the charge density difference $\Delta \rho = \rho_{doped-WSe_2} - (\rho_{WSe_2} + \rho_{dopant})$ along the c-axis for magic blue, Mo(tfd-COCF$_3$)$_3$, and F$_4$-TCNQ as shown in Figures 3.6(a)-(c). Using these profiles, we obtained the amount of charge transfer per dopant (ΔQ_{DFT}) for magic blue (0.24e), Mo(tfd-COCF$_3$)$_3$ (0.35e) and F$_4$-TCNQ (0.38e), respectively (details on the calculation in Supporting Information). In overall, our DFT calculations show an unambiguous p-type doping behavior for all the dopants and the same trend in ΔQ_{DFT} for magic blue and Mo(tfd-COCF$_3$)$_3$ as expected from αe values extracted from the experiments. A relatively large deviation of ΔQ_{DFT} from αe for F$_4$-TCNQ is possibly due to an overestimated LUMO level of F$_4$-TCNQ (-

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Figure 3.6 Computed planar-averaged charge density difference profiles along the out-of-plane for (a) magic blue-, (b) Mo(tfd-COCF$_3$)$_3$-, and (c) F$_4$-TCNQ-doped WSe$_2$. Shaded red and blue correspond to the positions of WSe$_2$ layer and molecular dopants, respectively. Insets show isosurface plots of the charge density difference for molecular dopant binding site in WSe$_2$. Yellow and blue isosurfaces represent the excessive and deficient charge densities respectively. The isosurface level is equal to 0.002 e/Å^3. Computed total and partial density of states (DOS) of (d) magic blue-, (e) Mo(tfd-COCF$_3$)$_3$-, and (f) F$_4$-TCNQ-doped WSe$_2$. The LUMO and HOMO levels of three molecular dopants are labeled. Since the total DOS of magic blue, Mo(tfd-COCF$_3$)$_3$, and F$_4$-TCNQ are much smaller than that of the WSe$_2$ supercell, we plotted the total DOS of magic blue, Mo(tfd-COCF$_3$)$_3$, and F$_4$-TCNQ fifteen times larger than the actual values.

6.0 eV) from the conventional DFT calculations, which is larger than numerous experimentally determined values (~-5.2 eV) from literature [19, 27, 38][19, 27, 38] unlike the computed values of magic blue and Mo(tfd-COCF$_3$)$_3$ (see Table 1). In addition, the relatively small values of ΔQ_{DFT} for all the dopants (compared to αe) can be potentially originated from multi-layer stacking feature of dopant molecules in our experiments, which would increase the overall αe (see Figure S13 in Supporting Information) [39].[39]

We have then examined the electronic structures of three molecular dopants and doped-WSe$_2$ systems to elucidate the relation between the electronic properties and the charge transfer. Figures 3.6(d)-(f) show the computed density of states (DOS) of WSe$_2$ (black line) with the dopant adsorptions (shaded black) and the partial DOS of magic blue, Mo(tfd-COCF$_3$)$_3$ and F$_4$-TCNQ (each atomic contribution represented in different colors). The LUMO and HOMO levels of the dopants are labeled. The computed DOS of the doped WSe$_2$ show clear evidence for p-type doping for all the dopants as shown from the downward shift in the Fermi level of WSe$_2$ and partially filling of the DOS at LUMO for all the dopant molecules. More specifically, for magic blue, the DOS at LUMO level is manly contributed by the atoms composing the tri-bromophenyl cation (C, N, and Br) which agrees well with the isosurface plot of the charge difference as visualized in the inset of Figure 3.6(a) (yellow region). In our DFT calculations, we found that the ground state of magic blue is the doublet state (S = 1/2) while that of the other two is the singlet state (S = 0). Thus, we plotted the DOS of magic blue with spin up and down components separately as shown in Figure 3.6(d). It is worthy to note that ΔQ_{DFT} for magic blue (0.24e) is smaller than that of Mo(tfd-COCF$_3$)$_3$ (0.35e) even though the LUMO level position and the dielectric constant of magic blue are comparable to those of Mo(tfd-COCF$_3$)$_3$ (see Table 3.1). αe values extracted from the experiments (0.38e for magic blue and 0.64e for Mo(tfd-COCF$_3$)$_3$) also show the same trend. According to our computed DOS (Figure 5d), the reduced spin degree of freedom in charge-transfer from WSe$_2$ to magic blue can be the origin of the smaller value of ΔQ_{DFT} of magic blue. Our computed DOS result clearly shows the selective transfer of spin-down electrons from WSe$_2$ to the LUMO of magic blue. In overall, our DFT calculation implies that spin configuration as well as the intrinsic

frontier orbital positions and dielectric constants of molecules play a significant role in determining the amount of charge transfer between WSe_2 and dopants.

3.4. Conclusion

In conclusion, we explored dopant dependent charge transport of molecular-doped WSe_2 FETs for three different dopants via experimental determination of the intrinsic mobility values of the doped WSe_2 channels. The reduction in the intrinsic mobility after doping could be interpreted as the creation of charged impurities in the form of dopant counterions on the WSe_2 surface. Comparison between the three dopants showed that the larger the degree of charge transfer between WSe_2 and dopants, the larger the carrier density generated in WSe_2, but also the larger the degree of Coulomb scattering induced by each dopant counterion. An agreement with DFT calculations corroborated the importance of considering the selective spin transfer as well as the relative frontier orbital positions of the dopant molecules. Our results will pave the way for controlling the carrier density and conductivity levels of TMDC through molecular doping and provide criteria for selecting appropriate molecular dopants for doping applications in TMDC nano-electronic devices such as carrier-type control of the active channel and contact doping for low-power operation.

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Chapter 4. Trap-mediated electronic transport properties of gate-tunable pentacene/MoS$_2$ p-n heterojunction diodes

In this chapter, we will discuss about the trap-mediated electronic transport properties of gate-tunable pentacene/MoS$_2$ p-n heterojunction diodes. We investigated the trap-mediated electronic transport properties of pentacene/molybdenum disulphide (MoS$_2$) p-n heterojunction devices. We observed that the hybrid p-n heterojunctions were gate-tunable and were strongly affected by trap-assisted tunnelling through the van der Waals gap at the heterojunction interfaces between MoS$_2$ and pentacene. The pentacene/MoS$_2$ p-n heterojunction diodes had gate-tunable high ideality factor, which resulted from trap-mediated conduction nature of devices. From the temperature-variable current-voltage measurement, a space-charge-limited conduction and a variable range hopping conduction at a low temperature were suggested as the gate-tunable charge transport characteristics of these hybrid p-n heterojunctions. Our study provides a better understanding of the trap-mediated electronic transport properties in organic/2-dimensional material hybrid heterojunction devices.

4.1. Introduction

Recently, two-dimensional (2D) materials have emerged as semiconductors for future nanoelectronic devices due to their ultrathin nature and favourable electronic properties.[1-3] Among these materials, graphene has attracted a lot of attention due to its excellent physical properties, such as high mobility, but has limits on its use as a semiconductor because of its zero band gap energy.[4-6] Unlike graphene, transition metal dichalcogenide (TMDC) materials, such as MoS$_2$, MoSe$_2$, and WSe$_2$, are being largely studied as semiconductors because these materials have 2D-layered structures with sufficient band gap energy that depends on the number of stacked layers.[7-9] In particular, MoS2 has been widely studied in many device applications, such as field-effect transistors

(FETs), memory, and sensors.[10-12] For example, it has been reported that single-layer MoS_2-based FETs have good mobility (~tens of cm^2/Vs) and high on/off ratios (~108).[3,10-12]

TMDCs have pristine surfaces free of dangling bonds due to van der Waals (vdW) bonding between the layers of the TMDCs, which enables vertical staking of other materials that do not have similar lattice constants to those of TMDCs. In particularly, many efforts have been made to demonstrate the novel physical phenomena in vertically and laterally stacked 2D layered materials and their heterostructures.[13-15] Most recently, there have been a few studies on vdW heterostructures based on 2D TMDCs combined with organic materials.[16-25] Organic materials have several favourable features, such as flexibility, low-cost production, low-temperature processing, and a lack of dangling bonds of organic materials.[26,27] Previous studies demonstrated the gate-tunable electronic and optoelectronic characteristics in vdW organic/inorganic p-n hybrid heterostructures.[16,18-25] In particular, Jariwala et al. reported an asymmetric control over the antiambipolar characteristics in pentacene/MoS_2 heterojunctions and observed the photovoltaic effect.[16] However, an understanding of the electrical transport properties of the organic/inorganic hybrid structures is still limited because organic materials exhibit the presence of chemical and structural defects due to imperfect crystallinity, which can often lead to charge trap densities on the order of $10^{18}/cm^3$.[28] Charge trapping at the p-n heterointerface plays an important role in the performance of p-n heterojunction devices. In particular, the gate-tunable electronic properties in organic/inorganic hybrid p-n junctions are strongly affected by the charge mobility of p-type and n-type materials, which is closely related to the charge trapping phenomena.[29-31] Therefore, a thorough understanding of the electronic transport associated with charge trapping in hybrid heterojunctions is required to facilitate

the design of electronic and optoelectronic devices based on 2D and organic semiconductors.

Here, we report trap-mediated charge transport properties in pentacene/MoS$_2$ hybrid heterojunction p-n diodes. We observed that the gate-tunable electronic conduction of the p-n junction was strongly affected by trap-assisted tunnelling through the vdW gap at the heterojunction interfaces between MoS$_2$ and pentacene. We also found that the energy distribution of the trap states is closely related to the carrier activation energy. Using the temperature-variable current-voltage characteristics, the gate-tunable charge transport can be explained by a space-charge-limited conduction and a variable range hopping conduction, especially at low temperature.

4.2. Experiments

4.2.1. Device fabrication process

Figure 4.1 shows the device fabrication processes of pentacene/MoS$_2$ p-n junction devices. First, SiO$_2$ (270 nm thick)/Si substrate was prepared and cleaned by acetone, isopropanol, and de-ionized (DI) water for 15 min each. Then, we transferred MoS$_2$ flakes from a bulk MoS$_2$ crystal onto the substrate by a mechanical exfoliation method. And we found suitable MoS$_2$ flakes that could be used as a field effect transistor (FET) using an optical microscope. To make patterns, we spin-coated methyl methacrylate (MMA) (9% concentration in ethyl lactate) and polymethyl methacrylate (PMMA) (5% concentration in anisole) as electron resist at 4000 rpm and baked the sample at 180°C for 90 s on a hot plate. And we made patterns on the electron resist layer using an electron beam lithography system with a 30 kV exposure.
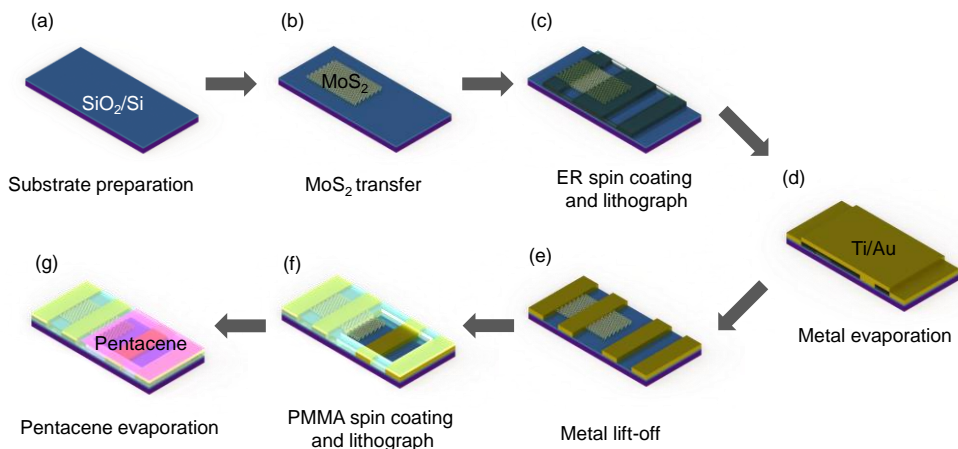
Figure 4.1 Schematics of fabrication process of pentacene/MoS$_2$ p–n junction devices.

After patterning, the devices were soaked in a methyl isobutyl ketone/isopropyl alcohol (1:3) solution during 1 min for pattern development. Next, Au (50 nm thick)/Ti (5 nm thick) was deposited as the source and drain electrodes using an electron beam evaporator (KVE-2004L, Korea Vacuum Tech) with a deposition rate of 0.5 Å /s at pressure of ~10^{-7} torr. After the lift-off process with acetone, the source and drain electrode patterns were completed. Then, we spin-coated the PMMA on MoS$_2$ devices and made patterns to make p-n junction devices by using the electron lithography system. PMMA coating prevents the unwanted effects that were caused by pentacene which had been deposited on MoS$_2$ FET channel. Finally, the pentacene active film (60 nm thick) was deposited by a thermal evaporator (GVTE1000, GV-Tech) with a deposition rate of 0.5 Å /s at pressure of ~10^{-6} torr.

4.2.2. Electrical characterization

All electrical characteristics of the devices were measured using a probe station (JANIS, ST-500) with a temperature variation capability and a semiconductor parameter

analyser (Keithley 4200-SCS).

4.3. Results and Discussions

4.3.1. Electrical characteristics of MoS$_2$ FET and pentacene FETs

Figure 4.2(a) shows the fabrication process of the pentacene/MoS$_2$ p–n junction devices. First, we transferred MoS$_2$ flakes from a bulk MoS$_2$ crystal (purchased from SPI Supplier, USA) onto a substrate by a mechanical exfoliation method (step 1). The substrate used in this study was a 270 nm thick SiO$_2$ layer on heavily doped p++-Si, which is used as a common back-gate electrode. Then, we made patterns on the MoS$_2$ flake and SiO$_2$ to form contact electrodes using an electron beam lithography system. Au (50 nm)/Ti (5 nm) were deposited as the contact electrodes using an electron-beam evaporator (step 2). After that, we spin-coated polymethyl methacrylate (PMMA) onto the MoS$_2$ surface and patterned the surface to prepare p-n junctions using the electron beam lithography system (step 3). The PMMA layer was also used as a protection layer to isolate the p-n junction area from the MoS$_2$ FETs. Finally, the pentacene film (60 nm) was deposited with a thermal evaporator to fabricate the p-n heterojunctions (step 4). Here, one end of the MoS$_2$ channel was in contact with the Ti/Au, and one end of the pentacene channel was in contact with Au. Note that because the work function of Ti (~4.3 eV) and Au (~5.1 eV) are close to the electron affinity of MoS$_2$ (~4.2 eV)[18,32] and the highest occupied molecular orbital (HOMO, ~4.9 eV)[33] of pentacene, these metal contacts can provide good electrical contacts on MoS$_2$ and pentacene. Figure 4.2(b) and (c) show an optical image of the fabricated pentacene/MoS$_2$ p-n junction device and an AFM image of a MoS$_2$ layer with electrodes, respectively. A MoS$_2$ flake is enclosed by the black dashed line in Figure 4.2(c).
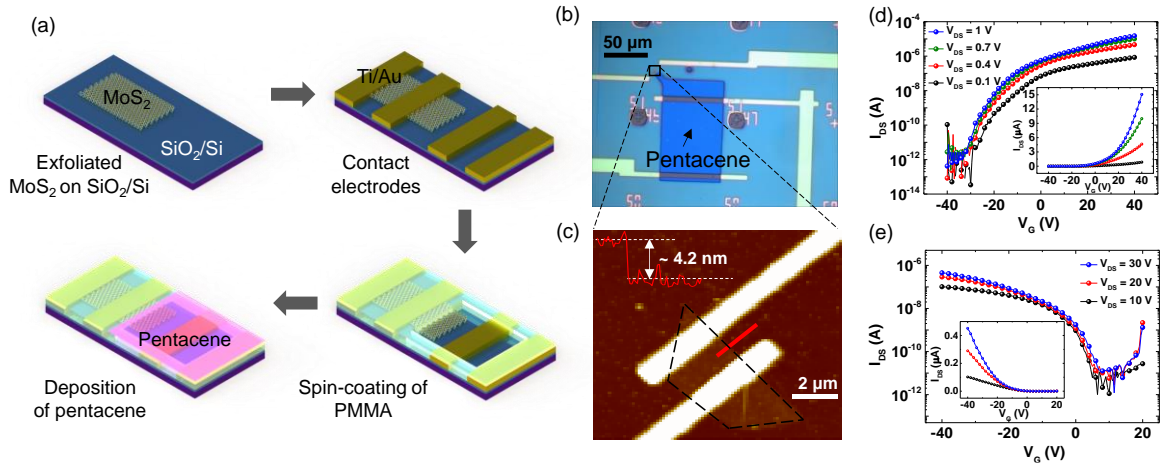
Figure 4.2 (a) Schematics of the device fabrication processes for the pentacene/MoS$_2$ p-n heterojunction devices. (b) Optical image of a device. The blue area is the pentacene used in the p-type semiconductor. (c) AFM image of the MoS$_2$ FET area. The red line shows the thickness of the MoS$_2$ film (~4.2 nm). (d) Electrical data of a MoS$_2$ FET. (e) Electrical data of a pentacene FET.

The red line in Figure 4.2(c) shows the topological profile of the MoS$_2$ flake (~4.2 nm thick), which corresponds to ~6 layers of MoS$_2$.

Figure 4.2(d) and (e) show the electrical characteristics of the fabricated MoS$_2$ and pentacene FET devices, respectively. MoS$_2$ and pentacene exhibit n-type and p-type nature, respectively. From these figures, the field-effect mobility (μ) of the MoS$_2$ and pentacene FETs was calculated by the following formula:

$$\mu = (dI_{DS}/dV_G) \times (L/WC_iV_{DS}) \tag{1}$$

where $C_i = (\varepsilon_0\varepsilon_r)/d = 1.3 \times 10^{-4} F/m^2$, W is the channel width, L is the channel length, Ci is the capacitance between the MoS$_2$ or pentacene channel and the p++-Si gate per unit area, ε_0 is the vacuum permittivity, ε_r is the dielectric constant of SiO$_2$, and d is the thickness of the SiO$_2$ layer. The field-effect mobility was estimated to be ~15.2 and 0.06 cm^2/Vs for MoS$_2$ and pentacene FETs, respectively. It has been reported that band-like transport are observed in MoS$_2$ devices beyond at a certain carrier density.[34] However, we could not

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observe such band-like transport in our MoS$_2$ devices because of insufficient carrier density. All measurements were performed in a vacuum (~10^{-4} torr) to prevent unwanted effects due to moisture and oxygen from the ambient environment.[35-37]

4.3.2. Gate-tunable electrical characteristics of pentacene/MoS$_2$ p-n junction device

Next, the gate-tunable electrical characterizations were conducted for the p-n heterojunction between MoS$_2$ and pentacene. Figure 4.3(a) shows a three-dimensional plot of the current-voltage (I_D-V_D) characteristics of a pentacene/MoS$_2$ p-n heterojunction device at different gate voltage (V_G) conditions. Here, the voltage was applied to the pentacene side electrode, and the MoS$_2$ side electrode was grounded, while a common gate voltage was applied to both MoS$_2$ and pentacene. From the I_D-V_D curves, we found that the p-n heterojunction device made a transition from nearly insulating behaviour at $V_G = 10$ V to rectifying behaviour at $V_G \leq 0$ V. Jariwala et al. have also reported similar behaviour for their pentacene/MoS$_2$ heterojunctions.[16]

When heterostructure devices consist of materials that lack dangling bonds, the different materials can bond by a vdW force at the heterojunction interface.[38-40] Such heterostructures, such as our pentacene/MoS$_2$ p-n heterojunctions, can have vdW gap between the materials, which act insulators. Then, the tunnelling phenomenon can occur through the vdW gap. To analyse this tunnelling phenomenon, we used the Fowler-Nordheim plot; that is, $\ln(I_D/V_D^2)$ versus $1/V_D$, as shown in Figure 4.3(b). In this plot, in the Fowler-Nordheim tunnelling (FNT) regime, the charges transport through a triangular barrier, and the current is proportional to $V^2 \exp[-\frac{8\pi d\sqrt{2m^*}\Phi^{3/2}}{3hqV}]$, and in the direct
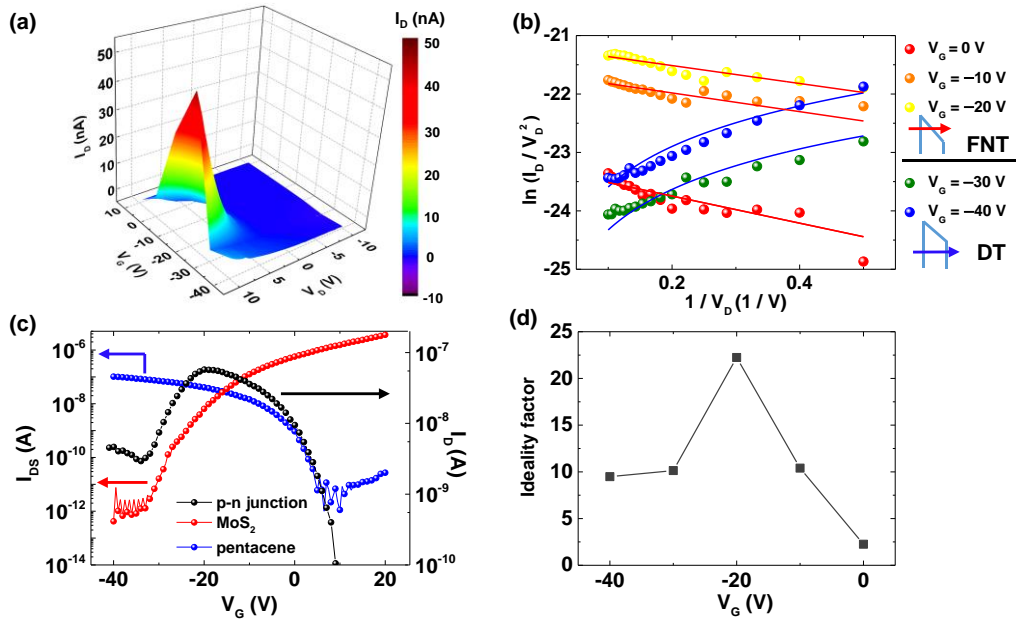
Figure 4.3 (a) Three-dimensional plot of the I_D–V_D curves of a pentacene/MoS$_2$ p–n heterojunction device with V_G varying from 10 V to –40 V. (b) Ln (I_D/V_D^2) versus $1/V_D$ plot of a pentacene/MoS$_2$ p-n junction device. Schematics show the Fowler-Nordheim tunnelling (FNT) and direct tunnelling (DT) for different gate voltage conditions. (c) Semilogarithmic I_{DS}–V_D curves of MoS$_2$ (red) and pentacene (blue), and semilogarithmic I_D-V_D curve of the pentacene/MoS$_2$ p-n junction device (black). (d) Gate-voltage-dependent ideality factor of the pentacene/MoS$_2$ p-n junction device.

tunnelling (DT) regime, the carriers pass through a rectangular barrier, and the current is proportional to $V \exp[-\frac{4\pi d\sqrt{2m^*\Phi}}{h}]$, where m* is the effective mass of the carrier, Φ is the barrier height, d is the tunnelling distance, h is Planck′s constant, q is the element charge, and V is the applied voltage.[41] Interestingly, at V_G = 0, –10, and –20 V, the current at a high forward bias exhibited a linear decrease in the FN plot, indicating that the transport mechanism is FNT dominant, whereas the forward current when V_G = –30 and –40 V exhibited logarithmic growth, indicating DT dominant transport. This type of tunnelling

transformation upon changes in the gate voltage can be understood by the energy band alignment, which will be explained in a later section.

Figure 4.3(c) further shows the gate-tunable electrical properties for the pentacene/MoS$_2$ p-n heterojunction with an asymmetric antiambipolar response. Here, the antiambipolar behaviour means that current versus gate voltage curve shows convex-up shape (black curve in Figure 4.3(c)). And asymmetry is shown in such a way that the slopes of the curve on left and right side of the peak current position were different, and the current decreased more rapidly on the left side than on the right side of the current peak position. It has been reported that the asymmetric characteristics can be controlled by the ratio of the mobility, the channel length, and the series resistances of MoS$_2$ and pentacene.[16] The mobility and series resistance are related by the trap density;[29-31] therefore, charge traps are an important source of asymmetric transconductance of the pentacene/MoS$_2$ p-n heterojunctions.

Figure 4.3(d) shows the ideality factors of the pentacene/MoS$_2$ p–n heterojunction devices as a function of the gate voltage. The ideality factor can be extracted by the following p–n diode equation

$$I = I_0(\exp\left(\frac{qV_D}{nk_BT}\right) - 1),\qquad\qquad(2)$$

where I_0 is the saturation current, q is the elementary charge, k_B is Boltzmann's constant, T is the temperature, V_D is the applied voltage, and n is the ideality factor of the p-n junction. The ideality factor of our device was between 2.2 and 22.2, which is much higher than the typical value of the ideality factor (between 1 and 2) observed for conventional p-n semiconductor junctions.[42] A large ideality factor value is a common feature of vdW heterostructure devices that results from the trap state.[17-19] Because the ideality factor varies with the gate voltage, it suggests that the influence of the trap density on the charge

transport conduction of the pentacene/MoS$_2$ p-n heterojunction device also depends on the gate voltage.

4.3.3 Space-charge-limited conduction of penatene/MoS$_2$ p-n heterojunction device

To understand the effect of trap sites in the pentacene/MoS$_2$ p-n heterojunction devices, we measured the I$_D$-V$_D$ curves at different temperatures from 100 to 250 K with a step of 25 K. Figure 4.4(a) shows the semilogarithmic scale log-log plot of I$_D$ versus V$_D$ at V$_G$ = –20 V, at which the ideality factor was highest (see Figure 4.3(d)). In Figure 4.4(a), the current and voltage of the p-n heterojunction devices follow a power-law relationship of I$_D$ ~ V$_D{}^m$, in which the slope (m) varies from 2.5 to 3.1 with decreasing temperature. It is known that the power-law dependence is characteristic of space-charge-limited conduction (SCLC) with the presence of exponentially distributed charge traps.[43] SCLC means that space charges, which consist of trapped carriers near the Fermi level, make electric fields and affect carrier conduction. In SCLC with exponentially distributed traps, the current is described as

$$I \sim q^{-m}\mu N_{DOS}(2m - 1/m)^m (m - 1/m)^{m-1}(\varepsilon_0 \varepsilon_r \ /N_t)^{m-1} \ V^m/d^{2m-1}, (3)$$

where N$_t$ is the density of the trap states, ε_0 is the vacuum permittivity, ε_r is the dielectric constant, μ is the mobility, N$_{DOS}$ is the density of state in the relevant band, and d is the channel length. In SCLC with exponentially distributed traps, the power-law parameter m decreases with increasing temperature and has a larger value than 2.[43] We observed this behaviour (inset of Figure 4.4(a)), which means the trap-ass isted SCLC mechanism is the dominant conduction in our pentacene/MoS$_2$ hybrid p-n devices. The slope of the graph (inset of Figure 4.4(a)) is related to the critical temperature, which we will discuss in a later
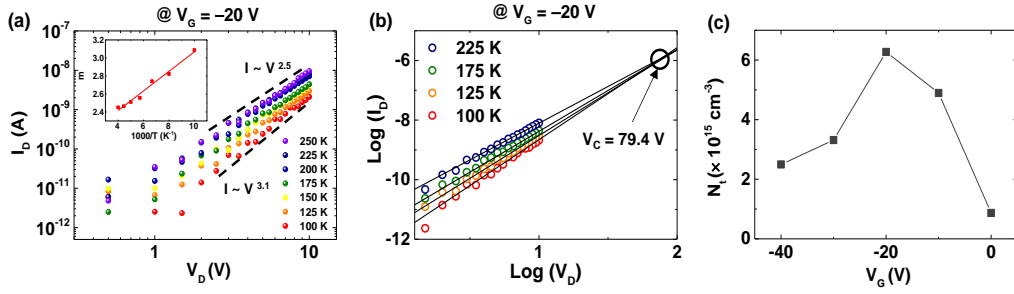
Figure 4.4 (a) Semilogarithmic scale log-log plot of the I_D–V_D data at $V_G = -20$ V. Inset shows the exponent m in $I_D \sim V_D^m$ as a function of temperature. (b) The power-law fitting lines in (a) meet at a critical voltage V_C. (c) The density of traps N_t as a function of gate voltage.

section. Also, this SCLC conduction was observed in control MoS_2 and pentacene FETs but it is observed only in certain conditions of gate voltage and temperature. In the case of pentacene/MoS_2 p-n heterojunction, the SCLC conduction was observed at all the gate voltage and temperature conditions. These results suggest that the SCLC conduction occurs not only in the junction of pentacene/MoS_2, but also in the series resistance of the MoS_2 and pentacene channels.

As shown in Figure 4.4(b), the power-law fitted lines at different temperatures in the log-log plot meet at a critical voltage (V_C), at which the density of traps can be calculated by the following relation: $N_t = \frac{2\varepsilon_0\varepsilon_r}{qL^2}V_C$, where N_t is the trap density in the channel, and L is the channel length.[44] As V_D increases, the trap sites are gradually filled by injected charge carriers from the electrode. At V_C, the traps are completely filled, and the conductivity of the device becomes independent of temperature.[44] The V_C of the device was ~79.4 V at $V_G = -20$ V (Figure 4.4(b)), which corresponds to $N_t \sim 6.3 \times 10^{15}$ cm^{-3}. Figure 4.4(c) shows the density of traps N_t as a function of the gate voltage, as determined from the V_C values at different gate voltages. Considering that higher trap density increases

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the ideality factor,[45] the ideality factor variation follows the trend of trap density variation (see Figure 4.3(d) and 4.4(c)). Note that our devices had the highest current at V_G = –20 V, where the trap density was the largest. This is because the current also depends on the activation energy of the charge carriers at the traps, which will be explained later (Figure 4.5(b)).

4.3.4 Variable-range hopping conduction of pentacene/MoS₂ heterjunction device

Figure 4.5(a) is an Arrhenius plot of the conductivity (σ) for gate voltages from –40 V to 0 V with a step of 10 V at a fixed V_D = 10 V. The activation energy (E_A) values were determined by thermally activated transport ($\sigma \sim \exp(-E_A/k_BT)$ in a high-temperature region (T > ~175 K), and E_A is plotted as a function of the gate voltage, as shown in Figure 4.5(b) (red filled circles). In the case of SCLC-dominant material, the larger the trap density, the larger the activation energy and the smaller the conductivity.[46] However, in our case, the tendency of the activation energy (Figure 4.5(b)) does not match the tendency of the trap density (Figure 4.4(c)). This tendency discrepancy can be due to the variation in the number of shallow traps that can be thermally activated in response to the gate voltage, which can be described by the critical temperature (T_C) values as a function of the gate voltage (blue open circles), as shown in Figure 4.5(b). As we mentioned previously, T_C can be calculated from the slope of the Arrhenius plot of m (Figure 4.4(a) inset). Therefore, as T_C increases, the activation energy increases due to the decrease in the number of shallow traps.[46] And, as the activation energy increases, the conductivity decreases due to the decrease in the carrier concentration.
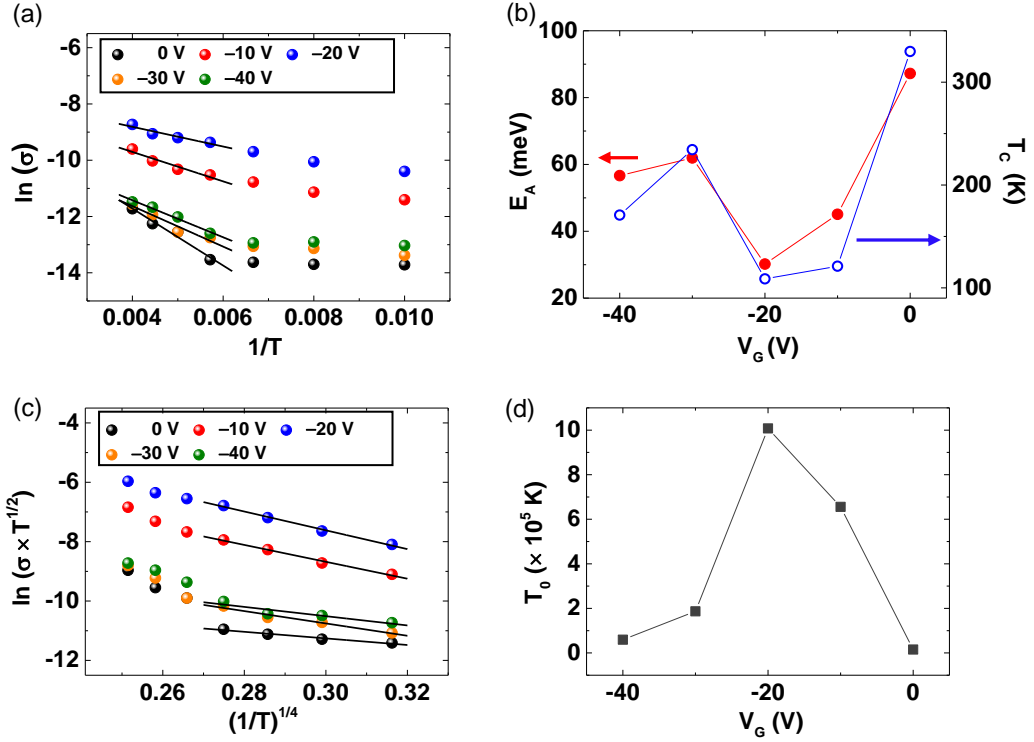
Figure 4.5 (a) Arrhenius plot of the conductivity σ for gate voltages from –40 V to 0 V at a fixed V_D = 10 V. (b) Activation energy (E_A) values determined from a high-temperature region (T > ~175 K) are plotted as a function of gate voltages. The T_C values (a parameter indicating the energy distribution of trap sites) are also plotted. (c) Plot of the conductivity of pentacene/MoS₂ hybrid p–n devices that follow the variable range hopping conduction model. (d) T_0 values (a parameter showing how actively variable range hopping conduction occurs) as a function of gate voltage.

In contrast to the high-temperature region (T > ~175 K), in the low-temperature region, the conduction of the pentacene/MoS₂ hybrid device does not obey thermally activated transport (see Figure 4.5(a) and 4.5(c)). The conduction in MoS₂ and pentacene with trap sites is often explained by a variable range hopping (VRH) conduction, especially at a low temperature.[47,48] VRH is a conduction in which the charge carriers transport by hopping through the trap states near the Fermi level.[49] Mott suggested that the conductivity of VRH-dominant 3-dimensional (3D) materials is given by $\sigma(T) =$

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$\sigma_0(T^{-\frac{1}{2}}) \exp[-(T_0/T)^{1/4}]$, where σ_0 is the characteristic conductivity, which is a function of $T^{-1/2}$, and T_0 is the characteristic temperature.[50] In our case, although the MoS$_2$ channel has a 2D structure, we assume that the structure of our device is 3D due to the pentacene channel region which has a 3D structure. Also, we found that the 3D VRH model was the best fitting dimensional model among 1D, 2D, and 3D fittings although the VRH fittings between dimensionalities were not significantly different. Figure 4.5(c) shows that the conductivity of the pentacene/MoS$_2$ hybrid p-n devices obeys the Mott's 3D VRH model. T_0 is the parameter showing how actively VRH conduction occurs; when T_0 is higher, hopping occurs more actively in the conduction.[47] Figure 4.5(d) shows the values of T_0 calculated from Figure 4.5(c) at various gate voltages. The variation in T_0 (Figure 4.5(d)) has a similar tendency to the tendency of the variation in N_t (Figure 4.4(c)), which indicates that as the number of trap states increases, VRH occurs more actively in the conduction. In summary, the discrepancy between the variation of the activation energy and the trap density in response to the gate voltage is due to the effect of the gate voltage-dependent number of shallow trap states, and the similar gate voltage dependency of the T_0 and trap density indicates that the more trap density, the more active VRH is. Note that VRH conduction was observed in control MoS$_2$ and pentacene at certain conditions of gate voltage and temperature, which suggests that VRH conduction occurs not only in the junction of pentacene/MoS$_2$, but also in the series resistance of MoS$_2$ and pentacene channels.

4.3.5 Energy band schematics

Figure 4.6 illustrates the energy band diagrams of the pentacene/MoS_2 p-n heterojunction. Figure 4.6(a) shows the electrical parameters of the materials; the work functions (Φ) of Ti and Au are 5.1 eV and 4.3 eV, respectively; the work functions of MoS_2 and pentacene are in the range 4.5-4.9 eV and approximately 4.5 eV, respectively; the electron affinities (χ) of MoS_2 and pentacene are 4.0 eV and 2.7 eV, respectively; and the energy gaps (E_G) of MoS_2 and pentacene are 1.2 eV and 2.2 eV, respectively.[32,33,51] Figure 4.6(b) and 4.6(c) show the energy band diagram in the forward bias condition at -20 V $\leq V_G \leq 0$ V and $V_G \leq -30$ V, respectively. Electrons are injected into the conduction band of MoS_2, and holes are injected into the highest occupied molecular orbital (HOMO) of the pentacene or traps near the Fermi level. These charges tunnel through the energy barrier of the vdW gap at the pentacene/MoS_2 junction interface. At -20 V $\leq V_G \leq 0$ V, both the electrons and holes can be charge carriers (Figure 4.3(c)), and they pass through the triangular energy barrier via FNT (see Figure 4.3(b)). It has been reported that structural defects of MoS_2 and grain boundary of pentacene layers can act as surface charge trapping sites.[52,53] Also, non-uniformly deposited pentacene layer on MoS_2 layer can contribute formation of interfacial trap sites between the layers. Those traps at the interface between MoS_2 and pentacene can assist the transport by increasing the tunnelling probability. In trap-assisted FNT, the larger the trap density, the higher the tunnelling probability.[54] And these trap density also can be affected by the gate voltage (see Figure 4.4(c)). In contrast, at $V_G \leq -30$ V, only holes can be charge carriers (Figure 4.3(c)). These holes pass through the rectangular barrier via DT (see Figure 4.3(b)). Similarly, the interface trap states also assist the tunnelling transport.

(a)

(b) At forward bias, −20 V ≤ V$_G$ ≤ 0 V

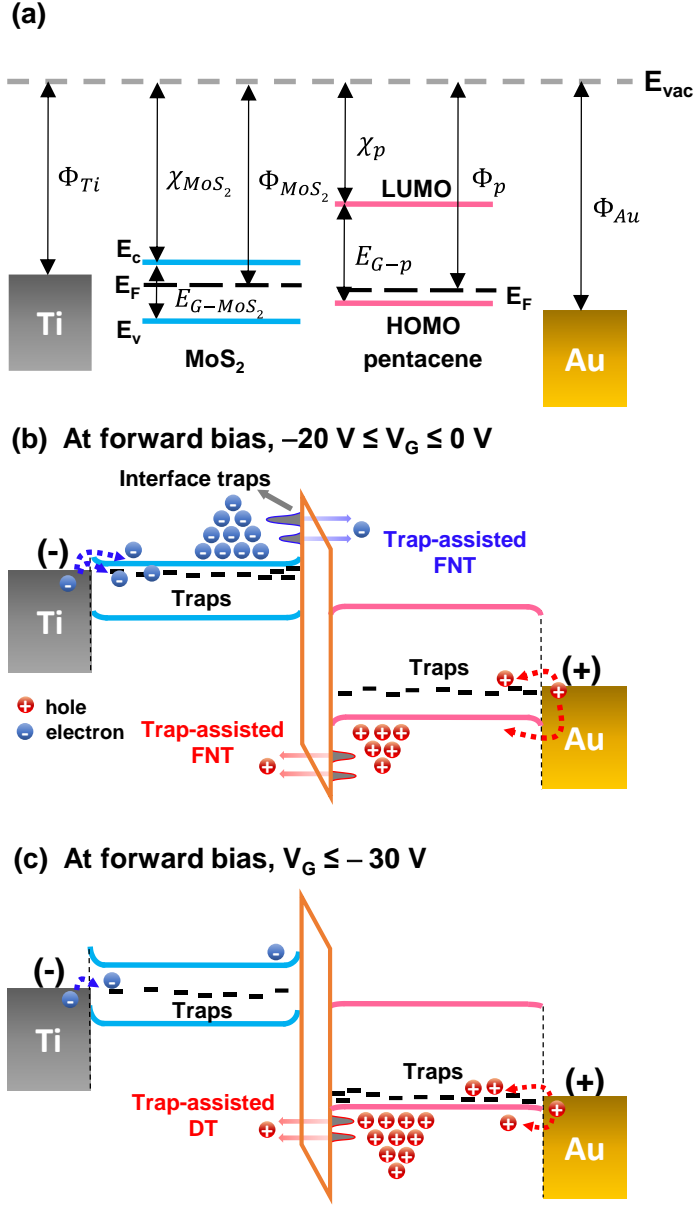**(c) At forward bias, V$_G$ ≤ − 30 V**

Figure 4.8 (a) Energy band profiles of MoS$_2$ and pentacene before contacting each other. (b,c) Energy band alignment of the pentacene/MoS$_2$ p-n junction device in the forward bias condition (b) at −20 V ≤ V$_G$ ≤ 0 V and (c) V$_G$ ≤ −30 V.

4.4. Conclusion

We investigated the electrical properties of pentacene/MoS$_2$ p-n heterojunction diodes at various gate voltages and temperatures. The current and conduction type of the p-n junction devices varied with the gate voltage, and the devices had a gate-bias-dependent large ideality factor. These phenomena resulted from the conduction nature of MoS$_2$ and pentacene with significant trap sites. From the temperature-variable current-voltage characterization, the gate-tunable electrical characteristics of the devices were explained by a space-charge-limited conduction and a variable range hopping conduction at a low temperature. Our study helps in the understanding of the role of traps and the electrical properties of organic/2-dimensional material van der Waals heterojunction devices.

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Chapter 5. Summary

In this thesis, I described the researches mainly focusing on the effect of the disorder originated from the defects on the charge transport of TMDCs. The each of three main chapters of the thesis is devoted to describing the different approaches to investigate the effect of the defect on the charge transport of TMDCs, respectively.

First, I demonstrated the effect of grain boundaries (intrinsic defects) on the charge transport of CVD-grown MoS_2. The *1/f* noise measurements showed that the grain boundaries can be act as a dominant noise source in MoS_2 FET. Furthermore, the *1/f* noise measurement results indicate that the correlated number-mobility fluctuation is dominant noise source at grain boundaries while mobility fluctuation is dominant noise source in single grain region of MoS_2. The percolative noise characteristics of the single grain region of MoS2 were concealed by the noise generated at the grain boundary.

Second, I investigated the effect of molecular dopants (extrinsic defects) in surface-charge-transfer doped WSe_2. I confirmed the reduction of intrinsic mobility of the doped WSe_2 compared to the pristine WSe_2, which is indicating the increased coulomb scattering after doping. Through the theoretical model, I demonstrated that the larger the degree of charge transfer between WSe_2 and dopants, the larger the carrier density generated in WSe_2, but also the larger the degree of Coulomb scattering induced by each dopant counterion. An agreement with DFT calculations corroborated the importance of considering the selective spin transfer as well as the relative frontier orbital positions of the dopant molecules.

Finally, I confirmed the trap-mediated transport in the pentacene/MoS_2 p-n junction device. The van der Waals gap in the pentacene/MoS_2 p-n junction device make a

tunneling phenomenon in the device. The temperature and gate voltage varying measurement showed that a space-charge-limited conduction and a variable range hopping conduction is dominant in charge transport of pentacene/MoS$_2$ devices at a low temperature.

국문초록

전이금속칼코겐 이차원 물질 전계효과 트랜지스터의 불순물에 의한 전기적 특성 변화 연구

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그래핀이나 전이 금속 칼코겐 화합물 물질을 포함한 이차원 물질은 얇다는 특징에서 오는 장점들 덕분에 많은 주목을 받아 왔다. 그래핀의 경우에는 전기적 밴드갭이 없어 반도체 소자로서 이용하기 힘든 반면에, 전이 금속 칼코겐 화합물들은 두께에 따라 바뀌는 밴드갭 때문에 차세대 소자로서 각광 받고 있다. 특히 반도체 성질을 가지는 전이 금속 칼코겐 화합물의 경우에는 높은 온/오프 전류비, 높은 이동도, 낮은 문턱 전압 이하 스윙값 등 전계효과 트랜지스터로서 좋은 성능을 보여준다. 이러한 이유로, 다양한 분야에 소자로 활용하기 위해 많은 연구가 활발히 진행되어오고 있다. 하지만 전이 금속 칼코겐 화합물의 경우에는 그래핀과는 다르게 많은 고유결함을 가지고 있기 때문에, 이론적으로 예측된 성능보다 아직 모자란 값들을 보여주고 있다. 게다가, 이차원이라는 구조적 특성 때문에 표면에 붙은 흡착물들 또한 불순물로 작용할 수 있다. 이러한 점으로 볼 때, 차세대 나노 전자 소자 구현에 있어서 결함이 전이금속 칼코겐 화합물의 전자 수송에 어떠한 영향을 주는지에 대한 연구가 필수적이다.

이러한 측면에서, 본 학위논문에서 첫 번째로 화학 기상 증착법으로 만든 이황화 몰리브덴 전계 효과 트랜지스터의 전기적, 노이즈 특성이 결정 입자 경계에 어떠한 영향에 받는지에 대해 논하고자 한다. 이황화 몰리브덴을 다양한 분야에 소자로 활용하기 위해서는, 대면적으로 합성할 때 필연적으로 만들어지는 결정 경계의 효과에 대한 이해가 필요하다. 이를 위해 전기적 측

정과 노이즈 측정을 이용하여 결정 경계가 전하 수송을 방해하고 전기적 노이즈를 발생시키는 요인이라는 것을 확인했다. 이러한 결정경계에서 발생한 노이즈는 단일 결정에서 발생한 노이즈와 발생 원인이 다르다는 것을 밝혀냈다. 또, 결정경계에서 발생한 노이즈는 단일 결정의 네트워크 전하수송의 네트워크 경향을 가린다는 것 또한 확인 할 수 있었다.

두 번째로, 텅스텐 셀레늄 화합물 전계 효과 트랜지스터의 분자 마다 다른 대전된 불순물에 의한 산란에 대하여 기술하고자 한다. 일반적으로, 전하 교환에 의해 생기는 도펀트 이온들은 물질의 이동도를 감소시킨다. 도핑 후에 저온에서 텅스텐 셀레늄 화합물의 이동도가 감소하는 것을 확인했는데, 이는 앞에서 언급한 것처럼 도펀트 이온들이 산란을 일으켜 이동도를 감소시킨 것이다. 이러한 특성을 이론 모델과 밀도 함수 이론 계산을 통해 분석하여, 분자 마다 다른 도펀트 이온들에 의한 산란 정도를 확인 할 수 있었고 전하 교환 특성의 미시적인 원인을 알아 볼 수 있었다.

추가적으로, 전이 금속 칼코겐 화합물 물질은 아니지만, 유기 반도체 물질인 펜타센과 이황화 몰리브덴으로 이루어진 p-n 접합 소자에서의 trap에 의한 전하 수송 특성에 대한 연구도 기술하고자 한다. 물질과 물질이 결합하면 물질 사이의 표면에 trap 상태들이 생길 수 있다. 이러한 표면의 trap 상태들에 의한 펜타센/이황화 몰리브덴 p-n 접합 소자의 전하 수송 특성이 space-charge-limited conduction의 특징이라 알려진 경향들과 잘 일치 하는 것을 확인 하였다. 게다가 펜타센/이황화 몰리브덴 p-n 접합 소자가 저온에서는 variable range hopping transport의 경향을 보이다가 점점 온도가 올라 갈수록 thermally activated transport로 변하는 것을 확인 할 수 있었다.

Keywords: 이 차원 물질, 전이 금속 칼코겐 화합물, 이황화 몰리브덴, 텅스텐 셀레늄 화합물, 결정 경계, 1/f 노이즈, 표면 전하 교환 도핑, 쿨롱 불순물 산란

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감사의 글

　　대학을 졸업하고 새롭게 대학원에 입학했을 때가 엊그제 같은데 어느새 학부 4년의 거의 두배의 시간인 7년의 시간을 마치고 제가 대학원을 졸업하게 되었습니다. 7년 동안 정신없이 학교를 다니다 보니 어느새 졸업을 할 때가 되었다는 느낌을 받지만, 돌이켜 생각해보면 대학원에서 제가 주변에서 많은 좋은 사람들을 만나서 많은 경험을 하고 새로운 것들은 많이 배워 개인적으로 성장을 할 수 있는 시간 이였던 것 같습니다. 또 대학원 기간 동안 힘든 시간이 많았는데, 많은 분들의 도움을 받아서 이겨내고 졸업까지 올 수 있지 않았나 라는 생각이 듭니다. 평소에는 제가 이런 감사의 말을 잘 전하지를 못했지만, 이 기회를 빌어 저의 박사학위기간 동안 도움을 주신 많은 분들께 감사의 말씀을 전하고 싶습니다.

　　가장 먼저 지도 교수님 이신 이탁희 교수님께 감사드리고 싶습니다. 교수님의 지도 덕분에 제가 하고 싶은 연구를 하면서 즐겁게 연구하며 대학원 생활을 할 수 있었던 것 같습니다. 7년의 대학원 기간 동안 교수님께서 보여주신 행동을 통해 연구적으로나 인격적으로 많은 부분을 배울 수 있었습니다. 언제나 교수님을 본받고 부끄럽지 않은 제자가 되도록 하겠습니다.

　　그리고 오랜 시간 동안 함께 열심히 놀기도 하고, 열심히 머리 맞대고 고민하면서 같이 연구를 하며 즐거운 대학원 생활을 만들어 준 MNE 사람들에게도 감사의 말씀을 전하고 싶습니다. 기훈이 형, 형이랑 같이 연구하면서 많은 점을 배울 수 있었습니다. 말로 다 표현하기는 힘들지만 저의 고민을 같이 고민해주시고 신경 써 주셔서 언제나 감사하게 생각하고 있습니다. 도핑 프로젝트를 좀 더 빨리 끝내서 더 많은 연구를 할 수 있었으면 좋았을 텐데 아쉽네요. 교수 임용 축하드리고 앞으로도 좋은 연구 많이 하시길 바랄게요. 경준이 형, 형의 추천 덕분에 MNE에도 들어 올 수 있었고, 형의 냉철한 일침이 아니였으면 대학원 기간 동안 제가 연구를 잘 할 수 있었을까 싶네요. 앞으로 한국에서 MNE사람들과 좋은 연구 해서, 원하는 바를 이루시면 좋겠네요. 우철이 형, 형과 MNE 사람 중에 가장 긴 시간을 함께 있었는데, 형 덕분에 대학원 생활이 즐거웠습니다. 형은 앞으로 무슨 일을 해도 잘 하실 거라 생각이 들어 앞으로가 기대됩니다. 화이팅 입니다. 준우 형, 형 덕분에 퇴근길에 너무 편하게 다녀서 언제나 감사했습니다. 가끔은 짓궂은 장난도 치시지만, 게임 메이트도 해주시고 저와 잘 놀아주셔서 대학원 기간을 즐겁게 보낼 수 있었던 거 같습니다. 형도 남은 대학원 기간 잘 보내셔서 졸업 하시고, 앞으로 원하시는 것 이루셨으면 좋겠네요. 지원 누나, 언제나 주변에 밝은 에너지를 주시고 제가 시답지 않은 말을 해도 잘 받아 주셔서 감사했습니다. 앞으로도 MNE를 밝게 해주시고 졸업까지 잘 하셨으면 좋겠네요. 이제 방장이 된 재영이, 처음에 MNE에 왔을 때는 잘

할 수 있을까 걱정도 했고 한 때의 사건이 있었지만, 이제는 조금의 걱정이 들지 않을 정도로 든든하다. 앞으로 대학원 생활 마무리 잘 해서, 원하는 바를 이뤄 가기를 바래. 311호에서 나랑 잘 놀아준 희범이, 내가 아무 말이나 해도 잘 받아줘서 고마워. 희범이도 지금 하는 연구랑 대학원 생활을 잘 마무리 해서, 원하는 진로를 잘 찾을 수 있으면 좋겠네. 민우는 지금 격동의 시기를 보내고 있는데, 나도 그 시기를 보낸 입장으로서 안쓰럽다. 잘 해결 되어서 즐거운 대학원 생활을 다시 이어갈 수 있기를. 종우는 내가 맨날 스타 한다고 자리 뺏어 써서 미안 했어. 지금 민우의 자리를 잘 채워서 앞으로 MNE의 핵심인 분자 팀의 기둥이 되어줘. 종훈이 형, 연구, 가정, 스타 모두를 잡는 형의 모습을 보면서 언제나 제 자신을 반성하고 많이 배운 것 같습니다. 저와 잘 놀아 주셔서 언제나 감사드리고, 앞으로 남은 대학원 생활 잘 마무리 하셨으면 좋겠습니다. 준태는 내가 언제나 미안한 감정을 가지고 있어. 내가 괜히 첫 주제부터 힘들 걸 줘서 고생하고 있는데, 내가 잘 못 알려주지 못해서 미안해. 그래도 준태가 꾸준히 잘 하고 있어서 잘 마무리 할 수 있지 않을까 싶다. 준태는 아직 졸업하려면 많이 남았지만, 그 기간 동안 많이 배우고 즐겁게 대학원 생활 할 수 했으면 좋겠다. 창준이는 내 대학원 신입생 시절을 보는 것 같아서, 내가 좀 괴롭히고 있는데 힘들지는 않았지? 창준이도 준태랑 같이 대학원 생활 하면서, 서로 시너지를 내서 좋은 결과 있기를 바랄게. MNE에서 가장 열심히 연구하는 경윤아, 경윤이를 보면서 언제나 게으른 나 자신을 반성 했던거 같아. 경윤이는 이렇게만 하면 원하는 결과를 얻을 수 있을거야. 앞으로 좋은 소식을 기대할게. 그리고 똑똑한 준석이, 준석이를 보면서 물리에 대한 열정을 잃지 않을 수 있었던 거 같아. 내가 이상한 얘기 해도 들어줘서 고맙고, 앞으로 MIT에서 하고 싶은 연구 마음껏 할 수 있기를 바라. 먼저 졸업 하셨지만, MNE에 처음 들어왔을 때부터 많은 도움을 주신 태영이 형, 영걸이 형, 진곤이 형, 현학이 형, 진수 형, 영록이 형, 대경이 형, 연식이 다들 감사드립니다.

KIST에 계신 정승준 박사님과 인호 형 에게도 감사드립니다. 승준 박사님, MNE에 계실 때, 제가 영어에 집중 하느라 같이 일은 하지 못했지만 박사님께서 연구에 대해 많이 가르쳐 주시고 신경 써주셔서 언제나 감사하게 생각하고 있습니다. 앞으로 좋은 연구 하시기를 바라겠습니다. 인호 형, 거의 신입생 때부터 MNE에서 만난 것 같은데 그 동안 오실 때 마다 유쾌한 에너지를 주셔서 감사했습니다. 앞으로 형도 승준박사님의 지도아래 대학원 기간을 잘 마무리 하실 수 있기를 바랄게요.

훈련소에서 만난 진하에게도 감사하다는 말을 전하고 싶습니다. 대학원 신입생 때부터 알았으면 좀 더 같이 잘 놀 수 있었을 거 같은데 아쉽다 진하. 지금 내가 포닥 지원 하는데 조언을 아끼지 않아줘서 너무 고맙다. 지금 준비하고 있는 연구 자연에 성공적으로 마무리 해서 목표를 이룰 수 있기를 바랄게.

그리고 학교안에만 있던 대학원생을 종종 학교 밖으로 끄집어 내서 함께

놀아준 국연 사람들에게 감사의 인사를 하고 싶습니다. 대학원 신입 일 때도 불려가서, 연주회에서 피리 불던 때가 엊그제 같은데 어느새 졸업을 하게 되었네요. 한솔이 형, 남중이 형, 남윤누나, 재원이, 구, 상화, 아령이, 정원누나, 선재, 현희 모두 감사합니다. 또 이제는 다들 자기의 길을 가느라 명절 때 밖에 못보는 완산고 친구들에게도 감사의 말을 전하고 싶습니다. 볼 때마다 고등학교 때의 생각이 나서 그 때의 기운을 받고 지쳐 있을 때 마다 힘을 받을 수 있었던 것 같아. 찬이, 민중, 상용이, 중건, 정현 (둘은 이름으로 부르기 굉장히 어색하다;;) 모두 고마워.

그리고 제가 아무것도 모르던 고등학교 때 물리를 공부한다고 했을 때, 말리지 않고 네가 하고 싶은 것을 하라며 물심양면으로 지원해주고 언제나 따뜻한 눈으로 지켜봐 주신 아버지, 어머니, 동생 재철이 에게도 감사하다는 말을 전하고 싶습니다. 아빠, 엄마가 아니였다면 어떻게 여기까지 왔을까 싶어요. 매일 같이 아들을 걱정하며 밤에 전화를 해주시는 엄마에게 사랑한다는 말 한마디 잘 못하는 무뚝뚝한 아들이지만, 엄마 아빠를 언제나 생각하고 사랑한다는 말을 전해 드리고 싶어요. 감사합니다 어머니 아버지. 동생 재철이는 어느새 의젓해서서, 형 보다 먼저 사회 생활을 하고 있다는 게 너무 기특하고 대견하다. 앞으로 네가 원하는 삶을 살아가기를 바랄게. 언제나 저를 너무 챙겨주셔서 죄송한 마음뿐인 할머니에게도 감사하다는 말씀을 전하고 싶습니다.

마지막으로 은기에게 감사의 말을 전하고 싶습니다. 은기야, 대학원에 입학하면서 만나기 시작 했는데, 어느새 7년의 시간이 지나 박사 졸업을 하게 되었네. 나의 대학원 기간 동안 함께 해줘서 고마워. 힘든 시간이 있으면 은기한테 하소연 하고, 은기의 위로를 받으며 대학원 생활을 잘 버티면서 마무리 할 수 있었던 것 같아. 은기도 지금 중대한 기로에 서 있는데, 은기는 잘 해낼 수 있을 거라 믿어. 우리 지금까지 해왔던 것처럼, 앞으로도 힘든 일이 있으면 서로 의지 하면서 헤쳐나가 보자. 앞으로도 잘 부탁할게. 사랑해.

미처 언급하지 못한 도움을 주신 모든 분들 에게도 감사의 말씀을 드립니다. 이제 박사 졸업을 하면서 인생의 분기점 앞에 서 있는데, 이렇게 감사한 분들에게 마음을 전할 수 있는 기회가 있어 기쁩니다. 앞으로도 성실하고 모든 것에 감사한 마음을 가지고 살아가겠습니다.