PH.D. DISSERTATION

A DESIGN OF ON-CHIP EYE OPENING MONITOR AT MEMORY FOR INTERFACE TESTING

인터페이스 테스트를 위한 메모리에서
온-칩 아이 오프닝 모니터 회로 설계

BY

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지도교수 김 수 환

이 논문을 공학박사 학위논문으로 제출함

2021 년 8 월

서울대학교 대학원

전기컴퓨터 공학부

이 재 환

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ABSTRACT

A DESIGN OF ON CHIP MONITORING AT MEMORY FOR INTERFACE TESTING

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This paper begins with a discussion on high-speed memory interfacing between DRAM memory and the controller. As the standards for DRAM memory become significantly strict and stringent, reliability between memory controllers and memory has become an important topic between companies.

Memory and memory controller manufacturers and customers attempt to minimize confusion between each other based on standard specification such as the JEDEC specification but conducting all the tests between every controller and DRAM have severe constraints and is almost impossible. In addition, when a problem occurs, unless all performances are monitored to test to correct the problematic part, it will proceed rather indirectly or it will be dependent on modeling.

As the market need for high-speed in DRAM is on the rise, a quick testing method on the DRAM side for the signal quality, which is most important at high-speed, is deemed

necessary. Therefore, this paper proposes a monitoring structure that applies the conventional receiver equalizer on the memory side for a memory interface at high speed and explains the test method.

Based on the assumption that back data closely associated with certain channels, and Inter-Symbol Interference is produced later on and as with the data of statistical significance like bit error rate 10^{-12}, if values for MER can be redefined via mutual agreements, verification process is expected to be much more reliable.

Keywords: Memory controller, memory interface, transceiver, training algorithm, on chip eye monitoring, algorithm, feedback, comparator, strongARM latch, decision feedback equalizer.

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CHAPTER 1 INTRODUCTION

1.1 MOTIVATION

Among with the development of cloud service, Internet of Things, artificial intelligence as shown in Figure 1.1.1, in recent days, programs that support memory controllers such as central processing units and application processors in electronic devices such as computers and smartphones, the needs for Random Access Memory (RAM) which temporarily reads and helps with high-speed processing are increasing. As shown in Figure 1.1.2, it can be proved as evidence of the increasing need for these memories in the total market growth graph.

Figure 1.1.1. Memory trend.

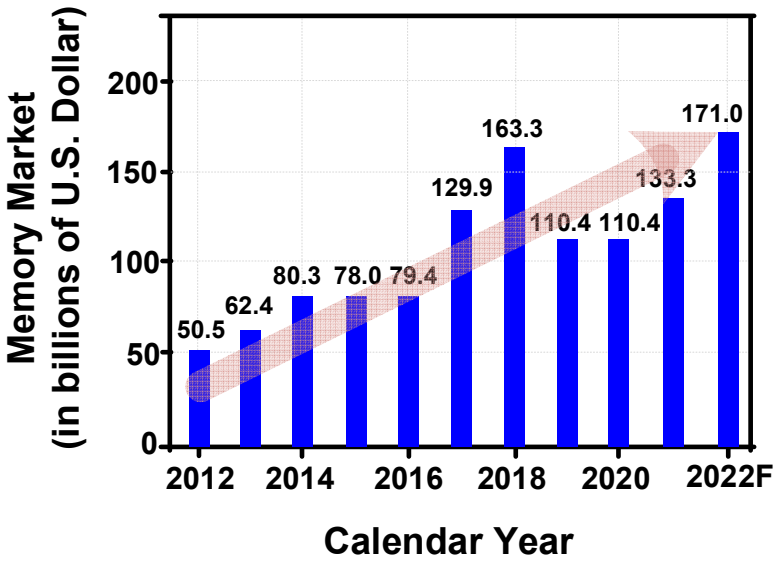


Figure 1.1.2. Total memory market.

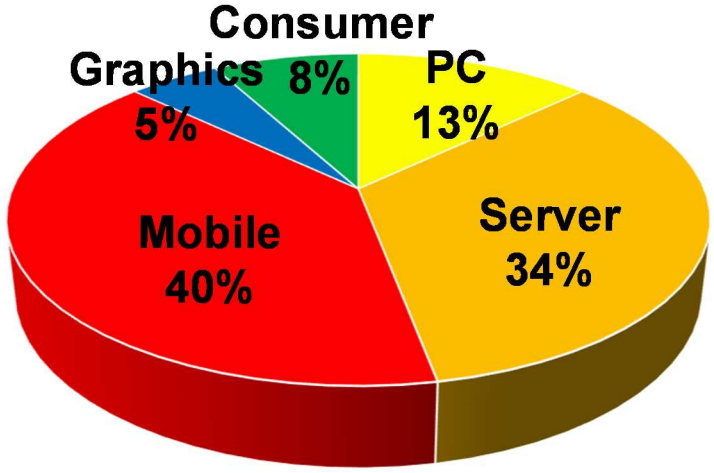


Figure 1.1.3. Penetration rate of DRAM by application, 2020-2021.

According to a survey of which DRAM is the most used in the memory market, by IC Insights, mobile has 40% market share, server and personal computer have 34% and 13% market share for each as shown in Figure 1.1.3. In line with the trend of such a market, the DRAM bandwidth such as LPDDR and DDR also tends to increase steadily as shown in Figure 1.1.4.

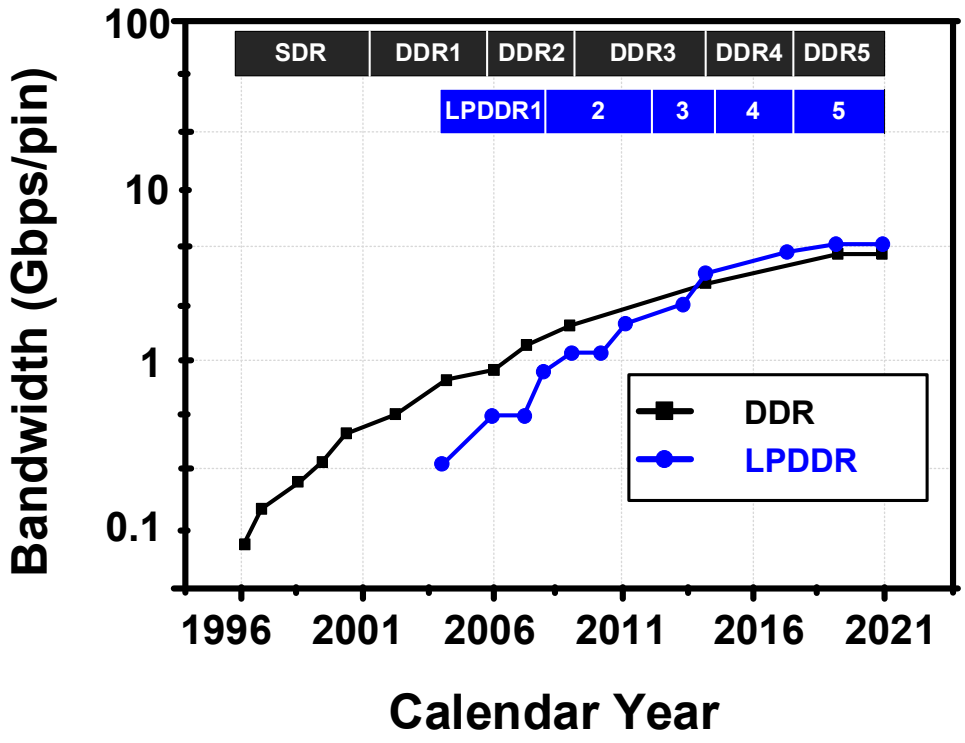


Figure 1.1.4. DRAM bandwidth.

Memory bandwidth is the rate at which data can be read or stored by process in the memory. Therefore, the speed of data and clock sent to the memory by the memory controller are being increased and not only the internal operation but also the high-speed interfacing problem through the channel can greatly affect the overall error.

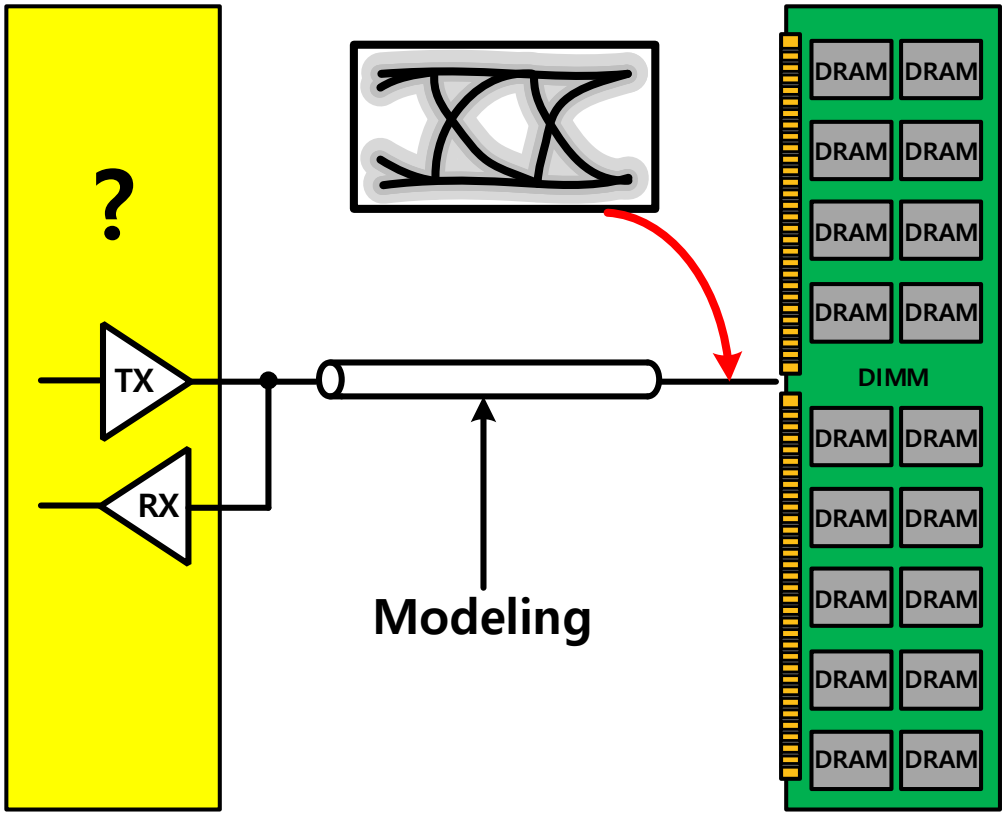


Figure 1.1.5. Memory interface.

In order to solve these interfacing errors, a decision feedback equalizer or a data testing mode between the controller and DRAM using the loop back path is introduced and this can be seen as counterevidence that the interface problem at high-speed can become an obstacle. In particular, signal quality analysis and testing methods will be important by going fast at a memory interface that uses single-ended.

The monitoring technique as shown in Figure 1.1.5 which can quickly grasp the problematic part between the memory controller and DRAM memory is necessary at memory interface on a line that does not degrade the system performance. Therefore, finding a new testing method for memory interfacing only on the DRAM side is the driving factor of this paper.

1.2 THESIS ORGANIZATION

This thesis is organized as follows.

Chapter 2 basically includes the contents that explain eye diagram, on-chip monitoring, receiver and memory background prior to this research.

In Chapter 3, a method for improving the reliability between the memory controller with high-speed for signal that transmitted from memory and a method to detect the interfacing problem of the memory controller on the DRAM side quickly by using the existing 2-Dimensional on-chip monitor and decision feedback equalizer will be explained.

In Chapter 4, the EOM algorithm will be explained and the results of simulation and measurement are implemented and the previous content is finally summarized in conclusion.

CHAPTER 2 BACKGROUND OF HIGH-SPEED INTERFACE

2.1 EYE DIAGRAM FOR HIGH-SPEED INTERFACE

2.1.1 IDEAL EYE DIAGRAM

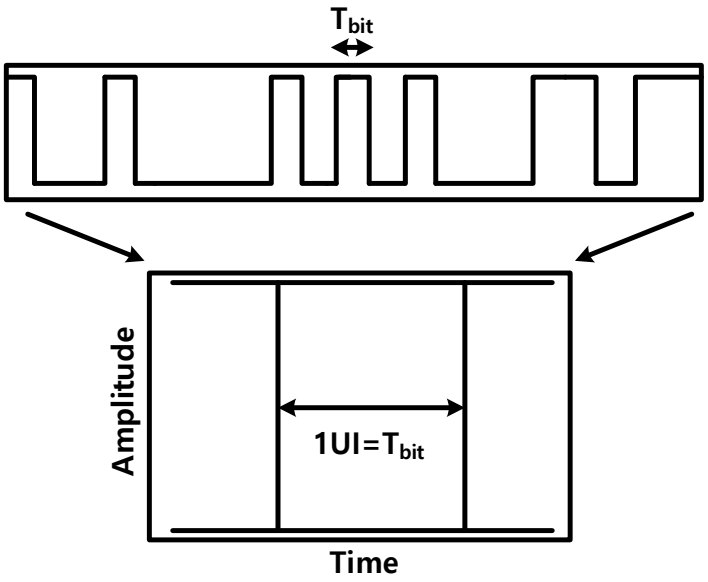


Figure 2.1.1. Ideal high-speed digital signal with eye diagram.

The eye diagram is a clear method to represent and analyze high-speed digital signals. The eye diagram allows quick and accurate grasp of the signal quality and provides direct or indirect information about variables that have a large effect on the data signal based on the position of the eye diagram. This can be used to analyze the most important signals in high-speed link communication and compensate for adverse effects [2.1.1][2.1.2].

The eye diagram is constructed from a digital waveform by folding that parts of corresponding to each bit into single graph with a signal amplitude in the vertical axis and time in the horizontal axis. These waveforms are called eye diagrams because they are similar to the eye shape by repeating and accumulating on the 1bit period T_{bit} standard of data. The eye opening corresponds to a 1-bit period and is typically called the unit interval (UI) of the eye diagram.

Figure 2.1.1 shows an ideal eye diagram. The rising time and falling time of signal has ignored and any information other than 1UI time information cannot be acquired. In real high-speed operation, eye is not opening by 1UI of the signal due to attenuation, noise, crosstalk and etc. It even causes a serious error that eye may be closed. This error is called bit errors [2.1.3][2.1.4].

2.1.2 REASON FOR NON-IDEAL EYE AT HIGH-SPEED LINK SYSTEM

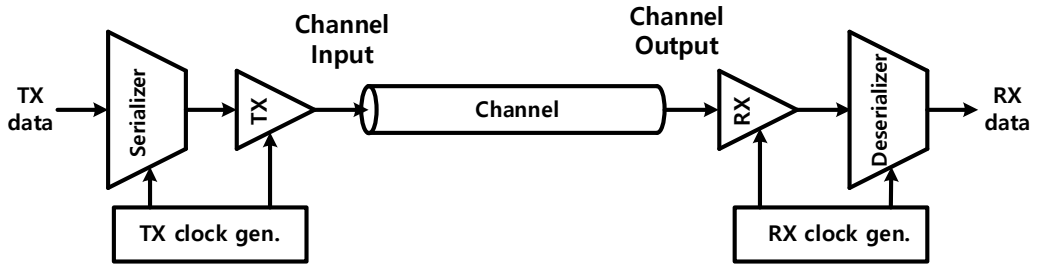


Figure 2.1.2. High-speed electrical link system.

Figure 2.1.2 shows the simplified block diagram of the high-speed link system. The transmitter sends the data to the channel, and the TX clock generator sends data to RX in time with 1 UI timing. At channel output, the receiver performs sampling of the transmitted data, and at the time RX clock generator plays a role of adjusting the sampling time in order to read the information data accurately.

In the high-speed serial link, an important element of signal integrity that we have dealt with is Inter-Symbol Interference (ISI). ISI corresponds to data dependent jitter, and there is a phenomenon in which bit information is leaking by the next number of bits as data advances at high-speed.

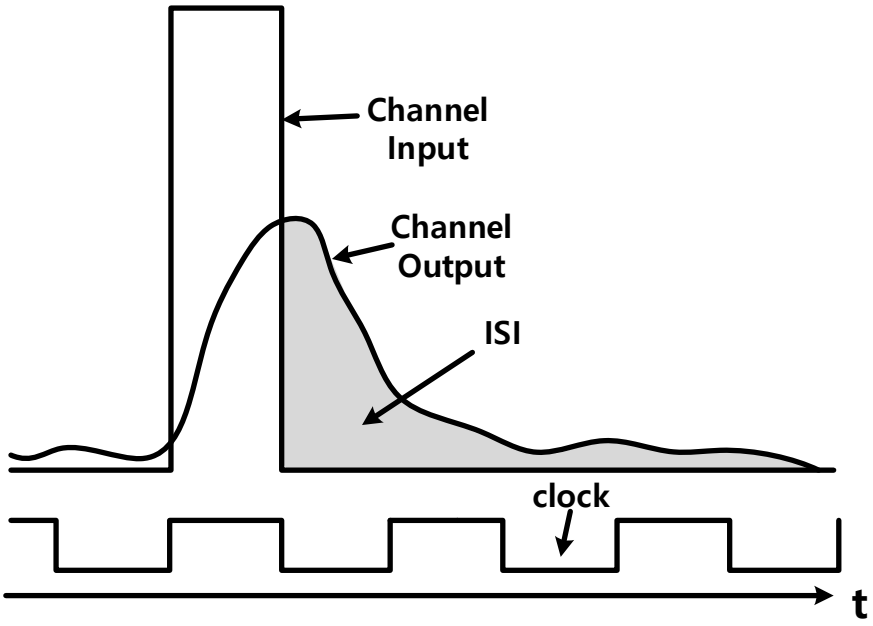


Figure 2.1.3. Channel pulse response at high-speed serial link.

The main cause of the ISI is reflection noise. The signal from the receiver of the channel has a smaller pulse amplitude than the signal at the time of transmission, and some signals of the received signal have fluctuation and lower rising time and falling time. That is, when overlaying the received pulse, it looks like an echo to subsequent bits. These echoes are the result of channel's impedance mismatch. These mismatches cause reflection to move back and forward between channels, degrading the remaining signal quality like a dreg, even after the original bits have passed.

There is also group delay that causes the ISI. This is a phenomenon in which different frequencies are propagated and displayed through different velocities in the same channels. When a single-bit pulse signal is injected into a channel, the continuous pulse is expanded and distributed using several bits. In Figure 2.1.3, the pulse amplitude of the channel output is smaller than that of the channel input, and it spreads much wider and longer to reach the next bit.

Looking at the received waveform that sums the individual pulse response with these ISIs as shown in Figure 2.1.4, even though the next data is 0 next to 1, it is difficult to see the waveform even the next data of 1 is 0 due to the dregs. This serves to cause a serious error, resulting in a situation where the eye is not opened properly.

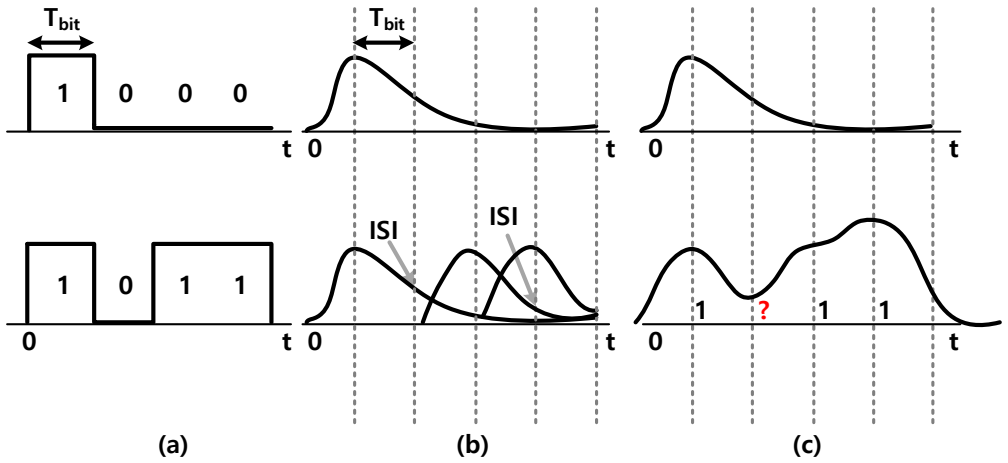


Figure 2.1.4. (a) Channel input (b) individual pulse response (c) received waveform (sum of pulse response).

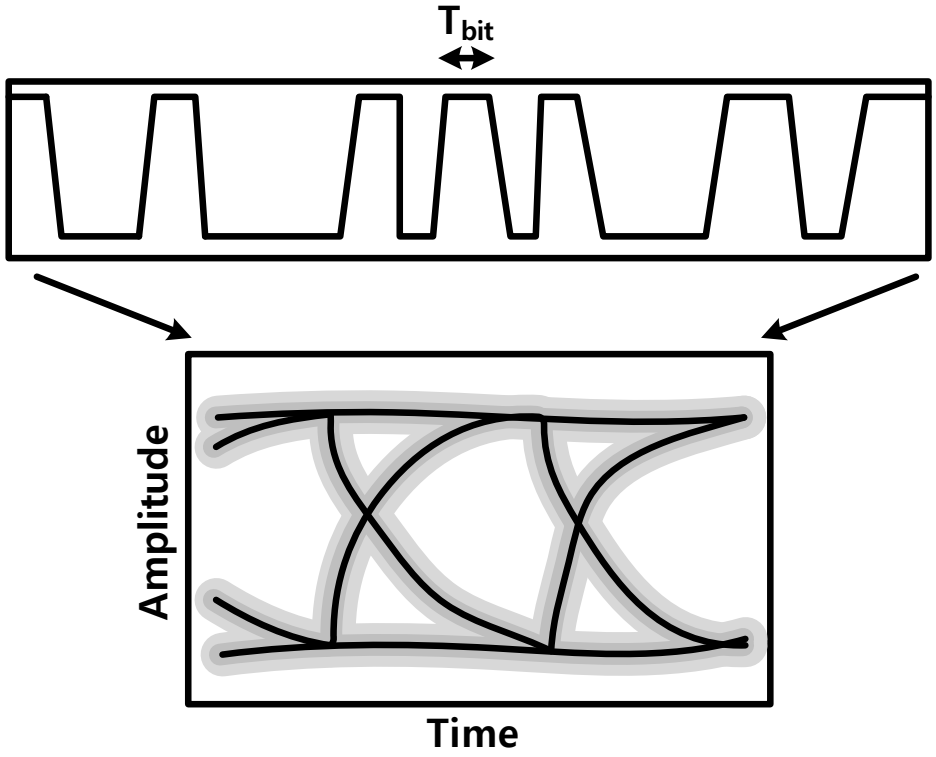


Figure 2.1.5. Typical high-speed digital signal with eye diagram.

In addition to these ISIs, power supply noise, reference clock noise, TX clock generator jitter and crosstalk that can occur in channel, decoupling, etc. can occur in TX. As shown in Figure 2.1.5, the eye shape, which is faster and smaller than the ideal eye shape, can be seen as more common.

2.1.3 INFORMATION FROM EYE DIAGRAM

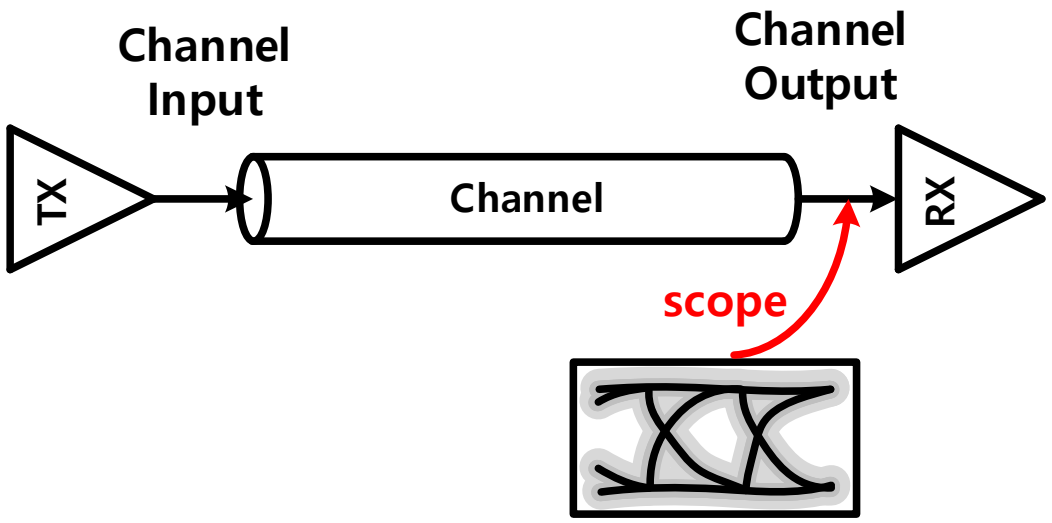


Figure 2.1.6. Typical eye diagram scope position.

Moreover, we should know what information can be obtained by using the eye diagram. Also, we should know whether to scope the eye diagram mainly from any location. As explained earlier, the eye diagram basically confirms the noise that can occur in TX and the problem that can occur from the channel. Therefore, it is typical way to scope after passing through the channel as like in Figure 2.1.6. This is because TX also has the role of allowing RX to receive signals in any channel.

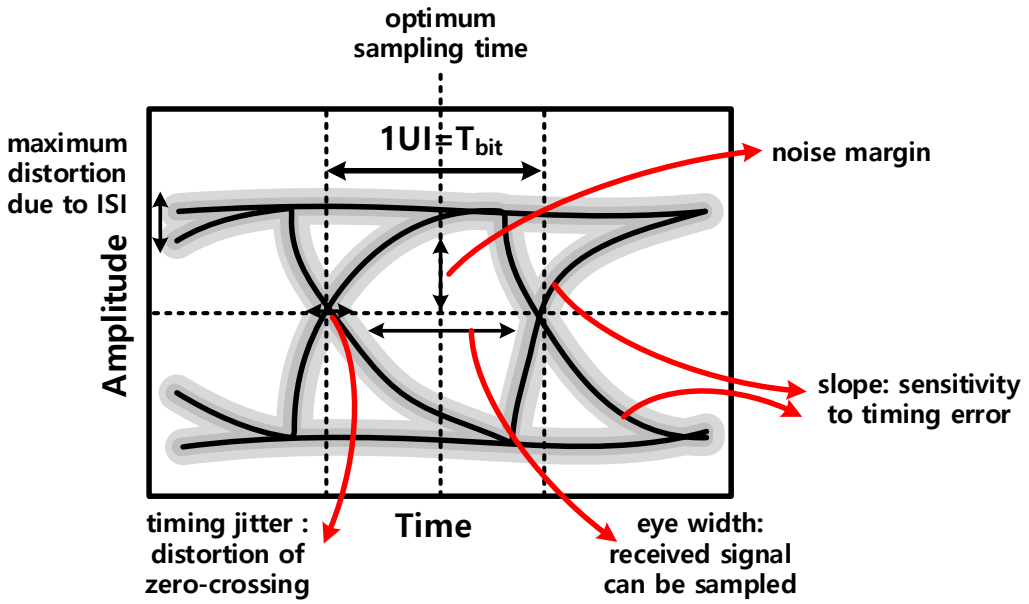


Figure 2.1.7. Eye diagram that can intuitively interpret various noise characteristics.

The purpose of the Eye diagram is to check the status of signal integrity at a glance as shown in Figure 2.1.7. The purpose of eye diagram is that after passing through channels such as maximum distortion due to ISI, optimum sampling time, noise margin, rising and falling slope, the digital signal intuitively provides the results produced by noise and other factors during the bit period. This is used as a method to check the performance of TX or RX is used to receive signal without error.

2.1.4 OFF-CHIP OSCILLOSCOPE EQUIPMENT FOR EYE DIAGRAM

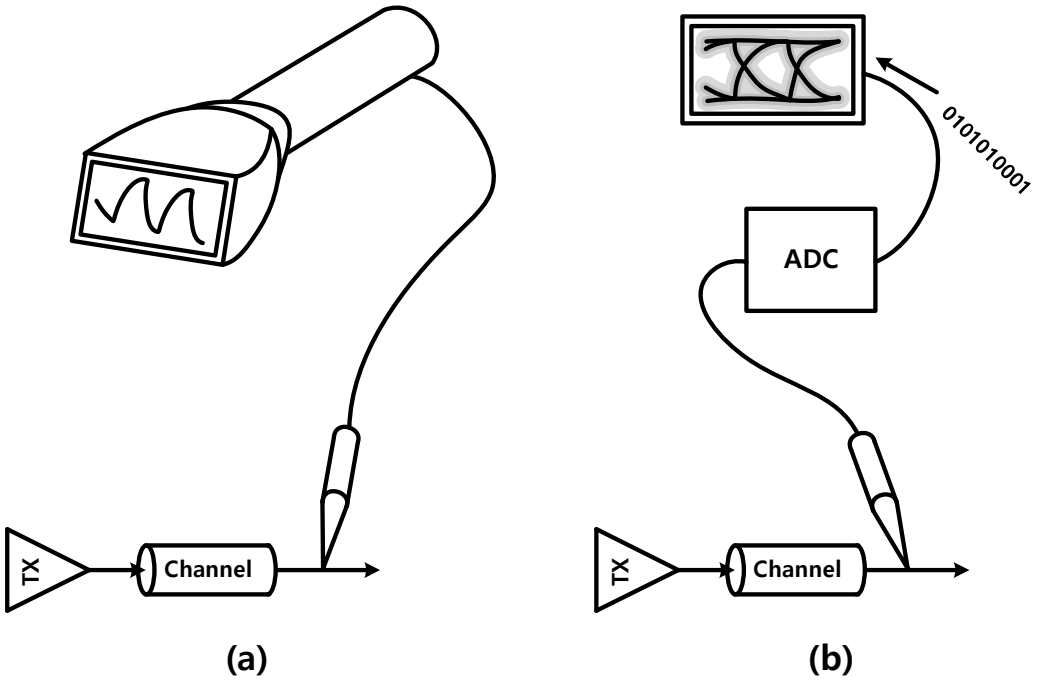


Figure 2.1.8. (a) Analog oscilloscope and (b) digital oscilloscope.

The Oscilloscope is basically an indispensable tool for everyone who designs, manufactures, and repairs electronic devices. It is also an effective tool which shows signal integrity visually. It was often used for the purpose of easily grasping the presence or absence in operation with a low-speed link that emphasizes logic design and logical operation circuits. However, it is important to understand characteristics for unclear signals in the high-speed waveform because the processor clock speed becomes exponentially

faster and there is a lot of noise in the system that requires a high bandwidth in GHz units. Since this can have a direct impact on the period of commercialization and the reliability of the product, more precise analysis is required for channel and noise analysis.

The types of oscilloscope electronic devices can be broadly divided into two categories: analog and digital. Analog devices operate continuously with varying voltages and digital devices operate individual binary numbers that indicate voltage samples. As shown in Figure 2.1.8, analog oscillators can quickly show moving waveforms. The advantage is that the price is low and the information comes out in real time. The disadvantage is that the accuracy falls at high-speed, and it is impossible to grasp the signal characteristics like the eye diagram. On the other hand, the digital oscillator uses an analog-to-digital converter (ADC) and a memory that can store signals to reconstruct the waveform and show it on the screen. At this time, it is easy to grasp and analyze the eye diagram and signal characteristics, and it is mainly used at high-speed.

2.1.5 THE REASON FOR HIGH-SPEED MONITORING WITH ON-CHIP

In recent days, digital systems with increasing complexity and data rates of gigabytes per second are increasing the demand for measurements that are more accurate and easier to implement. With integrated circuit design, the complexity increases due to the tendency of the gradual decrease in the size, and also as the voltage decreases. Accordingly, it is proved that the parasitic effect could not be captured accurately and that the existing RC circuit representation of on-chip interconnects was not accurate when the switching speed was in the multi-GHz range. Existing off-chip measurement techniques are relatively inaccurate, and precision-designed equipment is very expensive and requires a high accurate and delicate platform. A possible approach to avoid these drawbacks is to place the measurement circuit directly close to the circuit on where it is measured [2.1.5].

2.2 ON-CHIP MONITORING

2.2.1 BUILT IN JITTER MEASUREMENT (BIJM) CIRCUIT

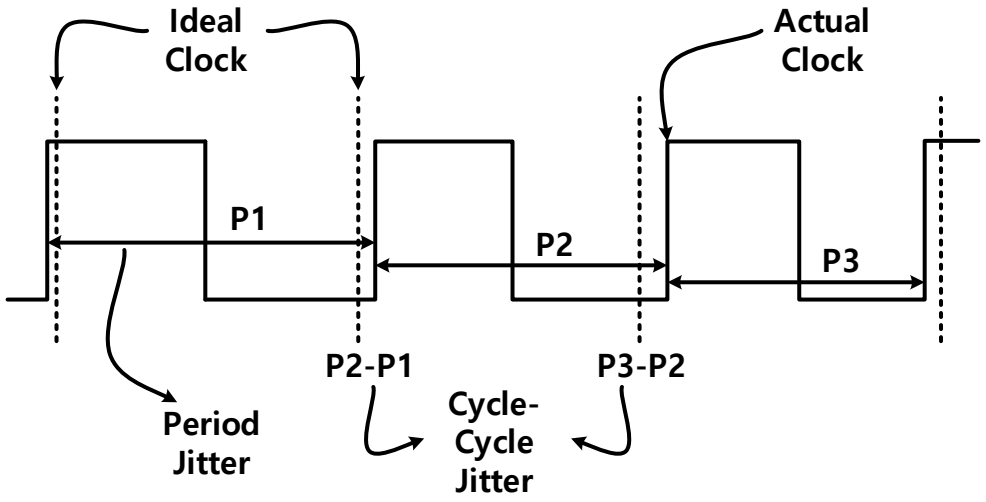


Figure 2.2.1. Analyzing jitter measurement.

Built-In Jitter Measurement (BIJM) is a very useful system for clock jitter analysis. As shown in Figure 2.2.1, Jitter shows the difference between the actual clock and the ideal clock and the jitter is larger, the more error on the data sampling can occur and also it can harm the speed of the data link. Traditionally, clock jitter analysis relies on external equipment such as spectrum analysis, automatic test equipment, and oscilloscopes [2.2.1].

However, as the clock frequency increases, accurate clock jitter measurements become more difficult. Therefore, many BIJM systems have been used to measure on-chip signal jitter distributions and overcome these limitations [2.2.2-2.2.5].

The adjustable delay line structure in the BIJM circuit can measure phase locked loop jitter, especially the on-chip Vernier Delay Line (VDL) structure use the timing difference between delay cells to digitize the tested signal jitter. The difference was used. The VDL structure increases the timing resolution of the BIJM system, but also increases a large area.

An on-chip vernier oscillator structure was used to overcome these increases in area. On-chip Vernier oscillator digitize the tested signal jitter by using the timing difference between Oscillators. The disadvantage is that the testing time increases and the ring oscillator noise accumulates, which can be a source of noise in the BJIM system.

BIJM circuits as above are an effort to measure jitter in ps units on-chip to expand timing resolution at high-speed. However, due to the complexity and large area of the circuit, it is major disadvantage in the design of integrated circuits.

2.2.2 TRANSITION EDGE HISTOGRAM FOR ON-CHIP EYE MONITOR

Transition edge histogram for eye monitoring is analyzed based on data sample edge information. The extracted edge information is used to determine the histogram of the signal transition. The relationship between the vertical opening of the Eye and the transition of the data is not considered, and the data horizontal information is counted using the point that is transitioned at the edge of the eye, and the eye is inferred [2.2.6][2.2.7].

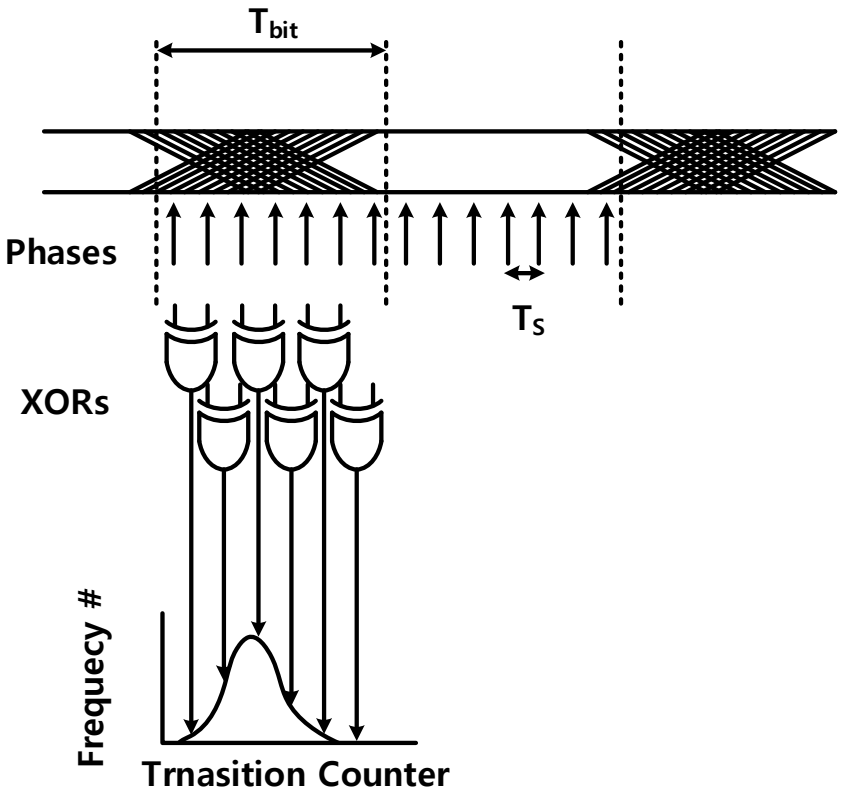


Figure 2.2.2. Concept of the edge histogram analysis.

The edge information extracted from the data sample used to determine the histogram of the signal transition as shown in Figure 2.2.2. Histogram analysis is implemented using XOR gates and compares two consecutive sample steps to detect the occurrence of data migration between them. The number of edges detected between all pairs of two consecutive sampling phases is accumulated by using a counter. The number of conversions is counted at each sampling position to generate an edge switching histogram. The larger the eye opening, the narrower the histogram, and the narrower histogram effectively measures the degree of opening of the eye but there is a limit to obtaining vertical and the entire eye information.

2.2.3 GRIDDED ON-CHIP EYE MONITOR

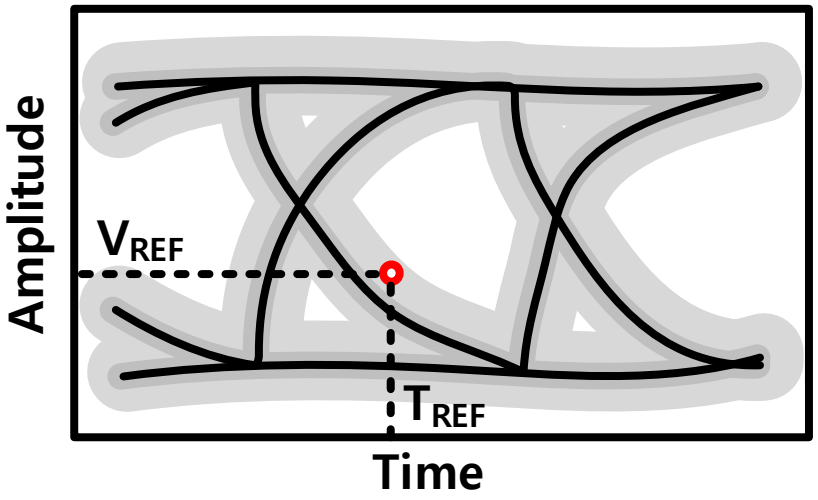


Figure 2.2.3. Gridded eye monitor.

The Gridded on chip eye monitor cannot know the opening of the eye at once, but it is created by sampling multiple grid-like signals and errors and accumulating the eye opening [2.2.8]. Therefore, it requires a large amount of memory and the longest processing time [2.2.9][2.2.10]. As shown in Figure 2.2.3, the point where the phase corresponding to TREF and the voltage level called VREF meet and the data are compared and counted. In general, only one comparator that has the reference voltage and clock in the input is used to compare with the data. It can be called an on-chip monitor that has a relatively simple structure and is the easiest to apply.

2.2.4 1-DIMENTIONAL ON-CHIP EYE MONITOR

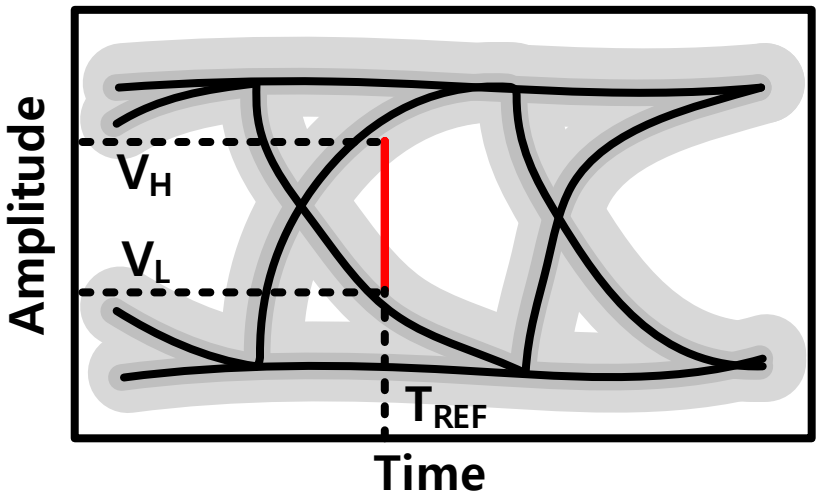


Figure 2.2.4. 1-D eye monitor.

In order to overcome the data processing time which is considered obstacle for Gridded EOM, 1-dimension as shown in Figure 2.2.4 is used instead of a point in the error recognition method which counts error when the data is counted between the voltage levels of VH and VL in the phase of T_{REF} [2.2.11-2.2.14]. While one comparator is added compared to the gridded eye monitor technology, information on vertical eye opening can be obtained quickly, and the testing time can be shortened accordingly. However, there is a drawback that the eye opening itself must be swept in a phase that cannot be confirmed in one UI.

2.2.5 2-DIMENTIONAL ON-CHIP EYE OPENING MONITOR

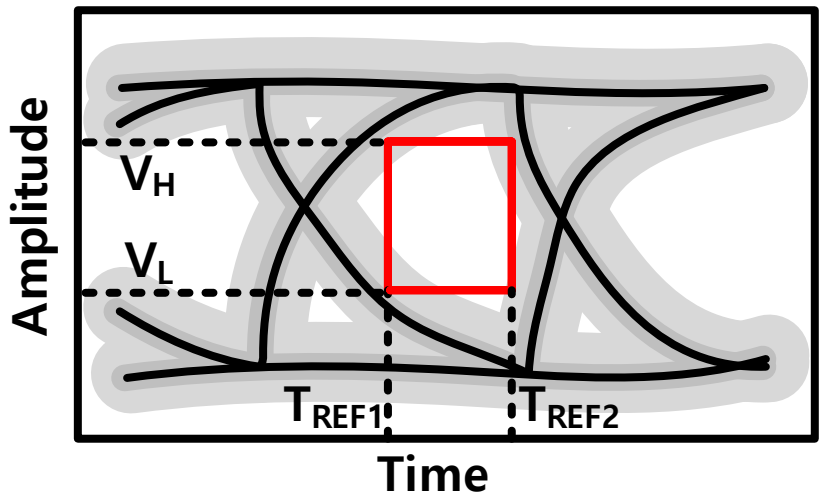


Figure 2.2.5. 2-D eye opening monitor.

Significant information on eye opening can be confirmed in 1UI and eye opening can be inferred more quickly by using vertical and horizontal information. As shown in Figure 2.2.5, counting is performed at each moment when data is recognized as an error that passes between the phase of $T_{REF1}$and T_{REF2} and the voltage level of VH and VL. The difference from the previous eye monitoring is that it can quickly check the information on the actual eye opening. In particular, masking error rate, which is calculated by dividing the error count by total transition can be used to grasp the error such as like bit error rate (BER) [2.2.15-2.2.23].

This part presents the architecture of a prior two-dimensional (2-D) EOM. There are two main parts in the 2-D EOM. The first one is to detect error in the early and late phases by using a circuit called logic retime which is the same as Figure 2.2.6 [2.2.15][2.2.18][2.2.19].

In the case of a MER, its error rate is calculated via estimating frequency of the error_out signal and dividing it by input bit rate, instead of counting the errors as shown in Figure 2.2.7. If this is applied to DRAM side, immediate confirmation of the output of frequency is not possible. Therefore, there needs to be a technique such as frequency detecting same as the time-to-digital converter in order to store frequency information. However, this is not an easy task because there is too much burden on the memory. Thus, we need a technology based on simple error counting that can precisely store error toggle..

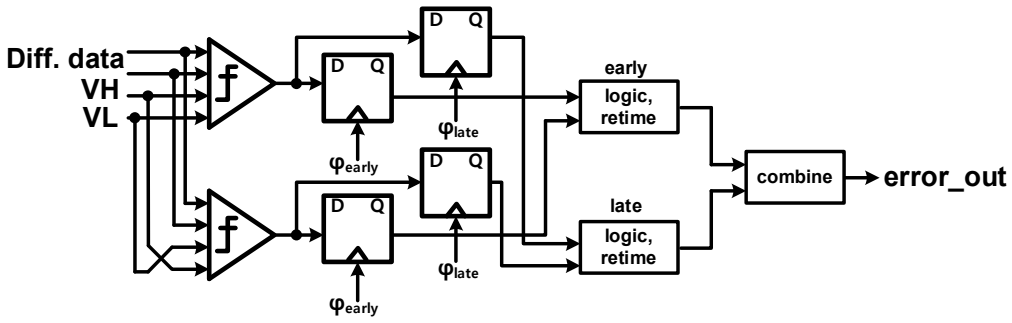
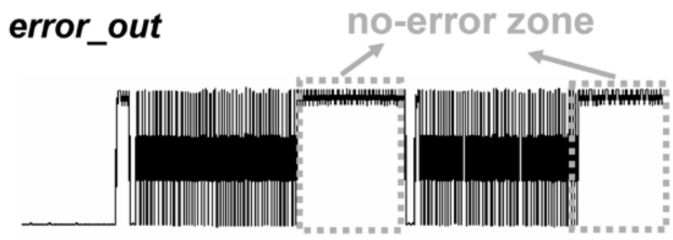
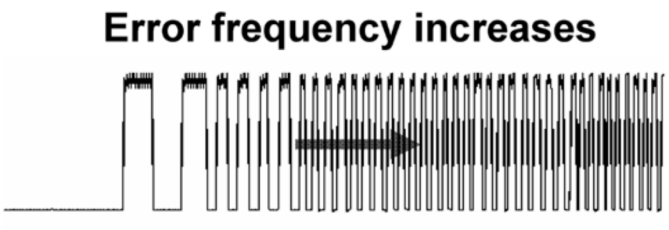


Figure 2.2.6. Prior EOM architecture.



(a)



(b)

Figure 2.2.7. Simulation results (a) (b) Prior EOM architecture.

The second one is architecture that as shown in Figure 2.2.8, it uses clock based comparator and XOR gate. This can calculate error by counting output and its structure is much simpler than the previously explained architecture. It receives different input INP and INN and each VH and VL compares these and uses XOR gate to confirm output. Because this is differential input, symmetric usage of VH and VL can be free of glitch problem depending on the comparator gain. However, glitch problem in memory systems with single-ended signaling may cause error in counting based error [2.2.20-2.2.22].

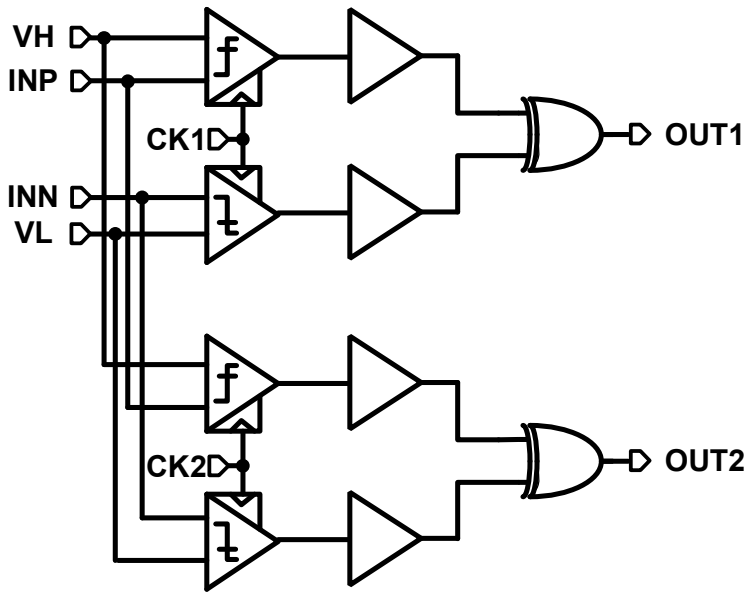


Figure 2.2.8. Prior EOM architecture.

2.3 MEMORY TESTING

2.3.1 WHAT IS DRAM?

Memory semiconductors are broadly divided into volatile and non-volatile memories and the DRAM belongs to volatile memory because DRAM requires continuous power supply to hold data. The purpose of DRAM is to support high-speed processing by reading the program from an electronic device such as a smartphone to the memory controller such as the Central Processing Unit or Application Processor and temporarily storing it at a higher processing speed than non-volatile memory. Because it searches data randomly with the coordinate values, the higher performance of DRAM makes the faster processing speed.

The DRAM cell is a highly economical semiconductor memory storage device that has the simplest structure. The DRAM cell is composed of one capacitor and one transistor. Electrons are stored in this capacitor, which is also called a condenser in other words. If the electron is sufficiently stored, it will be digitally '1', and if the electron is empty, it will be digitally '0'.

Therefore, in order to create a DRAM cell in the smallest area during the DRAM manufacturing process, a capacitor with a 3-dimensional structure is created in a small area and then an electron is put into capacitor and a transistor operates as a switch to take it out again.

One single cell transistor and one single switch are devices that store one bit. Then, the metal of the bit line for data for connecting this and the word line for notifying the

address are arranged in a grid inside the DRAM. These cells form a two-dimensional grid and sense amps, column decoders and row decoders are arranged around them.

Data can be read and written by using these DRAM cells and this information communicate at high-speed using the memory controller and TRX.

2.3.2 CONVENTIONAL MEMORY TESTING

The mutual reliability is most important between the memory controller and the memory. However, this reliability can easily be compromised in the event of an operational error. In order to minimize the malfunctions, mutually agreed promises such as the JEDEC specification is essential to avoid operational errors. However, unlike the document, there are many variables during actual operation, so the testing is important to grasp the cause as the speed increases.

Generally, the simplest and easiest way to test the controller is modeling the DRAM and channel characteristic information to determine if it meets the specific requirement by the DRAM and vice versa when testing the DRAM by modeling the signal which is generated by controller that sends data.

However, considering the possibility that inductance components such as T-coil will be added, especially when going at high-speed, variation and noise become intense. Therefore, accurate and precise modeling is more difficult.

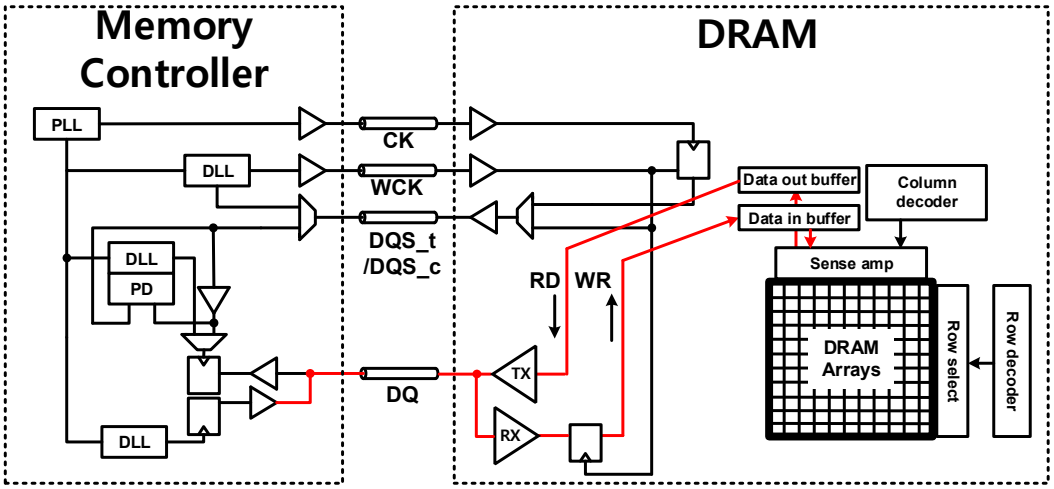


Figure 2.3.1 Conventional memory RD/WR testing method.

Figure 2.4.1 shows pass or fail test based on write and read which is one of the existing memory performance testing methods. The advantage is that it can test for long patterns, but the disadvantage is that the test time takes longer because all timing constraints should be considered during the actual command. Also, since read and write must work through the DRAM Arrays, it is not possible to know exactly whether the DRAM Arrays are the problem or the interface is the problem. The purpose of this paper is to grasp the interfacing problem at high-speed and to determine whether the signal sent by the memory controller is the problem or inside the DRAM is the problem. Therefore, the existing method is not an appropriate testing method.

2.3.3 MEMORY INTERFACE TESTING

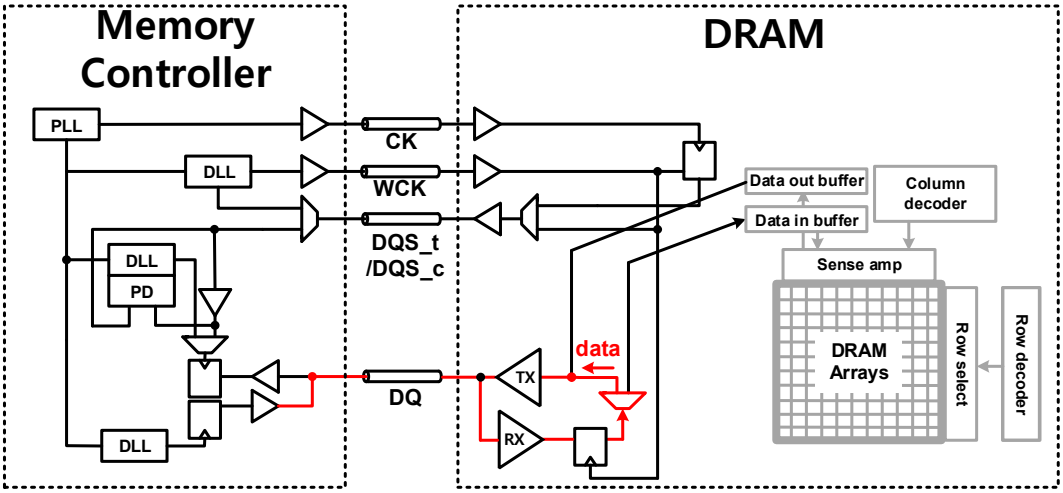


Figure 2.3.2 Conventional testing method for memory interface.

The testing method is the same with previous testing method that both methods' purpose is to test interface's problems but while previous testing method also includes DRAM cell errors, this method can only test performance for interfacing. However, the disadvantage is that it has to pattern match with controller and because the depth is too shallow to store enough pattern for the length the long pattern test is impossible.

CHAPTER 3 DESIGN OF RECEIVER WITH ON-CHIP EYE MONITORING

3.1 DRAM RECEIVER FOR MEMORY INTERFACE TEST

I present a method that quickly detects errors and promptly notifies problems with the interface of the system regardless of the pattern using the conventional test method described above. This allows to check information about sufficiently long data on the DRAM side on-chip and puts in a simple circuit that uses the existing mask error and applies it with a line that does not burden the system.

Figure 3.1.1 is an LPDDR JEDEC specification that defines the minimum eye mask size that is sent to memory from the standpoint of a memory controller. Minimum eye mask has to be guaranteed to read data from DRAM without error. The total mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD.

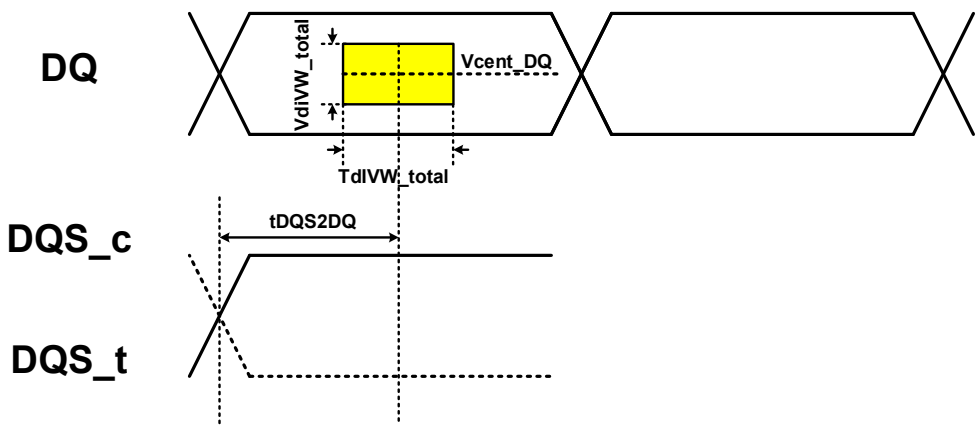


Figure 3.1.1. The DQ input receiver mask for voltage and timing.

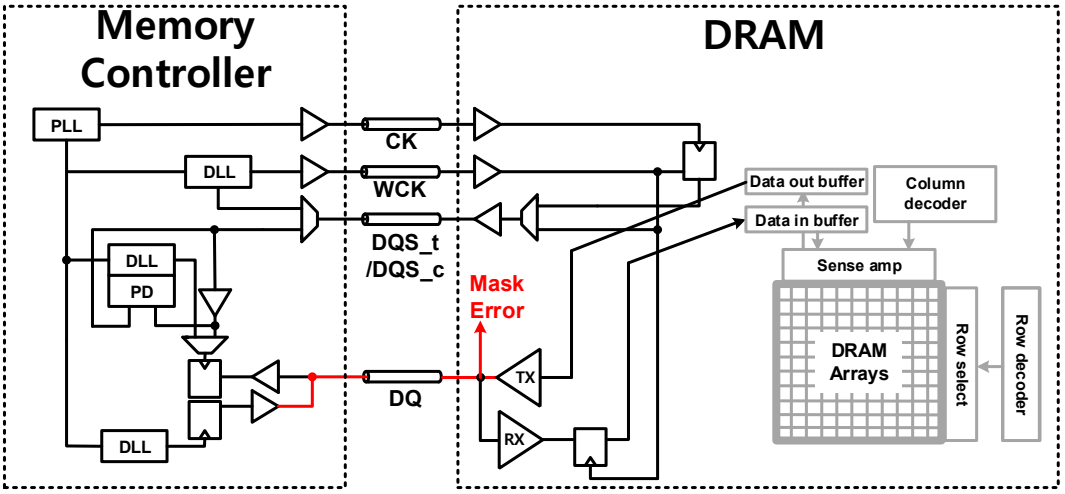


Figure 3.1.2. Proposed testing method for memory interface.

As shown in Figure 3.1.2, to test the actual noise of the eye mask type sent by the memory controller and the memory controller problem due to inaccurate modeling intuitively and quickly, the need for On-chip eye monitoring technology on DRAM-side is recognized and an architecture that applies existing receivers will be provided.

3.2 CONVENTIONAL EOM ARCHITECTURE

Figure 3.2.1 is the conventional 1-D EOM architecture shown in the existing paper. The Conventional 1-D EOM use the comparator to compare the data with VH, VL, and clock, and set them to the clock to obtain the respective outputs. Then toggles error by XOR the difference between the two. In other words, data operates according to the time when the clock is entered, and when data exceeds the voltage level between VH and VL, it is regarded as an error. That is, when passing through one dimension, it is recognized as an error, and VH and VL have a voltage level difference.

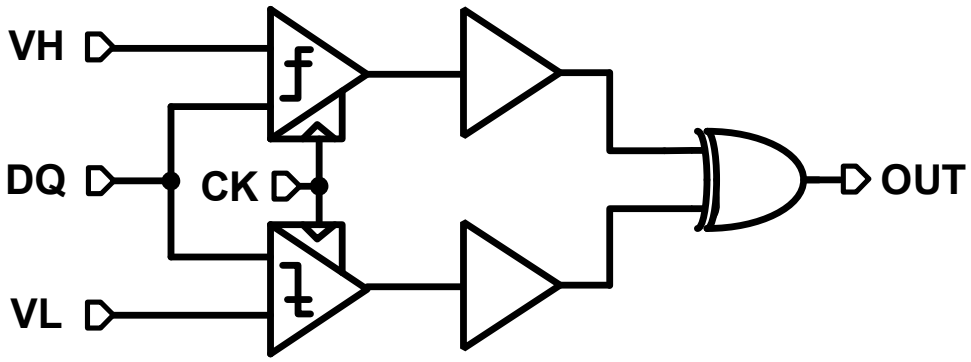


Figure 3.2.1. Conventional 1-D eye opening monitor architecture.

In general, when the comparator operates at high-speed, it uses strongARM latch comparator, and the XOR output is 1 when data passes through 1 dimension as shown in Figure 3.2.2. Therefore, it can be said that in case of output 1 is counting a lot, that means the dimension has high rate of error and in case of output 1 is counting few, which means the dimension has low rate of error. By using two sets of these 1-dimensional EOMs could implement a 2-dimensional EOM with an XOR mean.

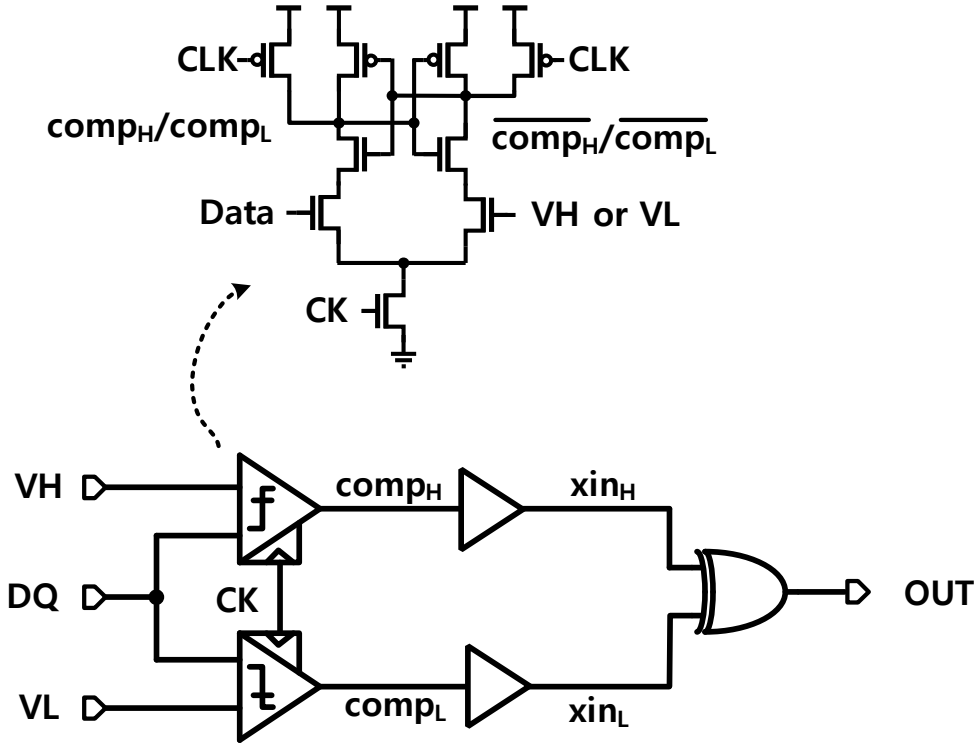


Figure 3.2.2. Conventional 1-D eye opening monitor with strongARM latch comparator.

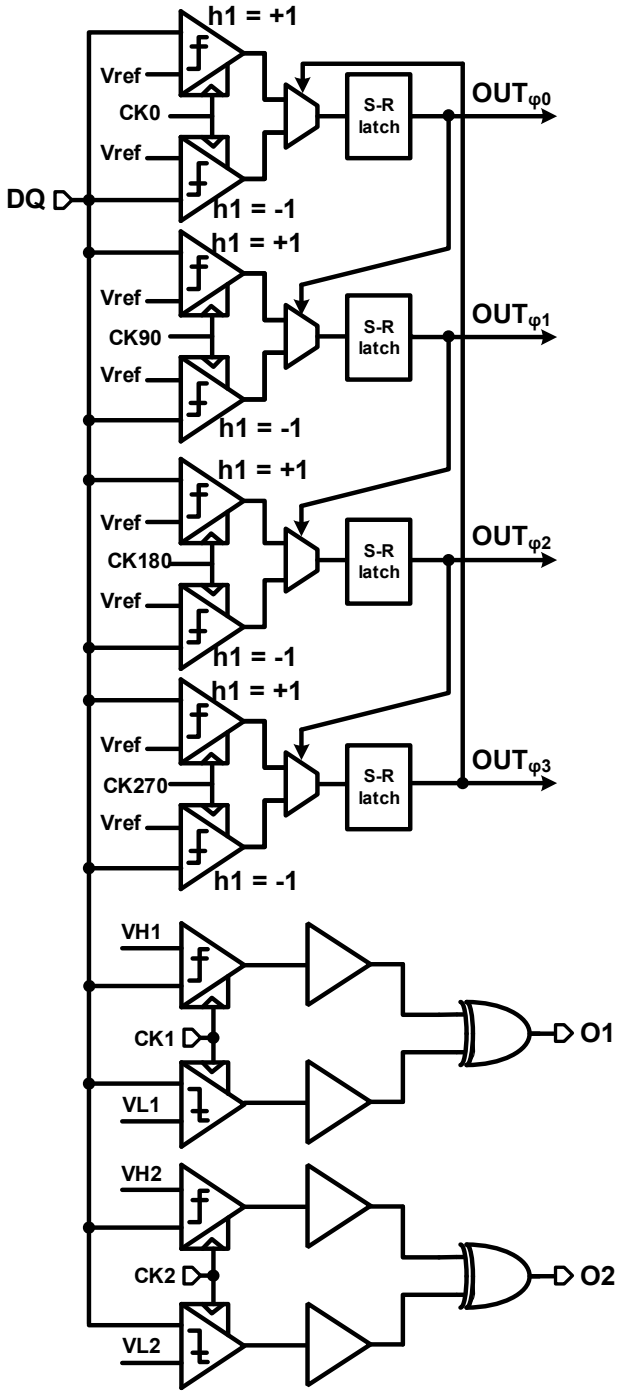


Figure 3.2.3. Memory equalizer with 2-D EOM architecture.

Decision feedback equalizer and 2-D EOM could be designed as shown in Figure 3.2.3. However, when using the on-chip EOM method with a rectangular mask with two reference voltages and two phases, it causes capacitance I/O (C_{IO}) on the four additional comparator receiver inputs, which seriously causes a decrease in signal quality at high-speed. Therefore, this chapter proposes a receiver with re-useable eye opening monitor by relaxing C_{IO}. The receiver has a clock generator and DFE with the eye monitoring technique for its signal quality.

When the receiver input has an additional circuit in the memory of the single-ended input, it becomes relatively vulnerable due to noise and ISI compared to the differential. In addition, the additional circuit will increase the C_{IO} which is DRAM bit capacitive load. The C_{IO} value and range are specified by the JEDEC standard committee, but the required specification is getting lower and lower in LPDDR5 compared to the LPDDR4X which is the previous standard. When the C_{IO} increases the charge and discharge times also increase, so the eye opening decreases. The results of the analysis show that the UI was reduced 2% each time when the C_{IO} increased by 0.1pF [3.2.1].

Despite increase of the C_{IO}, the eye shape inside the chip provides us a lot of information such as reference voltage, noise, and eye opening. Therefore, adding one comparator to the single input in the existing memory to implement on-chip eye monitoring [3.2.2] or drawing a shmoo with using one existing receiver comparator could make infer the eye form possible [3.2.3] [3.2.4]. However, while the method of using one comparator or drawing shmoo with an existing comparator has advantage that detailed information can

be obtained, it requires a large amount of processing time [3.2.5] [3.2.6].

Therefore, I applied 2-D EOM to single-ended input, which uses different reference voltages and two different phase information to determine whether an error is passed and if such error is in the rectangular shape. In addition, if four comparators are added, the increase in C_{IO} will cause a loss in terms of UI, so I will provide a solution for this problem.

3.3 PROPOSED RECEIVER

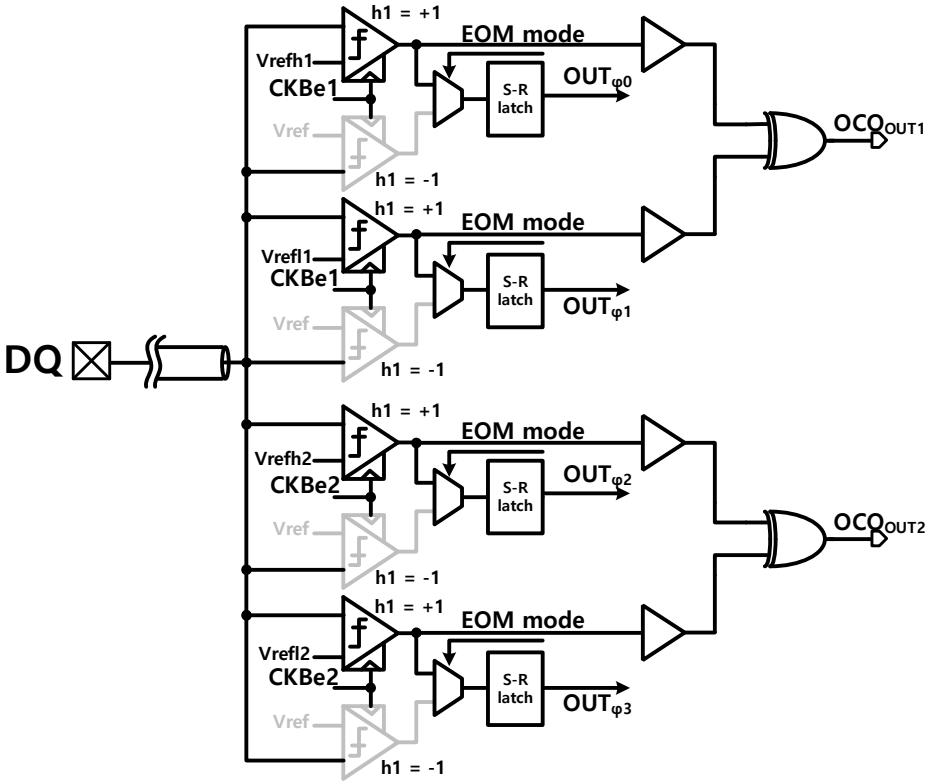


Figure 3.3.1. Combined equalizer and EOM.

As shown in Figure 3.3.1, re-using the comparator in loop-unrolling DFE enables appliance of an on-chip EOM without an additional circuit and use of a rectangular mask is the simplest and easiest algorithm. However, if the DFE comparator immediately has a buffer and an XOR gate on the backend, the size will be increased to maintain the same comparator gain, which will cause an additional C_{IO}. Therefore, after SR-latch, add an AND

gate of D-flip flop and toggle to solve this.

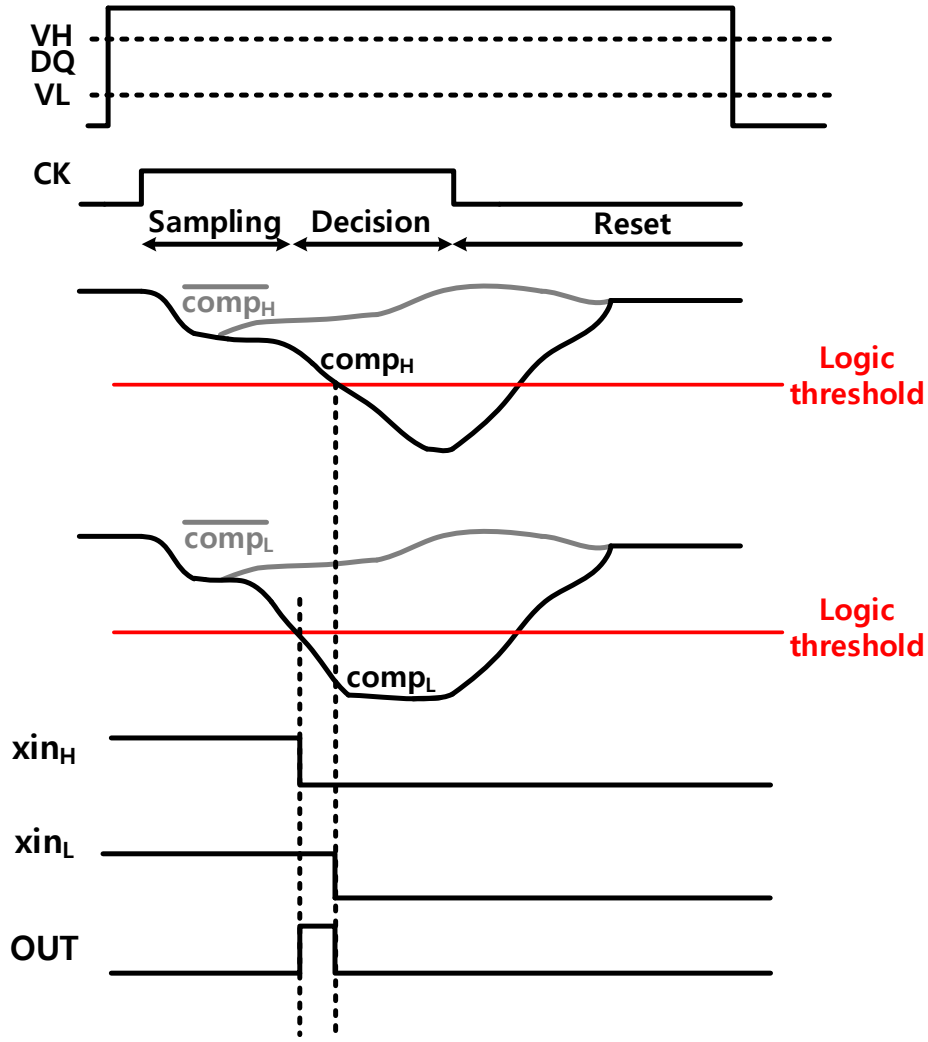


Figure 3.3.2. StrongARM latch comparator of EOM operation phase.

The advantage of using the SR-latch backend used in the loop-unrolling DFE could reduce glitch. The comparator at high-speed has different strengths based on VH and VL of different thresholds, and as shown in Figure 3.3.2, glitch that should not occur in XOR output according to two different slopes will occur. These glitches will be led to the inaccurate results caused by offsetting the error signal despite the same VH and VL and even being in the same phase.

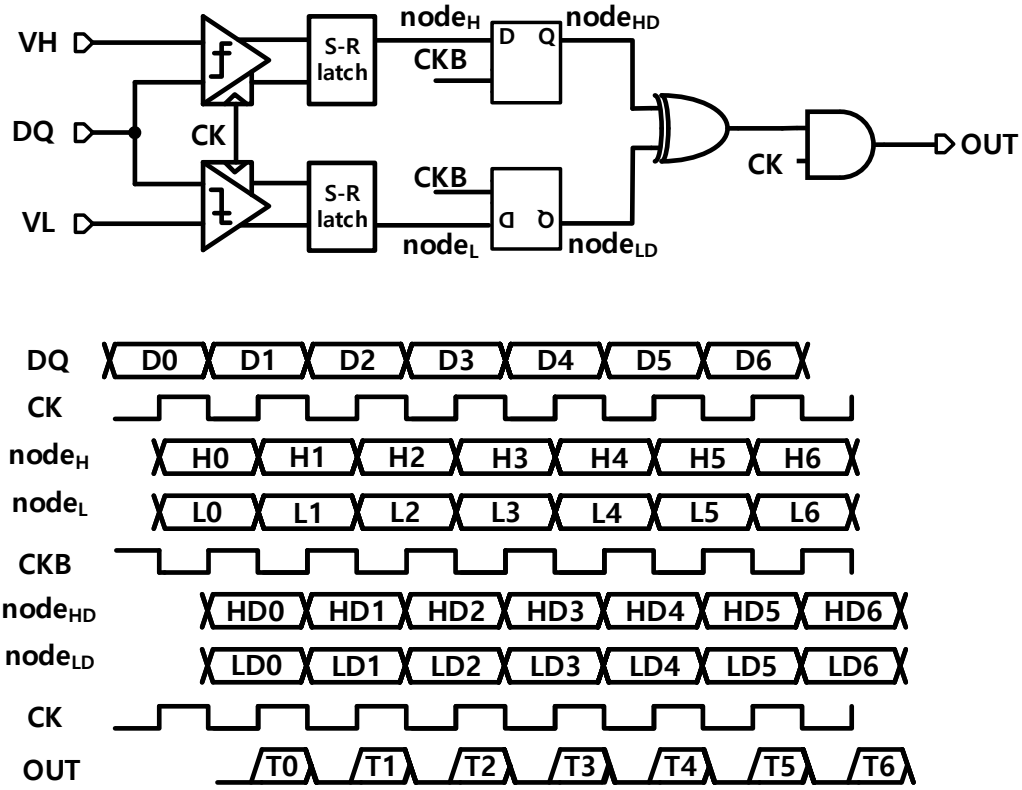


Figure 3.3.3. Proposed eye opening monitoring and its operation.

By adding D-flip and AND gate as shown in Figure 3.3.3, the glitch problem that has occurred in the past can be eliminated. It can be used without any additional design up to the SR-latch used exactly in the loop unrolling structure; 2D on-chip eye opening monitor can be applied to the memory receiver without additional C_{IO} and glitch.

As shown in Figure 3.3.4, this allows to quickly check the signal quality and it works in the foreground instead of the background for power saving. Before the actual operation, periodically check whether the signal is pass or fail by rectangular mask and proceed with the operation. If there is a performance degradation of the circuit itself, it is possible to come to a point where it changes to fail in a situation where it is passed for the same signal at high-speed.

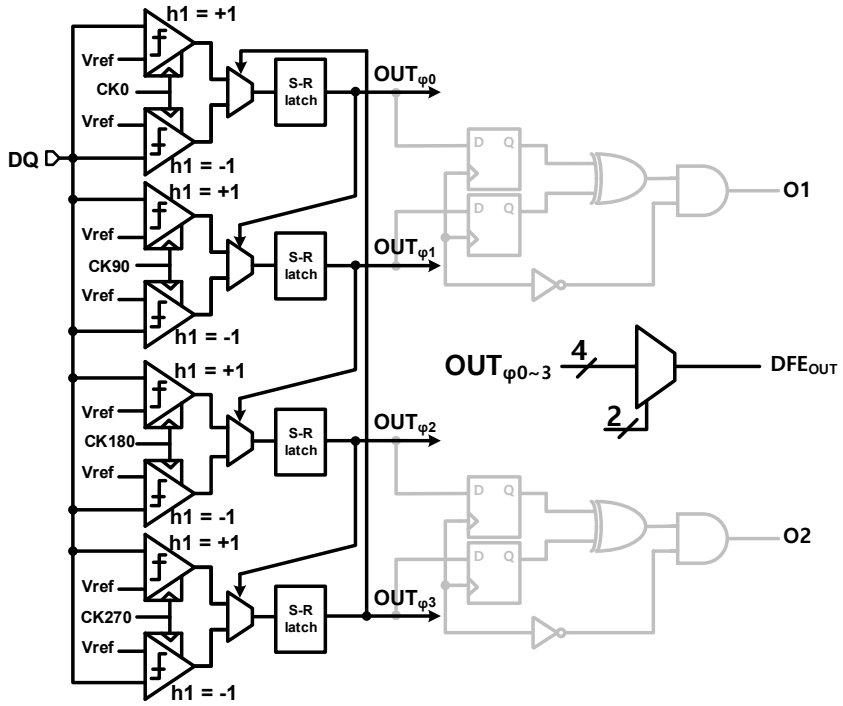


Figure 3.3.4. Proposed combined equalizer and EOM.

3.4 MASKING ERROR RATE

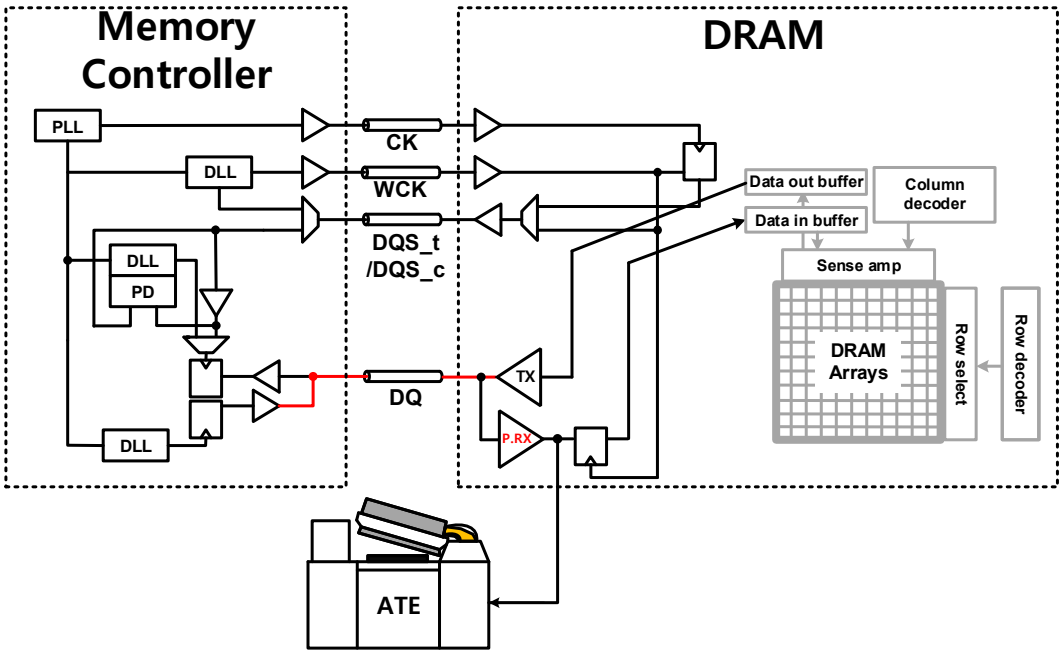


Figure 3.4.1. Proposed testing method for memory interface.

Masking error rate (MER) was first used by B. Analui in 2005 [2.2.15] and this chapter explains the correlation between BER which is the existing interface performance specification and MER that was gained via on chip monitoring.

The bit error rate is the number of bit errors divided by the total number of transferred bits during a time interval. In this ATE or BERT equipment, known PRBS pattern has been fed as input to the transmitter part of the source and data received at other side is looped back to the source. However, proposed testing method enables testing on long pattern without using known data. For EOM test in the DRAM side to obtain meaningful data such as bit error rate, similarities between masking error rate and bit error rate, which was studied on prior work, are explained. As the name implies, a bit error rate is defined as the rate at

which errors occur in a transmission system. This can be directly translated into the number of errors that occur in a string of a stated number of bits. The definition of bit error rate can be translated into a simple formula (3.4.1):

$$\text{BER} = \frac{\text{errors}}{total\ number\ of\ bits}. \tag{3.4.1}$$

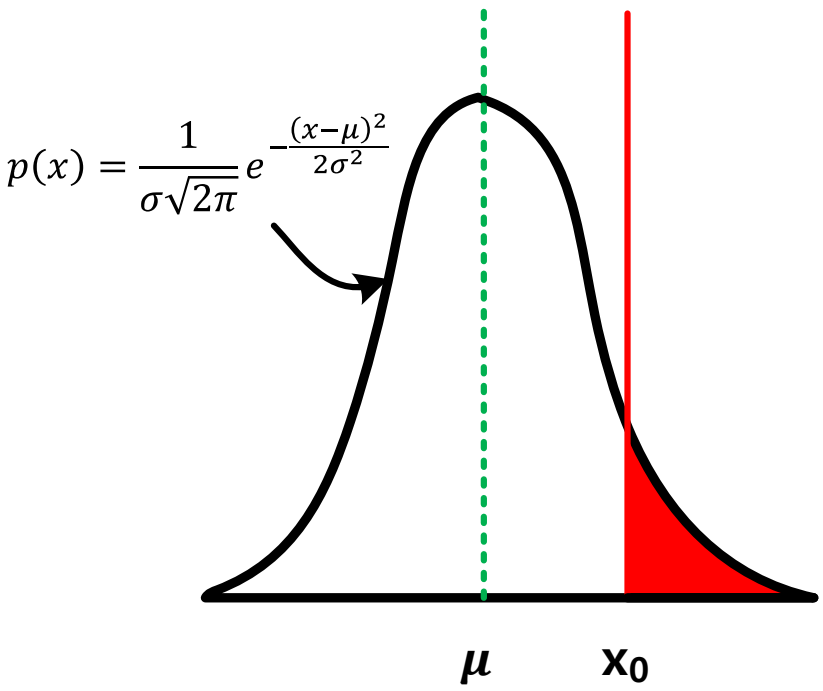


Figure 3.4.2. Normalized Gaussian probability density function Q.

Q functions are often encountered in the theoretical equations for BER involving AWGN channel. In this case these error probabilities are equal to formula (3.4.2). Such

formula is used for general cases [3.4.1] and the probability of bit error rate can be defined as below. Its process is omitted because it is widely used in Gaussian probability density function.

$$\text{Bit error rate} = \mathrm{Q}\left(\frac{1}{2\sigma}\right) \tag{3.4.2}$$

Similarly, the definition of mask error rate can be translated into a simple formula (3):

$$\text{MER} = \frac{\text{error count}}{total\ transition}. \tag{3.4.3}$$

Any data transition inside a rectangular mask is counted as error. Then, masking error rate is found by dividing error toggle count by total transition. Figure 3.4.3 shows VH and VL which are eye diagram with EOM voltage level and the difference between the two.

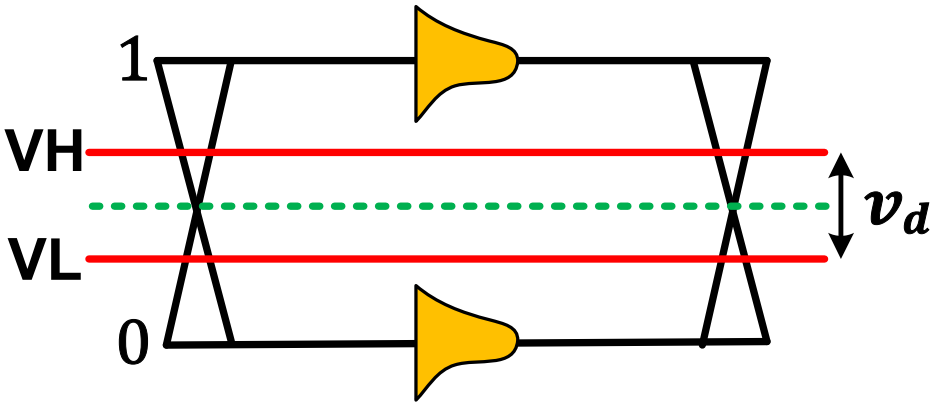


Figure 3.4.3. Eye diagram with EOM mask.

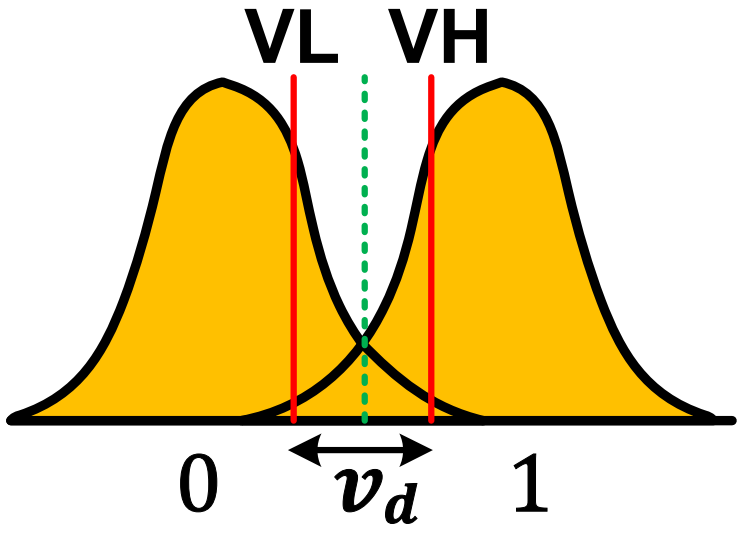


Figure 3.4.4. Normalized Gaussian probability density function with EOM mask.

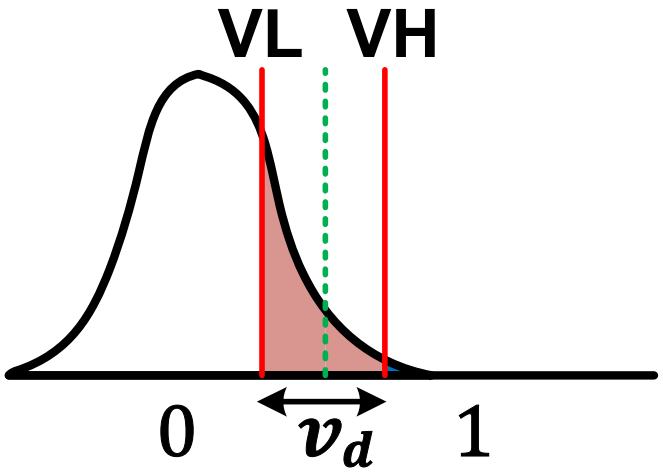


Figure 3.4.5. Normalized Gaussian probability density function for 1-side masking error rate.

Figure 3.4.4 shows normalized Guassian probability density function with EOM mask. This means that when incoming data is bigger than VL level or smaller than VH level, such case is considered error and error probability can be found via Gaussian probability.

As seen in Figure 3.4.5, when only one side is being looked at and in a case which the value is bigger than VL and if the figure is 0 and it is bigger than VH, this is not an error so such error probability is subtracted. If this is expressed with a formula, it takes a form of formula (3.4.4).

$$\mathrm{MER} = \mathrm{Q}\left(\frac{1-v_d}{2\sigma}\right) - Q\left(\frac{1+v_d}{2\sigma}\right). \tag{3.4.4}$$

Among this, $\mathrm{Q}\left(\frac{1-v_d}{2\sigma}\right)$ is prob{(0+noise)≥VL}, and in a case of $Q\left(\frac{1+v_d}{2\sigma}\right)$, it is prob{(0+noise)≤VH}. This means that when 1 side (one side) is being looked at, only $\mathrm{v_d}$ part is expressed for its probability. However, because the $Q\left(\frac{1+v_d}{2\sigma}\right)$ part is relatively more neglectable compared to $\mathrm{Q}\left(\frac{1-v_d}{2\sigma}\right)$, it can be defined as formula (3.4.5).

$$\mathrm{MER} \cong \mathrm{Q}\left(\frac{1-v_d}{2\sigma}\right). \tag{3.4.5}$$

The correlation between MER and BER is confirmed as seen in Figure 3.4.5 in a form of look-up table. This work was done based on the reference paper and indicates that even with using random data, MER can obtain significant data such as BER. The two main problems in the transmission of digital data signals are the effects of channel noise and ISI. The effect of the channel noise, assumed to be additive white Gaussian noise (AWGN), is organized in the absence of inter-symbol interference.

In the future, as with the BER 10^{-12}, if the figure for MER is reestablished under mutual arrangements by producing back data related to specific channels and ISI, a great amount of random data can be confirmed with using MER at the memory controller and there can be reliable verification on the interface.

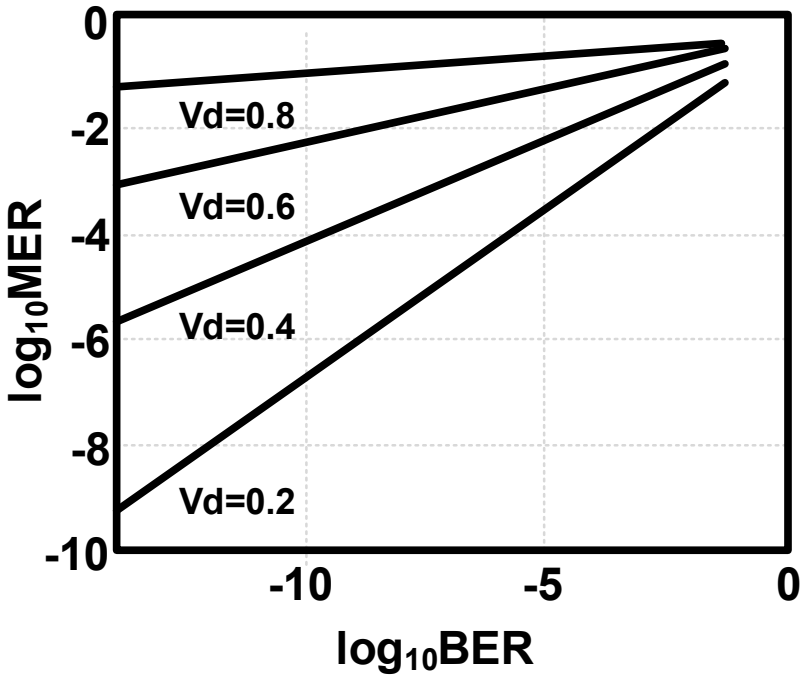


Figure 3.4.6. MER vs BER.

3.5 HYBRID SEARCH ALGORITHM

Existing papers about 2-dimensional EOM have stated that rectangular should be swept wide and to find mask sizes that would cause an error in iteration behavior. Since no papers that have been studied proposed an algorithm for increasing the size of the mask by what criteria, this paper will propose an algorithm for the first time. The gist of this paper is to study intuitively whether there is an interfacing problem when the DRAM receives in the memory controller or an error inside the DRAM by entering the test mode when the minimum eye mask required by the JEDEC specification is not achieved in the DRAM-side. Therefore, if the minimum eye mask is satisfied, it does not enter into the testing mode, and in the process of testing, it can be grasped quickly by scanning for eye opening that is opened by the current criteria to understand signal quality and controller problems.

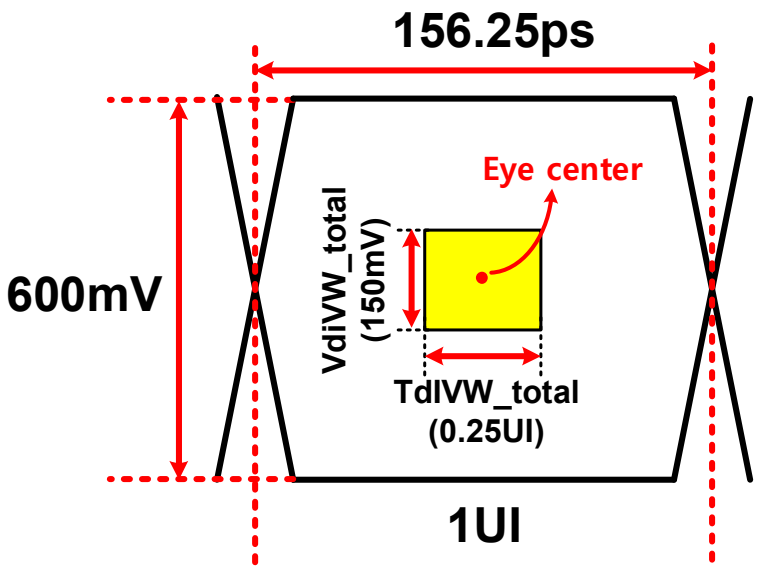


Figure 3.5.1. DRAM minimum mask from JEDEC specification.

Figure 3.5.1 shows the size of the minimum eye mask in the JEDEC specification explained earlier and VdiVW_total and VdIVW_total has set to 150mV and 0.25UI respectively, a voltage resolution and phase delay resolution are set to 3.89mV and 1.22ps each. The Eye center knows the center information in advance by memory training and the algorithm proposes on the assumption that the center is a symmetric eye mask that is not displaced.

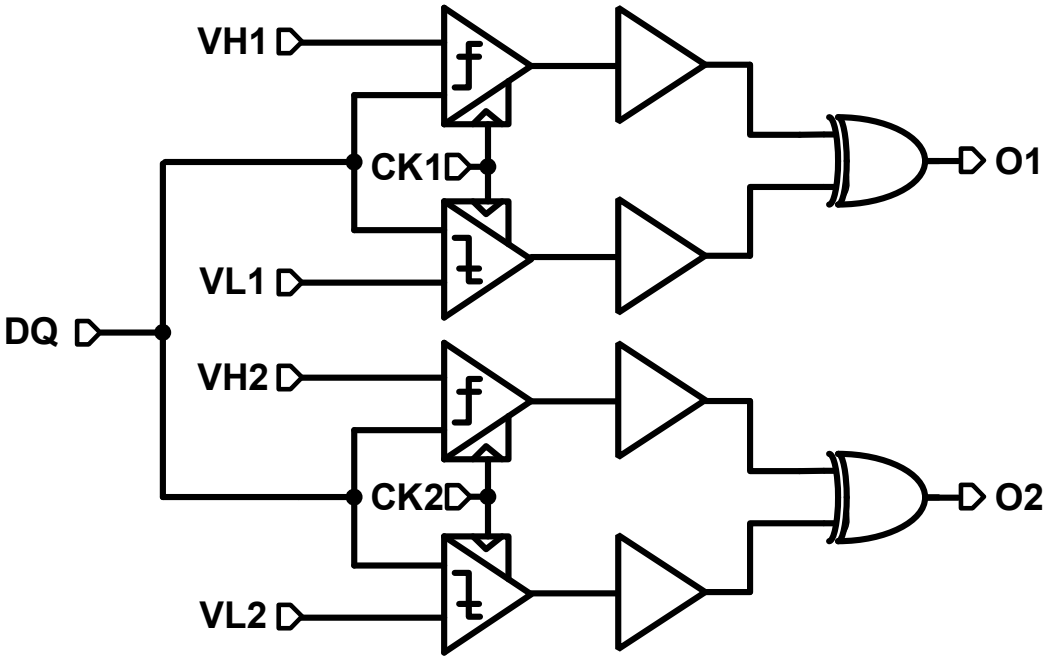


Figure 3.5.2. 2-Dimensional EOM simplified architecture.

Figure 3.5.2 shows the simplified 2-D EOM, and the voltage level and phase level of each EOM can be adjusted. This can be used to adjust the size of the eye mask as shown in Figure 3.5.3. Errors can be obtained on the left and right sides of the mask, and it can be distinguished from asymmetric eyes and a method of moving the step in another way to sense the transition of data can also be implemented.

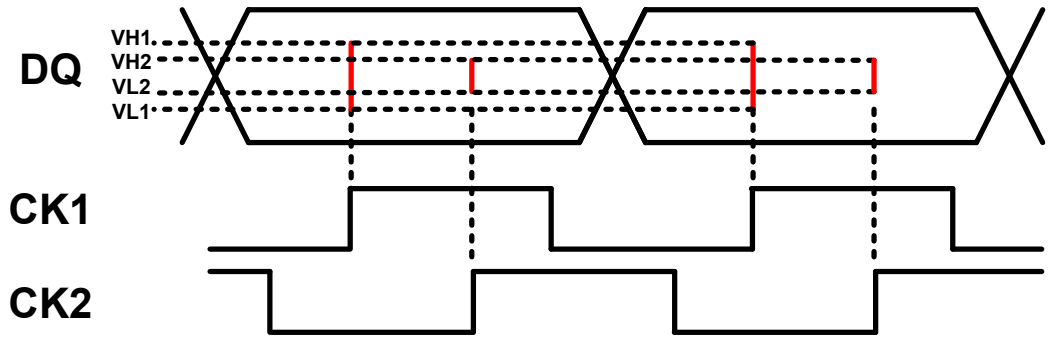
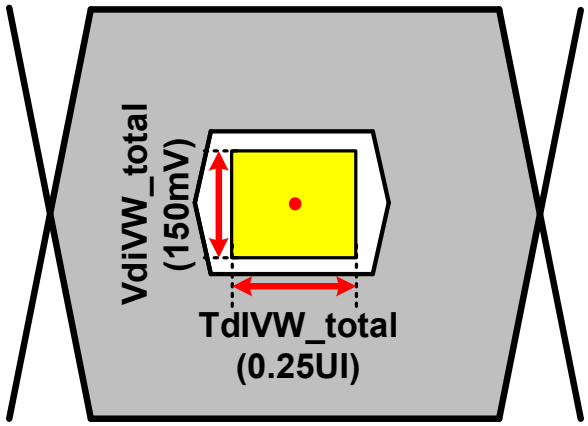
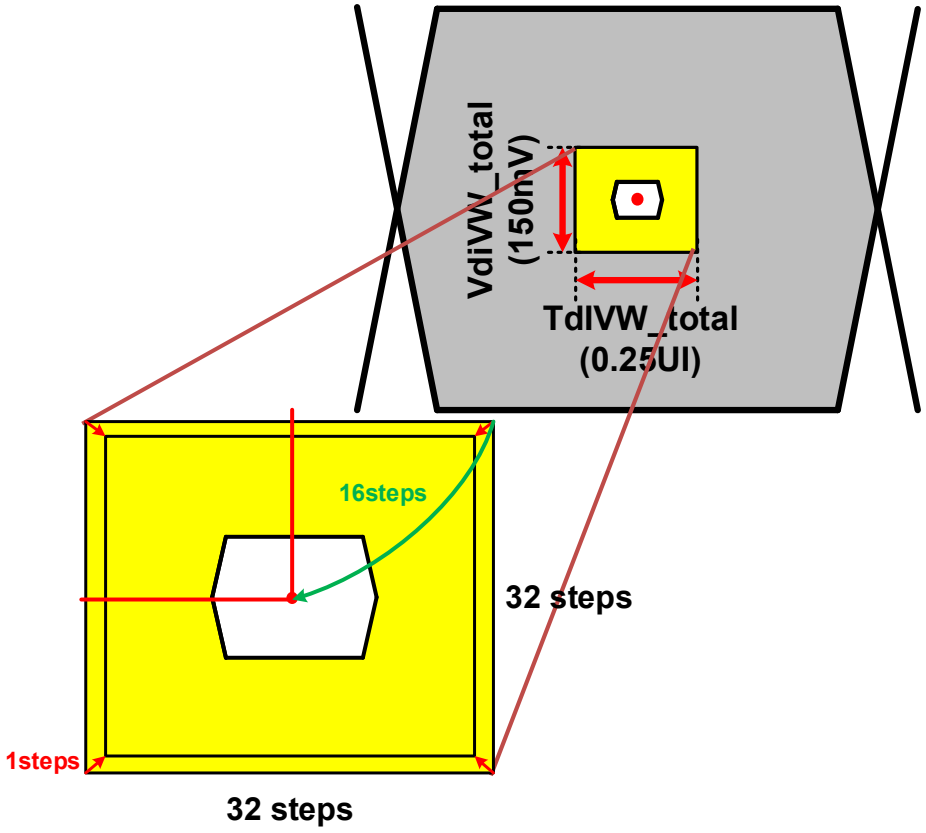


Figure 3.5.3. 2-Dimensional EOM operation.



(a)



(b)

Figure 3.5.4. Situation when there is no error (a) and there is an error (b).

Figure 3.5.4 shows the result of sensing the eye following the minimum eye opening specification with the initial mask. (a) shows the situation where no error has occurred and the DRAM active operation is performed without entering the test mode.

On the other hand, as shown in (b), when the eye is closed more than the start mask size of the eye sent by the controller, a bit error rate can be generated from the DRAM according to the variation, aging and external environment. Therefore, at this time, it is possible to quickly infer the problem by changing the TX equalizer coefficient setting value of the memory controller or interfacing after checking that the eye is opened to a minimum to some extent by entering the test mode.

In the situation of the vertical axis and horizontal axis of the entire eye are divided by 128 at 6.4Gbps, the resolution is set to 4.69 mV and 1.22ps respectively. At this time, 1 minimum eye mask specification can be set to 32 and the mask size can be reduced to 16 steps in overall on the assumption that the center is accurate.

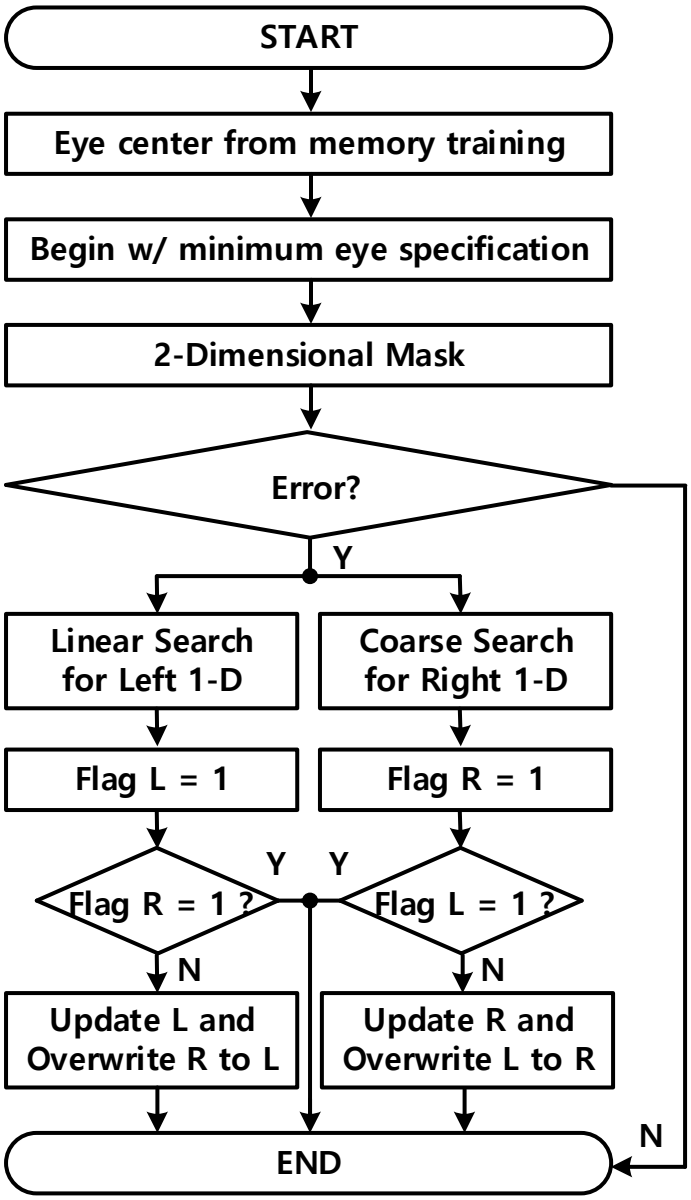


Figure 3.5.5. Hybrid search algorithm flow chart.

Figure 3.5.5 shows the flow chart of the hybrid search algorithm. In order to maximize the speed, reduce the size of mask in different steps and check the minimum opening size of eye. If reference voltage from the inside is used, there is the drawback that mux takes twice as much but when being tested, authorization can be made by the external device.

Hybrid search defines the left 1-D and the right 1-D and these two apply different algorithms. One involves a linear search and the other uses coarse search in which it begins from the middle.

Linear search refers to a method in which phase and voltage become smaller to 1 LSB. Its advantage is that the method is simple and can immediately move on when error is found meaning that the edge of eye can be quickly detected.

On the contrary, the other 1-D moves coarsely. This algorithm begins from the middle point between the center and the starting point and finds the shape of eye faster than the linear when the probability of the size of mask is half the entire size.

In addition, dimension in which it has discovered a situation with no prior error sends flag signal and finds aperture on mask by fixing the code value distant from the center. In a case of symmetric eye, the search process can be swift and accurate and in a case of asymmetric one, there is the advantage of additional discovery of asymmetric eye via increasing the dimension by 1LSB in which its code is changed based on accordance with the previously fixed dimension. This is possible because values for two dimensions can be each obtained.

As shown in Figure 3.5.6, the advantage of hybrid search is that it combines two dimensions and apply different algorithms and fixes the values by finding the edge of mask.

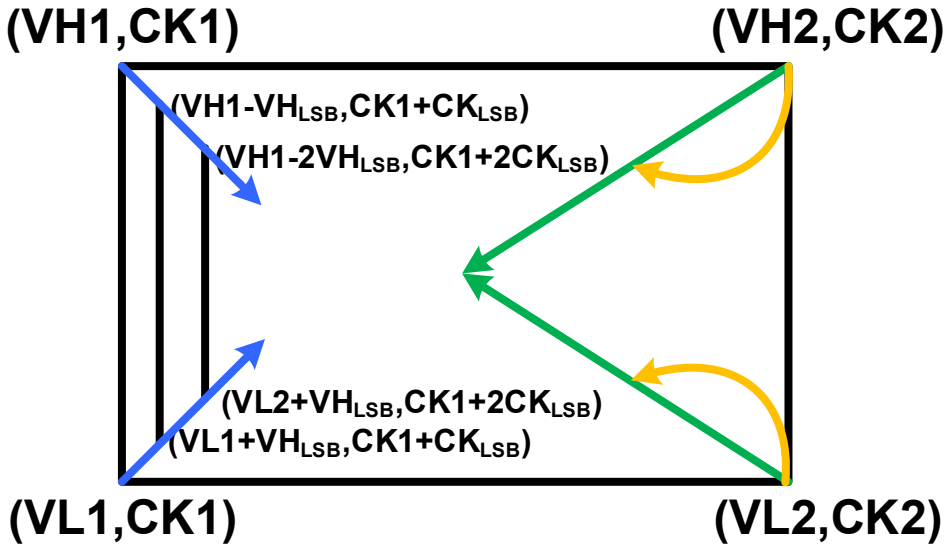


Figure 3.5.6. Hybrid search algorithm.

CHAPTER 4 RESULTS

4.1 RECEIVER WITH RE-USEABLE EOM

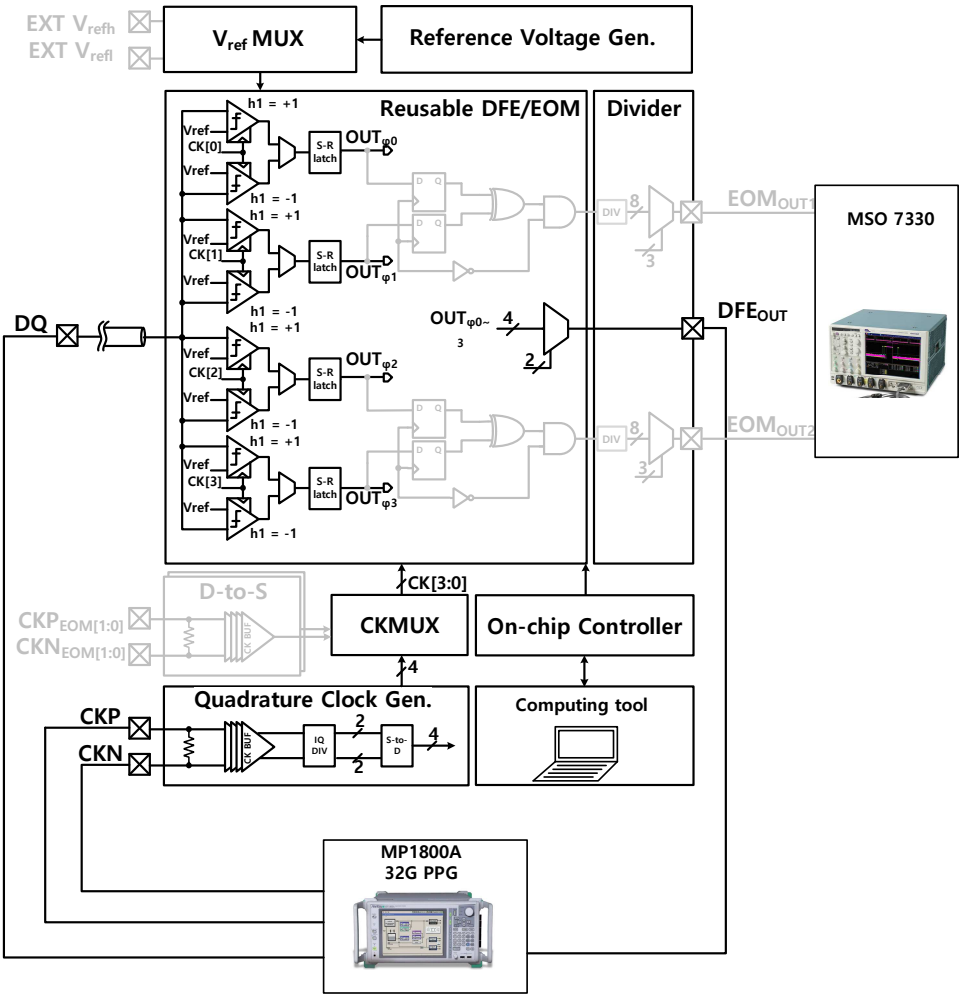


Figure 4.1.1. Receiver with re-useable EOM.

Figure 4.1.1 shows the block diagram and measure setting of the provided DRAM receiver. The Eye opening monitor re-uses the decision feedback equalizer to reduce C_{IO} and glitch and it works in the test mode on the foreground, so there is no additional power consumption when it is active. The reference voltage entering into the DFE and EOM could be generated externally or internally and it also could be adjusted with the computing tool using the on-chip controller.

4.2 SIMULATION RESULTS

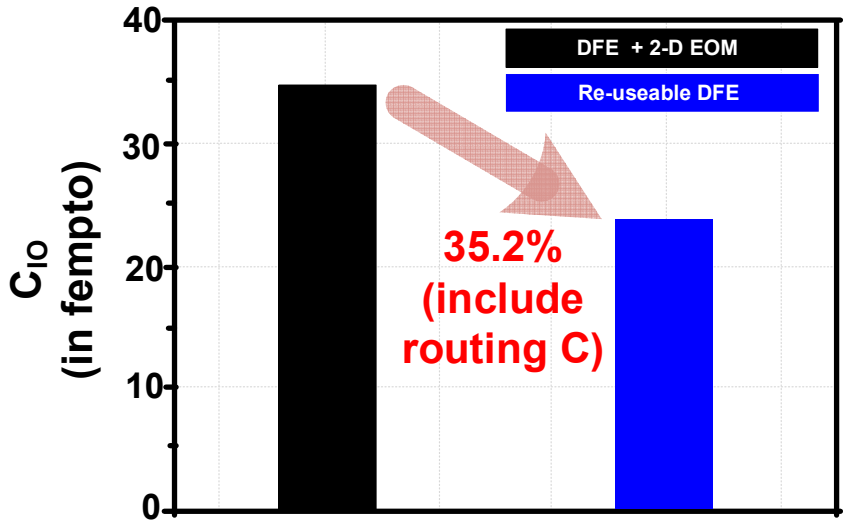
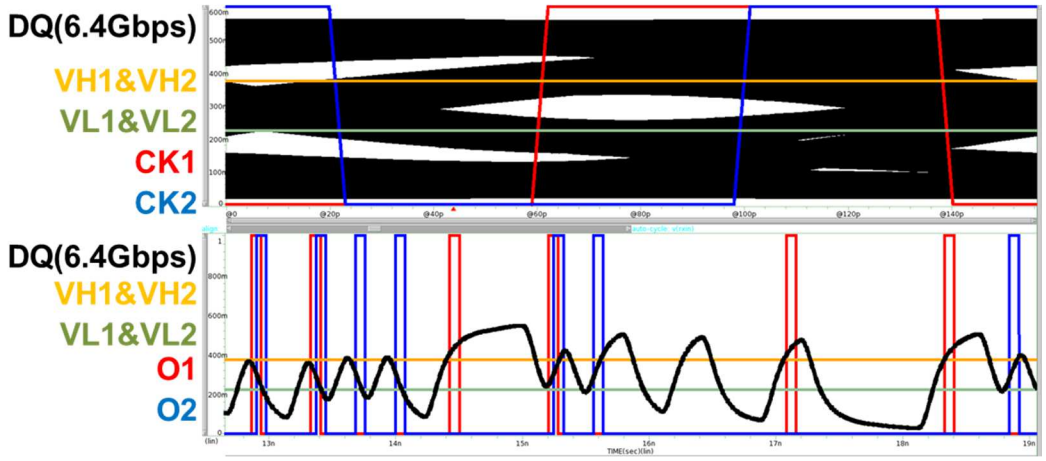
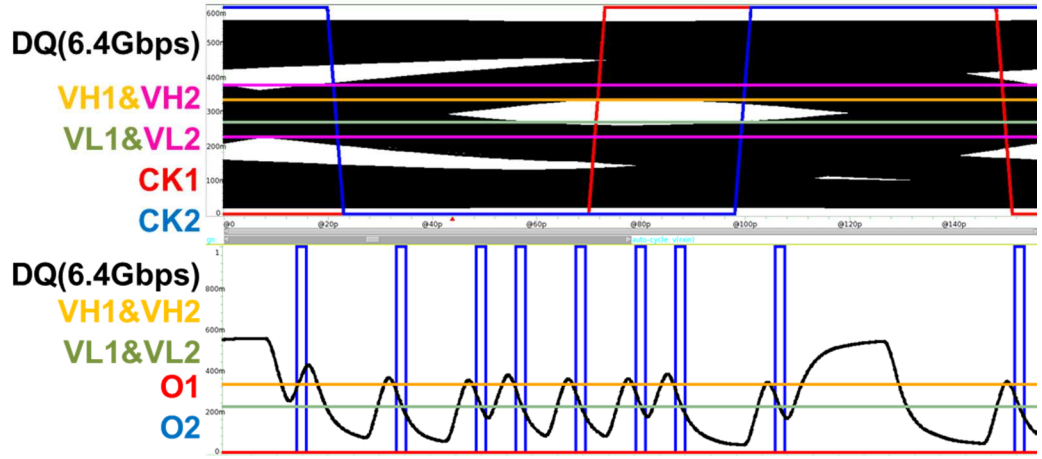


Figure 4.2.1. Input-to-output capacitance comparison.

Figure 4.2.1 shows the result of post-simulation which is a comparison that visualizes the improved part of the C_{IO} due to the shortened node in the comparator and layout. It decreased by 35.2%, which is a low fempto unit numerically, but I think the correct design method is to minimize it when it is about to enter ultra-high-speed in the future.

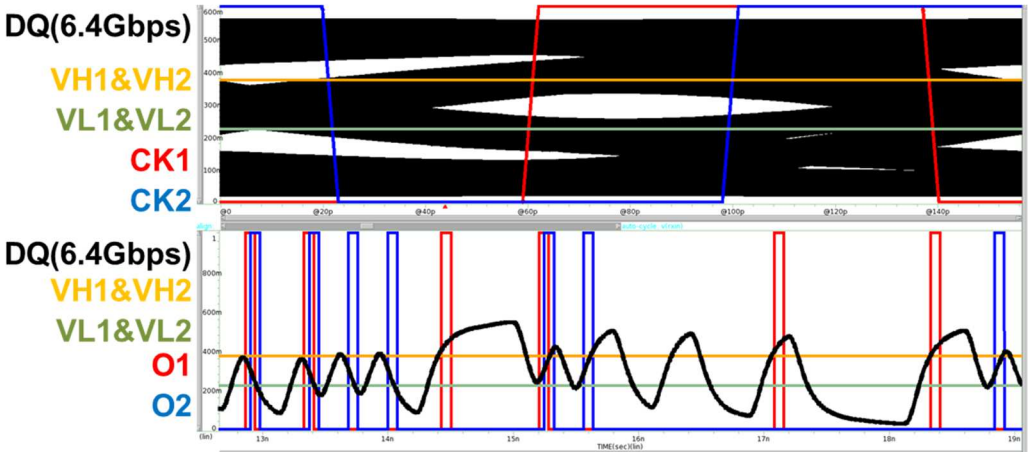


(a)

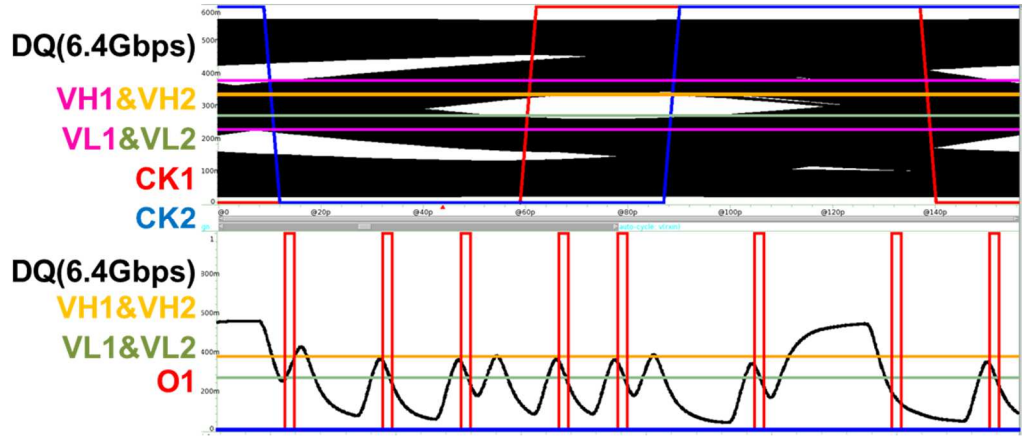


(b)

Figure 4.2.2. Algorithm simulation results of the left 1-D



(a)



(b)

Figure 4.2.3. Algorithm simulation results of the right 1-D

Figure 4.2.1 and Figure 4.2.2 show the eye error detect when an eye with a random eye size is set at DQ 6.4Gbps and the left 1-D uses the linear search algorithm and the right 1-D uses the coarse search algorithm. In the case of Figure 4.1.5, the eye was found with using the linear algorithm in nine steps and in the case of Figure 4.1.6, the eye was found in two steps. This is the case when the coarse search algorithm is faster, which shows an algorithm that quickly finds eye opening by applying the hybrid search algorithm respectively in 2-D EOM.

4.3 MEASUREMENT RESULTS

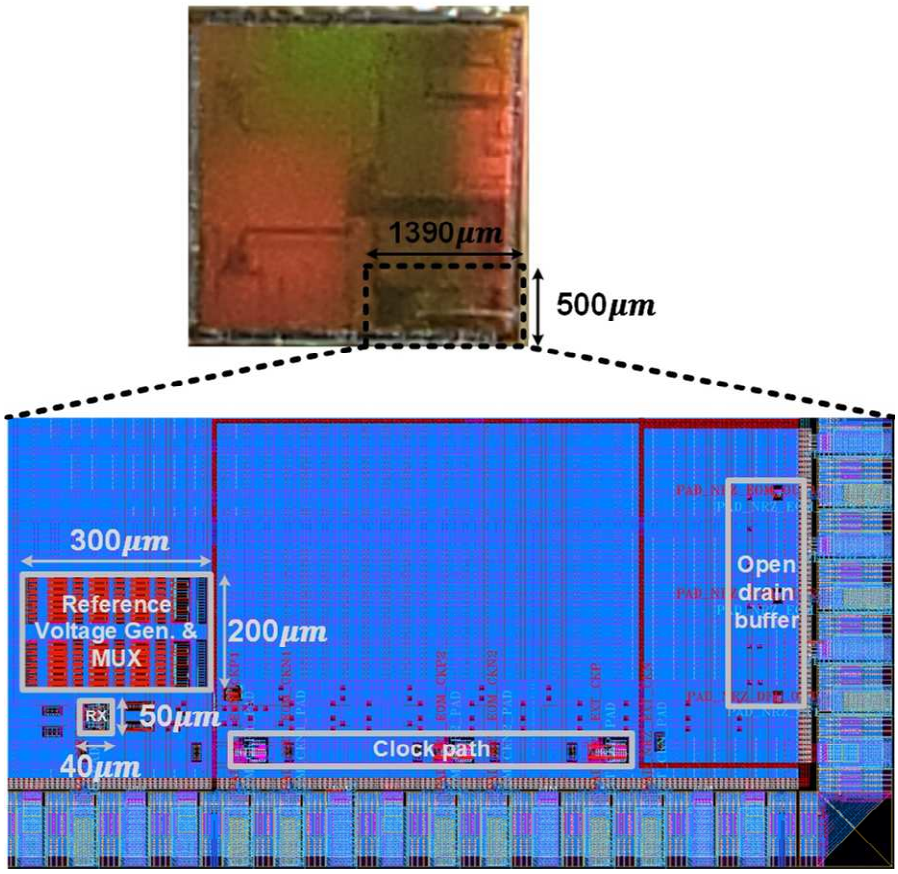


Figure 4.3.1. Chip photograph and magnified layout of the proposed RX.

Figure 4.3.1 shows the chip photograph and the magnified layout of the proposed RX. It shows the reference voltage and Vref MUX on the left and the receiver with the EOM and DFE are integrated. It describes a single-ended 1-tap decision feedback equalizer in 28nm LP process technology. The reusable EOM occupies an area of 40um X 50um and operates from a 1.0V supply with 3.24mA current.

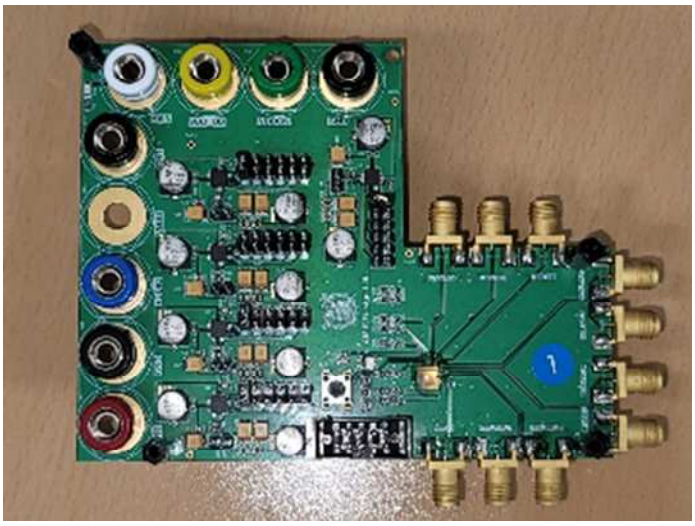


Figure 4.3.2. Printed circuit board of reusable EOM.

Figure 4.3.2 shows the printed circuit board of reusable EOM. Power domain is divided into core receiver power, clocking power, open-drain buffer power and on-chip controller digital power domain.. The receiver input receives the signal from the BERT device, and sends the output of the DFE to the BERT equipment to measure the BER. This is possible with known data and takes a bit of time.

After this process, this reusable EOM checks the center value of the eye and use the EOM to check whether EOM OUT1 and OUT2 each have one error toggle and one comes out without error. The EOM clock uses the sub-clock of the BERT equipment and by using this sub-clock, the algorithm could be applied.

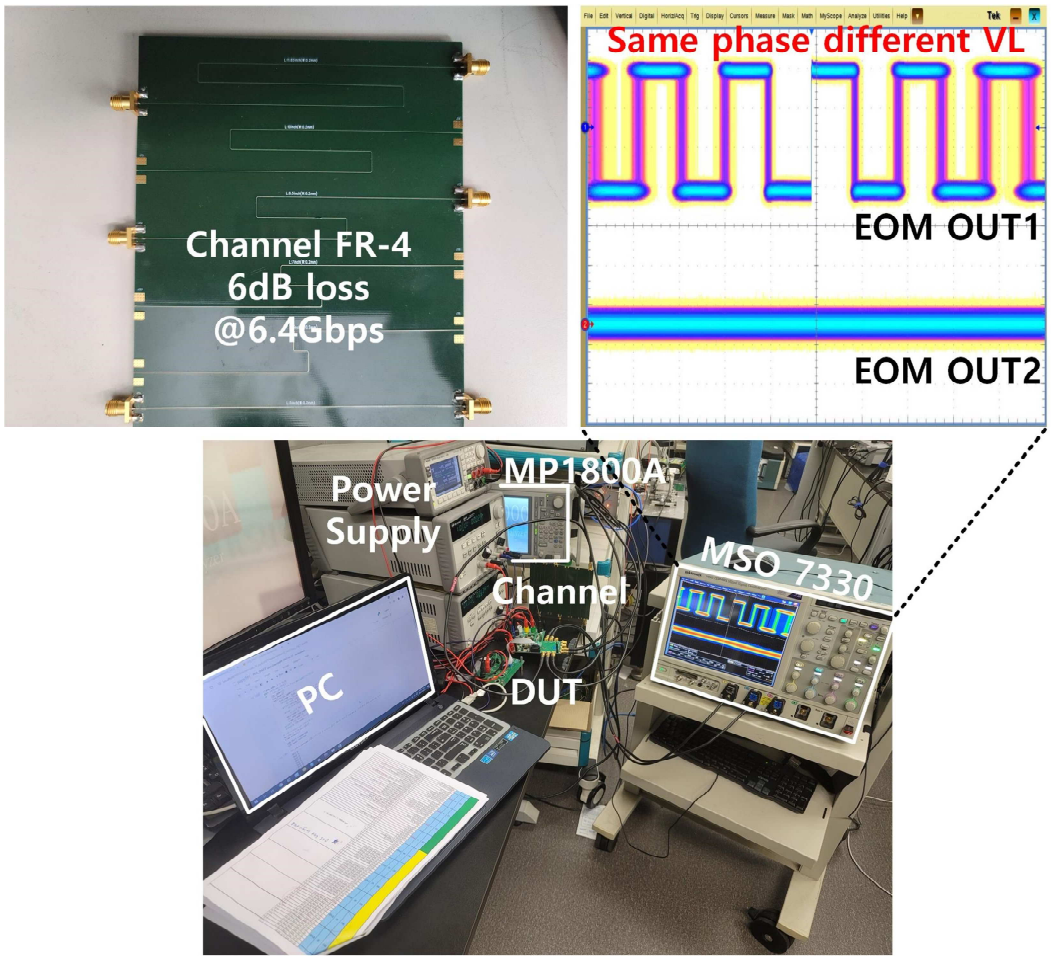


Figure 4.3.3. Test setup and measurement results

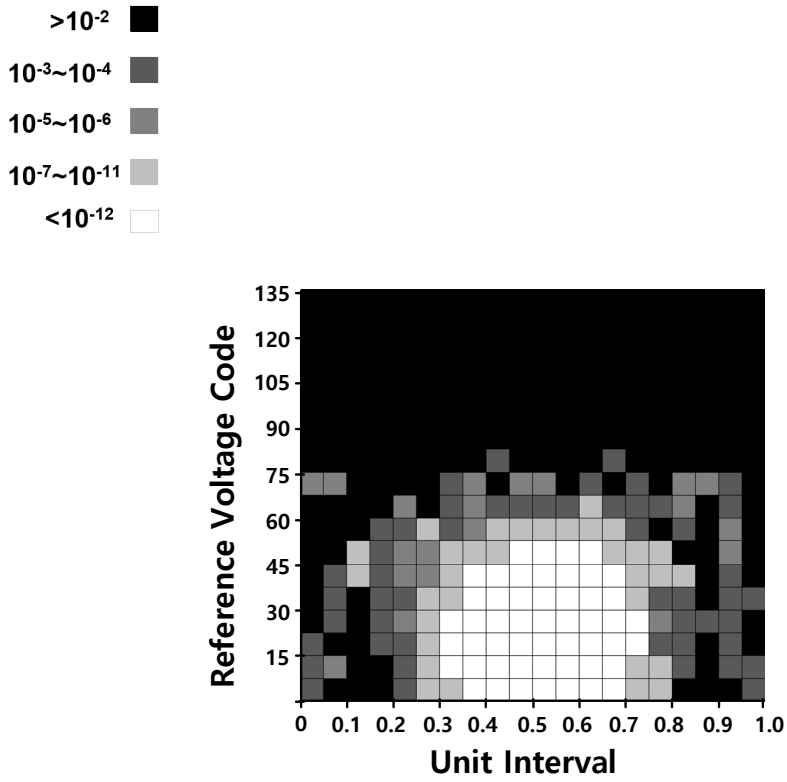
As shown in Figure 4.3.3, measurements are conducted to prove the preceding situation. First, aiming at the case where the size of the receiver's eye size does not meet the JEDEC specification, add an FR-4 channel with 6dB loss at 6.4Gbps and measure the BER by using the MP1800A BERT equipment.

We checked whether it is toggle or not in the oscilloscope and apply the algorithm by

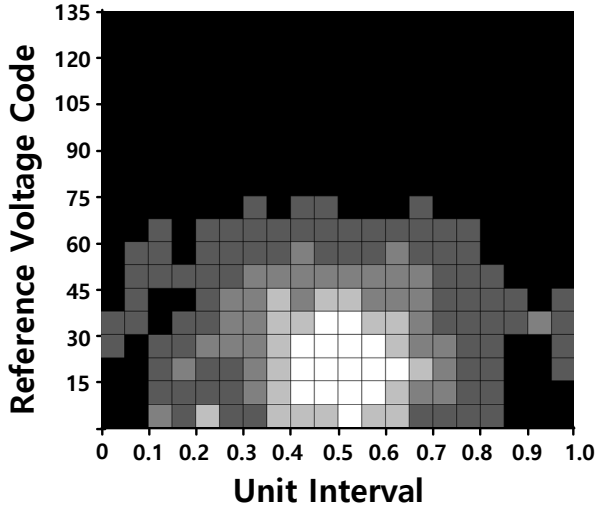
using a pc. The PC sets the environment to control the internal controller with a program which is written in python. Since there is only one sub-clock, 1-clock is applied at the same phase by using a splitter. Therefore, it was checked whether the EOM is in working order by changing different voltage levels in the same phase.

Figure 4.3.4 shows Shmoo by using BERT equipment, and it has the disadvantages of long processing time and it demands to know the pattern. The pattern was measured in PRBS7, and the EOM is possible to detect the interfacing problem for the memory controller quickly even with unknown random data by finding the center value of the eye and using the algorithm using the EOM mask.

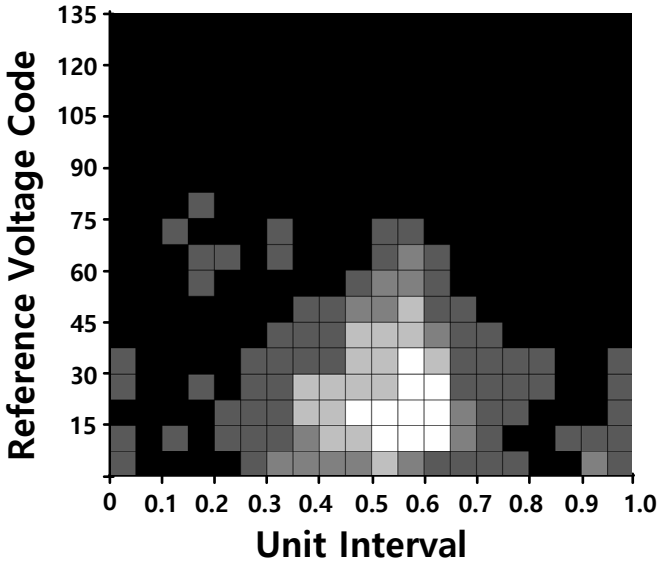
All channels used 5-inch, 8.5-inch, 11.85-inch FR3 PCB and to show the case of effect of algorithm I suggest, input voltage was also used for control via BERT equipment. Figure 4.3.4 presents shmoo plots of each eye measurement and as shown in the picture, different colors were used depending on each error rate. The worse channel loss is, the more eye is closed and numeric comparison is carried out on each case when three of these cases have undergone eye opening monitoring using algorithms. This indicates how many trials for algorithms there needs to be in order to minimize trial numbers.


>10-2
10-3~10-4
10-5~10-6
10-7~10-11
<10-12
Reference Voltage Code
135
120
105
90
75
60
45
30
15
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Unit Interval

(a)


Reference Voltage Code
135
120
105
90
75
60
45
30
15
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Unit Interval

(b)



(c)

Figure 4.3.4. Shmoo results of (a) 5-inch channel, (b) 8.5-inch channel, (c) 11.85-inch channel from BERT equipment.

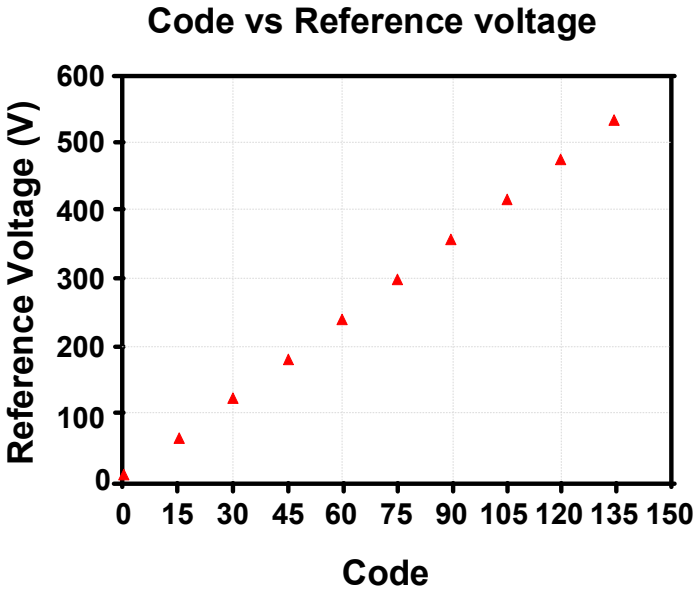
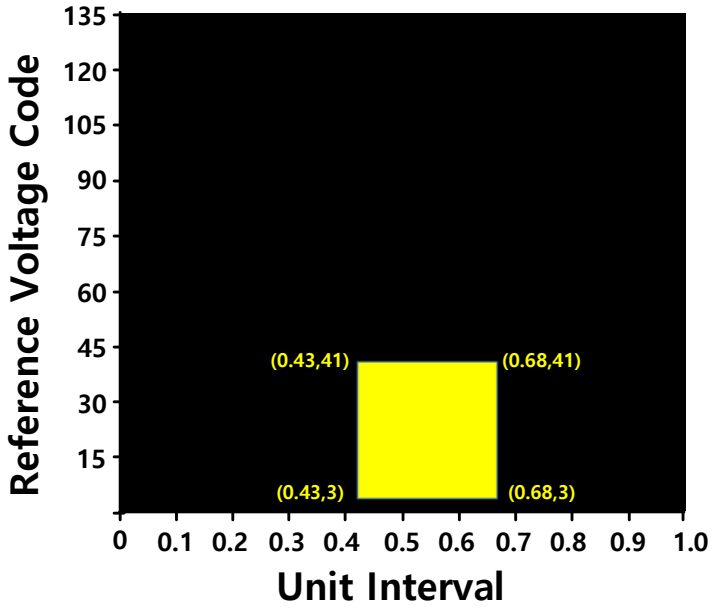


Figure 4.3.5. Code versus reference voltage value.

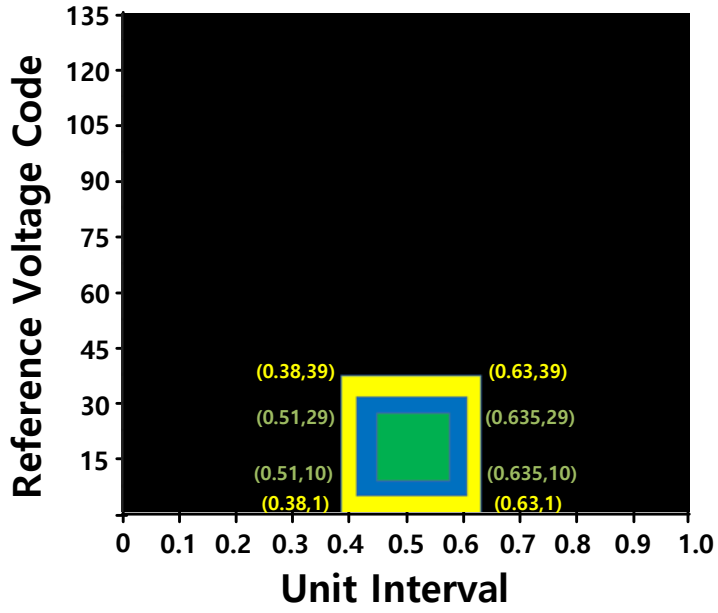
We need to check the actual code value and eye vertical opening value we would like to find out. So, as seen in Figure 4.3.5, post-simulation was done to confirm the value that fits each voltage value and code. With this, we can guess how open the actual eye is.

The center value can be found in the actual memory training value. In fact, center values can be different depending on variation and there are cases of training algorithms that are processed after fixating a half of the values of VDDQ. Therefore, rough values of eye center are decided even if eye center values may not be accurate.

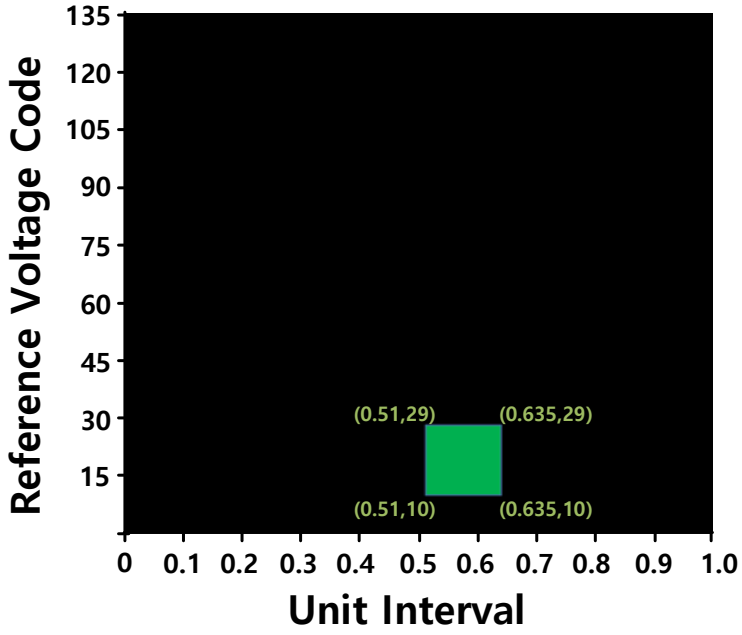
Therefore, because we have this information, we decide the phase information and voltage code value of the mask determined by the JEDEC specification from the center as initial.



(a)



(b)



(c)

Figure 4.3.6. Final eye opening for (a) 5-inch channel, (b) 8.5-inch channel, (c) 11.85-inch channel from on chip monitor.

As seen in Figure 4.3.6, whether eye is opened or closed can be quickly confirmed via applying 2-D EOM on three eye openings that have previously drawn shmoo.

First, in the case of (a), whether or not error output values are toggled needs to be checked after the size of eye that corresponds to JEDEC specification from rough eye center values is fixated. Then, if error is not toggled and algorithms are applied, it can be confirmed that for the case of (a), eye opening passes with only one trail. This makes it easy to quickly determine pass or fail when testing different memory controllers.

In the case of (b), it presents the worst case of when algorithms are used. When yellow rectangular is JEDEC specification, the end values of green rectangular is the median value of center and JEDEC specification. A blue rectangular located between the biggest and the smallest rectangular is an opened part of the actual eye and it is situated within the same distance from the two starting points of hybrid search, this is considered the worst case. This means that when hybrid search is used, it is a case of zero advantage.

Lastly, with the case of (c), it is passed from small rectangular and in the process of hybrid search, coarse search checks the pass within the shortest amount of time. From this point on, it is confirmed that eye can be more quickly detected when algorithms are applied compared to when they are not.

4.4 COMPARISON TABLES

Table 4.4.1. Comparison with EOM works.

Reference	JSSC [2.2.15]	T-VLSI [2.2.20]	IMSD [2.2.17]	EDSSC [2.2.18]	ISOCC [2.2.19]	This work
Process (nm)	0.13 CMOS	IBM 130nm	0.18 CMOS	40nm CMOS	0.18 CMOS	28nm LP
Using Eye Mask	Yes	None	Yes	Yes	None	Yes
Frequency	10Gbps	4Gbps	10Gbps	5Gbps	2Gbps	6.4Gbps
Equalizer scheme	FFE	None	FFE	CTLE+DFE	None	DFE
EOM scheme	2-D EOM	Hexagon 2-D EOM	2-D EOM	2-D EOM	2-D EOM	2-D EOM
Mask center detect	Known eye opening point	Known eye opening point	CDR	CDR	CDR	Memory Training
Mask aperture ratio algorithm	None	None	None	None	None	Hybrid Search Algorithm

As shown in Table 4.4.1, in this work, unlike other 2-D EOM papers, I proposed a new algorithm for the first time and the algorithm is not just a simple sweep to mask size. It also presents a quick way to find masks and worst eye shapes in 2-D EOMs with using appropriate algorithms to the memory interface specification.

Table 4.4.2. Comparison trial results with hybrid search algorithm.

Channel	Gridded EOM/ shmoo	This work	
		w/o algorithm	w/ algorithm
5-inch	360 trials	1 trial	1 trial
8.5-inch		5 trials	5 trials
11.85-inch		11 trial	1 trials

In order to show the improvements directly caused by algorithms, as previously explained in table 4.4.2, the cases of (a), (b), and (c) were compared for when algorithms were used and when they were not.

As for 5-inch, because it appeals to have a shape of big eye, trial numbers of w/o algorithm and w/algorithm are the same. In the case of 8.5-inch, it is considered as the worst situation because it has the same trial numbers of w/o algorithm and w/ algorithm and thus the algorithm does not have proper effect. On the other hand, by using w/ algorithm, 11.85-inch is a case that has the biggest effect and is the best condition. As the table above shows, the worst case has the same trial numbers. Therefore, it is confirmed that effect of w/algorithm takes place in all cases except for the worst case.

Also, in the case of gridded EOM which was used for drawing shmoo, because it checks every cases, there is time limitation to use this case for testing on a large amount of memory controller. If one wishes to test a large amount of memory controller and when verification is needed for more precise and detailed interface, interface testing can be carried out and in this process; trade-off of these two can be taken into consideration.

CHAPTER 5 CONCLUSIONS

This paper begins with a discussion of high-speed memory interfacing between DRAM memory and the controller. With the current situation that very strict standards exist for DRAM memory, reliability between memory controllers and memory has become an important topic among many companies. Memory and memory controller Manufacturers and customers have already minimized confusion with each other based on standard specification such as the JEDEC specification, but practically, there are many restrictions on conducting every existing test all controllers and DRAM. In addition, to test the problem when a problem occurs, the test is not proceeded directly unless monitor all the performances the test is conducted indirectly inferred or progressed depending on modeling. Therefore, in the situation of demanding higher speeds in the DRAM market, a faster test method which tests signal quality on the DRAM side was needed. In response to these requirements, this paper proposes a new monitoring structure that applies the existing receiver equalizer on the memory side for a high-speed memory interface in order to meet the needs for these motivations and test method was also described. Finally, in this paper, I proposed a hybrid search algorithm for the first time in EOM and the algorithm is different from the other ones that all existing 2-D EOM mask papers were only deal with a simple sweep of size. Proposed algorithm also fits the memory test using the memory interface specification. It is proposed that the method in this paper is designed to conform to ultra-high-speed and even when compared with existing algorithms, eye opening can be found with fewer steps.

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ABSTRACT IN KOREAN

본 논문은 DRAM 메모리와 컨트롤러 사이에 high-speed memory interfacing에 대한 고찰로부터 시작된다. 현재 DRAM 메모리에 대해 규격이 매우 엄격해져감에 따라 메모리 컨트롤러와 메모리 간에 신뢰성이 회사 간에 중요한 화두로 자리 잡고 있다. 메모리와 메모리 컨트롤러 제조사들 및 구매자들 간에 이미 JEDEC specification과 같은 표준 규격에 의거하여 서로간에 혼선되는 부분을 최소화 하지만, 실제 모든 테스트를 모든 컨트롤러와 DRAM 간에 진행하기에는 제약이 따른다. 또한 문제가 발생할 경우 문제가 되는 부분을 바로잡기 위해 test 하기에 모든 performance를 monitoring 하지 않는 이상 직접적인 test보다 간접적으로 유추하거나 modeling에 의존하여 진행한다. 따라서 DRAM의 시장 요구 속도가 고속으로 가고, 이에 따라 고속에서 가장 중요한 signal quality를 DRAM side에서 빠르게 testing 하는 방법이 필요하다. 따라서 본 논문에서 고속에서의 memory interface만을 위한 memory side에서의 기존 receiver equalizer를 응용한 monitoring 구조에 대해 제안하고 test 방법에 대해 서술한다.

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