공학박사 학위논문

Carbon-Based Diffusion Barrier for Copper Metallization

2022 년 2 월

서울대학교 대학원

재료공학부

이 상 봉

Carbon-Based Diffusion Barrier for Cu Metallization

반도체 구리 배선공정 적용을 위한 탄소 기반 구리 확산방지막에 대한 연구

지도교수 김 진 영

이 논문을 공학박사 학위논문으로 제출함

2022 년 2 월

서울대학교 대학원

재료공학부

이 상 봉

이상봉의 박사학위논문을 인준함

2022 년 2 월

위 원 장	장 호 원	(인)
부 위 원 장	김 기 범	(인)
위 원	김 진 영	(인)
위 원	김 형 근	(인)
위 원	조 성 용	(인)

Carbon-Based Diffusion Barrier for Copper Metallization

A DISSERTATION SUBMITTED TO

DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING

SEOUL NATIONAL UNIVERSITY

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Sangbong Lee

February 2022

ABSTRACT

CARBON-BASED DIFFUSION BARRIER FOR COPPER METALLIZATION

Sangbong Lee
Department of Materials Science and Engineering
The Graduate School
Seoul National University

As the challenges in aggressive scaling of the IC (integrated circuit) technology following Moore's law, the wire width of the back-end-of-line (BEOL interconnects) has been drastically reduced to less than tens of nm. As the RC delay of the interconnect has skyrocketed due to the scaling, it is being discussed as a crucial factor determining the latency of the entire IC device. Accordingly, there is an urgent need to find a viable solution for back-end-of-line (interconnects) that can transfer high current density with an acceptable level of RC delay.

The Cu interconnect, which was firstly proposed by IBM in the mid-1990s, has been adapted to most of the back-end-of-line interconnect of semiconductor manufacturing processes. It is expected to be continuously applied to not only the current 5 nm technology node,

but also the next generation technology nodes. This Cu interconnect inevitably requires a Cu diffusion barrier because Cu ions easily diffuse into adjacent Si or IMD (intermetal dielectric) with a relatively high diffusivity. As the wire width of the Cu interconnects has rapidly decreased less than 20 nm, the conventional TaN Cu diffusion barrier with a thickness of a few nm now faces an extreme challenge due to its 3D nature. On the other hand, two-dimensional (2D) materials, such as graphene, MOS_2, hexagonal Boron nitride (h-BN) can be atomically thin. Therefore, intensive research has been carried out to imply these 2D materials as a next generation Cu diffusion barrier. Previous results have suggested that 2D materials have promising Cu diffusion barrier properties, which encourages integrating these novel materials into state-of-the-art technologies. However, several key issues, such as defect modulation and back-end-of-line (BEOL) process integration issues, still hinder implicating of 2D materials as a Cu diffusion barrier. In this dissertation, we cover the opportunities and challenges of 2D carbon-based materials as a Cu diffusion barrier and address a way to process integration for semiconductor manufacturing. These challenges are divided into 1) defect modulation of chemical vapor deposition (CVD) graphene and 2) BEOL process integration of carbon-based materials.

In chapters 2-4, we covered the modulation of micro- and nanometer-scale defects in CVD-graphene by various approaches. Even in the case of graphene grown by chemical vapor deposition, which is known to have a relatively high level of crystallinity, various types of defects such as pinholes, grain boundaries, and cracks occur during the

synthesis and transfer process. Considering the 2-D nature of graphene sheet, these defects in graphene should be a fast diffusion path for Cu and hinder Cu blocking performance of graphene barrier severely.

In chapter 2, we investigated the effects of the bilayer period of atomic layer deposition of In-Zn-O transparent conducting oxide thin film. Here, the bilayer period is defined as the total number of ALD cycles in one supercycle. We show that the bilayer period of ALD determines whether deposited film exhibits a well-blended or layered structure and makes enormous discrepancies in phase evolution and following the physical properties of the film. In chapter 3, we propose a way to compensate for microscale defects in CVD-graphene by hybridization of CVD-graphene and transparent conducting oxide thin film, which is ALD-In_2O_3 in this case based on the results from the above chapter. We prepared graphene-In_2O_3 bilayer (GI-bilayer) and systematically investigated its electrical and optical properties. Excellent areal-uniformity of the electrical properties (standard deviation of sheet resistance: 12 Ω/sq) of GI-bilayer (7×7 cm^2) clearly demonstrated that various defects in CVD graphene are well compensated by homogeneously deposited In_2O_3 underlayer.

In chapter 4, atomic layer deposition (ALD) of Ru on CVD-graphene is introduced to patch defects in CVD-graphene, and following Cu blocking performance was evaluated by time-dependent-dielectric-breakdown (TDDB) test. ALD-Ru on CVD graphene shows selective deposition behavior, namely stuffing defects in graphene, and this defect stuffed CVD-graphene shows greater Cu blocking performance. Novel E-model was proposed based on 1-D flux model and implicated to

estimate activation energy and effective barrier thickness for Cu^+ ion to pass through the graphene diffusion barrier. In addition, electromigration (EM) reliability and enhancement in electrical conductivity of barrier itself are also investigated by agglomeration behavior of Cu on the barrier film and evaluating surface energy.

Finally, in chapter 5, the ultrathin amorphous carbon layer with the thickness of sub-1-nm is proposed as a next generation Cu diffusion barrier. This study focuses on the BEOL process integration issue of carbon-based materials. Conformal deposition of the amorphous carbon layer on the dielectric substrate was accomplished by grafting and following carbonization of hydroxyl group terminated polystyrene (PS-OH) polymer. Carbonization conducted under BEOL compatible temperature of below 460°C resulted in a uniform 1-nm-thick amorphous carbon layer on SiO_2 substrate. Time-dependent-dielectric-breakdown (TDDB) test evaluated that this amorphous carbon layer exhibited superior Cu blocking performance than the conventional TaN diffusion barrier under the thickness of 2 nm regime. Extrapolation of a dielectric lifetime under normal device operating conditions (~ 1 MV/cm, 100~150 °C) showed that this novel amorphous carbon layer is expected to exhibit 3-5 order of longer time to failure compared to conventional ALD-TaN diffusion barrier.

Keywords: Cu interconnect, Metallization, Diffusion barrier, Barrier metal, Graphene, Amorphous carbon, Atomic layer deposition (ALD)

Student Number: 2015-20850

Table of Contents

LIST OF TABLES

LIST OF FIGURES

Chapter 1

(approximately 1.2 nm thick; blue curve) and a-BN (3 nm thick; red curve) films. Thick blue and red lines denote averages. The number of devices measured is 100 for a-BN and 11 for hBN. (e) Breakdown field versus dielectric constant for low-κ materials reported in the literature (blue circles) and for a-BN (red circle). (f) Cross-sectional TEM images of Co/a-BN/Si interfaces after annealing for 1 h at 600 °C. The bottom image shows a magnified view of the area marked by the red box in the top image. No diffusion of Co into Si through a-BN is observed. HSQ, hydrogen silsesquioxane; MSQ, methylsilsesquioxane; BD, black diamond; FSG, fluorinated silicon glass; OSG, organosilicate glass; a-CH, amorphous hydrocarbon.[12]

Figure 1-8. Cu dual damascene fabrication process: (a) Via patterning, (b) Via and trench patterning, (c) Deposition of TaN (Cu diffusion barrier) and Ta (or Co, as liner material), (d) Cu electroplating and excess removal by CMP (chemical mechanical polishing), (e) Capping layer deposition. (Photo courtesy; Institute for Microelectronics.)

Figure 1-9. Diffusion of Cu ions into Si or IMD. Cu atoms enter the dielectric, they may create deep trap states with the concrete risk of dielectric leakage Cu forms brittle silicides with Si, which may cause expansion and semiconductor contamination

Chapter 2

Figure 2-2. Film growth behavior of ALD-IZO films (a) Growth rate of IZO films by varying the n_b. The estimated growth rate is denoted as 0.058 nm/cycle (b) In and Zn cation ratio of ALD-IZO films by varying the n_b. The estimated In and Zn atomic ratio was obtained by Equation (1) and denoted as the black and red line, respectively.

Figure 2-3. Electrical resistivities of ALD-grown IZO films as a function of the measured In cation ratio. Phases of IZO films (Wurtzite, amorphous, and Bixbyite) are grounded as colored boxes.[12]

Figure 2-4. X-ray diffraction (XRD) patterns of ALD-IZO films by varying the n_b.

Figure 2-5. Film crystallinity of ALD-IZO films by varying the n_b. TEM Plan-view (a–d) bright fields, (e–h) dark fields, and (i–l) selected area diffraction patterns (SADP) of ALD-IZO films. The n_b of the IZO films was varied with 10 (a, e, i), 100 (b, f, j), 130 (c, g, k), and 200 cycles (d, h, l), respectively. The diffraction patterns in IZO film are attributed to In_2O_3 bixbyite.

Figure 2-6. HRTEM Plan-view images of ALD-IZO films. The n_b of the IZO films was varied with (a) 10, (b) 100, (c) 130, and (d) 200 cycles, respectively.

Figure 2-7. Radial average of SAED patterns of ALD-IZO films by varying the n_b, corresponds to plan-view TEM images in

figure 2-5 (i-l). The diffraction patterns in IZO film are attributed to In_2O_3 bixbyite.

Figure 2-8. Film morphology of ALD-IZO films by varying the bilayer period. Cross-sectional HRTEM images of ALD-IZO films. The bilayer periods of films were varied with (a) 10, (b) 100, (c) 130, (d) 160, and (e) 200 cycles, respectively.

Figure 2-9. Cross-sectional HRTEM HAADF images of ALD-IZO films. The bilayer periods of films were varied with (a) 10, (b) 100, (c) 130, (d) 160, and (e) 200 cycles, respectively. The inset of Figure 2-9 (e) shows a typical EDS line profile of the IZO film with a bilayer period of 200 cycles.

Figure 2-10. XRR measurement results and corresponding simulation curves of ALD IZO films with the n_b of (a) 20, (b) 100, and (c) 200 cycles, respectively. The simulation curves are vertically offset for clarity.

Figure 2-11. Oblique-view AFM images and corresponding surface roughness of the IZO films with the n_b of (a) 10, (b) 100, (c) 130 and (d) 200 cycles, respectively. (e) AFM image of crystalline pure In_2O_3 films. The scanning area is 5 μm by 5 μm, and the z-axis scale is 12 nm.

Figure 2-12. Typical EDS line spectra of ALD-IZO films with he n_b of (a) 130, (b) 160, and (c) 200 cycles, respectively.

Figure 2-13. Electrical properties of ALD-IZO films by varying the n_b. (a) Electrical resistivities, and (b) Hall mobilities and (c) carrier concentrations of IZO films by varying the n_b.

Figure 2-14. TFT performance of ALD IZO film with the n_b of 200 cycles (a) Output characteristics of IZO TFT under different back-gate voltage (V_g). (b) Transfer characteristics at V_{sd} = 50 V.

Figure 2-15. Normalized electrical properties of ALD-IZO films by varying the n_b. (a) Resistivity, (b) Hall mobility, and (c) carrier concentration of IZO films are co-displayed with the data from the reference[12] that implies the electrical properties of IZO film along with the [In/(In+Zn)] cation ratio.

Figure 2-16. (a) Resistivity, (b) Hall mobility and carrier concentration of ALD-IZO films along with the n_b are co-displayed with the data from reference that implies the electrical properties of IZO film along with the [In/(In+Zn)] cation ratio.

Figure 2-17. Effect of bilayer period of ALD on the growth behavior and electrical properties of amorphous IZO film.

Chapter 3

Figure 3-1. Comparative experiment results for the degradation of sheet resistance of graphene, ITO, and graphene/ITO bilayer structure under uniaxial strain. The electrical resistance of graphene/ITO bilayer changed significantly less than that of bare ITO for the same applied strain and bending radius. In this experiment, the bilayer was fabricated by transferring single layer graphene on 80-nm-thick ITO films sputtered on PET substrate. (a) Electromechanical tensile test result (b) The change in sheet resistance versus bending radius.[17]

Figure 3-2. Electromechanical durability of graphene/ITO bilayer was accomplished by repeated bending tests. Comparative experiments for 60-nm-thick amorphous ITO (*a*-ITO), polycrystalline ITO (*c*-ITO), and *c*-ITO/graphene bilayer were conducted as a function of the number of bending cycles (N) at the radius of curvature of (d) 16 mm (e) 12 mm and (f) 8 mm, respectively.[19]

Figure 3-3. Schematic diagram of GI-bilayer. The GI-bilayer was prepared by transferring CVD-grown monolayer graphene onto ALD-grown In_2O_3. Underlying In_2O_3 layer in GI-bilayer provides an electrical bypath to circumvent the microscale defects on the graphene.

Figure 3-4. Fabrication process of GI-bilayer structure. ALD-In_2O_3 thin film was deposited on substrate, and CVD-grown graphene layer was transferred onto In_2O_3 layer subsequently.

Figure 3-5. Characterization of CVD-graphene layer grown by two-step process. (a) Raman spectrum of graphene on SiO_2. (b) and (c) SEM images of graphene transferred on SiO_2 substrate. (d) Optical Microscope image of graphene transferred on SiO_2 substrate.

Figure 3-6. Characterization of ALD In_2O_3 film. (a) Thickness of In_2O_3 film as a function of number of ALD cycles. (b) Sheet resistance and resistivity of ALD In_2O_3 (c) Hall mobility and sheet carrier concentration of In_2O_3. (d) Optical transmittance measurement results with respect to thickness of In_2O_3. Quartz substrate was used as a reference for calibration of the optical transmittance.

Figure 3-7. Electrical properties of GI-bilayer. (a) Measured R_s of Gi-bilayers as a function of thickness of In_2O_3 (black). Estimated R_s from values of bare graphene and In_2O_3 according to the combination of two parallel resistors, namely graphene and In_2O_3 R_s is also presented (red). (b) Sheet carrier concentration and Hall mobility of GI-bilayer on the thickness of underlying In_2O_3 layer. Sheet carrier concentration and Hall mobility of bare graphene are also represented for 0 nm of In_2O_3.

Chapter 4

Chapter 5

Chapter 1.

Review of Cu metallization:

From evolution to challenges of Cu metallization

1.1 Overview of Cu metallization

1.1.1 Evolution of Cu metallization [1-8]

Since the first invention of the integrated circuit (IC) on germanium by Kilby in 1958,[4] and next on silicon by Noyce,[8] aggressive downscaling of ICs has been realized for over 50 years following the Moore's Law, which postulates "the number of transistors placed on one IC approximately doubles every two years." [6] This kind of continuous innovation of microprocessor units (MPUs) has driven tremendous changes in human beings' lives with the evolution of various electronic devices that rely on remarkable computational capability and functional integration on-chip. In the first 30-40 years of this innovation, continuous downscaling of transistors' dimensions, such as gate length, gate dielectric thickness, or junction depth, led to the success of Moore's law. However, as ICs' dimension getting smaller and smaller, another part of IC plays an increasing role in overall device performance: That is "Interconnect."

Interconnect in an IC or a very large-scale integrated circuit (VLSI) is a kind of connecting bridge of each transistor, transporting electric signal by carrying the current through metal lines. Besides, insulating materials, so-called intermetal dielectric (IMD) and interlevel dielectric (ILD), separates each metal line with various lengths, widths, and thicknesses depending on

the vertical levels they are located (i.e., from local interconnect (M_x) to global interconnect (M_P)), as shown in **Figure 1-1**. In the beginning of IC fabrication, aluminum and silicon dioxide were first employed as metal and dielectric materials of IC interconnect, respectively. However, with continuous shrinkage of feature size and increase in speed of the ICs, the following interconnect had to meet the requirements of lower resistivity and better electromigration reliability. To settle this problem, IBM first announced the replacement of conventional Al metallization to Cu metallization in 1996,[1] which showed advantages of reducing resistance, process complexity, and improved reliability.[3] Copper wires conduct electricity with about 40% less resistance than Al, which results in an additional 15% burst in microprocessor speed. Copper wires are also significantly more durable and reliable and can be shrunk to smaller sizes than aluminum.[1, 3] Owing to these advantages, Cu/low-k metallization is still being used in today's most advanced technology node (5 nm technology node in 2021) in the semiconductor manufacturing. This chapter covers the advantages and challenges of Cu metallization and how semiconductor engineers have overcome those challenges for over 25 years regarding material or technology innovation.

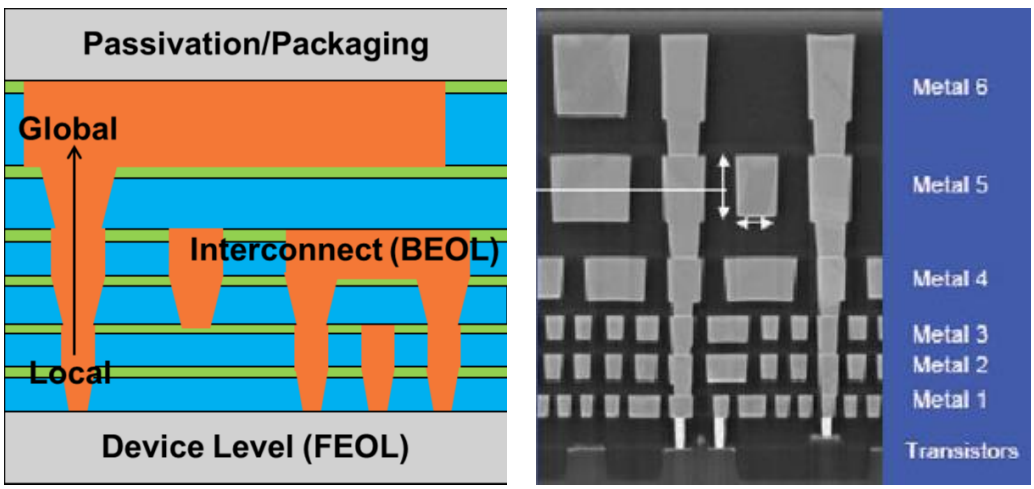


Figure 1-1. Typical interconnect (back-end of line, BEOL) structure of IC (left one), and SEM image of Cu interconnect with 6 levels of metal following 90 nm technology node. (right one, Photo courtesy of Intel)

1.1.2 Interconnect delay (RC delay) [9, 10]

Innovation of ICs in microprocessor units has been achieved through reductions in the feature size of the transistor. As feature size continues to shrink, corresponding metal wire density in interconnect gradually increases (i.e., reduced metal pitch and increase in the number of wiring layers) to accommodate increasing transistor density in an IC chip. As we move to the 3 nm node at around 2022-23, we will see continued BEOL scaling with critical M_x pitches < 25 nm using multi-pattering EUV. This wire pitch downscaling causes some crucial problems, such as excessive power dissipation, crosstalk, reliability degradation, and the most representatively, increased resistance-capacitance (RC) delays.

RC delay means measuring the time delay for electric signal propagation, where R denotes the resistance of metal lines in interconnect, and C denotes the effective capacitance between the metal line, correlated to a dielectric constant of interlevel or intermetal dielectric. This RC time constant of the multilevel Cu interconnect can be estimated using a simple model with Cu damascene architecture, as follow **Equation 1.1**.[9]

$$\mathrm{RC} = 2\mathrm{R}(\mathrm{C_V} + C_L) = \left[\frac{2\rho \mathrm{L}}{\mathrm{WT}}\right]\left[\frac{\varepsilon_0 \varepsilon_r WL}{H} + \frac{\varepsilon_0 \varepsilon_r TL}{X}\right] = 2\rho\varepsilon_0\varepsilon_r\left(\frac{L^2}{TH} + \frac{L^2}{WX}\right) \quad \text{(Eq. 1.1)}$$

where, R = resistance of the interconnect, C_v=Interlayer capacitance, C_L=Interlayer capacitance, ρ= resistivity of the interconnect metal, L= length of the interconnect, W= width of the interconnect, T= thickness of the metal layer, $\varepsilon_0, \varepsilon_r$ = The permittivity of vacuum and relative permittivity of dielectric, H= height of the dielectric layer, X= Spacing between adjacent Cu wire, P= pitch of the line. All of this dimensional information is denoted in **Figure 1.2 and Figure 1.3**.

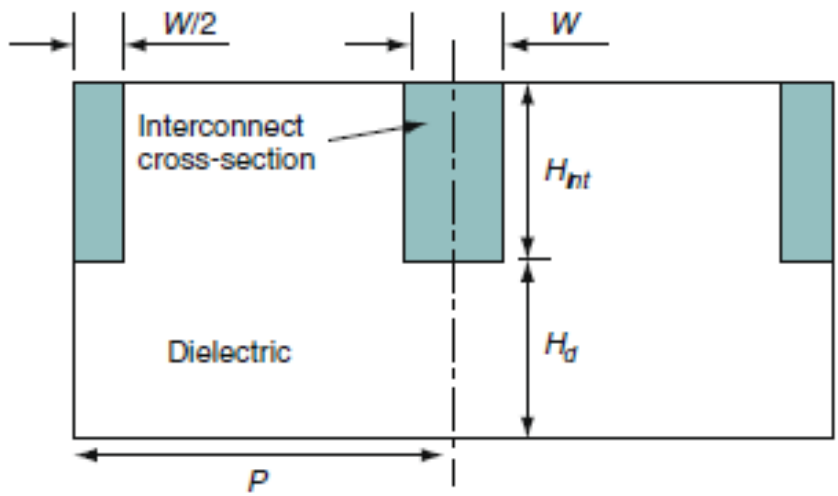


Figure 1-2. Cu damascene architecture with Cu interconnects embedded within the dielectric layer.[9]

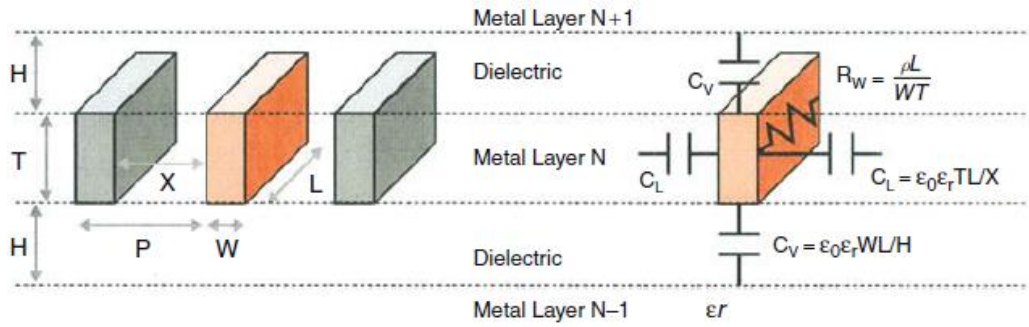


Figure 1-3. Multilevel Cu interconnect and dielectric layers. (figure courtesy A. Pratt, Advanced Energy Industry Inc.)[9]

Assuming that H_d=H_{int}=H=T, and P = 2W, (i.e., X=W) for simplicity, we can rewrite the Equation 1.1, as follow.

$$RC = 2\rho\varepsilon_0\varepsilon_r L^2\left(\frac{1}{T^2} + \frac{1}{P^2}\right) \qquad \text{(Eq 1.2)}$$

Along the **Equation 1.2**, there are two major parameters that contribute RC time constant: wire dimensional parameters (L, T, and P), and interconnect materials parameter (the resistivity of metal line, and the permittivity of dielectric layer). As the feature size shrinks, this RC delay is now becoming the rate-limiting parts are how we store and move information. According to the equation 1.2, assuming that length scaling of 0.7x at each technology node and constant dielectric permittivity and the aspect ratio of metal wire, line resistance (R) will increase by 1.4x, resulting

in the increase in RC delay time. **Figure 1-4** and **Figure 1-5** shows RC delay time with shrinking the feature size. As feature size shrinks, interconnect RC delay time dominates overall product's latency, even more severe than transistor gate delay. While designing solution such as a Cu/low-k dielectric interconnect has been introduced to reduce this RC delay time by reducing both wire resistance (due to Cu) and C (due to low-k materials), aggressive scaling of a transistor, and the scaling difference between transistor and interconnect delay with pitch size results in more than 1000x delay difference between them. To continue the use of Cu/low-k dielectric interconnect in the future technology nodes, it requires new materials engineering solution: the lower dielectric permittivity and the lower wire resistivity. Some solutions to address these issues are listed next section. (section 2.X)

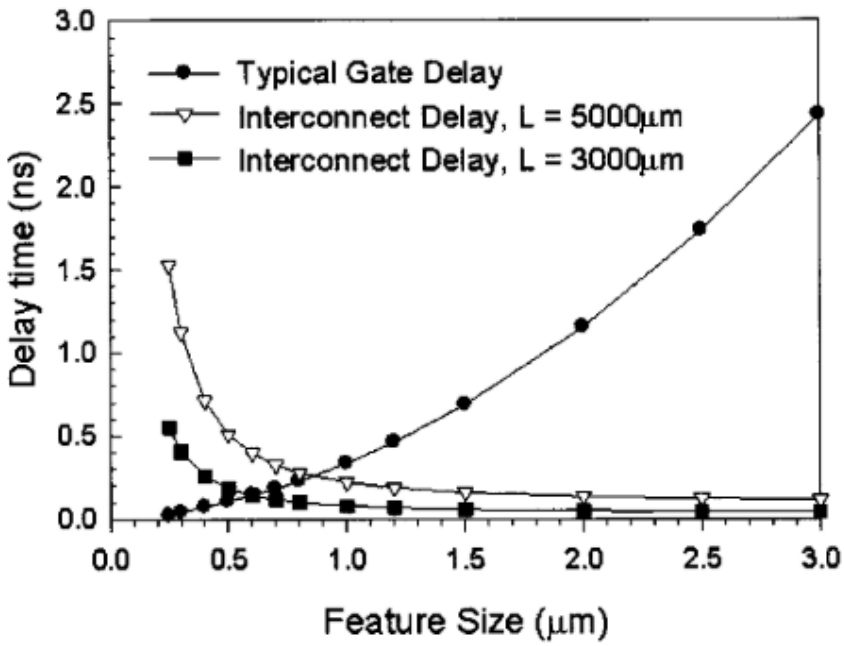


Figure 1-4. RC delay constant as a function of feature size. As the feature size decrease along with device scaling, Interconnect delay dominant whole device latency.[10]

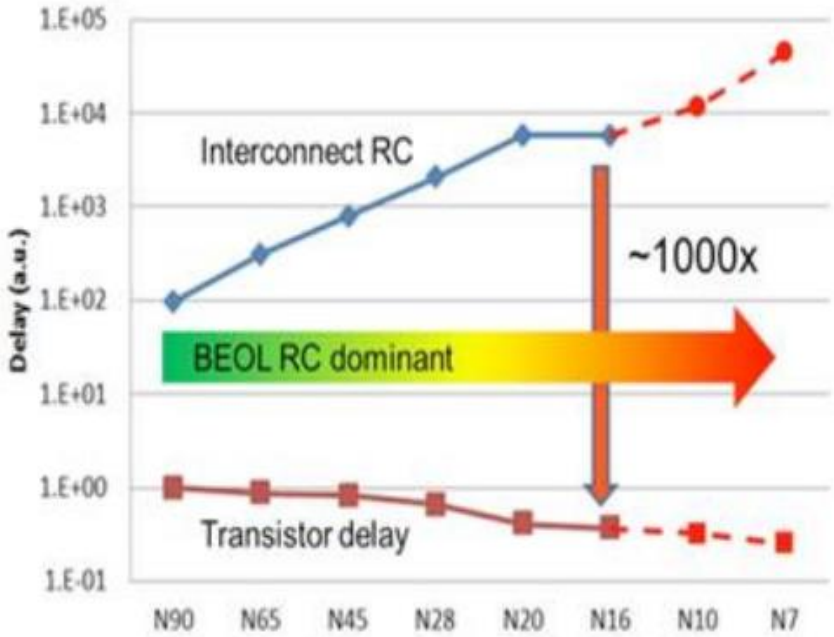


Figure 1-5. Transistor delay and interconnect delay as a function of technology node. Interconnect RC delay is a dominant factor to overall product performance. The scaling difference between interconnect and transistor delay results in BEOL RC domination. (photo courtesy: ITRS 2003)

1.1.3 low-k dielectric

Dielectric constant k (also called relative permittivity) is the ratio of the permittivity of a substance to that of free space. A material containing polar components increases dielectric constant. The dipoles align with an external electric field, adding the electric field of every dipole to the external field. As a result, a capacitor with a dielectric medium of higher k will hold more electric charge at the same applied voltage or, in other words, its capacitance will be higher. The dipole formation is a result of electronic polarization (displacement of electrons), distortion polarization (displacement of ions), or orientation polarization (displacement of molecules) in an alternating electric field. These phenomena have characteristic dependencies on the frequency of the alternating electric field, giving rise to a change in the real and imaginary part of the dielectric constant between the microwave, ultraviolet, and optical frequency range.[11]

In an effort to further reduce RC delays in interconnect, various materials with low dielectric permittivity have been employed as interlevel or intermetal dielectric materials. There are two major ways to reduce dielectric constant of IMD or ILD materials, as shown in **Figure 1-6**.[11] Decreasing polarizability could be achieved by replacing Si-O bonds in silica to less polar Si-F or Si-C bonds. A more fundamental reduction can be

achieved by using virtually all nonpolar bonds, such as C-C or C-H, for example, in materials like organic polymers. Recently, researchers in SAIT (Samsung advanced institute of technology, Samsung electronics Co.,) proposed 3-nm-thick amorphous boron nitride films with ultralow k values of 1.78 and 1.16 at operation frequencies of 100 kilohertz and 1 megahertz, respectively. The films are mechanically and electrically robust, with a breakdown strength of 7.3 megavolts per centimeter, which exceeds requirements.[12] As another approach to reduce the dielectric constant, introducing porosity to the amorphous SiO_2 matrix or doping the matrix with additional elements, such as fluorine, hydrogen, nitrogen has been demonstrated.[9, 11, 13] Typically, Lee *et al.* investigated the deposition of plasma-enhanced CVD SiOCH film with the dielectric constant of 2.55 using a Si precursor with Si-C-C-Si bond structure.[14]

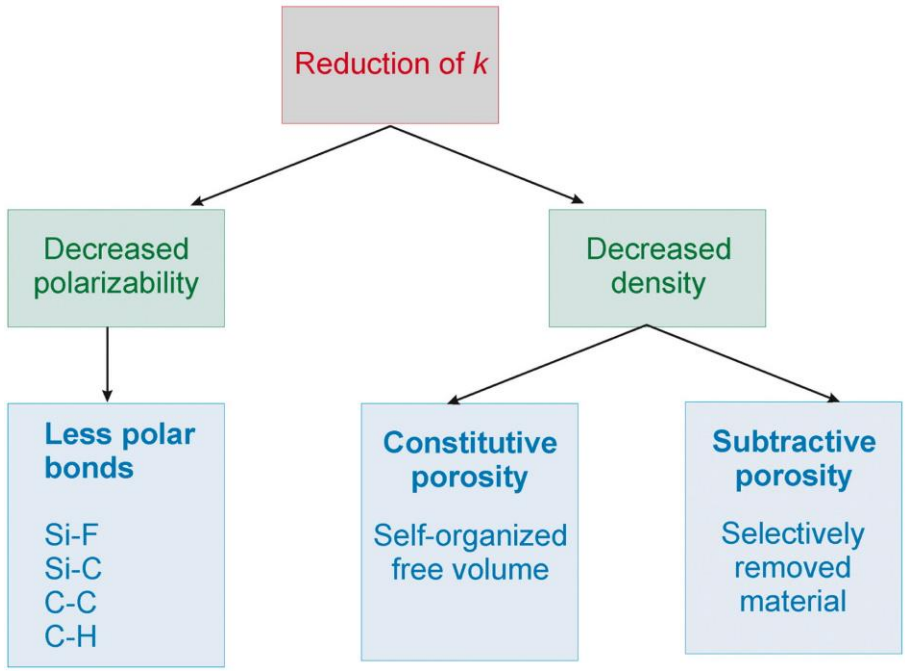


Figure 1-6. Possibilities for reducing the dielectric constant of materials.[11]

Not only a low dielectric constant, there are some requirements and process integration properties that interlayer dielectric (ILD) or intermetallic dielectric (IMD) material should satisfy. There are various requirements such as low thermal expansion coefficient, isotropy of electrical properties for wiring design, low reactivity with metal wiring, and mechanical strength to withstand CMP process, retarded adsorption of water molecules to prevent increase in permittivity due to moisture, thermal stability that can withstand the processing temperature (about 400°C for Cu). Along these requirements,

many low-k materials could not be implied to mass production due to low yield and reliability problems due to their brittle and soft properties during the multilayer wiring process despite their low dielectric constant. Currently, in the case of an ultra-low dielectric material (k<2.2), the introduction of many pores into the thin film is unavoidable, making it more difficult to satisfy the above-mentioned conditions, such as mechanical hardness. Namely, since porosity of 40% or more must be introduced, the mechanical strength (modulus, hardness) of the thin film becomes very weak, and the introduced pores tend to have an interconnected open-cell pore structure. When the open-cell pore structure is formed, the electrical leakage current increases, Cu diffusion increases, and the mechanical strength of the thin film deteriorates.

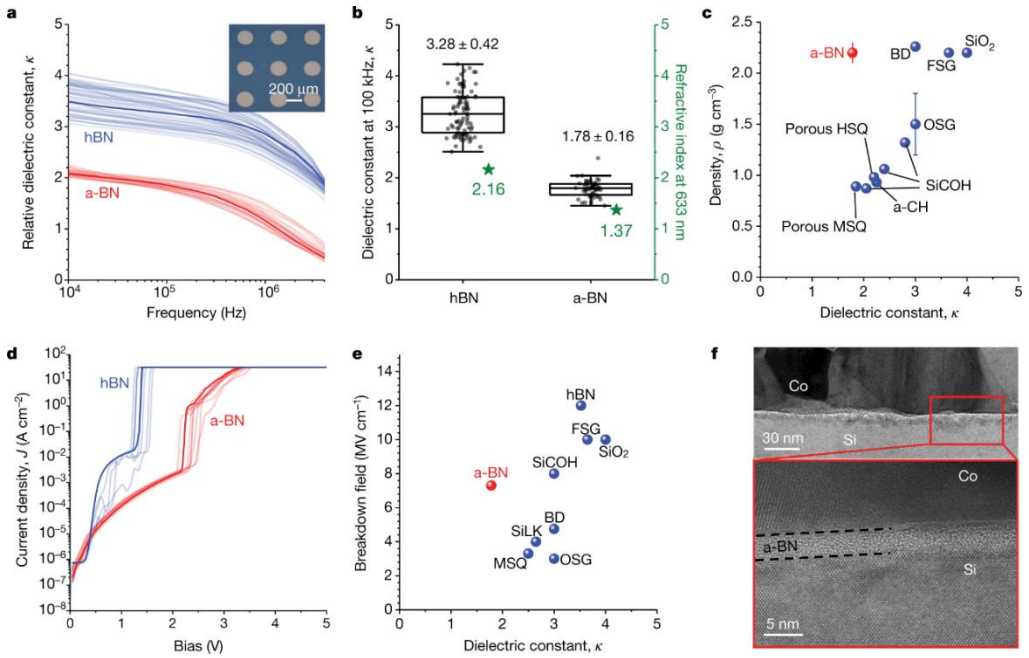


Figure 1-7. Ultralow dielectric constant amorphous boron nitride.[12] a, Relative dielectric constant as a function of frequency for a-BN and hBN. The dielectric constants were determined by capacitance–frequency measurements on metal–insulator–metal structures (inset). Thick blue and red lines denote averages. b, Statistical distribution of dielectric constants measured at 100 kHz and refractive indices (green stars) obtained by ellipsometry for a-BN and hBN. The box indicates a region with a 25% and 75% distrib¹ution relative to the average value, and the top and bottom bars mean maximum and minimum values. The number of devices measured in a and b is 250 for a-BN and 330 for hBN. c, Density versus dielectric constant for low-κ materials reported in literature (blue circles) and a-BN (red circle). d, Typical current density–voltage curves for hBN (approximately 1.2 nm thick; blue curve) and a-BN (3 nm thick; red curve) films. Thick blue and red lines denote averages. The number of devices measured is 100 for a-BN and 11 for hBN. e, Breakdown field versus dielectric constant for low-κ materials reported in the literature (blue circles) and for a-BN (red circle). f, Cross-sectional TEM images of Co/a-BN/Si interfaces after annealing for 1 h at

600 °C. The bottom image shows a magnified view of the area marked by the red box in the top image. No diffusion of Co into Si through a-BN is observed. HSQ, hydrogen silsesquioxane; MSQ, methylsilsesquioxane; BD, black diamond; FSG, fluorinated silicon glass; OSG, organosilicate glass; a-CH, amorphous hydrocarbon.[12]

1.1.4 Cu dual damascene structure

This section describes how the copper interconnects are manufactured. Semiconductor engineers have utilized the so-called Cu dual damascene process that is developed by IBM in the last 1990s.[1] This dual damascene structure inserted since at 220/180 nm technology node, and have extended so far.

As shown in **Figure 1-8**, in the dual damascene process, a low-k dielectric material is first deposited on the surface of the device. Based on a carbon-doped oxide material, low-k films are used to insulate one part of the device from another. The next step is to pattern tiny vias and trenches in the dielectric material. The vias/trenches are becoming smaller at each node. So, in today's mostly advanced node, chipmakers are trying to introduce extreme ultraviolet lithography (EUV) process to pattern the vias. Following that step, the patterned structure is etched, forming a via and trench. Then, using physical vapor deposition (PVD), a thin barrier material based on tantalum

nitride (TaN) is deposited inside the trench. Then, a tantalum (Ta), or recently cobalt (Co) liner material is deposited over the TaN barrier. And finally, the via/trench structure is filled with copper using electrochemical deposition (ECD). The process is repeated multiple times at each layer, creating a copper wiring scheme.[15]

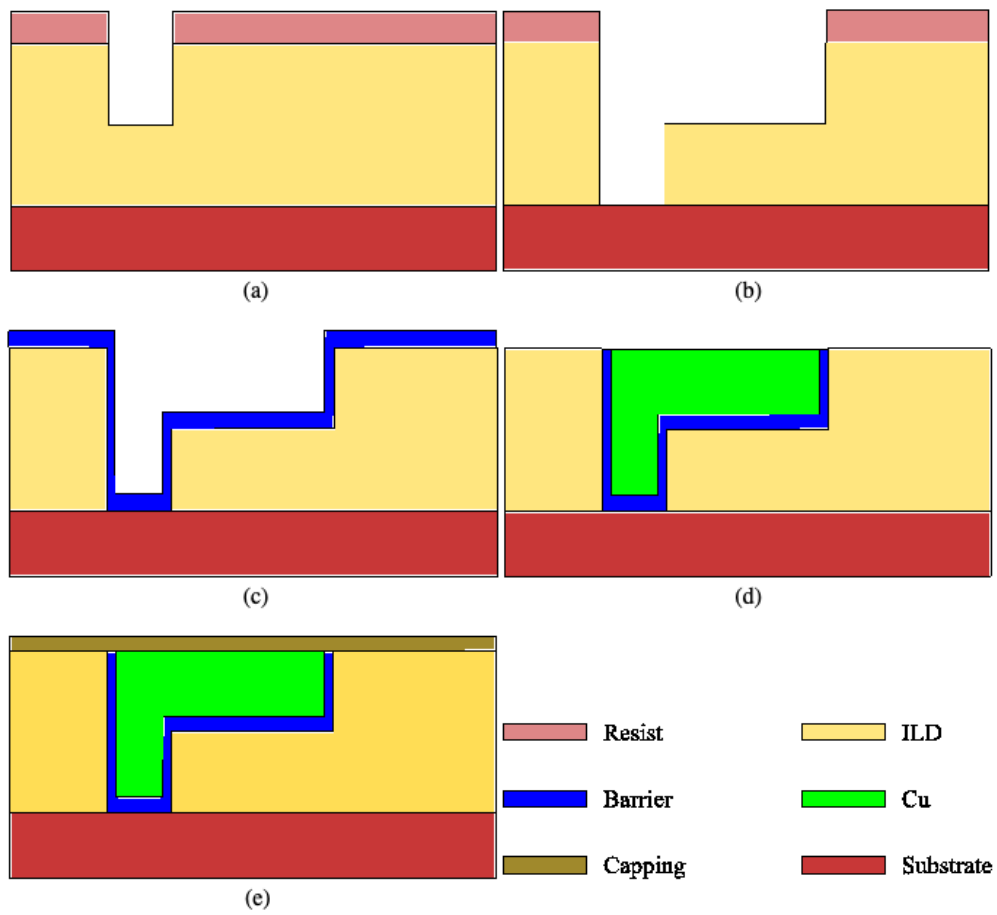


Figure 1-8. Cu dual damascene fabrication process: (a) Via patterning, (b) Via and trench patterning, (c) Deposition of TaN (Cu diffusion barrier) and Ta (or Co, as liner material), (d) Cu electroplating and excess removal by CMP (chemical mechanical polishing), (e) Capping layer deposition. (Photo courtesy; Institute for Microelectronics.)

1.1.5 Diffusion barrier

Although Cu offers sorts of advantages in interconnect performance, it definitely requires an additional layer between Cu metal line and dielectric materials: Diffusion barrier. Because Cu exhibits high diffusivity into Si and various dielectric materials (e.g., $D_0 = 4.71 \times 10^{-3}$ $cm^2/V{\cdot}s$ for Cu in Si)[5], Cu ions could readily migrate into adjacent Si or dielectric. For instance, once Cu diffuses into the underlying Si transistor level, it creates deep states in the bandgap of Si or forms a copper silicide phase.[2, 7] These deep level traps straightforwardly degrade the minority carrier lifetimes that cause the high junction leakage current in transistors and following short retention time in memory devices.[2]

To solve these problems, a suitable barrier material with good adhesion to Cu is required to prevent Cu from diffusing into the dielectric layer, as shown in **Figure 1-9**. The qualified diffusion barrier materials need to be refractory and inactive to both conductors and insulators at rather high temperatures, normally including transition metals such as tantalum (Ta),[16] tungsten (W),[17] titanium (Ti)[18], and their composites with nitrogen (N), carbon (C) or Si, such as Ta/TaN, W_2N, TiN, and so on. As those state-of-the-art barrier materials are typically poorly conductive, pre-deposition of a Cu seed layer is often needed for the electroplating of Cu, but the Cu seed layer is

prone to dissolution in an acidic electrolyte in the subsequent electroplating process, making it hard to obtain a uniform Cu layer. However, direct plating of uniform Cu film on diffusion barrier materials is of crucial importance in the modern fabrication process.

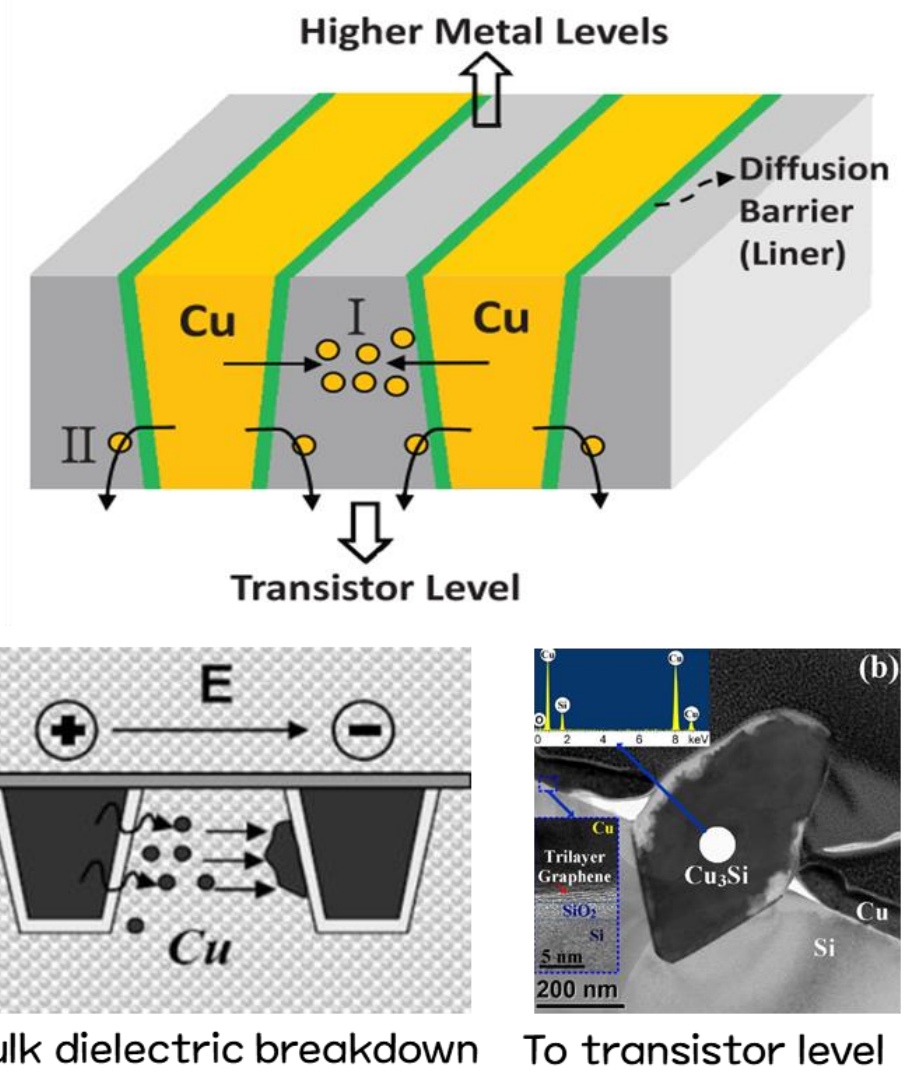


Figure 1-9. Diffusion of Cu ions into Si or IMD. Cu atoms enter the dielectric, they may create deep trap states with the concrete risk of dielectric leakage Cu forms brittle silicides with Si,[13] which may cause expansion and semiconductor contamination

1.1.6 Electromigration reliability[19]

Electromigration (EM) is an atomic movement of metal atoms caused by a massive flow of electrons, electron wind. Experimental evidence shows that grain boundaries/triple points account for electromigration in Al-interconnects. So, in a conventional integrated circuit (IC) Al-Cu alloy film is used to create Al-interconnecting lines, because Cu itself has a reduced susceptibility combined with reduced EM. Experimental data show that in median time to failure (t_{50}) the performance for copper damascene line is higher than Al-Cu without plug. This median time to failure of EM can be describe as **Equation 1.3**, so called Black's equation, where j is current density, E_a is an activation energy of diffusion along the dominant diffusion path.[20]

$$\mathbf{MTTF} = \mathbf{A j^{-2} \exp\left(\frac{E_a}{k_B T}\right)} \qquad \text{(Eq 1.3)}$$

On the other hands, the Cu migration leading to EM failures can be characterized by the Cu drift velocity through the Nernst-Einstein equation, as shown in **Equation 1.4**:[21]

$$\boldsymbol{v_d = \frac{D_{0,eff}}{kT} e^{\frac{-\Delta H}{kT}} \left(Z^* e \rho j - \Omega \frac{\Delta \sigma}{\Delta L}\right)} \qquad \text{(Eq 1.4)}$$

where Z*e is the effective charge of the mobile species, and j is the current density. The second term represents the backflow stress gradient due to Cu accumulation at the anode, which involves activation energy and thermal energy of effective Cu diffusion. The EM driving force term is mostly defined by the circuit design and applications, and process integration has very little control over it. Though process integration provides certain options for modifying the backflow stress gradient term, such as employing a thicker liner and a stronger ILD, these techniques are frequently incompatible with technology scaling for RC reduction. The Cu diffusivity term is now the sole parameter that the process integration may change. To be more explicit, the metal connection objectives of process integration for EM performance enhancement are lower $D_{o,eff}$ and greater D_H. Cu can diffuse from the cathode to the anode in several ways throughout the EM process, including through Cu surfaces at the Cu/Cap or Cu/liner interfaces, Cu grain boundaries, and the bulk of the Cu grains. The rapid Cu diffusion channel during EM was determined to be along the Cu and the dielectric cap contact for Cu lines characterized by bamboo like grain morphologies. In recent years, most process integration efforts have concentrated on improving the Cu/cap interface in order to lower Cu drift velocity, v_d.

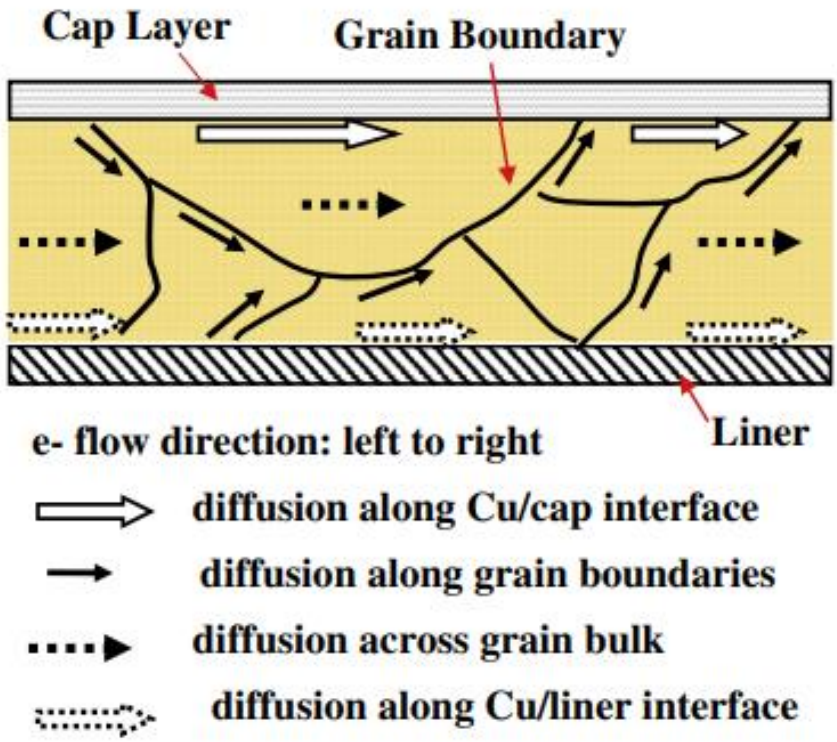


Figure 1-10. Schematic illustration of Cu diffusion/migration paths in Cu lines[19]

1.2 Challenges in Cu metallization

1.2.1 Conductor

Along the aggressive downscaling of IC structure by Moore's law, following interconnect in IC chip has also entered below 10 nm dimension of half-pitch. At these feature sizes, Cu's resistivity dramatically increases due to increased grain boundary and surface scattering. The residual resistivity of a metal is a collection of all other scattering sites present in the material, specifically flaws and impurities, because the degrees of thermal vibration have not yet been activated at low enough temperature. There will be a variety of defects in the microstructure of polycrystalline metals, including grain boundaries, dislocations, and vacancies. Impurities in a metal can act as a scattering site in addition to flaws. Augustus Matthiessen, a British scientist, was the first to include all of these factors in a metal's resistivity in 1864. The resistivity of Cu interconnects was determined by Matthiessne's rule, which describes a resistivity of interconnect as its bulk resistivity, surface scattering, and grain boundary scattering of interconnect structure, as shown in **Equation 1-5**[22]

$$\boldsymbol{\rho_{total} = \rho_{th} + \rho_{imp} + \rho_{def}} \quad \text{(Eq 1.5)}$$

where ρ_{th} is the resistivity due to temperature, ρ_{imp} is the resistivity due to impurities, and ρ_{def} is the the resistivity due to defects. While temperature, defects, and impurities do in fact contribute to resistivity, some deviation from the simple summation postulated by Matthiessen has been reported for specific metals.

From a process perspective, when critical dimensions reduce, it becomes more difficult to fill these vertical and horizontal interconnects, and reliability decreases as well. The industry needs to address these challenges and trade-offs so that pitch scaling can continue. Copper (Cu) is predicted to be the dominant connecting metal until at least 2025, while non-Cu solutions (such as Co and Ru) are expected to be utilized for local interconnects (M0). Due to electromigration limitations, Pt group metals such as Cobalt (Co) will be embedded at the local interconnect, particularly for the via, due to its better integration window to fill narrow trenches on top of electromigration performance as well as lower resistance compared to Cu at scaled dimensions. Even when an increase in resistivity owing to electron scattering in Cu or greater bulk resistivity in Ru, Co, and Ir is already visible, a hierarchical wiring method such as scaling line length and width together can still solve the problem.

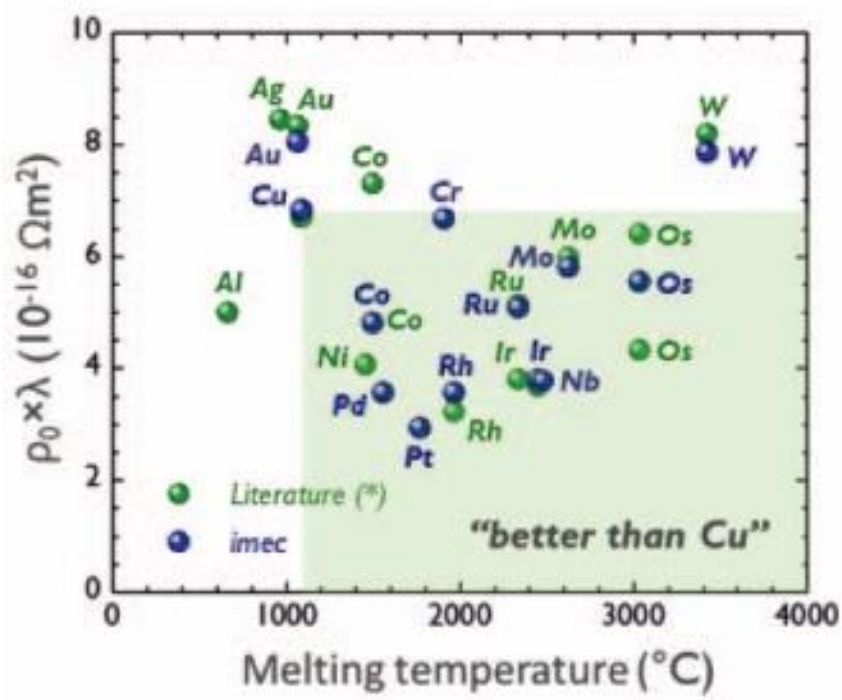


Figure 1-11. FoM (Figure of Merit, mean free path times bulk resistivity) versus melting temperature for different metals.[23]

Accordingly, industry has to be looking towards new conductors to solve some of these challenges. Several metal candidate elements has been emerged to replace conventional Cu metallization. That is Pt group metals, such as Ru, Co, and Ir.[24] Although Ru, Co, and Ir have higher bulk resistivity (ρ_o) than Cu, their lower mean free path leads to a lower FoM (figure of merit) that represents a bulk resistivity times mean free path value. It is expected that metals with lower FoM will have less size induced resistivity increase in

the regime of a few nm of half pitch. Considering that the half pitch of interconnects in future technological nodes will be as low as 10 nm or below, these new conductors could be possible replacements for Cu metallization for the future technological nodes.[10]

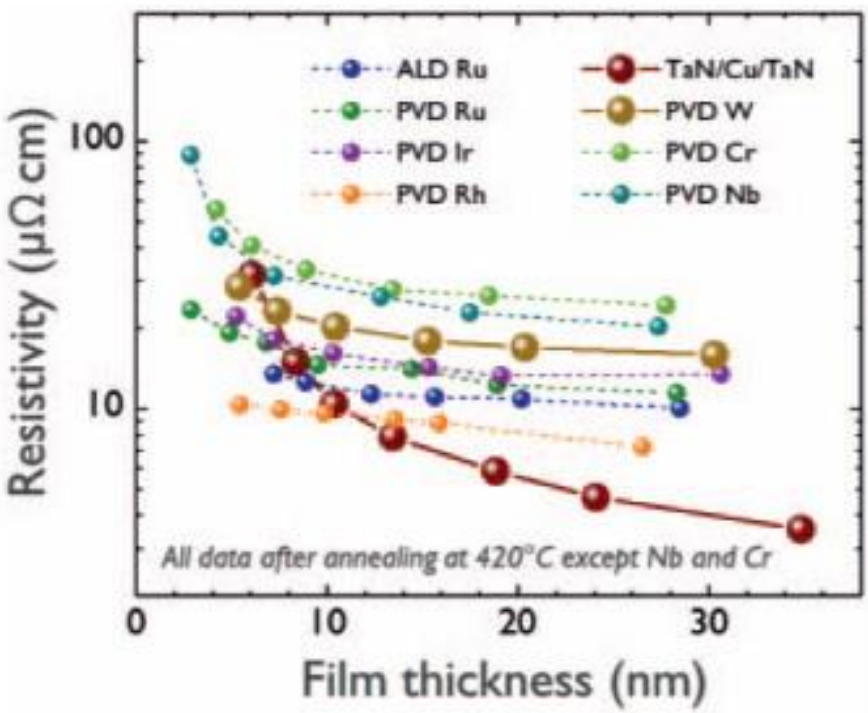


Figure 1-12. Thin film resistivity versus film thickness for different metals.[23]

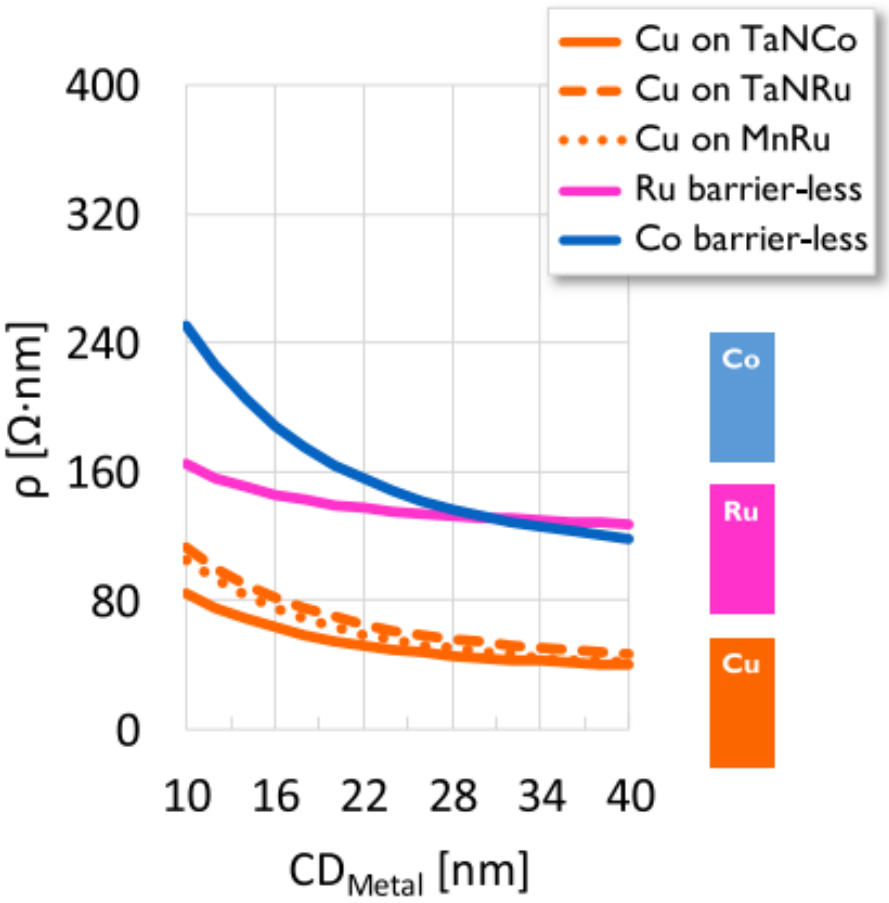


Figure 1-13. Resistivity as a function of metal CD (AR = 2) for Cu, Ru, and Co fills. (N.B.: CDMetal is metal width only, excluding the metal barrier.) For the same metal cross-section, Cu outperforms Ru and Co. Ru resistivity exhibits a relative flat behavior and a crossover with Co occurs at around 30 nm metal CD. Cu resistivity is the lowest for TaNCo and the highest for TaNRu.[25]

1.2.2 Intermetal dielectrics (IMD)

As described above section (section 1.1.3), due to the aggressive downscaling of the multi-layer metal wiring, the resistance of the fine metal wires and the capacitance between the closely arranged metal wires has strongly increased. At this point, the RC delay, coming from a resistivity of metal line and a capacitance of intermetal dielectric (IMD) has exponentially increased, which resulted in lowering the operation speed of the device. To address this issue, two kinds of majority approaches have investigated: lowering a resistivity of metal, and introducing low-k dielectric. In the earlier stage of interconnect, Al metal was replaced by Cu, which has the bulk resistivity of 1.68 x 10^{-8} Ohm·m. On the other hand, reducing a dielectric constant of IMD is crucial factor for a fabrication of a next generation memory and logic cell. Replacing conventional SiO_2 (k~4) intermetal dielectric with SiOF et al. which has a dielectric constant below 3. Another ultralow-k dielectric materials, such as highly porous polymeric and metal organic framework has been proposed in the field of research. However, reduction of the dielectric constant of IMD is slowing down in the industrial process, due to their manufacturability and poor stability coming from its chemical, mechanical or adhesive properties. Poor mechanical and chemical stability of ultralow-k dielectric materials results in delamination or damage in dielectric layers during the CMP (Chemical mechanical polishing) process,

which is crucial huddle to jump for implying ultralow-k materials to mass production.

In the manufacturing point of view, a strict requirement of dielectric constant was required in 5 and 3 nm technology node as presented in IRDS 2021 (International Roadmap for Devices and Systems). In this roadmap, a dielectric constant of 2.20 ~ 2.55 would be required for 3 nm technology node. SiCOH or air gap (k=1.0) would be candidates to meet this requirement. Over the last several years, there has been a lot of discussion on practical strategies to overcome the lifespan decrease in small linewidths.

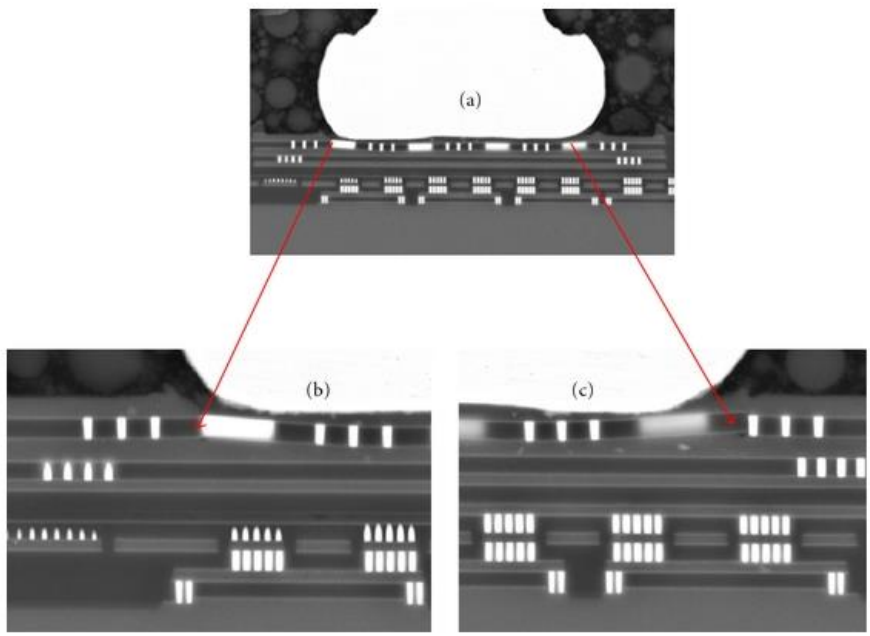


Figure 1-14. (a) Cratering at both Cu ball bond edges of leg (b), (c) IMD (Intermetal dielectric crater and crack) at silicon level.[26]

1.2.3 Reliability- Electromigration

Reliability is an important requirement for almost all users of integrated circuits. Challenge to realize what you need Increased reliability with (1) scaling, (2) new materials and equipment, and (3) more demanding mission profiles. (High temperature, extreme durability, high current) and (4) Increased time and cost constraints. Its reliability challenge is further complicated by the need to implement multiple large-scale technology changes in a short period of time. Interactions between changes can make failure modes difficult to understand and control.[27] In addition, addressing multiple critical issues at the same time puts a strain on limited reliability resources.[28]

In the electromigration point of view, the void is positioned at the cathode end of the connecting wire carrying a single via with a drift velocity dominated by interfacial diffusion, according to an effective scaling model. Lifetime is predicted to scale with w*h/j, where w is the linewidth (or through diameter), h is the connection thickness, and j is the current density, according to the effective scaling model.[29] While the geometrical model predicts that each subsequent generation's lifetime will be cut in half, it can also be influenced by slight process differences in connection dimensions. The connection geometry scaling limits J_{max} (maximum equivalent DC

current density) and JEM (DC current density at the electromigration limit). J_{max} rises with scaling as the connection cross-section shrinks and the maximum operational frequency rises. Beyond the 45nm node, recent studies suggest that grain structure plays an increasingly crucial role in determining drift velocity and consequently EM dependability. Process solutions using a Cu alloy seed layer (e.g., Al or Mn) have proven to be the most effective way to extend lifespan. The use of the short length effect and the implantation of a thin metal layer (e.g., CoWP or CVD Co) between the Cu trench and the dielectric SiCN barrier are also feasible candidates. The short length effect has dominated the current density design rule for interconnects, and has effectively extended the current carrying capabilities of conductor lines.

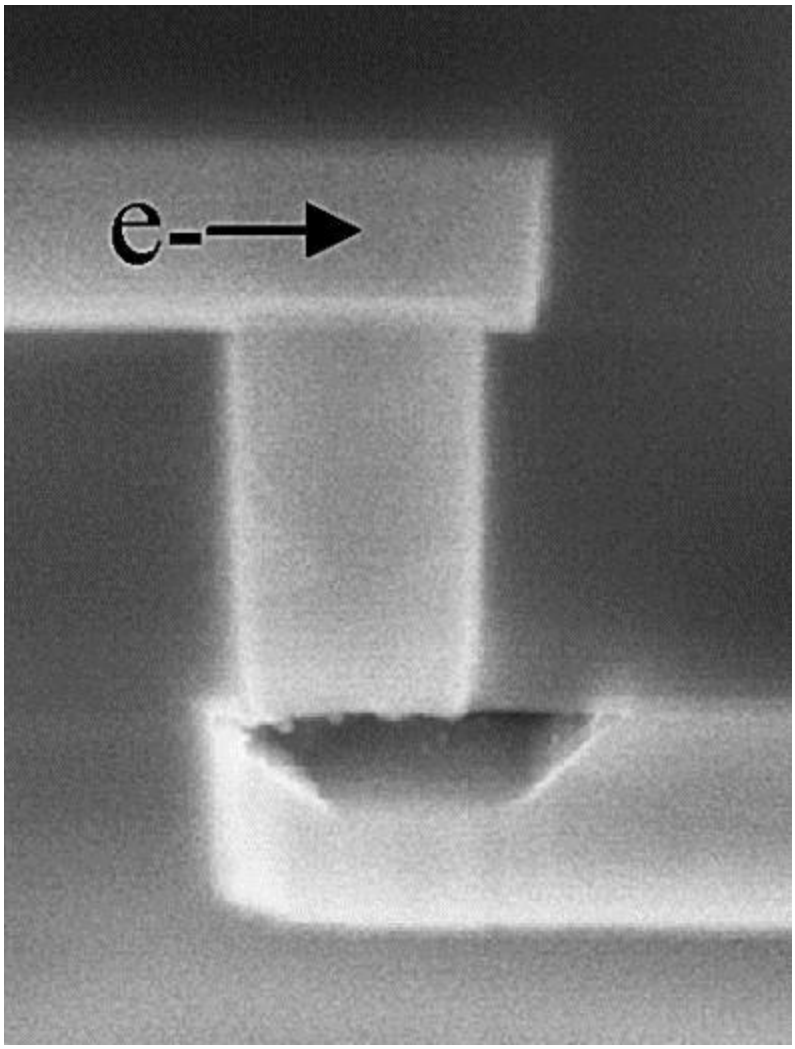


Figure 1-15. An example of electromigration-induced voiding, which can lead to interconnect failure by open circuit.[27]

1.2.4 Barrier material

As described above section (see section 1.1.*), Cu diffusion barrier is essential to Cu interconnect to prevent a diffusion of Cu species into intermetal dielectric (IMD) materials that should result in shortage of neighboring metal line. This Cu diffusion barrier layer should not only inhibit Cu diffusion into the neighboring dielectric, but also provide an appropriate, high-quality interface with Cu in order to restrict vacancy diffusion and ensure acceptable electromigration lifetimes. The industry solution Ta(N) has been well-known.

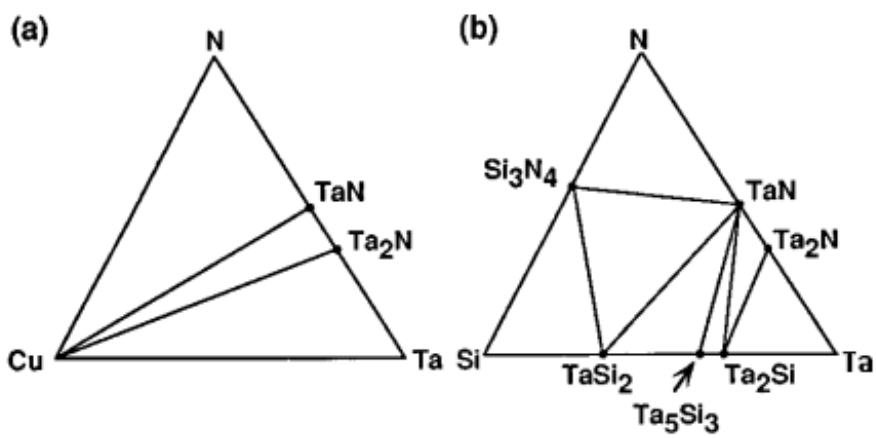


Figure 1-17. Isothermal section of a ternary phase diagram of (a) Cu-Ta-N and (b) Ta-N-Si systems drawn at 900K.[30]

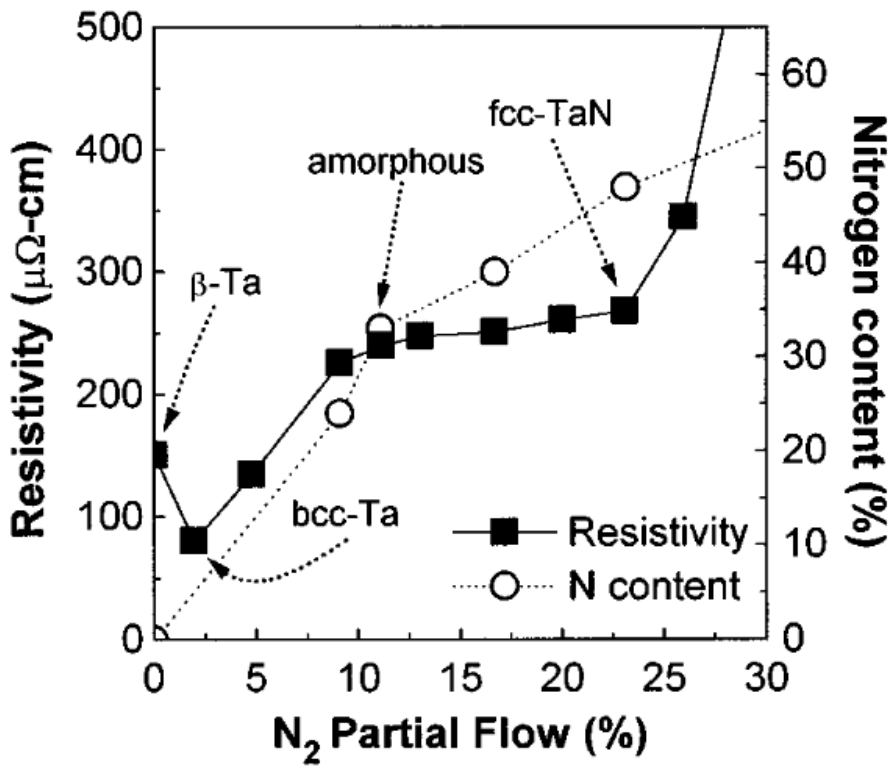


Figure 1-16. The electrical resistivity and the nitrogen content of the films deposited at various N_2/Ar gas ratios.[30]

As a material that satisfies the requirements of diffusion barrier mentioned earlier, the Ta liner/TaN barrier system first proposed by my supervisor, Professor Ki-Bum Kim, is still being applied to practical semiconductor processes. They published the paper about the TaN Cu diffusion barrier in 1995.[30] As the N_2 partial flow of the sputtering gas is increased in the DC magnetron sputtering process of Ta, Beta-Ta/ bcc Ta mixture / bcc Ta / amorphous Ta_2N / FCC TaN This is the content confirming that the sequential phase change appears. In addition to Cu migration as a failure mechanism of the barrier, the occurrence of failure due to the interfacial reaction between the TaN barrier and Si at high temperature was confirmed by analyzing the Ta-Si-N ternary phase diagram, XRD, and AES depth profile at 900℃.

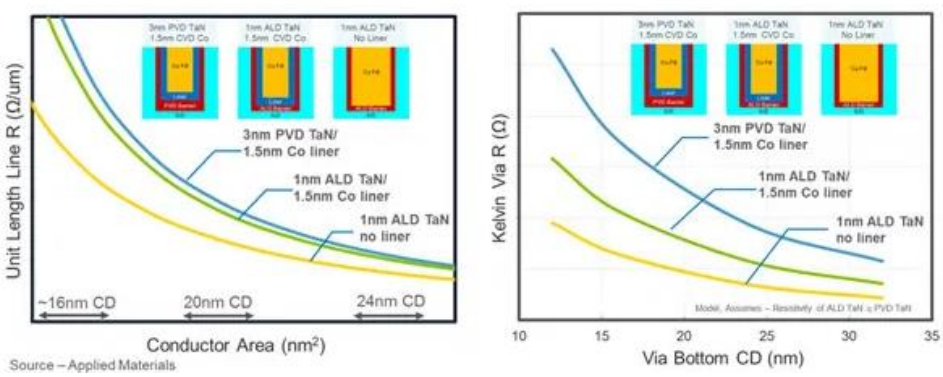


Figure 1-18. (a) Interconnect line resistance as a function of conductor area along with various thicknesses of diffusion barrier and liner materials, and following (b) Kelvin via resistance as a function of via bottom CD.

However, these Ta/TaN barriers have reached their limits as IC dimension scaling has progressed aggressively. First, as the wire pitch decreases to the level of several tens of nm, the portion occupied by the barrier in the total wire volume increases, which greatly increases the overall wiring resistance. **Figure 1-18** shows the result of plotting the total wiring resistance according to the wire pitch and the material and thickness of the Cu diffusion barrier applied thereto. These plots were calculated based on the steinhogl model below.[31]

$$\rho(Cu)_{eff} = \frac{\rho(Cu)_{bulk}}{\left(1-\frac{B}{H}\right)\left(1-2\frac{B}{W}\right)+\left(\frac{1.7}{\rho_B}\right)\left(\frac{B}{W}\right)\left(2+\frac{W}{H}-2\frac{B}{H}\right)}[\mu\Omega \cdot cm] \quad \text{(Eq 1-6)}$$

where W and H are the width and height of Cu interconnect, and B is the thickness of diffusion barrier, and ρ_B is a resistivity of the diffusion barrier. In the **Equation 1-6**, it can be seen that the effective resistivity of Cu wire is affected by the thickness of the barrier and the resistivity of the barrier itself.

In addition, reducing a cross-sectional area of Cu line in metallization, namely restricted Cu line volume also a crucial issue for the next generation Cu metallization. Diffusion barriers and adhesion liners, which are required for Cu interconnects, will occupy a growing percentage of the line volume, resulting in an even greater increase in line resistance. Such barriers and liners do not scale well because the dielectric breakdown and electromigration properties are badly impacted by significantly lower thicknesses of Cu diffusion barrier.

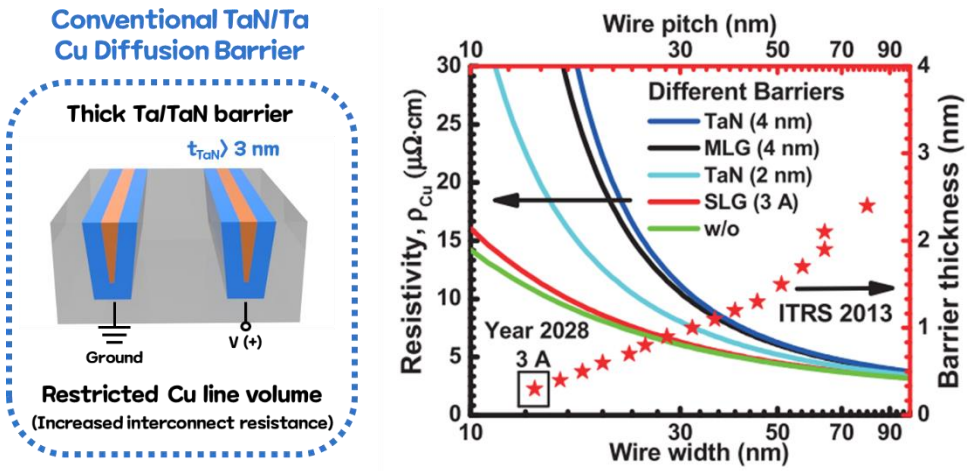


Figure 1-19. Restricted Cu line volume and following increasement in interconnect resistance. For a next generation Cu interconnect, as wire width decreases, resistivity of Cu line

As shown in **Figure 1-18 and Figure 1-19**, when the current 4 nm or 2 nm level of TaN barrier is applied, it can be seen that the wiring specific resistance increases to the level of several tens of um cm at a wire pitch of 30 nm or less. According to ITRS roadmap, which proposes an overall roadmap for semiconductor systems, it is predicted that a thin diffusion barrier of 3A level will be required by 2028 to secure Cu wiring resistance according to a decrease in wire pitch.

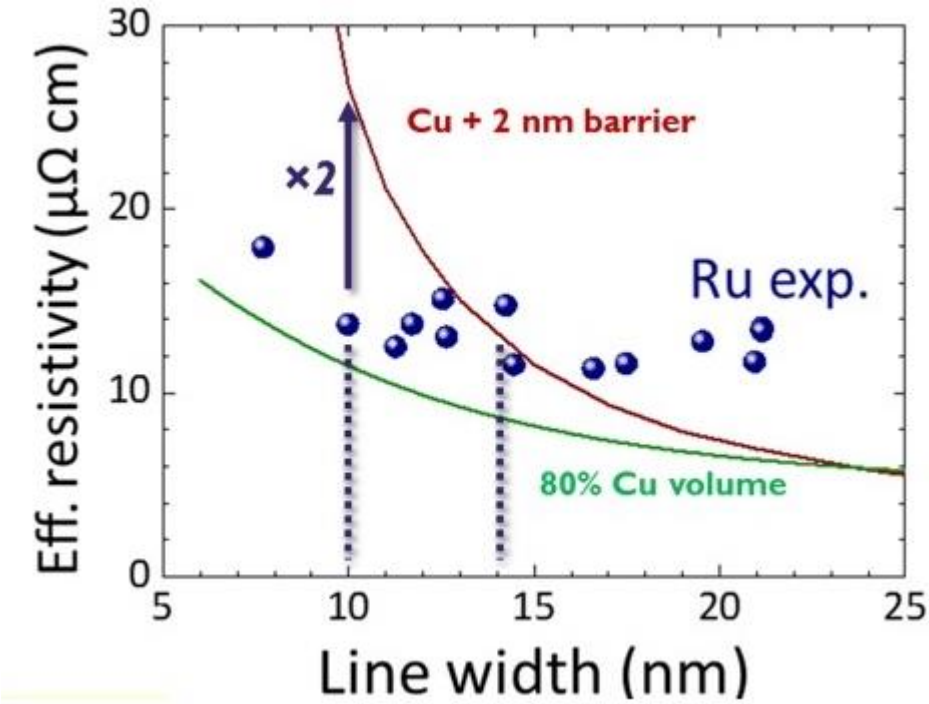


Figure 1-20. Effective resistivity as a function of linewidth for copper and ruthenium. Image courtesy of IMEC.

However, when scaling the existing TaN barrier to the level of 1 nm, proper Cu blocking performance cannot be secured. According to the workshop results from IMEC and Global Foundry in 2015,[32] as shown in **Figure 1-20 and Table 1-1**, when TaN barrier thickness is lowered to 1 nm or less, Cu interconnect structure resulted in failure due to the significant diffusion of Cu ions into subsequence dielectric materials. In addition, when the TaN thickness is lowered to 1 nm, the resistivity of the barrier itself increases by

more than 2 orders of magnitude, and there are additional issues such as difficulty in securing thermal stability. Therefore, there is a strong demand for a diffusion barrier of a new material that can replace the existing TaN.

Thickness [nm]	TDDB at 100 ℃	TDDB at 200 ℃
TaN [0.5]	Failure	Not measured
TaN [1.0]	Failure	Failure
TaN [2.0]	Withstand	Withstand
Ta/TaN [0.5/0.5]	Withstand	Failure

Table 1-1. Summary of barrier/liner combinations, thickness in nm, and reliability test results: TDDB at 100°C, 200°C.[32]

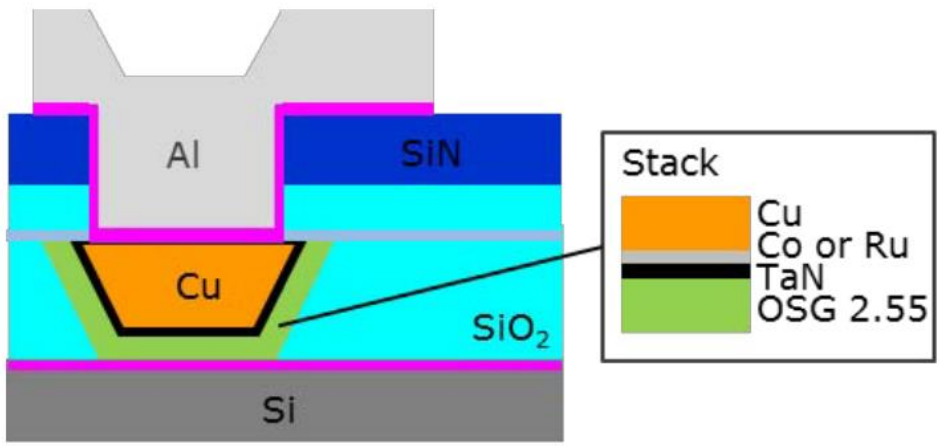


Figure 1-21. Planar capacitor (pcap) details for the experiments of Table 1-1. 60 nm OSG was followed by varying thickness PVD TaN barrier and PVC Co or Ru liner, followed by PVD Cu seed and electroplated Cu.

References

(1) *IBM's 100 icons of progress: Cu interconnects*. IBM, https://www.ibm.com/ibm/history/ibm100/us/en/icons/copperchip/

(2) Aboelfotoh, M.; Svensson, B. Copper passivation of boron in silicon and boron reactivation kinetics. *Physical Review B* **1991**, *44* (23), 12742.

(3) Andricacos, P. C. Copper on-chip interconnections. *The Electrochemical Society Interface* **1999**, *8* (1), 6.

(4) Kilby, J. Miniaturized electronic circuits. *USP3, 138,743* **1964**.

(5) McBrayer, J. D.; Swanson, R. M.; Sigmon, T. W. Diffusion of Metals in Silicon Dioxide. *Journal of The Electrochemical Society* **1986**, *133* (6), 1242-1246.

(6) Moore, G. E. Cramming more components onto integrated circuits. McGraw-Hill New York, NY, USA:: 1965.

(7) Mühlbacher, M.; Greczynski, G.; Sartory, B.; Mendez-Martin, F.; Schalk, N.; Lu, J.; Hultman, L.; Mitterer, C. TiN diffusion barrier failure by the formation of Cu3Si investigated by electron microscopy and atom probe tomography. *Journal of Vacuum Science & Technology B* **2016**, *34* (2), 022202.

(8) Noyce, R. N. Semiconductor device-and-lead structure. U.S. Patent: 1961.

(9) Gupta, T. Introduction. In *Copper Interconnect Technology*, Springer New York, 2009; pp 1-65.

(10) Havemann, R. H.; Hutchby, J. A. High-performance interconnects: An integration overview. *Proceedings of the IEEE* **2001**, *89* (5), 586-601.

(11) Shamiryan, D.; Abell, T.; Iacopi, F.; Maex, K. Low-k dielectric materials. *Materials Today* **2004**, *7* (1), 34-39.

(12) Hong, S.; Lee, C.-S.; Lee, M.-H.; Lee, Y.; Ma, K. Y.; Kim, G.; Yoon, S. I.; Ihm, K.; Kim, K.-J.; Shin, T. J.; et al. Ultralow-dielectric-constant amorphous boron nitride. *Nature* **2020**, *582* (7813), 511-514.

(13) Jeng, S.-P.; Havemann, R. H.; Chang, M.-C. Process integration and manufacturasility issues for high performance multilevel interconnect. *MRS Online Proceedings Library (OPL)* **1994**, *337*. Pileggi, L. Coping with RC(L) interconnect design headaches. In *Proceedings of IEEE International Conference on Computer Aided Design (ICCAD)*, 5-9 Nov. 1995, 1995; pp 246-253.

(14) Lee, J.; Ahn, S. H.; Jung, I.; Han, K.-H.; Kim, G.; Nam, S.-D.; Jeon, W. S.; Kim, B. H.; Choi, G. H.; Choi, S. Robust porous SiOCH (k= 2.5) for 28nm and beyond technology node. In *2011 IEEE International Interconnect Technology Conference*, 2011; IEEE: pp 1-3.

(15) Edelstein, D.; Uzoh, C.; Cabral, C.; DeHaven, P.; Buchwalter, P.; Simon, A.; Cooney, E.; Malhotra, S.; Klaus, D.; Rathore, H.; et al. A high performance liner for copper damascene interconnects. In *Proceedings of the IEEE 2001 International Interconnect Technology Conference (Cat. No.01EX461)*, 6-6 June 2001, 2001; pp 9-11.

(16) Catania, P.; Doyle, J. P.; Cuomo, J. J. Low resistivity body-centered cubic tantalum thin films as diffusion barriers between copper and silicon. *Journal of Vacuum Science & Technology A* **1992**, *10* (5), 3318-3321.

(17) Holloway, K.; Fryer, P. M. Tantalum as a diffusion barrier between copper and silicon. *Applied Physics Letters* **1990**, *57* (17), 1736-1738.

(18) Holloway, K.; Fryer, P. M.; Jr., C. C.; Harper, J. M. E.; Bailey, P. J.; Kelleher, K. H. Tantalum as a diffusion barrier between copper and silicon: Failure mechanism and effect of nitrogen additions. *Journal of Applied Physics* **1992**, *71* (11), 5433-5444.

(19) Park, K.-S.; Kim, S. Seedless Copper Electrodeposition onto Tungsten Diffusion Barrier. *Journal of The Electrochemical Society* **2010**, *157* (12), D609.

(20) Pauleau, Y.; Dassapa, F. C.; Lami, P.; Oberlin, J. C.; Romagna, F. Silicide formation in metal/Si structures and diffusion barrier properties of CVD tungsten films. *Journal of Materials Research* **1989**, *4* (1), 156-162.

(21) Shen, B. W.; Smith, G. C.; Anthony, J. M.; Matyi, R. J. Diffusion barrier properties of thin selective chemical vapor deposited tungsten films. *Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena* **1986**, *4* (6), 1369-1376.

(22) Farahani, M. M.; Turner, T. E.; Barnes, J. J. Evaluation of Titanium as a Diffusion Barrier Between Aluminum and Silicon for 1.2 μm CMOS Integrated Circuits. *Journal of The Electrochemical Society* **1987**, *134* (11), 2835-2845.

(23) Li, B.; Christiansen, C.; Badami, D.; Yang, C.-C. Electromigration challenges for advanced on-chip Cu interconnects. *Microelectronics Reliability* **2014**, *54* (4), 712-724.

(24) Auth, C.; Aliyarukunju, A.; Asoro, M.; Bergstrom, D.; Bhagwat, V.; Birdsall, J.; Bisnik, N.; Buehler, M.; Chikarmane, V.; Ding, G.; et al. A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects. In *2017 IEEE International Electron Devices Meeting (IEDM)*, 2-6 Dec. 2017, 2017; pp 29.21.21-29.21.24.

(25) Blech, I. A. Electromigration in Thin Aluminum Films on Titanium Nitride. *J Appl Phys* **1976**, *47* (4), 1203-1208.

(22) Bass, J. Deviations from Matthiessen's rule. *Advances in Physics* **1972**, *21* (91), 431-604.

(26) Croes, K.; Adelmann, C.; Wilson, C. J.; Zahedmanesh, H.; Pedreira, O. V.; Wu, C.; Leśniewska, A.; Oprins, H.; Beyne, S.; Ciofi, I.; et al. Interconnect metals beyond copper: reliability challenges and opportunities. In *2018 IEEE International Electron Devices Meeting (IEDM)*, 1-5 Dec. 2018, 2018; pp 5.3.1-5.3.4.

(27) Gall, D. Electron mean free path in elemental metals. *J Appl Phys* **2016**, *119* (8), 085101.

(28) Ciofi, I.; Roussel, P. J.; Baert, R.; Contino, A.; Gupta, A.; Croes, K.; Wilson, C. J.; Mocuta, D.; Tőkei, Z. RC Benefits of Advanced Metallization Options. *Ieee T Electron Dev* **2019**, *66* (5), 2339-2345.

(29) Gan, C. L.; Ng, E. K.; Chan, B. L.; Hashim, U.; Classe, F. C. Technical Barriers and Development of Cu Wirebonding in Nanoelectronics Device Packaging. *J Nanomater* **2012**, *2012*.

(30) Hau-Riege, C. S. An introduction to Cu electromigration. *Microelectron Reliab* **2004**, *44* (2), 195-205.

(31) Liu, Y. C.; Lin, S. K. A Critical Review on the Electromigration Effect, the Electroplastic Effect, and Perspectives on the Effects of Electric Current Upon Alloy Phase Stability. *Jom-Us* **2019**, *71* (9), 3094-3106.

(32) Pierce, D. G.; Brusius, P. G. Electromigration: A review. *Microelectron*

Reliab **1997**, *37* (7), 1053-1072.

(33) Min, K. H.; Chun, K. C.; Kim, K. B. Comparative study of tantalum and tantalum nitrides (Ta2N and TaN) as a diffusion barrier for Cu metallization. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **1996**, *14* (5), 3263-3269.

(34) Steinhögl, W.; Schindler, G.; Steinlesberger, G.; Engelhardt, M. Size-dependent resistivity of metallic wires in the mesoscopic range. *Phys Rev B* **2002**, *66* (7), 075414.

(35) Witt, C.; Yeap, K. B.; Leśniewska, A.; Wan, D.; Jordan, N.; Ciofi, I.; Wu, C.; Tokei, Z. Testing The Limits of TaN Barrier Scaling. In *2018 IEEE International Interconnect Technology Conference (IITC)*, 4-7 June 2018, 2018; pp 54-56.

Chapter 2.

Effect of Bilayer Period of Atomic Layer Deposition (ALD) on the Growth Behavior and Electrical Properties of Amorphous In-Zn-O Film

This chapter is based on the paper published in

ACS Applied Materials & Interfaces, (2020)

2.1 Introduction

Transparent conducting oxides (TCOs) have attracted considerable attention as a key material in modern optoelectronic devices on account of their high optical transmittance and electrical conductivity.[1-3] Indium-tin-oxide (ITO) is one of the most widely utilized multicomponent metal oxides as a market-leading TCO due to its low resistivity of ~ 1×10^{-4} Ω·cm with an electron concentration of up to 10^{21} cm^{-3}.[4] Recently, indium-zinc-oxide (IZO) has also attracted significant interest due to its superior electron mobility (5–60 $cm^2/V \cdot s$) and thermal stability up to 600 °C.[5-11] The resistivity of IZO films was reported to vary in a wide range (from 10^{-4} to 10^{-1} Ω·cm) depending on the chemical composition. Therefore, IZO films not only can fulfill the requirements of the TCO but also that of the active materials of the thin film transistor (TFT) due to the high on-off ratio (10^4–10^6 with a wide bandgap of 3.8–4.0 eV).[10-13] In particular, the IZO films demonstrate their lowest resistivity in an amorphous phase, which offers a unique advantage in applying flexible electronics due to the inherent flexibility of the amorphous phase compared with that of the crystalline phase.[12] In addition, the IZO nanolaminate, alternately stacked with layers of In_2O_3 and ZnO that are nanometers thick, has been employed as active materials of TFT with high field-effect mobility of up to 30 $cm^2/V \cdot s$ due to the formation of a 2-dimensional electron gas (2DEG) layer at its heterointerfaces between In_2O_3

and ZnO.[14]

The IZO thin films with varying compositions have been deposited by various deposition technologies, such as sputtering[6-8, 10, 13, 15-17], pulsed laser deposition (PLD)[18], chemical vapor deposition,[19] and wet-solution process.[20-22] Among them, atomic layer deposition (ALD) has garnered significant attention because of its unique advantages of precise controllability of the film thickness and excellent conformality.[23-24] Moreover, the self-limiting surface reaction in ALD allows precise control of the stoichiometry of the film at the atomic level.[23, 25-26] In general, the ALD-IZO film is produced by the sequential deposition of several cycles of the In-O and Zn-O supercycles.[9, 12, 23, 25, 27-28] Here, a supercycle is defined as an ALD unit cell consisting of a certain number of successive In-O and Zn-O ALD cycles, as shown in **Figure 2-1**. The properties of the ALD film can be modulated by two parameters in one supercycle, i.e., the cycle ratio in one supercycle, and the total number of ALD cycles in one supercycle, which is designated as the bilayer period (n_b) in this report. The former has a crucial effect on the stoichiometry of the ALD film, as postulated by numerous previous reports on the ALD-IZO.[9, 12, 25, 27-30]. As a representative example, our group systematically investigated the structural and electrical properties of ALD-IZO films with respect to the cycle ratio of In-O and Zn-O.[12] We determined that the ALD-IZO films exhibited an amorphous phase within 43.2–91.5 at% In and demonstrated the lowest

resistivity (3.9×10^{-4} Ω·cm) at 83.2 at% In, thereby revealing a remarkable property of the ALD-IZO for the TCO.[12] On the other hand, the n_b is also a critical factor influencing the microstructure evolution, either with the well-intermixed alloy or the layered structure, considering that the n_b controls the thickness of each sublayer.[25] This structural evolution can be determined by the solid-state diffusion in the deposited film, which is related to the thickness of each sublayer and the diffusion characteristics of the cations into the adjacent layers. The effect of n_b on the film microstructure has been reported for ALD-ZnO/Al_2O_3, ZnO/SnO_2, and SnO_2/TiO_2 films.[31-40] In the case of Al_2O_3/ZnO,[37] it has been reported that the grain size of the ZnO sublayer decreased as the n_b decreased; and, the film microstructure eventually transformed from nanocrystalline into amorphous. As a result, the elastic modulus of the Al_2O_3/ZnO nanolaminate decreased as the n_b decreased. The aforementioned was described by the inverse Hall-Petch relation, which predicts a decrease in hardness with decreasing grain size of nanocrystalline materials.[41] Additionally, in the case of Al_2O_3/TiO_2, a critical bilayer thickness of 1.5 nm was required to maintain the nanolaminate structure, which was confirmed by the intensive X-ray reflectivity measurement.[32]

As previously reported, the n_b functions as a critical factor in the microstructure evolution and the accompanying physical properties of the ALD-IZO film. However, to our knowledge, there is no comprehensive study

on the effect of the n_b on the ALD-IZO film. Therefore, we investigated the means by which the physical properties and microstructure evolution of the ALD-IZO film was modified by the n_b systematically at a fixed cycle ratio. The ALD-IZO films were deposited with an n_b from 10 to 200 cycles (10, 40, 100, 130, 160, and 200 cycles) for a fixed cycle ratio of In-O: Zn-O = 9:1, since this cycle ratio provides the lowest resistivity film in our previous work.[12] The film growth behavior, chemical composition, microstructure, and electrical properties of the ALD-IZO films were studied by varying the n_b. An improved understanding of the n_b dependency of ALD-IZO films could facilitate the reliable synthesis of IZO thin films toward their potential integration into future electronics.

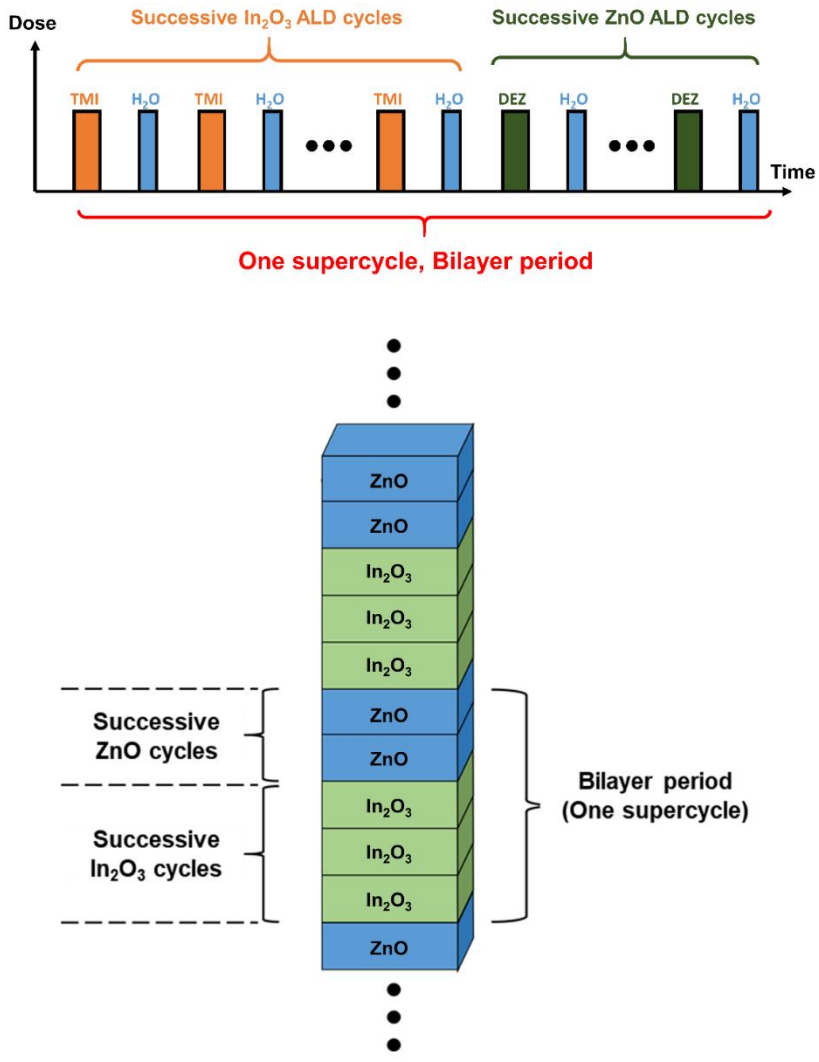


Figure 2-1. ALD process design of IZO films for different bilayer periods. In this work, IZO ALD processes were designed with the varied bilayer period, which was defined as the total number of ALD cycles in one supercycle. One supercycle is the ALD unit cell consisting of a certain number of successive In-O and Zn-O ALD cycles.

2.2 Experimental details

In our previous research, we reported the ALD-IZO by varying the cycle ratio of In_2O_3 and ZnO.[12] Therefore, our deposition was conducted by adopting the reported method. All IZO thin films were deposited in a traveling-wave type ALD apparatus (LUCIDA D-100, NCD Co., Ltd., Korea) at a deposition temperature of 220 °C. Thermally grown SiO_2 (100 nm) on Si wafers were used as a substrate. Diethylzinc (DEZ, EG Chem Co., Ltd., Korea) and trimethylindium (TMI, EG Chem Co., Ltd., Korea) were used as precursors for the ZnO and In_2O_3, respectively. The DEZ canister was cooled to 10 °C, whereas the TMI canister was heated to 50 °C and the working pressure increased to 50 mTorr during exposure. Water vapor maintained at 25 °C was used as a reactant. The optimized ALD cycle consists of a 1 s precursor pulsing combined with a 5 s extended exposure without evacuation – 20 s N_2 purging – H_2O pulsing (0.5 s for ZnO and 3 s for In_2O_3) – 20 s N_2 purging. The IZO films were deposited with varying numbers of successive ZnO ALD cycles while maintaining the same 10% ZnO ALD cycle ratio. The number of total ALD cycles of IZO films was adjusted to 800 cycles to investigate the growth rate of IZO films and electrical properties affected by the number of successive ZnO cycles. The film thicknesses were examined by ellipsometry (Gartner Scientific Corp., L2W15S830) at a wavelength of 632.8 nm. The structural characterizations were identified using X-ray

diffractometry (Bruker, New D8 Advance), transmission electron microscopy (TEM, JEOL, JEM-2100F, and ARM-200F), and X-ray reflectivity (Malvern Panalytical, X'pert Pro). The electrical properties were measured by Hall measurements (BIO-RAD, HL5500PC) using the Van der Pauw configuration. The cation ratios were determined by inductively coupled plasma atomic emission spectroscopy (ICP-AES, Perkin-Elmer, OPTIMA 4300DV).

2.3 Results and discussion

2.3.1 Design of ALD sequences

Based on our previous report on the ALD-IZO, the cycle ratio of In-O: Zn-O = 9:1 is selected because it demonstrated the lowest resistivity (3.9×10^{-4} Ω·cm) under various deposition conditions. The cation ratio of this low-resistivity film was measured as 83.2% of [In/(In+Zn)] by ICP-AES, which indicates that it is a well-intermixed amorphous phase (43.2–91.5% at% [In/(In+Zn)]). To investigate the microstructure and physical properties of the ALD-IZO film as a function of the n_b, it was varied from 10 to 200 cycles, as summarized in **Table 2-1**. For instance, IZO[180:20], designated as n_b = 200 cycles, was deposited by repeating the supercycle consisting of 180 successive cycles of In-O and 20 cycles of Zn-O. Throughout the entire experiment, the total number of ALD cycles was adjusted to approximately 800 cycles to exclude the effect of the ALD cycle ratio on the growth behavior and physical properties of films.[12] Therefore, the number of repeated supercycles decreased from 80 to 4 as the n_b increased.

Samples	Bilayer period (n_b)	The number of successive ALD cycles in one supercycle		The number of repeated supercycles	The # of total ALD cycles
		In-O	Zn-O		
IZO (9:1)	10	9	1	80	800
IZO (18:2)	20	18	2	40	800
IZO (27:3)	30	27	3	27	810
IZO (36:4)	40	36	4	20	800
IZO (90:10)	100	90	10	8	800
IZO (117:13)	130	117	13	6	780
IZO (144:16)	160	144	16	5	800
IZO (180:20)	200	180	20	4	800

Table 2-1. ALD process design of IZO films for different bilayer periods (n_b). The ALD cycle ratio (In-O/Zn-O) was fixed at In-O: Zn-O = 9:1 and the total number of ALD cycles were adjusted to 800 for whole samples in this study.

2.3.2 Film growth behavior

The growth rates of the ALD-IZO films (nm/cycle) and the cation ratios (at%) were investigated with increasing values of the n_b, which is shown in **Figure 2-2**. The thicknesses of IZO films were examined by ellipsometry, and the growth rates were determined by dividing the film thickness by the total number of ALD cycles. Figure 2-2 (a) shows the growth rate of the IZO films as a function of the n_b. It is noted that the growth behavior is divided into two separate regions. For the shorter n_b from 10 to 40 cycles (*i.e.*, ALD supercycle from IZO[9:1] to IZO[36:4]), the growth rate remains almost constant at 0.03 nm/cycle, which is identical to that of the amorphous IZO[9:1].[12] In contrast, for the extended n_b from 100 to 200 cycles (i.e., ALD supercycle from IZO[90:10] to IZO[180:20]), the growth rate increases linearly as the n_b increases. To investigate the growth behavior of In-O and Zn-O during the IZO ALD process, we estimated an expected growth rate of IZO films using the rule of mixture and compared it to measured ones. The estimated growth rate of the IZO film (G_{IZO}) can be calculated as 0.06 nm/cycle by the rule of mixture ($G_{IZO} = 0.9 \times G_{In_2O_3} + 0.1 \times G_{ZnO}$), implying a distinct growth rate of each In_2O_3 ($G_{In_2O_3}$= 0.05 nm/cycle) and ZnO (G_{ZnO}= 0.15 nm/cycle). As shown in Figure 2-2 (a), the measured G_{IZO} was lower than the estimated G_{IZO} over a range of n_b. Also, the value of the measured G_{IZO} approaches to that of the estimated G_{IZO} as the n_b increased (*i.e.*, the

number of interfaces between In-O and Zn-O decreased). This kind of much lower film growth rate and its restoration with increasing the n_b suggests that at least one of the precursors does not grow as well on its counterpart as on itself. A similar growth behavior of ALD ternary oxide was also observed in the ALD-ZnO/Al_2O_3 and ZnO/SnO_x films.[31, 34] Here, analysis on film growth rate with respect to the n_b provides a clue about the inhibited growth on each countersurface. For instance, Mulling *et al.* showed that the growth rate was noticeably lower than the expected value until n_b = 40 cycles (i.e., ZnO: SnO_x = 30:10); however, the growth rate restored when the n_b increased to 160 cycles (i.e., ZnO: SnO_x = 120: 40).[34] This growth behavior is presumed that it was caused by a retarded adsorption of precursors onto its counterpart surface resulting from the surface chemistry during the deposition.

However, it should be noted is that we could not conclude which material's growth are significantly retarded on its counterpart surface at this point. To study that, the chemical composition of the IZO films was characterized as a function of the n_b, as shown in Figure 2-2 (b). When n_b < 40 cycles, the Indium cation ratio (C_{In}) was measured as 84.6%, which is the same level as that of the amorphous IZO with the lowest resistivity (*i.e.*, n_b = 10 cycles with IZO [9:1]). Subsequently, the C_{In} gradually decreased as the n_b increased (i.e., the number of interfaces between In-O and Zn-O decreased). When n_b = 200 cycles, the measured C_{In} exhibited 69.5% which is the same

as the estimated value. Here, C_{In} was estimated by the rule of mixture using the growth rate and film density of the In_2O_3 and ZnO, as seen in Eq.1.

$$C_{In} = \frac{0.9 \times G_{In2O3} \times d_{In}}{0.9 \times G_{In2O3} \times d_{In} + 0.1 \times G_{ZnO} \times d_{Zn}} \times 100(\%) = 69.5\% \qquad \text{(Eq.1)}$$

where, d_{In} (3.77×10^{22} #/cm^3) and d_{Zn} (5.12×10^{22} #/cm^3) are the densities of In in In_2O_3 and Zn in ZnO, respectively.[12] As shown in Figure 2-2 (b), the measured C_{In} was higher than the estimated value. An excess of C_{In} compared to the estimated value over a range of the n_b implies the disruption of ZnO growth on the In_2O_3 surface. Obviously, this deviation between measured and estimated C_{In} values decreased as the number of interfaces between In-O and Zn-O decreased where the disruption of ZnO growth on In_2O_3 occurred (*i.e.*, as the n_b increased). Consequently, based on the analysis of the effect of n_b on film growth rate and cation composition, we could conclude the inhibited growth of ZnO on In_2O_3 surface during ALD IZO process, while a detail mechanism is not available.

As an experimental proof for the retarded adsorption of precursors onto each counterpart surface, *in situ* ellipsometry or *in situ* FTIR study had better show the growth behavior during the ALD process due to its sub-monolayer level of sensitivity. Interrupted adsorption on the counter surface or etching effect coming from incomparable ALD precursors have been reported elsewhere by introducing *in situ* spectroscopy during ALD.

Therefore, *in situ* spectroscopy during the IZO ALD process may give us a direct experimental proof of the retarded adsorption of the Zn precursor on the In_2O_3 surface, and make our statement more reliable. However, since most commercial ALD reactors rarely provide the possibility to attach *in situ* spectroscopic tools, we have to construct a reactor that enables infrared spectroscopy to perform *in situ* FTIR analysis. Thus, even though we accepted all the benefits of these experiments, we have suffered from the difficulty to construct *in situ* spectroscopic equipment with an ALD reactor.

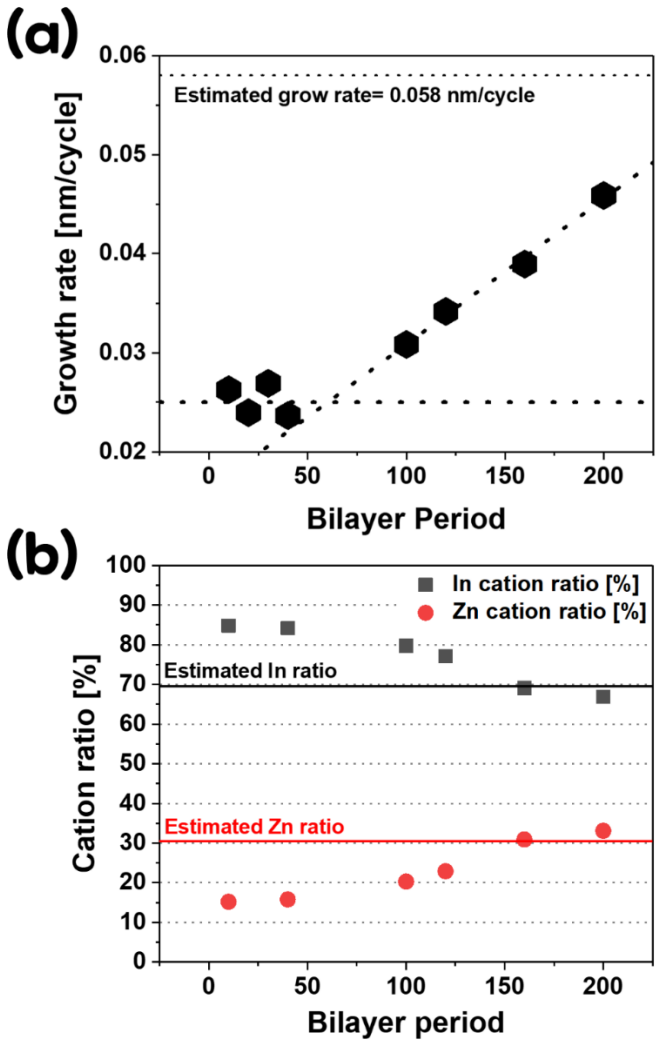


Figure 2-2. Film growth behavior of ALD-IZO films (a) Growth rate of IZO films by varying the n_b. The estimated growth rate is denoted as 0.058 nm/cycle (b) In and Zn cation ratio of ALD-IZO films by varying the n_b. The estimated In and Zn atomic ratio was obtained by Equation (1) and denoted as the black and red line, respectively.

As a following experiment, organized attempts have been made to understand the surface chemistry of ALD IZO. A surface chemistry-oriented simulation and experiment are being prepared for our In-Zn-O and In-Ga-Zn-O thermal ALD. As the first approach, we have attempted to perform a density functional calculation to quantify the adsorption energy of the Zn precursor on the In_2O_3 surfaces. We found that (110) surface of In_2O_3 (bixbyite structure, space group #206 $Ia\bar{3}$) have 80 atoms in the smallest commensurate unit. Thus, a detailed study with adsorbents on the surface, including structure relaxations and thermodynamic calculations are still going on and cannot be reported in this revision period. As a second approach, we have attempted to construct quadrupole mass spectroscopy (QMS) within our thermal ALD system (LUCIDA D100, NCD Co., Ltd.). This work would be incorporated into our ongoing future work that is investigating the growth chemistry of not only ALD In-Zn-O film but also In-Ga-Zn-O film. We expect that the surface chemistry of ALD-IZO will be elucidated in our successive study to achieve clear insight into why the growth process of Zn precursor on the In_2O_3 surface is suppressed.

In our previous work, we attempted to reveal the surface chemistry of ALD-IZO film by investigating the film growth rate and its composition along with the bilayer period. We compared it to the linear combination of its constituent binary oxide rely on the rule of mixture. Consequently, we found

two important observations correlated to the surface chemistry of the ALD-IZO;

1. The measured film growth rates are much lower than the estimated values (the rule of mixture). And then, the film growth rate increases with decreasing the number of interfaces between In_2O_3 and ZnO (*i.e.,* the bilayer period increases). It suggests that at least one of the material's growth is significantly retarded at the interfaces.

2. The measured Zn cation ratios are lower than the estimated values (the rule of mixture) over a range of the bilayer period. An excess of Indium composition compared to the estimated value implies the interrupted growth of Zn contents during the process. Also, the deviation between measured and estimated Zn composition decreases as the number of interfaces between In_2O_3 and ZnO decreases. (*i.e.,* the bilayer period increases)

For instance, the IZO film with the bilayer period of 100 cycles had the 0.03 nm/cycle of growth rate, which is 2-fold lower than the estimated value. In addition, it had the Zn cation ratio of 20.3%, which was noticeably lower than theoretically estimated value (30.5% of Zn/[In+Zn]). Both of much

lower film growth rate and Zn cation ratio rather than estimated values strongly suggest the disrupt growth of ZnO during the ALD-IZO process. Accordingly, we believed that the inhibited growth of the ZnO on the In_2O_3 surface had been sufficiently demonstrated by examining the growth rate and cation composition of IZO films with *ex situ* ellipsometry and ICP-OES.

2.3.3 Microstructure analysis

We observed the structural changes in the ALD-IZO films with the increase in n_b (10, 100, 130, and 200) using XRD and plan-view TEM. All the IZO films, along with the n_b, would be expected to exhibit an amorphous phase since the Indium cation ratio was measured as 66.9–84.8 at% In, which correlates with the amorphous regime (43.2–91.5 at% In), as shown in **Figure 2-3**. (quoted from the results of Dr. Do-Joong Lee *et al.*)[12] For the n_b up to 130 cycles, the typical XRD patterns of amorphous thin films appeared. Whereas, a peak at 2θ = 31° was observed in the longest n_b (200 cycles), as shown in **Figure 2-4**. This broad peak is attributed to the (222) plane of the In_2O_3 bixbyite structure (space group #206 $Ia\bar{3}$, a = 1.0117 nm). This means that the increase in n_b, (*i.e.* the increase in successive cycles of In-O), leads to the formation of the bixbyite In_2O_3 in the IZO film.

More detailed results were obtained in the bright field and dark field plan-view TEM images, the corresponding selected area diffraction patterns (SADP), and the high-resolution images of the ALD-IZO with the n_b of 10, 100, 130, and 200 cycles. (**Figure 2-5**, and **Figure 2-6**) The plan-view TEM results clearly show the change in the crystal structure as a function of the increase in the n_b. The IZO films up to n_b = 100 cycles exhibit a fully amorphous phase with a broad peak near the bixbyite (222). The sporadic

spot patterns of bixbyite In_2O_3 start to appear when n_b = 130 in the SADP (Figure 2-5 (k)). The dark field (Figure 2-5 (g)) and HRTEM images (Figure 2-6 (c)) also confirm that the nanocrystalline bixbyite In_2O_3 exists in the amorphous matrix. The TEM images of the IZO[180:20] reveals that the IZO film forms a completely nanocrystalline bixbyite phase. The bixbyite In_2O_3 grains of ~ 3–15 nm can be observed in the dark-field image. In addition, the HRTEM image with its SADP was well-matched to the In_2O_3 bixbyite structure (indexed in Figure 2-5 (l)).

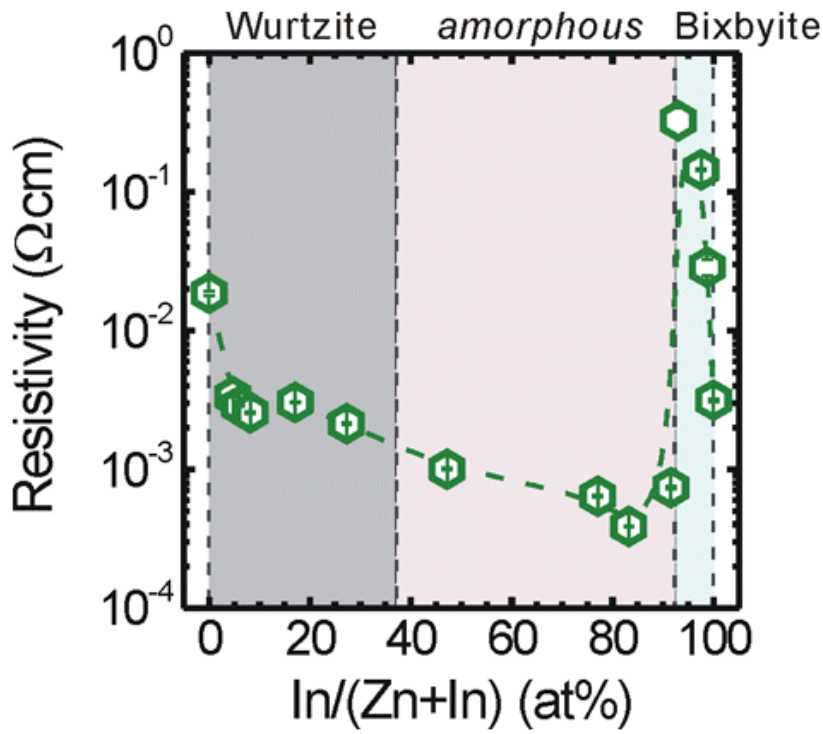


Figure 2-3. Electrical resistivities of ALD-grown IZO films as a function of the measured In cation ratio. Phases of IZO films (Wurtzite, amorphous, and Bixbyite) are grounded as colored boxes.[12]

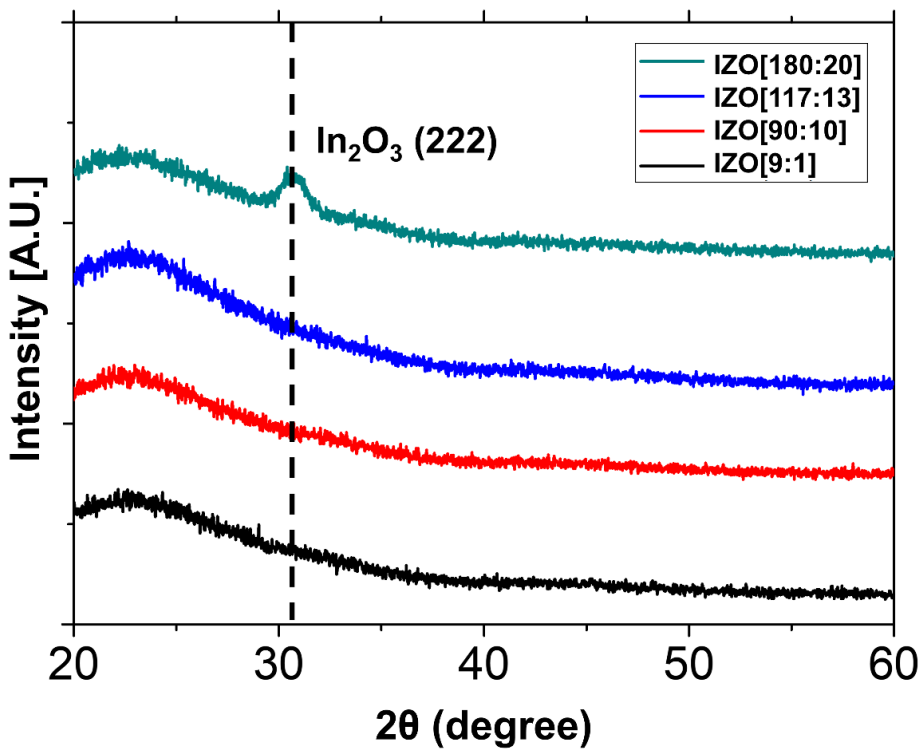


Figure 2-4. X-ray diffraction (XRD) patterns of ALD-IZO films by varying the n_b.

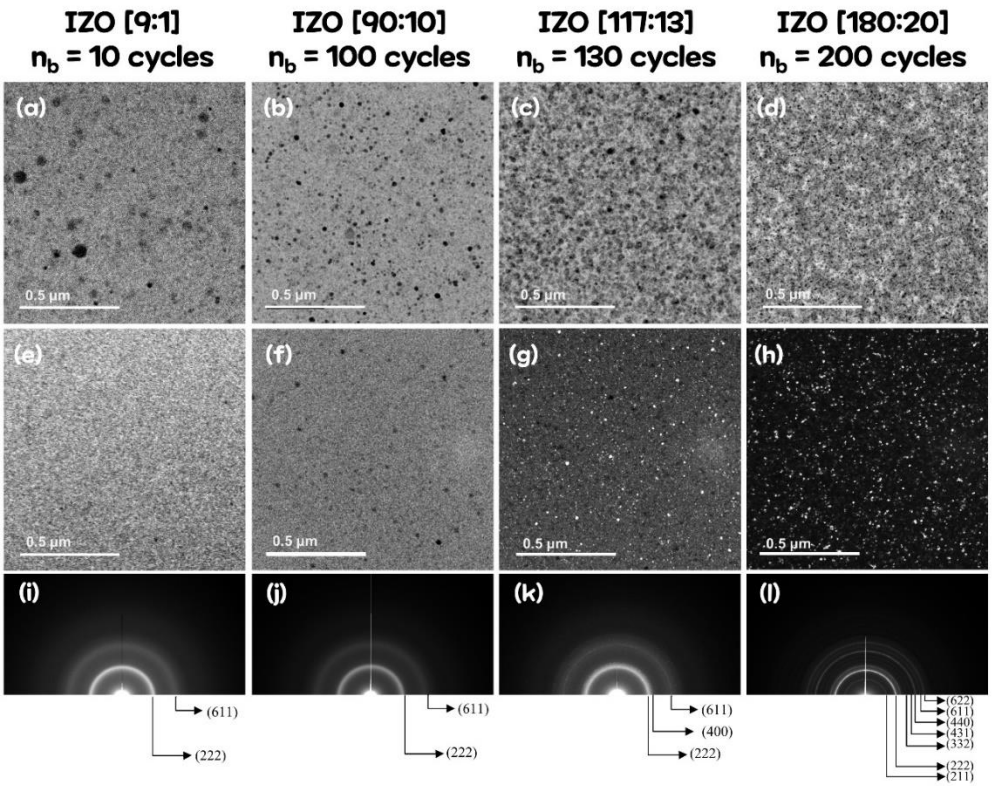


Figure 2-5. Film crystallinity of ALD-IZO films by varying the n_b. TEM Plan-view (a–d) bright fields, (e–h) dark fields, and (i–l) selected area diffraction patterns (SADP) of ALD-IZO films. The n_b of the IZO films was varied with 10 (a, e, i), 100 (b, f, j), 130 (c, g, k), and 200 cycles (d, h, l), respectively. The diffraction patterns in IZO film are attributed to In_2O_3 bixbyite.

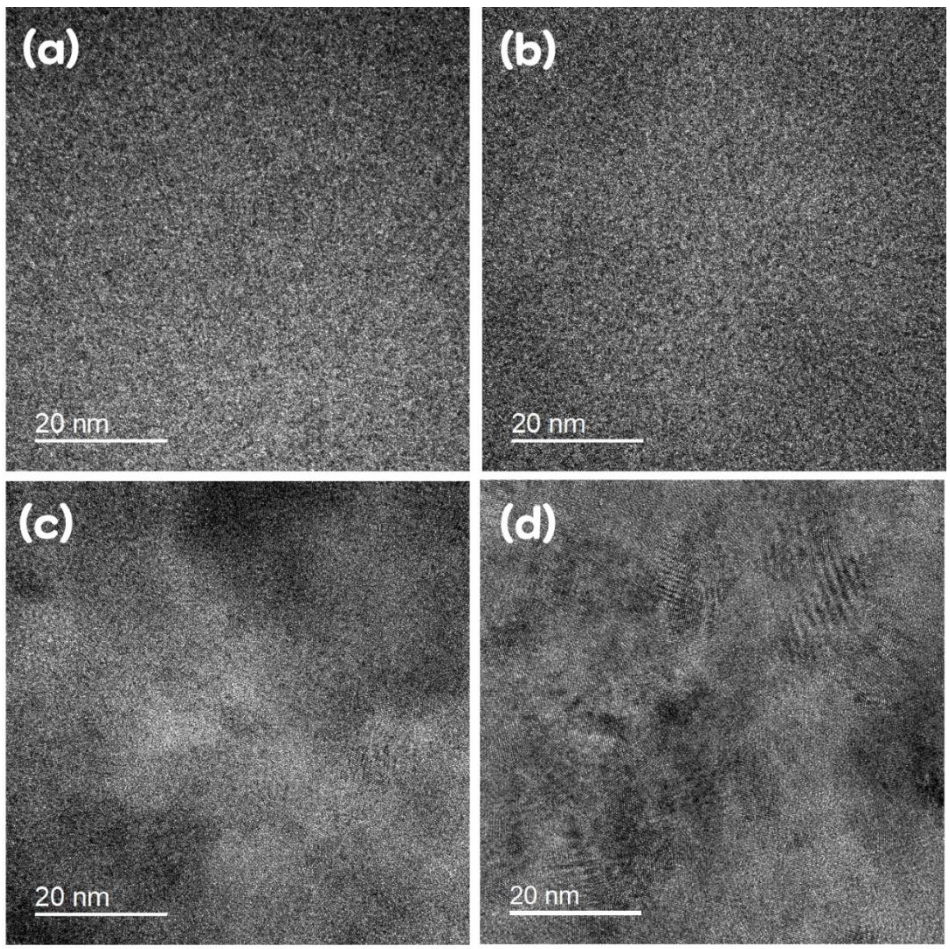


Figure 2-6. HRTEM Plan-view images of ALD-IZO films. The n_b of the IZO films was varied with (a) 10, (b) 100, (c) 130, and (d) 200 cycles, respectively.

These results can be confirmed again by the radial average of the SADP intensity, which is shown in **Figure 2-7**. The IZO films with the n_b of 10 and 100 cycles, (*i.e.,* IZO[9:1] and IZO[90:10]) show the typical amorphous structure with broad peaks that corresponded to bixbyite (222) and (611), respectively. The IZO film with the n_b of 130 cycles (*i.e.,* IZO[117:13]) started to appear at the peaks corresponding to bixbyite (222), (400), and (611). Finally, the IZO film with the n_b of 200 cycles reveals a fully bixbyite In_2O_3 structure with an additional sharp peak of (211), (400), (440), and (622) where the intensity is well-matched to the calculated random powder X-ray diffraction (XRD). On the other hand, it should be noted that there is no wurtzite ZnO correlated diffraction pattern for the entire series of samples.

To reveal a microstructure change instead of a crystal structure change (*i.e.,* the transition of the crystal structure from amorphous to nanocrystalline as well as the transition of the morphology from a well-intermixed to a layered structure), we observed the cross-sectional TEM as the n_b increased. **Figure 2-8** shows the high-resolution images, whereas **Figure 2-9** illustrates the high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) images when $n_b = 10, 100, 130, 160,$ and 200, respectively. Similar to the plan-view TEM images, it was confirmed that the IZO films up to the n_b of 100 cycles exhibit the completely amorphous phase. The bixbyite crystalline began to appear from the n_b of

130 cycles. Finally, the entirely crystalline bixbyite In_2O_3 formed at n_b = 160. The microstructure of IZO[9:1] (Figure 2-8 (a) and 2-9 (a)) consisted of a well-intermixed amorphous phase with a smooth surface. Although the IZO[90:10] remained an amorphous phase in a whole layer, an intensity undulation in the thickness direction is observed in HRTEM (Figure 2-8 (b)) and HAADF-STEM (Figure 2-9 (b)) images. Since the intensity of the HAADF image represents the mass differences, an alternative layered structure of In-rich and Zn-rich sublayers indicated to have appeared from IZO[90:10]. In IZO[117:13], where amorphous and crystalline phase coexist, there is an apparent crystalline region with a rough surface, whereas the amorphous region exhibits a smooth surface. The IZO[144:16] exhibits a fully crystalline bixbyite In_2O_3 layered structure with a rough surface, and the IZO[180:20] clearly reveals a layered crystalline structure with a repeated supercycle of 4, based on the design in Table 2-1.

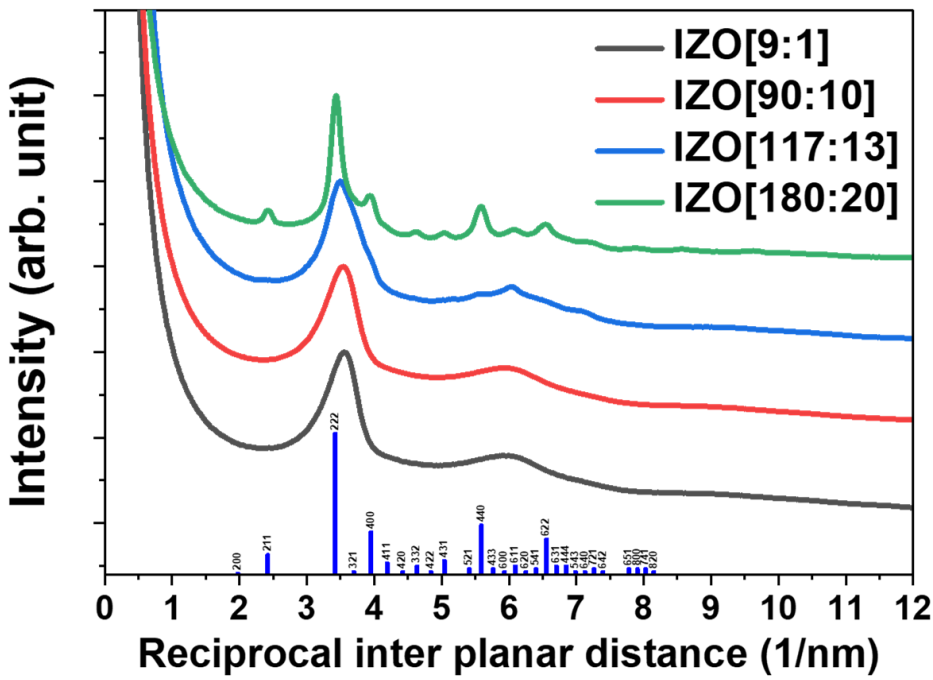


Figure 2-7. Radial average of SAED patterns of ALD-IZO films by varying the n_b, corresponds to plan-view TEM images in figure 2-5 (i-l). The diffraction patterns in IZO film are attributed to In_2O_3 bixbyite.

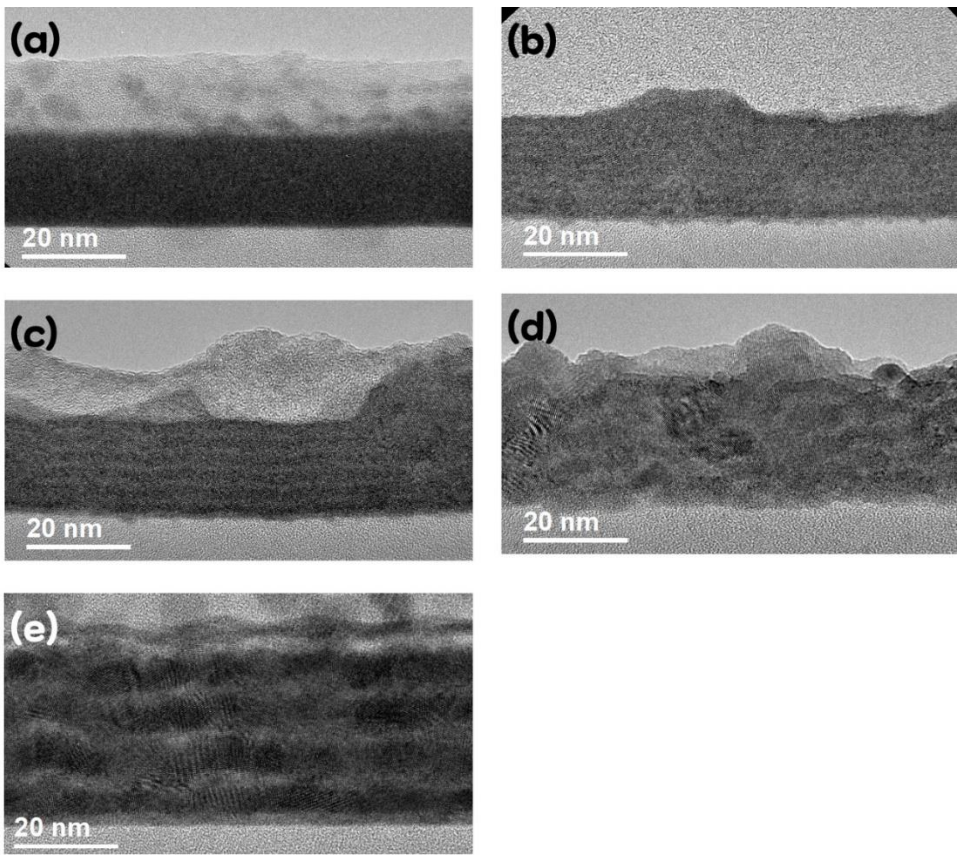


Figure 2-8. Film morphology of ALD-IZO films by varying the bilayer period. Cross-sectional HRTEM images of ALD-IZO films. The bilayer periods of films were varied with (a) 10, (b) 100, (c) 130, (d) 160, and (e) 200 cycles, respectively.

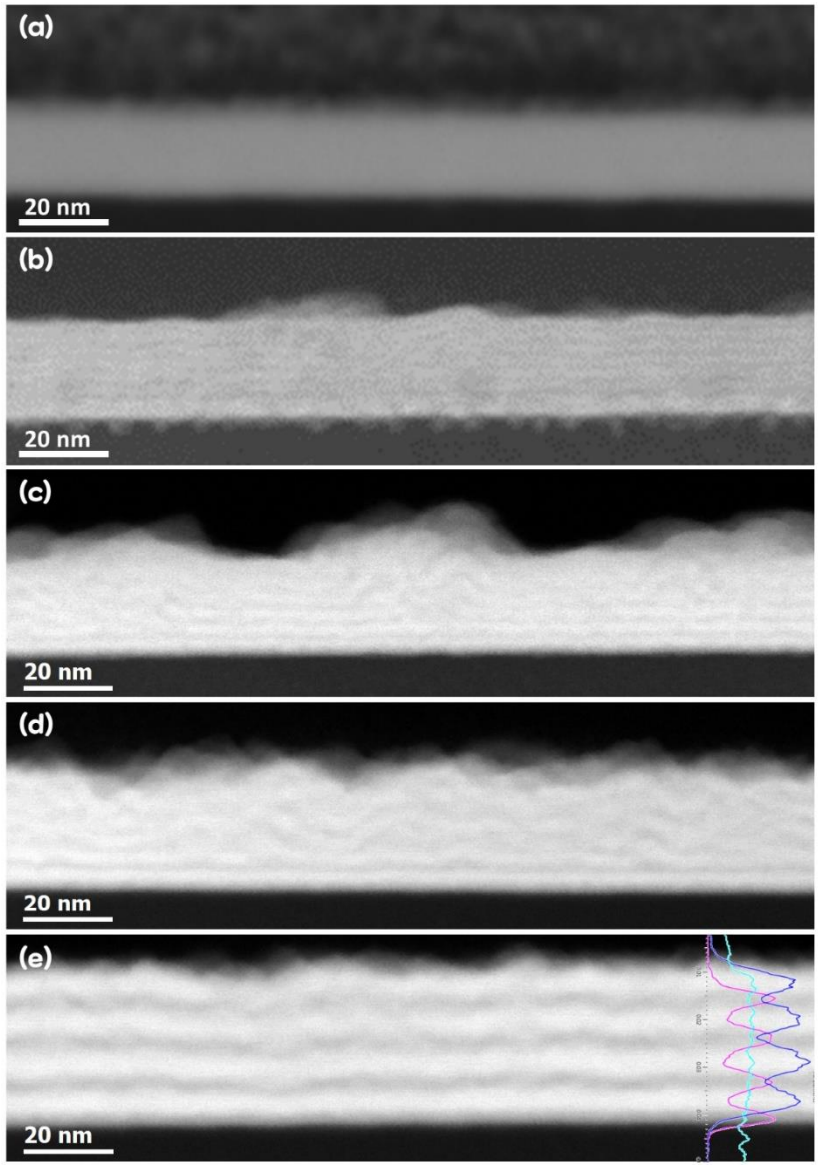


Figure 2-9. Cross-sectional HRTEM HAADF images of ALD-IZO films. The bilayer periods of films were varied with (a) 10, (b) 100, (c) 130, (d) 160, and (e) 200 cycles, respectively. The inset of Figure 2-9 (e) shows a typical EDS line profile of the IZO film with a bilayer period of 200 cycles.

X-ray reflectivity (XRR) is a powerful tool used to characterize the physical parameters of thin films and multilayers. It provides information about film thickness, density, and interfacial roughness from measured reflectivity curves and corresponding simulation. Therefore, we have attempted to perform XRR measurement for the IZO film with the n_b from 20 to 200 cycles. Here, the measured reflectivity curve was simulated using X'pert Reflectivity software, assuming that all sublayers have identical thicknesses and density per material. Measured (black line) and simulated (red line) XRR curves of the IZO film with the n_b of 20, 100, and 200 cycles are shown in **Figure 2-10**. The IZO film with n_b of 20 cycles only exhibits periodic fringes coming from total thickness, implying well-intermixed film as discussed in the previous manuscript. This result is also consistent with the corresponding cross-sectional HRTEM image in Figure 2-8, and Figure 2-9. As the n_b increases above 100 cycles, film morphology transition from well-intermixed to nanolaminate was again confirmed by XRR measurement with the existence of distinct sublayers. More importantly, thicknesses of the In_2O_3 and ZnO sublayer were extracted as 2.37 and 0.23 nm, respectively. Both of sublayer thicknesses are well-matched to the directly measured thicknesses based on HRTEM images. Therefore, extrapolated ZnO sublayer thickness in the previous manuscript was replaced to the thickness of 0.23 nm, which was obtained by XRR measurement. In addition, small Bragg peaks are observed that are expected to rely on a periodicity of nanolaminate.

Visible Bragg peak at ≈ 1.6° was attributed to a repetition of 2.6 nm thick bilayer structure with the n_b of 100 cycles. A period of this small Bragg peak becomes shorter as the n_b increases to 200 cycles, as shown in Figure 2-10. Therefore, we could conclude that film morphology transition from well-intermixed to nanolaminate at the n_b of 100 cycles was again confirmed by XRR measurements. This kind of morphological transition of ternary oxides along with the n_b has also been reported in the ALD-Al_2O_3/ZnO, Al_2O_3/TiO_2, and Al_2O_3/HfO_x nanolaminates.[32, 35, 37] It is reported that as the n_b decreased, the morphological transition from the Al_2O_3/TiO_x layered structure to the single homogeneous Al_xTi_yO phase occurred as the bilayer thickness decreased to 0.8 nm using XRR measurements.[32] Similar phenomena were also observed for the ALD-Al_2O_3/ZnO and Al_2O_3/HfO_x with critical bilayer thicknesses of 1.3 and 1.0 nm, respectively. Notably, the impact of the bilayer thickness on the microstructure of IZO thin films was also reported by the sequential layer-by-layer ion beam sputtering of In_2O_3 and ZnO.[36] The authors prepared the In_2O_3/ZnO multilayer structure by varying the equivalent sublayer thicknesses of In_2O_3 and ZnO from 0.3 nm to 1.7 nm, and showed that the transition from a well-intermixed to a layered structure occurred at 1.5 nm sublayer thickness.

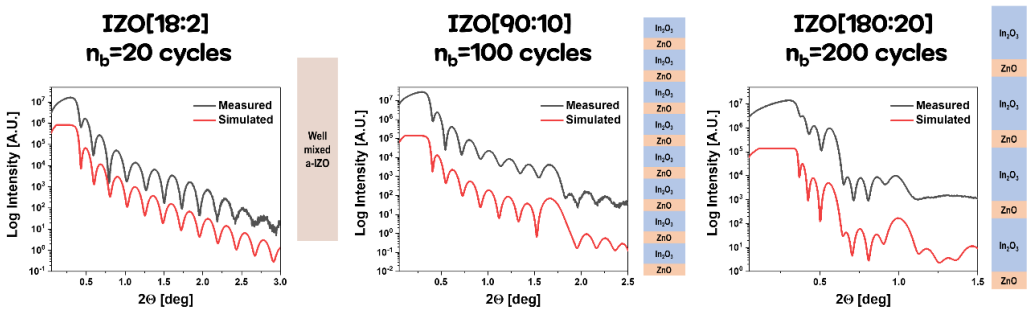


Figure 2-10. XRR measurement results and corresponding simulation curves of ALD IZO films with the n_b of (a) 20, (b) 100, and (c) 200 cycles, respectively. The simulation curves are vertically offset for clarity.

IZO [18:2] (n_b=20)	Thickness (nm)	Roughness (nm)	Density (g/cm³)
Well-intermixed IZO	18.371	0.386	6.497

Table 2-2. Thickness, interface roughness, and density of sublayers in ALD-IZO film with the n_b of 20 cycles, which were determined by curve fitting based on the results of XRR measurement in Figure 2-10 (a).

IZO [90:10] (n_b=100)	Thickness (nm)	Roughness (nm)	Density (g/cm³)
In_2O_3 (Top)	2.365	0.6	5.95
ZnO	0.235	0.2	3.5
In_2O_3	2.365	0.3	6.05
ZnO	0.225	0.195	3.8
In_2O_3	2.365	0.42	5.99
ZnO	0.232	0.2	3.8
In_2O_3	2.369	0.3	5.95
ZnO	0.225	0.2	3.8
In_2O_3	2.369	0.301	5.95
ZnO	0.225	0.169	3.8
In_2O_3	2.375	0.434	5.95
ZnO	0.225	0.2	3.78
In_2O_3	2.371	0.476	5.95
ZnO	0.225	0.137	3.8
In_2O_3	2.375	0.303	5.95
ZnO	0.235	0.2	3.8
In_2O_3 sublayers (Averaged)	2.37 ± 0.002	0.39 ± 0.05	5.96 ± 0.02
ZnO sublayers (Averaged)	0.23 ± 0.002	0.19 ± 0.01	3.76 ± 0.05

Table 2-3. Thickness, interface roughness, and density of sublayers in ALD-IZO film with the n_b of 100 cycles, which were determined by curve fitting based on the results of XRR measurement in Figure 2-10 (b).

IZO [180:20] (n_b=200)	Thickness (nm)	Roughness (nm)	Density (g/cm^3)
In_2O_3 (Top)	7.75	1.81	5.85
ZnO	0.75	0.58	3.89
In_2O_3	7.75	1.2	5.9
ZnO	0.75	0.5	3.85
In_2O_3	8.82	1.56	5.9
ZnO	0.83	0.58	3.86
In_2O_3	8.66	1.75	5.85
ZnO	0.8	0.8	3.9
In_2O_3 sublayers (Averaged)	8.24 ± 0.29	1.58 ± 0.14	5.88 ± 0.01
ZnO sublayers (Averaged)	0.78 ± 0.02	0.61 ± 0.06	3.88 ± 0.01

Table 2-4. Thickness, interface roughness, and density of sublayers in ALD-IZO film with the n_b of 200 cycles, which were determined by curve fitting based on the results of XRR measurement in Figure 2-10 (c).

In the case of the XRR curve with the n_b of 200 cycles, rough surface significantly affected to the fringes pattern. Surface roughening of the IZO film with increasing the n_b which was attributed to the crystallization of bixbyite In_2O_3 and its abundance increase has already discussed in our previous manuscript. To confirm this more clearly, we investigated the surface roughness by AFM, as shown in **Figure 2-11**. As the crystallization of In_2O_3 get stated above 130 cycles of the n_b surface roughness gradually increases up to 2.33 nm of root-mean-square roughness for the 200 cycles of the n_b. Whereas, amorphous IZO films with the n_b from 10 to 100 cycles, the films exhibit ultrasmooth surfaces with a surface roughness of ~ 0.3 nm.

Finally, EDS line profiles along with the n_b were investigated. A typical EDS line profile of the IZO film with a layered structure (i.e., n_b = 200 cycles in the inset of Figure 2-9 (e)) shows the alternative atomic composition of the In and Zn atoms across the film. The figure clearly depicts four different In and Zn peaks, since the deposition in the ALD sequence occurred with four repeated supercycles. Those of another n_b are also presented in **Figure 2-12**, and exhibit the same trend. Throughout these results, we examined the cation ratio of each In-rich and Zn-rich sublayer, which was measured at several arbitrary EDS line profiles across the layered-structured film. The cation ratio of the In-rich sublayers exhibits 84.6%, 82.7%, and 82.8% [In/(In+Zn)] for the n_b of 130, 160, and 200 cycles,

respectively. The cation ratios all exhibit similar In content, regardless of the n_b. Also, that the cation ratios of the Zn-rich sublayers are also examined as 33.2%, 38.0%, and 39.6% [Zn/(In+Zn)] for the n_b of 130, 160, and 200 cycles, respectively. Consequently, for shorter n_b (i. e., the n_b of 10 to 40 cycles), sublayer mixing occurred, thereby yielding a single amorphous phase IZO film. For a more extended n_b (*i.e.,* the n_b from 100 to 200 cycles), the film morphology transitions from a well-intermixed to a layered structure, together with the evolution of the bixbyite In_2O_3 nanocrystalline within the In-rich sublayer.

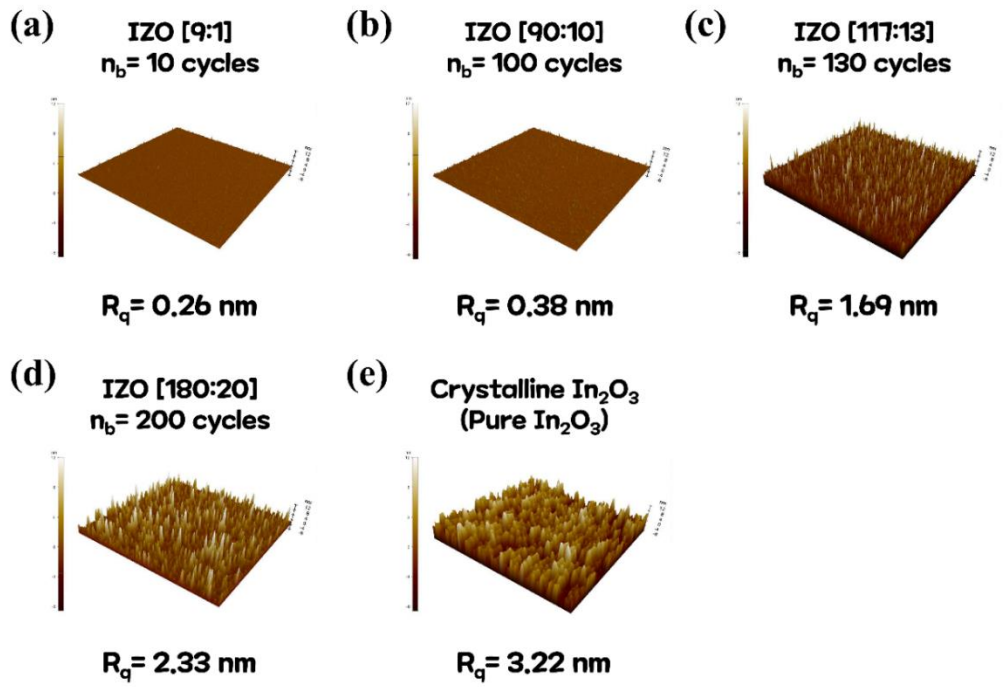


Figure 2-11. Oblique-view AFM images and corresponding surface roughness of the IZO films with the n_b of (a) 10, (b) 100, (c) 130 and (d) 200 cycles, respectively. (e) AFM image of crystalline pure In_2O_3 films. The scanning area is 5 μm by 5 μm, and the z-axis scale is 12 nm.

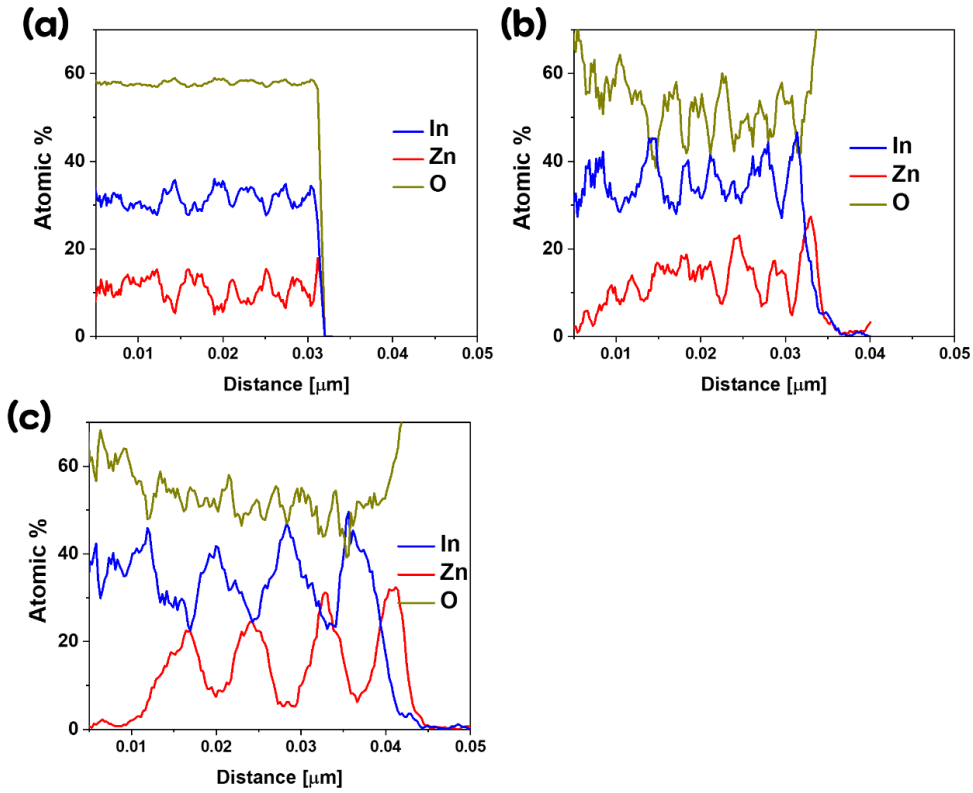


Figure 2-12. Typical EDS line spectra of ALD-IZO films with he n_b of (a) 130, (b) 160, and (c) 200 cycles, respectively.

2.3.4 Electrical properties of ALD-IZO films

We investigated the dependence of electrical resistivities and corresponding Hall mobilities and carrier concentrations on the n_b, as shown in **Figure 2-13**. In Figure 2-13 (a), the resistivity initially exhibits almost constant values up to n_b = 40 with the lowest resistivities as 5.0×10^{-4} Ω·cm. As the n_b increased to 100 cycles, the resistivity increased and exhibited the highest value of 2.9×10^{-3} Ω·cm at n_b = 200 cycles. Figure 2-13 (b) and 2-13 (c) shows the Hall mobility and carrier concentration of the IZO films as the n_b increases, respectively. Notably, the Hall mobility of the IZO films (Figure 2-13 (b)) could also be separated into two regimes, namely, the nearly constant regime for shorter bilayer periods ($n_b \leqq 40$) and the decrease regime for longer bilayer periods ($n_b \geqq 100$). On the other hand, the carrier concentration (Figure 2- 13 (c)) is gradually decreased from 3×10^{20} to 1×10^{20} cm^{-3} as n_b increases.

At this point, we noticed that ALD IZO film with the n_b beyond 100 cycles could be used as the active layer of TFT devices rely on the increase of resistivity with increasing the n_b. To figure out this, we have attempted to investigate the ALD IZO film performance of TFTs. IZO based TFTs were fabricated by using back-gate approaches. The n^{++} silicon of the substrate was used as a back-gate electrode, and the SiO_2 layer acted as the gate

dielectric. The IZO film with the n_b of 200 cycles and a thickness of 50 nm was deposited onto SiO_2 dielectric as an active layer. Post deposition of 20 nm SiO_2 and thermal annealing at 200℃ were conducted to passivate IZO active layer. These devices were characterized by output and transfer curves at room temperature. As shown in **Figure 2-14**, nonlinear n-type transport behavior of the output curve is clearly observed. The transfer characteristic result shows that the obtained maximum on/off current ratio is ~ 5 because the IZO TFTs cannot be turned off effectively due to the high leakage current. Here, the magnitude of leakage current was measured ~10^{-6} A level. This high leakage current is probably due to current through the gate dielectric and high conductivity of the IZO active layer.

At this point, it should be noted that the IZO films with the n_b below 100 cycles exhibit totally metallic behavior with a resistivity of ~ 5.0×10^{-3} Ω·cm. Even though the ALD cycle ratio we used in this work is appropriate for electrode application, we were able to obtain saturated transport behavior by increasing the n_b from 10 to 200 cycles. Therefore, we could suggest that an increase in the n_b in ALD IZO can play a key role in achieving desirable TFT performance. Moreover, all the IZO films in this work were deposited based on the In-O: Zn-O=9:1 of ALD cycle ratio (*i.e.,* 83.2 at% of In/(In+Zn) cation ratio as shown in Figure 2-3[12]) that exhibited the lowest resistivity among the various cation ratios of IZO films. The increase of the n_b based on the other

ALD IZO cycle ratio should present better transistor characteristics.

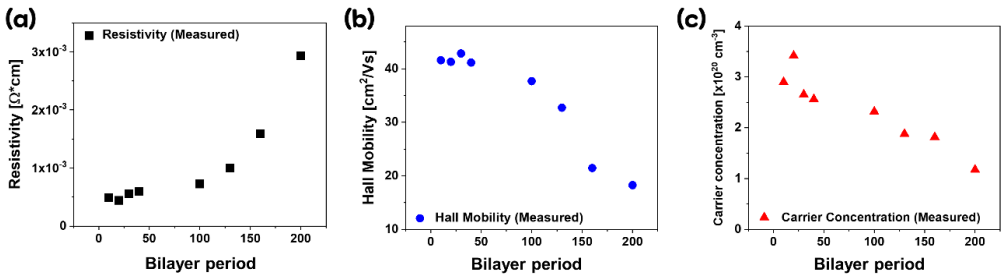


Figure 2-13. Electrical properties of ALD-IZO films by varying the n_b. (a) Electrical resistivities, and (b) Hall mobilities and (c) carrier concentrations of IZO films by varying the n_b.

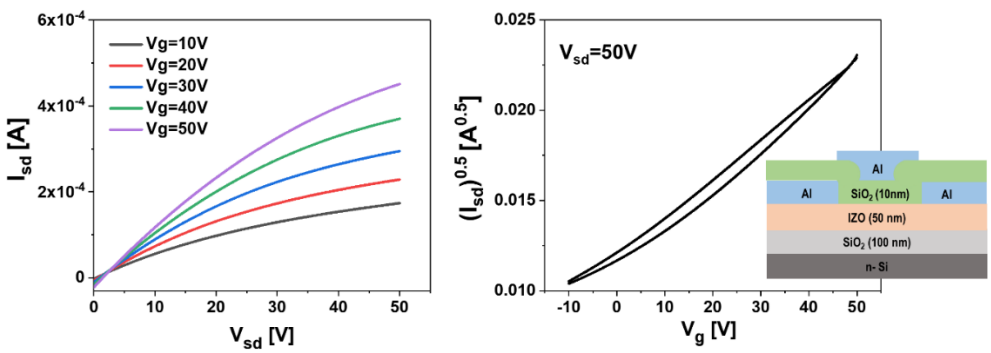


Figure 2-14. TFT performance of ALD IZO film with the n_b of 200 cycles (a) Output characteristics of IZO TFT under different back-gate voltage (V_g). (b) Transfer characteristics at V_{sd} = 50 V.

To interpret the change of electrical property along with the n_b, we first consider whether the change in cation ratio along with the n_b would impact the electrical properties of the IZO films, since the cation ratio of [In/(Zn+In)] noticeably decreased from 84% to 67% as n_b increased. To examine the effect, we referred to our previous results on the electrical properties of ALD-IZO films as a function of the cation ratio.[12] In that work, we systematically investigated the electrical properties of the IZO films as a function of the [In/(In+Zn)] cation ratio, which were deposited when n_b < 20 cycles. **Figure 2-15** (a-c) shows film resistivity, Hall mobility and carrier concentration of the IZO films as a function of the [In/(In+Zn)] cation ratio, respectively. Here, the electrical properties of both our previous report (designated as reference IZO)[12] and those of the IZO films along with the n_b (designated as bilayer IZO) were shown as normalized, setting each of the low-resistivity values to 1 (*i.e.*, setting the highest mobility value to 1). This rescaling method enables the comparison of the relative change in resistivity along with the cation ratio to account for difference in resistivity values between the two. Those of the apparent electrical properties for each were also displayed in **Figure 2-16**. Interestingly, up to the n_b of 130 cycles, all the resistivities, mobilities, and carrier concentrations on the n_b exhibited similar behavior to that of the [In/(In+Zn)] cation ratio. These results suggested that the dependence of the electrical properties on the n_b, which

we mentioned in Figure 2-13 (a)–(c), strongly correlate with the effect of the cation ratio up to the n_b of 130 cycles.

On the other hand, the IZO films with the n_b of 160 and 200 cycles exhibited significantly higher resistivities together with lower Hall mobilities compared with those of the reference IZO films with the same cation ratio. We noticed that all of the reference IZO films in this regime was deposited with an n_b of 10 or 5 cycles, and its crystal structure was well-intermixed amorphous. Therefore, we suggest that the structural inhomogeneity for the longer n_b cause the inherent electrical property of the film. Namely, a further increase in the resistivity for longer n_b is associated with the transition of the crystal structure of the In-rich sublayer from amorphous to nanocrystalline. As the n_b increased, the phase transition from amorphous to nanocrystalline occurred within the In-rich sublayers, which canceled the advantage of high-electron mobility due to the overlapped In 5s orbital of the amorphous oxides.[6, 42-43] Another probable source of the decrease in Hall mobility for longer n_b is scattering by ionized impurity centers.[16, 20, 44] Once the crystal structures of the In-rich sublayers were transformed from the amorphous to the nanocrystalline In_2O_3 bixbyite, the Zn atoms either incorporated into a substitutional site (Zn_{In}^{-}) or induced In vacancies (V_{In}^{3-}).[11, 20, 45] These charged impurities could function as both ionized scattering centers and electron acceptors.[44] They might reduce the

Hall mobility as well as the charge carrier concentration for IZO films with a longer n_b.[16, 45] Further increases in the n_b deteriorated the mobility due to the surface roughening caused by appearance and the increased abundance of bixbyite In_2O_3 nanocrystals, as shown in the cross-sectional TEM images. This surface roughening along with the n_b was further investigated by atomic force microscope (AFM), as shown in Figure 2-11. As crystallization of In_2O_3 get stated above 130 cycles of the n_b, surface roughness gradually increases up to 2.33 nm of root-mean-square roughness for the 200 cycles of the n_b. Whereas, amorphous IZO films with the n_b from 10 to 100 cycles exhibit ultrasmooth surfaces with surface roughness of ~ 0.3 nm.

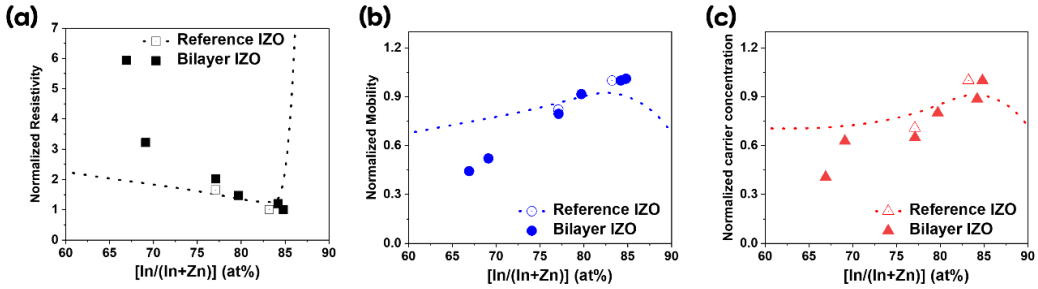


Figure 2-15. Normalized electrical properties of ALD-IZO films by varying the n_b. (a) Resistivity, (b) Hall mobility, and (c) carrier concentration of IZO films are co-displayed with the data from the reference[12] that implies the electrical properties of IZO film along with the [In/(In+Zn)] cation ratio.

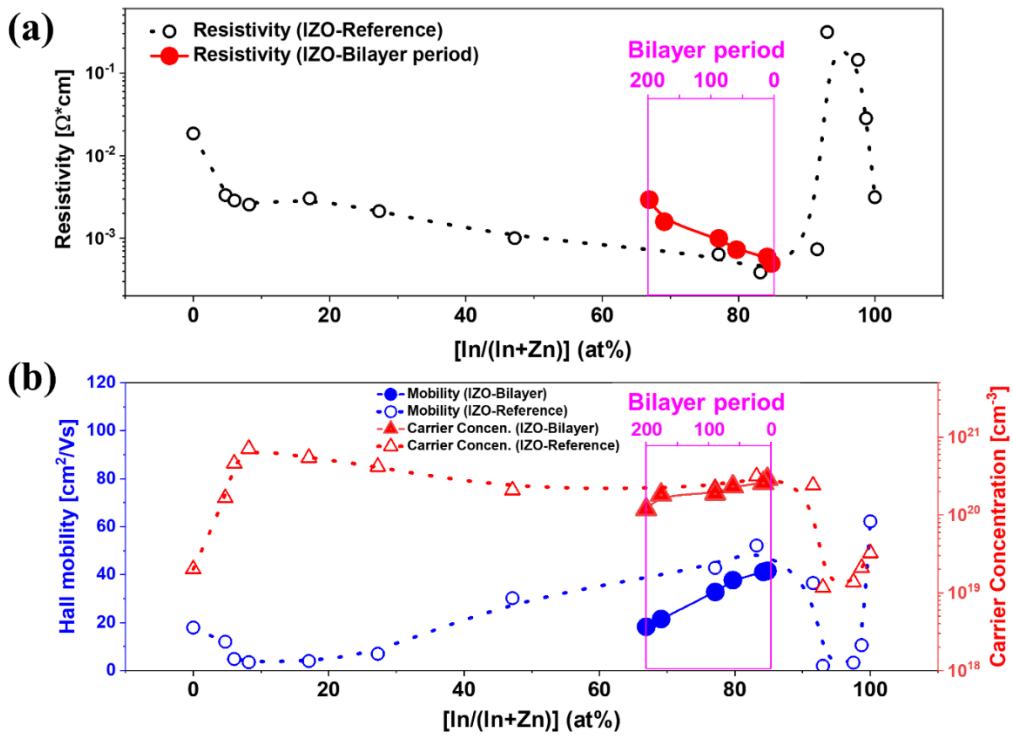


Figure 2-16. (a) Resistivity, (b) Hall mobility and carrier concentration of ALD-IZO films along with the n_b are co-displayed with the data from reference that implies the electrical properties of IZO film along with the [In/(In+Zn)] cation ratio.

Consequently, the dependence of the electrical properties of the IZO film along with the n_b was interpreted in two ways: change in Indium cation ratio and film microstructure with increasing n_b. For the n_b up to 130 cycles, the decrease in both the mobility and carrier concentration, and the

subsequent increase in resistivity are attributed to changes in the [In/(In+Zn)] cation ratio along with the n_b. Otherwise, for longer n_b, the appearance of the Zn-incorporated nanocrystalline bixbyite In_2O_3 and its abundance increase deteriorates both Hall mobility and carrier concentration, which yields the further increase in the electrical resistivity of the IZO films.

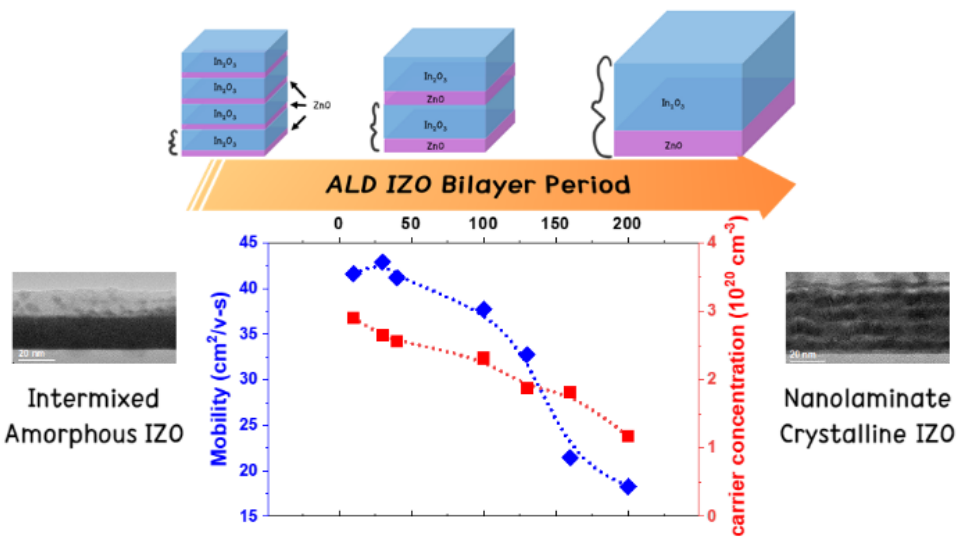


Figure 2-17. Effect of bilayer period of ALD on the growth behavior and electrical properties of amorphous IZO film.

2.4 Summary and Conclusion

In this work, we investigated the growth behavior, microstructures, and electrical properties of the ALD-IZO films among various n_b from 10 to 200 cycles. The growth rates were almost constant at first, but linearly increase as the n_b increases above 100 cycles. The restoration of the growth rate and cation ratio for a longer n_b clearly indicates the retarded adsorption of the DEZ precursor on its counter surface. We interpret that the behaviors of growth rate and electrical resistivity, along with the n_b as a transition in the microstructure of the IZO films. Structural analysis by XRD and intensive TEM measurement show that microstructure transitions from the well-intermixed amorphous phase to the layered structure with nanocrystalline In_2O_3 bixbyite occurred as the n_b increased; there was an onset of crystallization at n_b = 130 cycles, and that of morphology at n_b = 100 cycles. This structural and morphological transition resulted in noticeable changes in the growth behavior and electrical properties. The electrical properties of the IZO films also exhibit two distinct regions along with the n_b. For shorter n_b, the resistivity of the IZO film was 5 $\times 10^{-4}$ Ω·cm with a high mobility of 42 $cm^2/V{\cdot}s$, which can be applied in transparent conducting electrode applications. Meanwhile, as the n_b increases beyond 100 cycles, the resistivity of the IZO film rapidly increases up to 6 times higher than the lowest value, implying that a modulating the n_b can play a key role to obtain

desirable transport properties of the IZO film. A combined analysis of the effect of the n_b on the physical properties of films in this study provides insight into the tunability of microstructure and the processability of desirable films by controlling the n_b in the ALD process.

References

(1) Ellmer, K. Past Achievements and Future Challenges in the Development of Optically Transparent Electrodes. *Nat. Photonics* **2012,** *6*, 809-817.

(2) Dawar, A.; Joshi, J. Semiconducting Transparent Thin Films: Their Properties and Applications. *J. Mater. Sci.* **1984,** *19*, 1-23.

(3) Cao, W.; Li, J.; Chen, H.; Xue, J. Transparent Electrodes for Organic Optoelectronic Devices: A Review. *J. Photonics Energy* **2014,** *4*, 040990.

(4) Mizuhashi, M. Electrical Properties of Vacuum-Deposited Indium Oxide and Indium Tin Oxide Films. *Thin Solid Films* **1980,** *70*, 91-100.

(5) Song, J. I.; Park, J. S.; Kim, H.; Heo, Y. W.; Lee, J. H.; Kim, J. J.; Kim, G. M.; Choi, B. D. Transparent Amorphous Indium Zinc Oxide Thin-Film Transistors Fabricated at Room Temperature. *Appl. Phys. Lett.* **2007,** *90*, 022106.

(6) Taylor, M. P.; Readey, D. W.; van Hest, M. F. A. M.; Teplin, C. W.; Alleman, J. L.; Dabney, M. S.; Gedvilas, L. M.; Keyes, B. M.; To, B.; Perkins, J. D.; Ginley, D. S. The Remarkable Thermal Stability of Amorphous In-Zn-O Transparent Conductors. *Adv. Funct. Mater.* **2008,** *18*, 3169-3178.

(7) Park, S. Y.; Song, J. H.; Lee, C. K.; Son, B. G.; Lee, C. K.; Kim, H. J.; Choi, R.; Choi, Y. J.; Kim, U. K.; Hwang, C. S.; Kim, H. J.; Jeong, J. K. Improvement in Photo-Bias Stability of High-Mobility Indium Zinc Oxide Thin-Film Transistors by Oxygen High-Pressure Annealing. *IEEE Electron Device Lett.* **2013,** *34*, 894-896.

(8) Kim, H.; Choi, D.; Park, S.; Park, K.; Park, H. W.; Chung, K. B.; Kwon, J. Y. Impact of Bias Stability for Crystalline InZnO Thin-Film Transistors. *Appl. Phys. Lett.* **2017,** *110,* 232104.

(9) Sheng, J.; Lee, H. J.; Oh, S.; Park, J. S. Flexible and High-Performance Amorphous Indium Zinc Oxide Thin-Film Transistor Using Low-Temperature Atomic Layer Deposition. *ACS Appl. Mater. Interfaces* **2016,** *8*, 33821-33828.

(10) Oh, S.; Yang, B. S.; Kim, Y. J.; Oh, M. S.; Jang, M.; Yang, H.; Jeong, J. K.; Hwang, C. S.; Kim, H. J. Anomalous Behavior of Negative Bias Illumination Stress Instability in an Indium Zinc Oxide Transistor: A Cation Combinatorial Approach. *Appl. Phys. Lett.* **2012,** *101*, 092107.

(11) Ramamoorthy, K.; Kumar, K.; Chandramohan, R.; Sankaranarayanan, K. Review on Material Properties of IZO Thin Films Useful as Epi-n-TCOs in Opto-Electronic (SIS Solar Cells, Polymeric LEDs) Devices. *Mater. Sci. Eng., B* **2006,** *126*, 1-15.

(12) Lee, D. J.; Kwon, J. Y.; Kim, J.; Kim, K. J.; Cho, Y. H.; Cho, S. Y.; Kim, S. H.; Xu, J.; Kim, K. B. Ultrasmooth, High Electron Mobility Amorphous In-Zn-O Films Grown by Atomic Layer Deposition. *J. Phys. Chem. C* **2014,** *118*, 408-415.

(13) Yaglioglu, B.; Yeom, H. Y.; Beresford, R.; Paine, D. C. High-Mobility Amorphous In2O3-10 wt %ZnO Thin Film Transistors. *Appl. Phys. Lett.* **2006,** 062103.

(14) Faber, H.; Das, S.; Lin, Y. H.; Pliatsikas, N.; Zhao, K.; Kehagias, T.; Dimitrakopulos, G.; Amassian, A.; Patsalas, P. A.; Anthopoulos, T. D. Heterojunction Oxide Thin-Film Transistors with Unprecedented Electron Mobility Grown from Solution. *Sci. Adv.* **2017,** *3* , e1602640.

(15) Gomes, L.; Marques, A.; Branco, A.; Araujo, J.; Simoes, M.; Cardoso, S.; Silva, F.; Henriques, I.; Laia, C. A. T.; Costa, C. IZO Deposition by RF and DC Sputtering on Paper and Application on Flexible Electrochromic Devices. *Displays* **2013,** *34*, 326-333.

(16) Leenheer, A. J.; Perkins, J. D.; van Hest, M. F. A. M.; Berry, J. J.; O'Hayre, R. P.; Ginley, D. S. General Mobility and Carrier Concentration Relationship in Transparent Amorphous Indium Zinc Oxide Films. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2008,** *77*, 115215.

(17) Morales-Masis, M.; Nicolas, S. M. D.; Holovsky, J.; Wolf, S. D.; Ballif, C. Low-Temperature High-Mobility Amorphous IZO for Silicon Heterojunction Solar Cells. *IEEE J. Photovoltaics* **2015,** *5*, 1340-1347.

(18) Naghavi, N.; Marcel, C.; Dupont, L.; Rougier, A.; Leriche, J.-B.; Guéry, C. Structural and Physical Characterisation of Transparent Conducting Pulsed Laser Deposited InO–ZnO Thin Films. *J. Mater. Chem.* **2000,** *10*, 2315-2319.

(19) Yan, Y.; Pennycook, S. J.; Dai, J.; Chang, R. P. H.; Wang, A.; Marks, T. J. Polytypoid Structures in Annealed In2O3–ZnO Films. *Appl. Phys. Lett.* **1998,** *73*, 2585.

(20) Haming, M.; Issanin, A.; Walker, D.; von Seggern, H.; Jagermann, W.; Bonrad, K. Interrelation between Chemical, Electronic, and Charge Transport Properties of Solution-Processed Indium-Zinc Oxide Semiconductor Thin Films. *J. Phys. Chem. C* **2014,** *118*, 12826-12836.

(21) Tetzner, K.; Isakov, I.; Regoutz, A.; Payne, D. J.; Anthopoulos, T. D. The Impact of Post-Deposition Annealing on the Performance of Solution-Processed Single Layer In2O3 and Isotype In2O3/ZnO Heterojunction Transistors. *J. Mater. Chem. C* **2017,** *5*, 59-64.

(22) Wang, C. L.; Liu, X. Q.; Xiao, X. H.; Liu, Y. L.; Chen, W.; Li, J. C.; Shen, G. Z.; Liao, L. High-Mobility Solution-Processed Amorphous Indium Zinc

Oxide/In2O3 Nanocrystal Hybrid Thin-Film Transistor. *IEEE Electron Device Lett.* **2013,** *34*, 72-74.

(23) George, S. M. Atomic Layer Deposition: An Overview. *Chem. Rev.* **2010,** *110*, 111-131.

(24) Sonsteby, H. H.; Fjellvag, H.; Nilsen, O. Functional Perovskites by Atomic Layer Deposition - An Overview. *Adv. Mater. Interfaces* **2017,** *4*, 1600903.

(25) Mackus, A. J. M.; Schneider, J. R.; MacIsaac, C.; Baker, J. G.; Bent, S. F. Synthesis of Doped, Ternary, and Quaternary Materials by Atomic Layer Deposition: A Review. *Chem. Mater.* **2019,** *31*, 1142-1183.

(26) Miikkulainen, V.; Leskelä, M.; Ritala, M.; Puurunen, R. L. Crystallinity of Inorganic Films Grown by Atomic Layer Deposition: Overview and General Trends. *J. Appl. Phys.* **2013,** *113*, 021301.

(27) Sanctis, S.; Krausmann, J.; Guhl, C.; Schneider, J. J. Stacked Indium Oxide/zinc Oxide Heterostructures as Semiconductors in Thin Film Transistor Devices: a Case Study Using Atomic Layer Deposition. *J. Mater. Chem. C* **2018,** *6*, 464-472.

(28) Kim, D.; Nam, T.; Park, J.; Gatineau, J.; Kim, H. Growth Characteristics and Properties of Indium Oxide and Indium-Doped Zinc Oxide by Atomic Layer Deposition. *Thin Solid Films* **2015,** *587*, 83-87.

(29) Krausmann, J.; Sanctis, S.; Engstler, J.; Luysberg, M.; Bruns, M.; Schneider, J. J. Charge Transport in Low-Temperature Processed Thin-Film Transistors Based on Indium Oxide/Zinc Oxide Heterostructures. *ACS Appl. Mater. Interfaces* **2018,** *10*, 20661-20671.

(30) Illiberi, A.; Katsouras, I.; Gazibegovic, S.; Cobb, B.; Nekovic, E.; van Boekel, W.; Frijters, C.; Maas, J.; Roozeboom, F.; Creyghton, Y.; Poodt, P.; Gelinck, G. Atmospheric Plasma-Enhanced Spatial-ALD of InZnO for High Mobility Thin Film Transistors. *J. Vac. Sci. Technol., A* **2018,** *36*, 04F401.

(31) Elam, J. W.; Sechrist, Z. A.; George, S. M. ZnO/Al2O3 Nanolaminates Fabricated by Atomic Layer Deposition: Growth and Surface Roughness Measurements. *Thin Solid Films* **2002,** *414*, 43-55.

(32) Sintonen, S.; Ali, S.; Ylivaara, O. M. E.; Puurunen, R. L.; Lipsanen, H. X-ray Reflectivity Characterization of Atomic Layer Deposition Al2O3/TiO2 Nanolaminates with Ultrathin Bilayers. *J. Vac. Sci. Technol., A* **2014,** *32*, 01A111.

(33) Chaaya, A. A.; Viter, R.; Baleviciute, I.; Bechelany, M.; Ramanavicius, A.; Gertnere, Z.; Erts, D.; Smyntyna, V.; Miele, P. Tuning Optical Properties of

Al2O3/ZnO Nanolaminates Synthesized by Atomic Layer Deposition. *J. Phys. Chem. C* **2014,** *118*, 3811-3819.

(34) Mullings, M. N.; Hagglund, C.; Tanskanen, J. T.; Yee, Y.; Geyer, S.; Bent, S. F. Thin Film Characterization of Zinc Tin Oxide Deposited by Thermal Atomic Layer Deposition. *Thin Solid Films* **2014,** *556*, 186-194.

(35) Ho, M. Y.; Gong, H.; Wilk, G. D.; Busch, B. W.; Green, M. L.; Lin, W. H.; See, A.; Lahiri, S. K.; Loomans, M. E.; Raisanen, P. I.; Gustafsson, T. Suppressed Crystallization of Hf-Based Gate Dielectrics by Controlled Addition of Al2O3 Using Atomic Layer Deposition. *Appl. Phys. Lett.* **2002,** *81*, 4218.

(36) Zhilova, O. V.; Pankov, S.; Sitnikov, A. V.; Kalinin, Y. E.; Kashirin, M. A.; Makagonov, V. A. Optical and Electrical Properties of Thin-Film Hetero-Structures of the In2O3-ZnO System. *Mater. Res. Express* **2019,** *6*, 086330.

(37) Raghavan, R.; Bechelany, M.; Parlinska, M.; Frey, D.; Mook, W. M.; Beyer, A.; Michler, J.; Utke, I. Nanocrystalline-to-Amorphous Transition in Nanolaminates Grown by Low Temperature Atomic Layer Deposition and Related Mechanical Properties. *Appl. Phys. Lett.* **2012,** *100*, 191912.

(38) Hagglund, C.; Grehl, T.; Tanskanen, J. T.; Yee, Y. S.; Mullings, M. N.; Mackus, A. J. M.; Maclsaac, C.; Clemens, B. M.; Brongersma, H. H.; Bent, S. F. Growth, Intermixing, and Surface Phase Formation for Zinc Tin Oxide

Nanolaminates Produced by Atomic Layer Deposition. *J. Vac. Sci. Technol., A* **2016,** *34*, 021516.

(39) Chang, S. L.; Takoudis, C. G. Growth Behavior and Structural Analysis of Atomic Layer Deposited SnxTi1-xOy Films. *J. Vac. Sci. Technol., A* **2018,** *36*, 01A121.

(40) Li, D. H.; Zhai, C. H.; Zhou, W. C.; Huang, Q. H.; Wang, L.; Zheng, H.; Chen, L.; Chen, X.; Zhang, R. J. Effects of Bilayer Thickness on the Morphological, Optical, and Electrical Properties of Al2O3/ZnO Nanolaminates. *Nanoscale Res. Lett.* **2017,** *12*.

(41) Schiøtz, J.; Di Tolla, F. D.; Jacobsen, K. W. Softening of Nanocrystalline Metals at Very Small Grain Sizes. *Nature* **1998,** *391*, 561-563.

(42) Kwon, J. Y.; Lee, D. J.; Kim, K. B. Review Paper: Transparent Amorphous Oxide Semiconductor Thin Film Transistor. *Electron. Mater. Lett.* **2011,** *7*, 1-11.

(43) Hosono, H. Ionic Amorphous Oxide Semiconductors: Material Design, Carrier Transport, and Device Application. *J. Non-Cryst. Solids.* **2006,** *352*, 851-858.

(44) Lany, S.; Zunger, A. Dopability, Intrinsic Conductivity, and Nonstoichiometry of Transparent Conducting Oxides. *Phys. Rev. Lett.* **2007,** *98, 045501.*

(45) Martins, R.; Barquinha, P.; Pimentel, A.; Pereira, L.; Fortunato, E. Transport in High Mobility Amorphous Wide Band Gap Indium Zinc Oxide Films. *Phys. Status Solidi A* **2005,** *202*, R95-R97.

Chapter 3.

Defect Engineering in CVD-graphene as a Copper Diffusion Barrier (Part Ⅰ)

: Electrical properties of graphene/In_2O_3 bilayer with remarkable uniformity as a transparent conducting electrode

This chapter is based on the paper published in

Nanotechnology, (2019)

3.1 Introduction

Transparent conducting electrode (TCE) is one of the most important components of various optoelectronic devices such as touch screen panels,[1] displays,[2] solar cells,[3] and light-emitting diodes.[4] In such applications, a sheet resistance less than 100 Ω/sq with a high optical transmittance to visible light (above 90%) is typically required to satisfy the minimum industrial standard established for TCE materials.[5] Currently, Sn-doped indium oxide—known as indium tin oxide (ITO)—is widely used as a TCE material because of its low resistivity (~10^{-4} Ω·cm) as well as its high optical transmittance at visible wavelengths.[6] However, TCEs based on oxide materials have a limited application in flexible electronics owing to their inherent brittle nature originated from either ionic or covalent bonding in plastic deformation.[7,8] In this context, graphene has been proposed as an attractive TCE material for flexible optoelectronic devices.[9-11] As is well known, graphene comprises a single layer of carbon atoms having in-plane sp^2-bonds and shows a unique combination of electrical, optical, and mechanical properties that are suitable for flexible TCEs.[12-15] In that sense, graphene has been considered as reinforcement to improve the mechanical flexibility of brittle oxides.[16-20]

One such example is constructing a bilayer structure consisting

of graphene and oxide film. Multiple studies have already shown that graphene compensated mechanical properties of brittle oxides, leading enhanced flexibility of graphene/oxide bilayer structures. **Figure 3-1** and **Figure 3-2** show the representative results in the previous research[17,19], which demonstrate better flexibility of graphene/oxide film bilayer compared to bare oxide. As shown in Figure 3-1, Liu *et al.* reported enhanced flexibility of graphene/ITO bilayer structure by conducting both electromechanical tensile and bending tests.[17] Results presented in Figure 3-1 exactly addresses the flexibility of the graphene/oxide bilayer. During the tensile and bending tests, degradation of electrical properties of the bilayer is much smaller than that of bare oxide and almost similar to the tendency of bare graphene. Lee *et al.* also demonstrated significant enhancement in electromechanical durability of polycrystalline ITO/graphene bilayer structure compared with bare ITO films under repeated bending as shown in Figure 3-2.[19] These results clearly show a beneficial effect of graphene in suppressing the fracture of ITO films in bilayer structure. Besides, throughout analysis on mechanical parameters of graphene/AZO bilayer, Choi *et al.* reported that fracture energy of AZO/graphene was drastically improved compared with bare AZO films, thereby crack initiation of AZO films in bilayer structure could be remarkably retarded.[20] Accordingly, we believed that the mechanical

flexibility issue of graphene/oxide bilayer has been sufficiently demonstrated by the previous research. Therefore, we focused on the investigation of the electrical and optical properties of GI-bilayer in this work. The change of electrical properties by hybridization of graphene and In_2O_3, which have different electrical transport behavior, (*p*- and *n*-type, respectively) is main contents in our work. Unfortunately, we have not achieved improved electrical properties compared to conventional transparence conducting oxide. However, it is highly expected that sheet resistance of graphene/oxide film composite can be easily reduced by using oxides having higher conductivity or by increasing the number of layers of graphene, which is the future work we are planning to do. A detailed analysis of the transport properties of each sublayer, rather than just change of sheet resistance, has not been reported so far.

As well as the advantages of the hybridization on mechanical properties, there have been several attempts to investigate the electrical properties of graphene/oxide bilayer structure.[21-27] In spite of significant progress for growth, transfer, and doping of graphene,[28-32] several limitations still exist for practical applications of graphene-based electrodes: electrical conductivity of single-layer graphene is still too lower than that of conventional ITO, and a lack of large-area electrical reliability of graphene electrode.[13, 33] In particular, both macro- and micro-scale defects that can be generated during the

growth and transfer process are known to critically deteriorate the large-area electrical reliability of graphene electrode.[34, 35] Several methods including usage of heptane as a transfer medium with improved contact between graphene and target substrate have been proposed to minimize microscale defects in graphene.[33-36] However, these approaches are still far from industrial applications due to the number of target substrates they can be applied to being limited[34] or the additional requirement for a suspending holder.[36] To overcome these shortcomings of the electrical properties of graphene via hybridization with oxide, considerable efforts have been devoted.[21-27] On depositing a few nm of MoO_3, V_2O_5, WO_3, and ZnO on graphene, metal oxide induced charge transfer doping of graphene was attributed to the work function difference of two materials.[22-24, 26] In addition, Lee *et al.* demonstrated flexible organic light emitting diodes which exhibited superior external quantum efficiency of 40.8% for single-junction structure owing to the synergetic interplay of graphene/TiO_2 bilayer electrode.[16] In that sense, graphene/oxide hybridization could provide a strategy for the realization of graphene-based electrodes in optoelectronic devices.

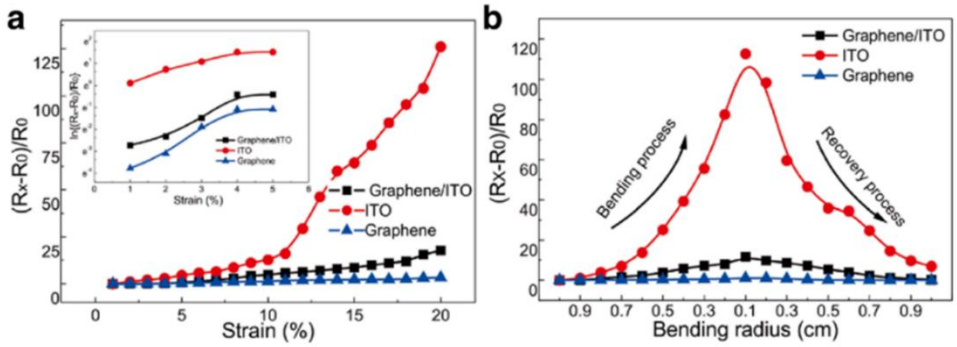


Figure 3-1. Comparative experiment results for the degradation of sheet resistance of graphene, ITO, and graphene/ITO bilayer structure under uniaxial strain. The electrical resistance of graphene/ITO bilayer changed significantly less than that of bare ITO for the same applied strain and bending radius. In this experiment, the bilayer was fabricated by transferring single layer graphene on 80-nm-thick ITO films sputtered on PET substrate. (a) Electromechanical tensile test result (b) The change in sheet resistance versus bending radius.[17]

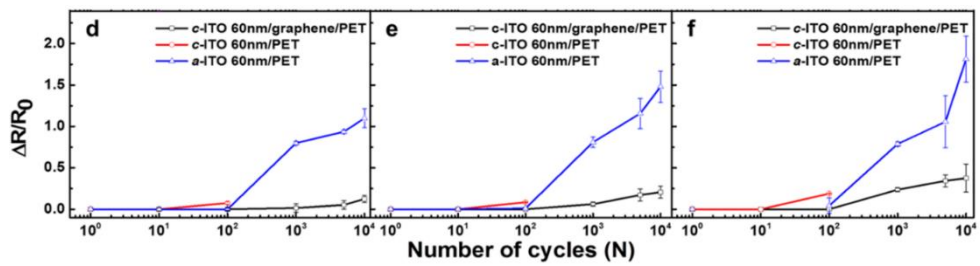


Figure 3-2. Electromechanical durability of graphene/ITO bilayer was accomplished by repeated bending tests. Comparative experiments for 60-nm-thick amorphous ITO (*a*-ITO), polycrystalline ITO (*c*-ITO), and *c*-ITO/graphene bilayer were conducted as a function of the number of bending cycles (N) at the radius of curvature of (d) 16 mm (e) 12 mm and (f) 8 mm, respectively.[19]

To this end, we propose a bilayer structure comprising graphene and In_2O_3, focusing on large-area electrical uniformity and analysis on its transport properties. This new structure is termed as GI-bilayer. The GI-bilayer was prepared by transferring CVD-grown monolayer graphene onto atomic layer deposition (ALD)-grown In_2O_3. As shown in **Figure 3-3**, homogeneously deposited conducting In_2O_3 layer was introduced as a complementary layer to provide an electrical path to circumvent the microscale defects on the graphene and enhance the electrical property of graphene. We report the effects of a complementary In_2O_3 layer on the areal-uniformity of the sheet resistance, electrical properties, and optical transparency in terms of the thickness of the In_2O_3 layer. In addition, we also conducted a detailed analysis of the change in electrical properties of graphene and In_2O_3 sublayers induced by hybridization. It provides insight into the effects of the hybridization on electrical properties of the p-n-layer-stacked bilayer. (*i.e.*, *p*-type of graphene and *n*-type of In_2O_3) As a result, we could obtain large-area uniformity of the conductance using the In_2O_3 underlayer only with a few nanometers thick despite the presence of microscale defects on the graphene. Moreover, the GI-bilayer exhibited remarkably enhanced electrical conductance owing to p-type doping on the graphene. Hall measurements and following analysis with multilayer Hall measurement model,[37] Raman spectrum, and ultraviolet

photoelectron spectroscopy (UPS) are used to further investigate the nature of p-type doping on the graphene in GI-bilayer.

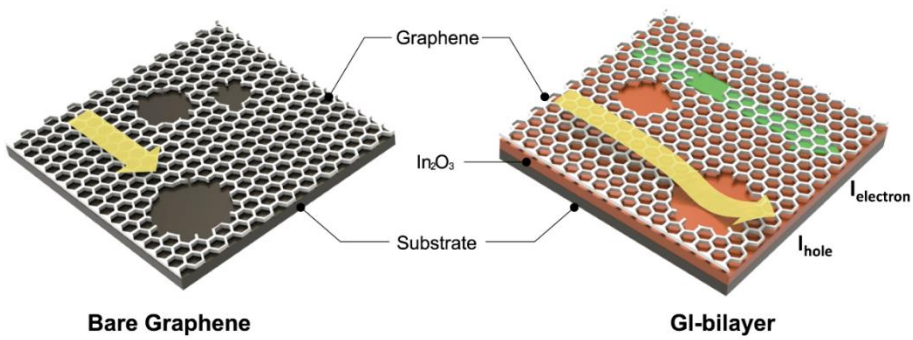


Figure 3-3. Schematic diagram of GI-bilayer. The GI-bilayer was prepared by transferring CVD-grown monolayer graphene onto ALD-grown In_2O_3. Underlying In_2O_3 layer in GI-bilayer provides an electrical bypath to circumvent the microscale defects on the graphene.

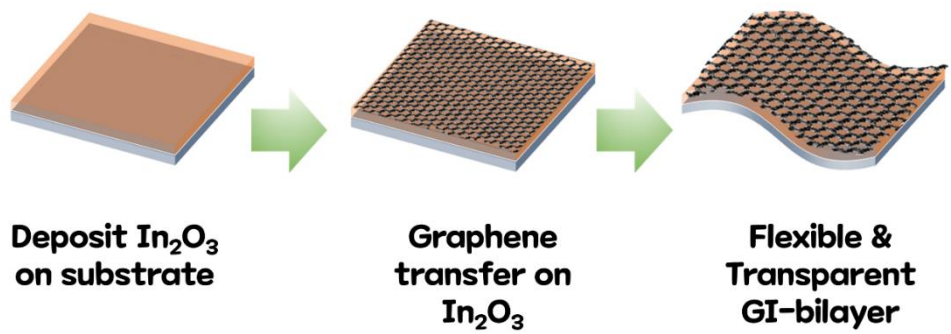


Figure 3-4. Fabrication process of GI-bilayer structure. ALD-In2O3 thin film was deposited on substrate, and CVD-grown graphene layer was transferred onto In_2O_3 layer subsequently.

3.2 Experimental details

3.2.1 Deposition of In_2O_3 film

In_2O_3 thin films were deposited using an flow-reactor type ALD system (LUCIDA D-100, NCD Co., Ltd., Korea) at a deposition temperature of 217 ℃ as reported in our previous results.[38] Trimethylindium (TMIn, EG Chem Co., Ltd., Korea) and water vapor (H_2O) were used as a precursor and a reactant, respectively, and the temperature of the canisters containing them was maintained at 50 ℃ and room temperature, respectively. One ALD cycle consisted of TMIn 1 s pulse—N_2 purge 10 s—H_2O 3 s pulse—N_2 purge 10 s.

3.2.2 Graphene growth and transfer

Monolayer graphene was synthesized by CVD on electropolished 25-μm-thick copper foils (Alfa Aesar #13382). First, Cu foil was loaded into a quartz tube and heated to 1015 ℃ in an Ar and H_2 atmosphere under ambient conditions. A two-step growth process under gas flows of Ar (50 sccm), H_2 (12 sccm), and CH_4 (0.5 and 1 sccm for each step) was implemented to grow a fully covered graphene layer on Cu foil with a grain size of ~50 μm.[25] GI-bilayer was prepared by transferring

graphene onto the ALD-grown In_2O_3 thin film substrate by PMMA-assisted wet transfer, as shown in **Figure 3-4**.[13] After transferring the graphene, annealing was conducted at 300 ℃ for 1 h in a H_2 environment under ambient conditions to remove the PMMA supporting layer.

3.2.3 Characterization

The thickness of the In_2O_3 film was measured by ellipsometry (wavelength: 632.8 nm). Surface morphology of the CVD-grown graphene was observed by scanning electron microscopy (MERLIN compact field emission SEM, ZEISS), and the quality of the synthesized graphene was determined by Raman spectroscopy (UniRam system with Princeton charge-coupled device detector and 532 nm laser source). Sheet resistance of GI-bilayer was measured by a four-point probe station. The electrical transport properties of graphene, In_2O_3, and GI-bilayer were investigated using a Hall measurement system (HL 5500PC, BIO-RAD). For Hall measurements, 1 × 1 cm^2 samples were prepared with van der Pauw (VDP) test configuration and subjected to a 0.510 T magnetic field at room temperature. Work function of the graphene in GI-bilayer and bare graphene were determined by UPS. The

measurements conducted by an AXIS Ultra DLD (Kratos, Inc.) equipped with a He Ⅰ lamp ($h\nu$ = 21.2 eV) in normal emission geometry. UV-vis spectrum was acquired by a Carry 5000 UV-vis-NIR spectrometer (Varian) to investigate the optical properties of bare graphene, In_2O_3 films, and the GI-bilayer.

3.3 Results and Discussion

3.3.1 Characterization of CVD-graphene and ALD-In_2O_3

Figure 3-5 shows the Raman spectrum of CVD-grown graphene transferred on the SiO_2 substrate and SEM micrographs of two different regions of the graphene layer obtained. The Raman spectrum clearly shows a G band (~1580 cm^{-1}) and 2D band (~2700 cm^{-1}) while the defective D band (~1350 cm^{-1}) was only very weakly detected. The intensity ratio of the G and 2D bands (I_{2D}/I_G : ~2) and narrow FWHM (Full width half maximum) of the 2D band (28 cm^{-1}) clearly indicate that a monolayer dominant graphene was synthesized by our CVD process.[39] The sheet resistance (R_s) of graphene was measured as 860 Ω/sq, with a sheet carrier concentration of 5.37×10^{12} cm^{-2} and Hall mobility of 1490 $cm^2/V{\cdot}s$: these values suggest that the quality of our graphene was comparable to that of other undoped monolayer graphene specimens.[14] Nonetheless, various types of defects were observed on the graphene surface as shown in Figure 3-5 (b). These defects include not only the typical wrinkles, but also the areas representing non-graphene regions formed by delamination. These microscale defects were mainly formed during the PMMA-assisted wet etching of the Cu substrate and subsequent transfer process.[21] Even though a portion of graphene had been damaged during the handling process, most of graphene surface

exhibited typical clean morphology of CVD-grown graphene as shown in Figure 3-5 (c). The nonuniformity of the electrical properties of graphene related to these defects and its compensation with underlying In_2O_3 layer will be discussed later.

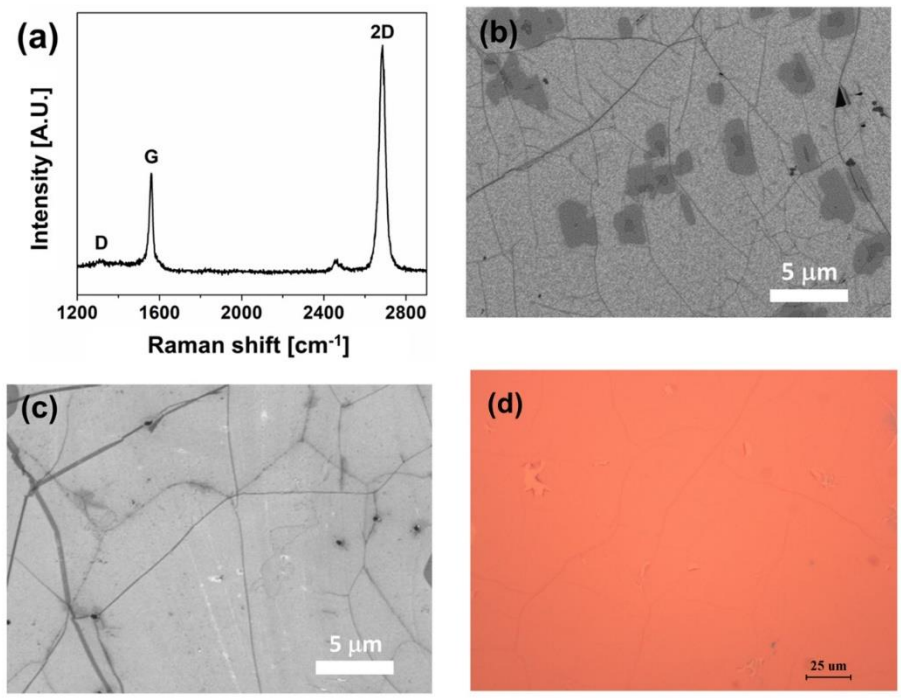


Figure 3-5. Characterization of CVD-graphene layer grown by two-step process. (a) Raman spectrum of graphene on SiO_2. (b) and (c) SEM images of graphene transferred on SiO_2 substrate. (d) Optical Microscope image of graphene transferred on SiO_2 substrate.

Figure 3-6 shows the growth behavior and electrical and optical properties of ALD-In_2O_3 films. Firstly, Figure 3-6 (a) shows the thickness of the In_2O_3 film as a function of the number of ALD cycles. As typical in the ALD growth, the thickness increased linearly as increasing the number of ALD cycles. A growth rate per cycle (GPC) was 0.042 nm and this value well agrees with our previous results.[38] Figure 3-6 (b) shows the sheet resistance (left) and resistivity (right) of the ALD-grown In_2O_3 films as a function of the film thickness (10–50 nm). The resistivities of the ALD-In_2O_3 film were almost constant down to a thickness of 30 nm (~ 1.5×10^{-3} Ω·cm), but it gradually increased up to 3.0×10^{-3} Ω·cm as the film thickness decreased further down to 10 nm. Apparently, it seems that surface scattering effect became more dominant in the films thinner than 20 nm.[40] The measured Hall mobilities also confirmed this hypothesis, as the analysis showed an almost constant value of mobility (~45 cm^2/Vs) except that of 10-nm-thick In_2O_3 (30 cm^2/Vs). Optical transmittances of the In_2O_3 films are shown in Figure 3-6 (d). The In_2O_3 film exhibited highly transparent characteristics over the visible region and a transmittance of 90.8% or more is obtained when the film thickness was below 30 nm at a wavelength of 550 nm. However, the optical transmittance decreased gradually to 85.3% and 78.0% as the film thickness increased to 40 and 50 nm, respectively.

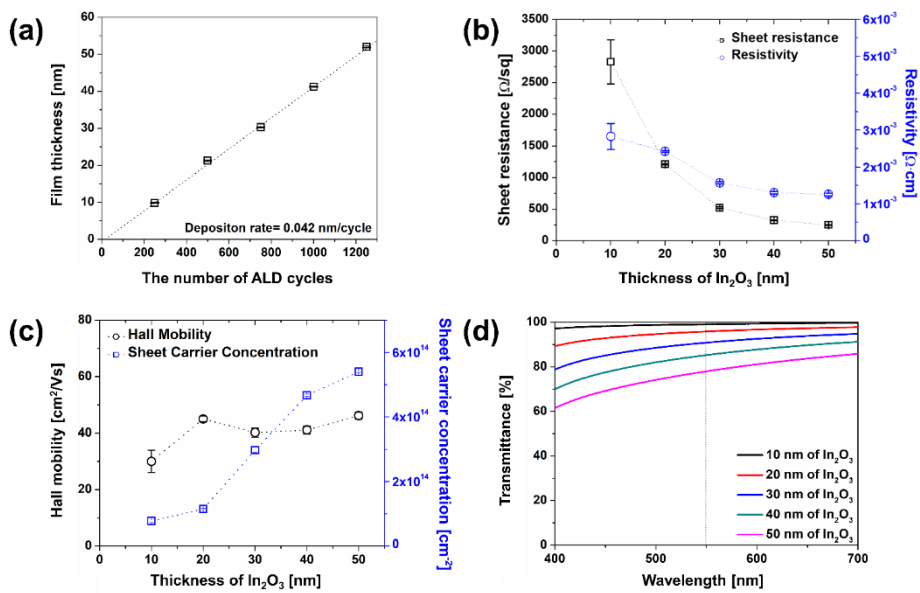


Figure 3-6. Characterization of ALD In_2O_3 film. (a) Thickness of In_2O_3 film as a function of number of ALD cycles. (b) Sheet resistance and resistivity of ALD In_2O_3 (c) Hall mobility and sheet carrier concentration of In_2O_3. (d) Optical transmittance measurement results with respect to thickness of In_2O_3. Quartz substrate was used as a reference for calibration of the optical transmittance.

3.3.2 Electrical and optical properties of GI-bilayer

We studied the electrical and optical properties of the GI-bilayer, as shown in **Figure 3-7**. Figure 3-7 (a) shows the sheet resistance of the GI-bilayer with various thicknesses of the In_2O_3 films both measured (black dot) and calculated (red dot) based on a parallel resistor model. The reference point (thickness of zero) is also shown for the bare graphene with a sheet resistance of 863 Ω/sq. As the thickness of the In_2O_3 films increased from 10 nm to 50 nm, the R_s of GI-bilayer gradually decreased down to 237 Ω/sq. Notably, even the GI-bilayer with the 10-nm-thick In_2O_3 layer showed a dramatically low R_s (443 Ω/sq) compared to that of the bare graphene (863 Ω/sq). Both the bare 50-nm-thick In_2O_3 film and the GI-bilayer with the same thickness of In_2O_3 exhibited R_s values of 251 and 231 Ω/sq, respectively. This indicates the charge conduction was dominated by more electrically conducting In_2O_3 film in this case.

Assuming that graphene and In_2O_3 in the GI-bilayer can be considered as two individual resistors, the sheet resistance of GI-bilayer can be considered as that of a parallel series of the two resistors. Therefore, we can calculate the expected R_s of GI-bilayer as a combination of two parallel resistors (*i.e.,* the combination of graphene and In_2O_3 R_s). The values of each sublayer in GI-bilayer can be taken

from the experimentally measured values, namely $R_{s,Gr}$ = 863 Ω/sq and $R_{s,In}$ as shown in Figure 3-6 (b). The combination of graphene and In_2O_3 R_s is represented as a red line in Figure 3-7 (a). Interestingly, at the low thickness region (10- and 20-nm-thick In_2O_3), an obvious difference was noted between the measured value (black line) and the combination of graphene and In_2O_3 R_s (red line). In the case of GI-bilayer with 10-nm-thick In_2O_3, the measured R_s was 443 Ω/sq and the combination of the graphene and In_2O_3 R_s values was 661 Ω/sq. This result strongly indicates that the electrical property of graphene sublayer is modified by the underlying In_2O_3 in GI-bilayer. On the other hand, it seems that the measured R_s value is rather slightly higher than the combination of graphene and In_2O_3 R_s for GI-bilayer with 40- and 50-nm-thick In_2O_3. For instance, the estimated and measured R_s of GI-bilayer with 40-nm-thick In_2O_3 exhibited 237 and 278 Ω/sq, respectively. It would be attributed to contact resistance between graphene and underlying In_2O_3 sublayer which played a significant role only if the charge conduction was dominated through underlying In_2O_3 film. Contact resistance of vertical transport between graphene and In_2O_3 was estimated as 42 and 46 Ω by assuming partially connected In_2O_3 layer with series contact resistances formed in areas lying below the top contacts on graphene layer. [37]

Figure 3-7 (b) shows both the sheet carrier concentration and Hall mobility of GI-bilayer as a function of the underlying In_2O_3 layer thickness. Hall mobilities of GI-bilayers gradually decreased from 982 $cm^2/V{\cdot}s$ to 47.4 $cm^2/V{\cdot}s$ as increasing thickness of In_2O_3. Interestingly, we found that the major carrier in the GI-bilayer changed from the hole (p-type, up to a 30-nm-thick In_2O_3) to electrons (n-type, for 40-nm and 50-nm thick In_2O_3). The sheet carrier concentration gradually increased from 5.37×10^{12} cm^{-2} for the bare graphene to 9.31×10^{13} cm^{-2} for the GI-bilayer with 30-nm-thick In_2O_3. Then, the majority carrier of GI-bilayer changed from hole to electron as shown in Figure 3-7 (b). In this region, the R_s of the In_2O_3 layer was significantly lower than that of graphene (863 Ω/sq for graphene and 278 Ω/sq for 40 nm of In_2O_3). The thick In_2O_3 film dominated the electron conduction of the overall GI-bilayer. As follow, the sheet carrier concentration and Hall mobility of GI-bilayer showed similar values for 40- and 50-nm bare In_2O_3, as shown in Figure 3-7 (b).

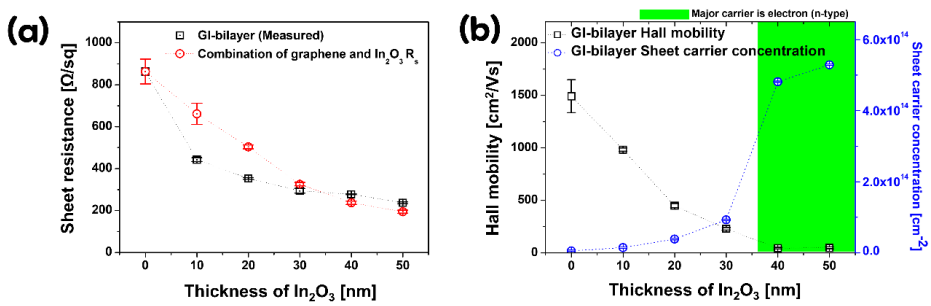


Figure 3-7. Electrical properties of GI-bilayer. (a) Measured R_s of Gi-bilayers as a function of thickness of In_2O_3 (black). Estimated R_s from values of bare graphene and In_2O_3 according to the combination of two parallel resistors, namely graphene and In_2O_3 R_s is also presented (red). (b) Sheet carrier concentration and Hall mobility of GI-bilayer on the thickness of underlying In_2O_3 layer. Sheet carrier concentration and Hall mobility of bare graphene are also represented for 0 nm of In_2O_3.

The majority charge carrier in each sublayer was different: In_2O_3 is an *n*-type material, and graphene is a *p*-type material. Therefore, the electrical properties observed for GI-bilayer should be interpreted as concomitant conduction of electrons and holes in each sublayer. In this point of view, we conducted detail analysis to identify the electrical properties of each sublayer in the GI-bilayer. Similar analysis has been proposed by Arnaudov, B. and Bierwagen *et al.*, who determined the electrical properties of a *p*-*n*-layer-stacked structure using Hall measurements, as shown in **Figure 3-8**.[37, 41] They used this model to analyze the electrical properties of *p*-doped InN, which shows a strong surface electron accumulation layer. Here, the surface accumulation layer works as an *n*-type conduction path independent of the *p*-type bulk region.[41]

Therefore, this model can be directly used to extract the electrical properties of each sublayer of GI-bilayer, as shown in **Figure 3-9**. The model provides an estimate of the total sheet conductance (σ_{tot}) as the sum of the sheet conductance of the 2-dimensional *p*-type layer (σ_p) and that of the bulk *n*-type layer (σ_n), as follows:

$$\sigma_{tot} = \sigma_p + \sigma_n = \sigma_p + \frac{1}{\rho_n} t \quad (1)$$

where t and ρ_n are the thickness and resistivity of In_2O_3, respectively. σ_{tot} is the inverse of the measured R_s of GI-bilayer as shown

in Figure 3-9 (a). Thus, σ_{tot} as a function of t as shown in Figure 3-9 (a). The value of σ_{tot} increased linearly with the thickness, which means that the experimental data matched the model given by Eq. (1) well. The inverse of the slope of the fitted line in Figure 3-9 (b) (ρ_n) is 2.28 $\times 10^{-3}$ Ω·cm, which is comparable to the measured value as shown in Figure 3-9 (b). On the other hand, the R_s of graphene in GI-bilayer extracted from the y-intercept of the fitted line in Figure 3-9 (a) was 510 Ω/sq. Again, it was confirmed that the R_s of graphene decreased drastically for the GI-bilayer compared to that (863 Ω/sq) of bare graphene.

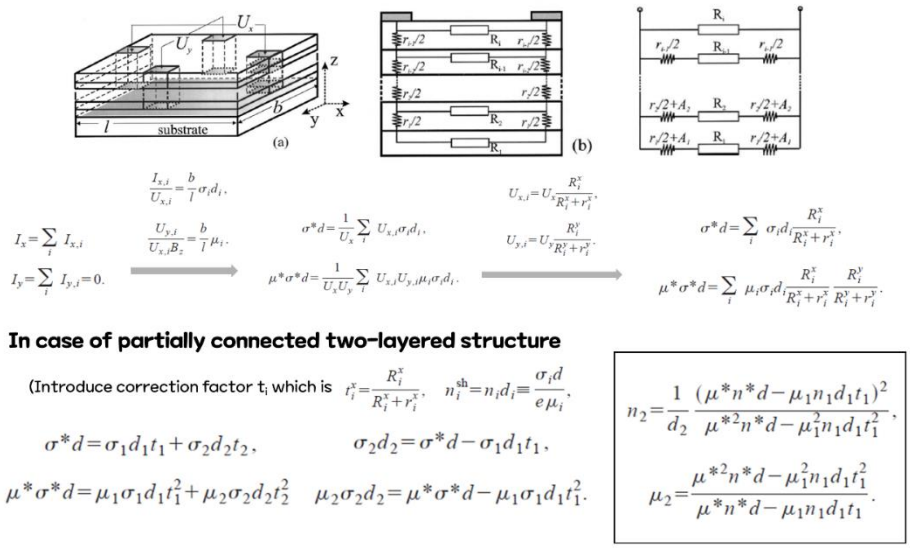


Figure 3-8. Multilayer Hall measurement model in case of partially connected two-layered structures.[37] This model was implied to investigate electrical properties of each sublayer of GI-bilayer in this work.

The sheet carrier concentration and Hall mobility of each sublayer could also be extracted based on Bierwagen's approach.[41] When both electrons and holes work as effective charge carriers in composite materials, the Hall coefficient is expressed using Eq. (2) and rewritten as a function of sheet conductance (σ) and mobility (μ) as shown by Eq.

(3), where sheet conductance $\sigma=nq\mu$, and sheet carrier concentration n .[41, 42]

$$R_H = \frac{\mu_p^2 p + \mu_n^2 n}{q(\mu_p p + \mu_n n)^2} = \frac{1}{n_{tot} q} = \frac{\mu_{tot}}{\sigma_{tot}} \quad (2)$$

$$\sigma_{tot}\mu_{tot} = \sigma_n \mu_n + \sigma_p \mu_p \quad (3)$$

where σ_{tot}, μ_{tot}, and n_{tot} are the measured values of the GI-bilayer, and σ_p, μ_p, σ_n, μ_n, n, and p are the properties of each *p* and *n*-type sublayer. Figure 3-9 (b) shows the linear fitting of $\sigma_{tot}\mu_{tot}$ as a function of σ_n based on Eq. (3). By substituting the σ_p values given by Eq. (1), we can easily extract the mobility of graphene in GI-bilayer from the y-intercept for the linear fitting of $\sigma_{tot}\mu_{tot}$ against σ_n with Hall effect data for the GI-bilayer. The extracted mobility value of graphene in GI-bilayer was 1469 cm^2/Vs (Figure 3-9 (b)), almost the same as that of bare graphene (1490 $cm^2/V{\cdot}s$). In addition, the sheet carrier concentration of graphene in GI-bilayer was obtained from the extracted sheet conductance (Figure 3-9 (a)) and Hall mobility (Figure 3-9 (b)). The calculated sheet carrier concentration of graphene in GI-bilayer increased from 5.37×10^{12} (bare) to 8.34×10^{12} cm^{-2} (in GI-bilayer). In other words, graphene in GI-bilayer is *p*-type-doped by the underlying In_2O_3, which results in the enhancement of the sheet conductance of graphene in GI-bilayer. Electrical properties of bare

graphene and graphene in GI-bilayer, which reflect the enhancement of sheet carrier concentration and corresponding sheet conductance of graphene in GI-bilayer are listed in **Table 3-1**.

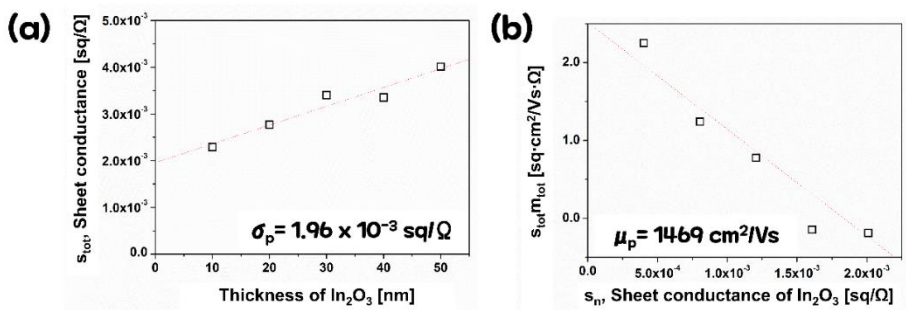


Figure 3-9. Extracted sheet conductivity and charge carrier mobility of graphene sublayer in GI-bilayer by multilayer Hall measurement model. (a) Sheet conductance (σ_{tot}) of GI-bilayer according to thickness of In_2O_3 film and linear fit to extract sheet conductance of graphene sublayer in GI-bilayer (σ_p). (b) Plot of σ_{tot}·μ_{tot} against σ_n and linear fit to extract mobility of graphene sublayer in GI-bilayer (μ_p).

	Sheet Conductance [$\times 10^{-3}$ sq · Ω^{-1}]	R_s [Ω/sq]	Carrier mobility [$cm^2/V \cdot s$]	Sheet carrier concentration [$\times 10^{12}$ cm^{-2}]
Bare Graphene	1.28	863	1490	5.37
Graphene in GI-bilayer	1.96	510	1469	8.34

Table 3-1. Electrical properties of bare graphene and graphene in GI-bilayer.

We also measured the optical transmittance of the GI-bilayers for visible light prepared on quartz substrates, as shown in **Figure 3-10**. For each thickness of In_2O_3, the optical transmittance was observed as simply the sum of the absorption values of bare In_2O_3 and graphene. With the In_2O_3 films thinner than 20 nm, we could achieve industrially applicable optical transmittance of the GI-bilayer: more than 93% transparency at a wavelength 550 nm.

Raman spectroscopy and UPS analysis were further conducted to elucidate the *p*-type doping of graphene in the GI-bilayer, as shown in **Figure 3-11**. On comparing the positions of the G and 2D bands, a blue shift in the peak position (from 1592 to 1600 cm^{-1} for G band, from 2722 to 2728 cm^{-1} for 2D band) was clearly observed. This blue shift was reported for numerous *p*-type doped graphene[39, 43] and is regarded as a feature of *p*-type doping of graphene. Therefore, *p*-type doping of the graphene in the GI-bilayer was double-checked.

Furthermore, UPS analysis more directly revealed a change in the electronic energy state of graphene. Figure 3-11 (b) shows the enlarged UPS spectrum of bare graphene and GI-bilayer. UPS can be used to determine the work function by checking the cut-off binding energy since it depends on work function of materials ($\Phi_F = h\nu - E_{cutoff}$, Figure 3-11 (b)). Fermi levels of the bare graphene and graphene in the

GI-bilayer were 4.74 eV and 4.88 eV, respectively. This depicts down-shift of the Fermi level due to the *p*-type doping, which is consistent with Hall measurement results and Raman spectrum. Therefore, it is clear that the hole concentration of graphene in the GI-bilayer increased by the doping and it resulted in the remarkable conductance enhancement of the GI-bilayer.

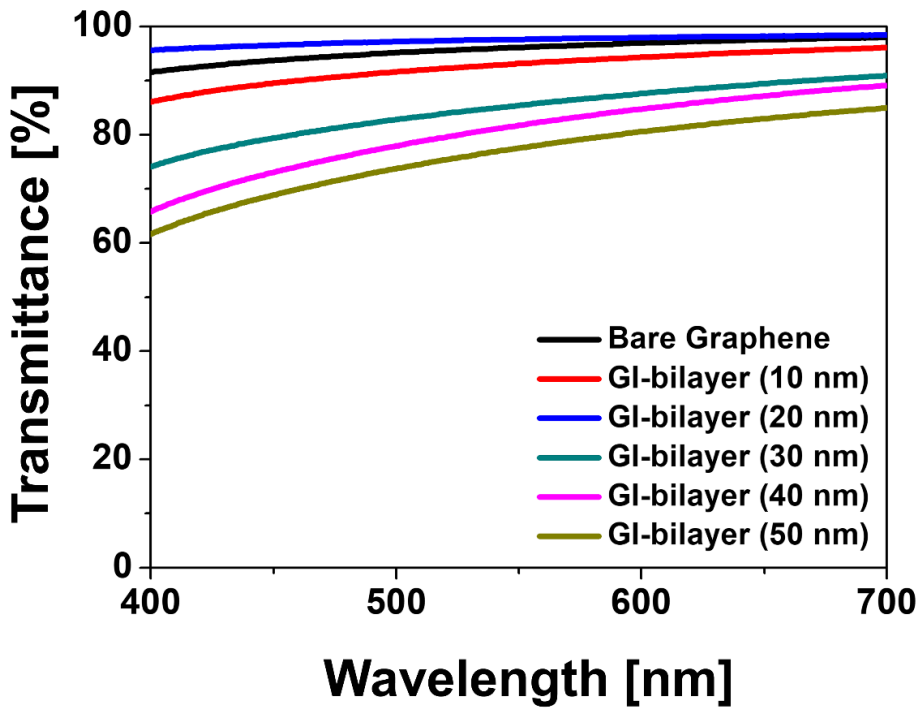


Figure 3-10. Optical transmittance of bare graphene and GI-bilayers according to the thickness of In_2O_3.

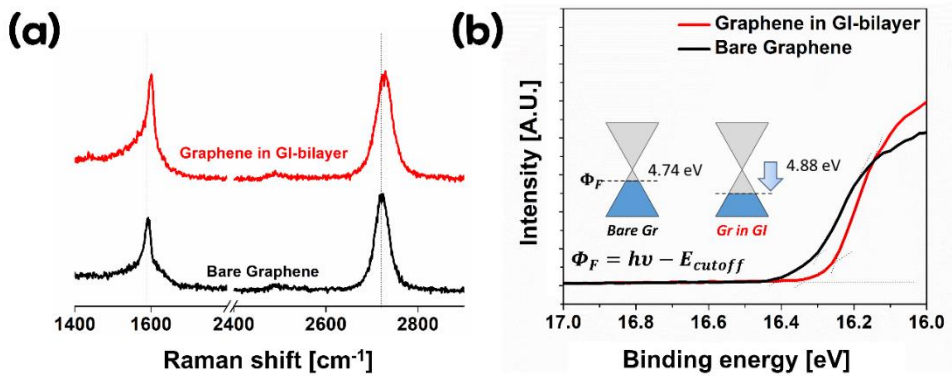


Figure 3-11. *P*-type doping on graphene in GI-bilayer. (a) Representative Raman spectrum of bare graphene (black) and graphene in GI-bilayer (red). Perpendicular guidelines indicate peak position of G and 2D bands of the bare graphene. (b) Enlarged UPS spectrum for low-kinetic-energy part of bare graphene and the one in the GI-bilayer. Schematic represents Fermi level shift of the graphene.

3.3.3 Large-areal sheet resistance uniformity of GI-bilayer

Reliability of the TCE with a large-area uniform R_s is another major requirement for practical application. In this context, large-area R_s uniformity of GI-bilayer was investigated. Figure 3-12 shows a histogram and mappings within 7 × 7 cm^2 scale of bare graphene and the GI-bilayer. The R_s was measured at 11 × 11 points fairly distributed in the whole area. In the R_s mapping of graphene on SiO_2 wafer, some macroscale areas showed a significantly higher R_s compared to the mean value, as shown in **Figure 3-12**.[21, 27] On the other hand, excellent R_s uniformity of GI-bilayer is indicated by the same color in the contour map and the narrow distribution of the R_s histogram. We also confirmed outstanding R_s uniformity of the GI-bilayer by the standard deviation of R_s and % R_s uniformity, which are listed in **Table 3-2**. The % R_s uniformity, which is a reliability parameter for practical manufacturing processes, is defined by the following equation;[44]

$$\%\ R_s \text{ Uniformity } (\%) = \frac{(R_{s,Max} - R_{s,Min})}{2 \times R_{s,Avg}} \times 100\% \quad (4)$$

where $R_{s,Max}$, $R_{s,Min}$, and $R_{s,Avg}$ are the highest, lowest, and average values of the measured sheet resistance (Ω/sq), respectively. A wide distribution of measured R_s data denotes poor R_s uniformity with a high %

R_s uniformity value. In the case of bare graphene, R_s uniformity of 151.1% was noted and this value is about three times higher than the average value. The R_s standard deviation for GI-bilayer decreased by an order of magnitude compared to that bare graphene, from 149.74 Ω/sq to 7.5 Ω/sq. The % R_s uniformity of GI-bilayer also showed a value of only 17.7%, which is acceptable for practical applications. This drastic enhancement in the R_s uniformity can be attributed to the underlying In_2O_3 layer, which compensated the charge transport degradation on the defects of graphene. The excellent R_s uniformity of GI-bilayer provides another key advantage for practical applications.

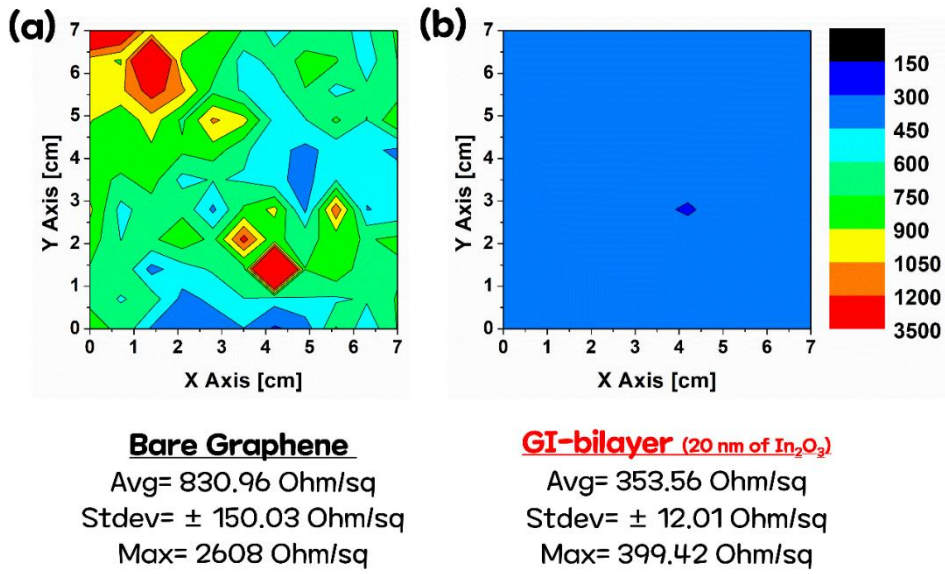


Figure 3-12. Large-area R_s uniformity of the GI-bilayer. Contour map of R_s for (a) bare graphene, and (b) GI-bilayer with 20-nm-thick In_2O_3 sublayer.

Material	R_s average [Ω/sq]	R_s standard deviation [Ω/sq]	% R_s uniformity (%)
In_2O_3 only	1211.4	11.4	1.82
Bare graphene	863.24	149.74	151.1
GI-bilayer	353.56	7.5	17.7

Table 3-2. Areal sheet resistance uniformity of bare In2O3, bare graphene and the GI-bilayer.

3.4 Summary and Conclusion

In this work, we investigated the electrical and optical properties of the GI-bilayer as a transparent conducting electrode with the improved areal-uniformity. By introducing the In_2O_3 underlayer, the sheet resistance of graphene decreased significantly from 863 Ω/sq (conventional monolayer graphene) to 510 Ω/sq (graphene in the GI-bilayer). This decrease was interpreted as a result of *p*-type doping on the graphene induced by the underlying In_2O_3 layer. Multilayer Hall measurement model, Raman spectroscopy and UPS, suggested a clue of *p*-type doping of graphene in GI-bilayer. More importantly, it should be emphasized that the GI-bilayer exhibited the extreme uniformity on the large-area scale [standard deviation of only 12 Ω/sq over the large area of 49 cm^2 owing to the super-uniform ALD-grown In_2O_3 layer underneath the graphene. Specifically, it was proposed that the In_2O_3 underlayer acted as a current bypath for a damaged region on the graphene. These results suggest that our GI-bilayer is a promising material that can be used in the fabrication of a highly reliable transparent conducting electrode.

References

(1) Tseng, S. F.; Hsiao, W. T.; Huang, K. C.; Chiang, D.; Chen, M. F.; Chou, C. P. Laser scribing of indium tin oxide (ITO) thin films deposited on various substrates for touch panels. *Appl. Surf. Sci.* **2010**, *257*, 1487-1494.

(2) Chen, M.; Pei, Z. L.; Sun, C.; Gong, J.; Huang, R. F.; Wen, L. S. ZAO: an attractive potential substitute for ITO in flat display panels. *Mat. Sci. Eng. B-Solid* **2001**, *85*, 212-217.

(3) Thomas, S.; Deepak, T. G.; Anjusree, G. S.; Arun, T. A.; Nair, S. V.; Nair, A. S. A review on counter electrode materials in dye-sensitized solar cells. *J. Mater. Chem. A* **2014**, *2*, 4474-4490.

(4) Ohta, H.; Hosono, H. Transparent oxide optoelectronics. *Mater Today* **2004**, *7*, 42-51.

(5) De, S.; Coleman, J. N. Are There Fundamental Limitations on the Sheet Resistance and Transmittance of Thin Graphene Films? *Acs Nano* **2010**, *4*, 2713-2720.

(6) Minami, T. Present status of transparent conducting oxide ing oxide thin-film development for Indium-Tin-Oxide (ITO) substitutes. *Thin Solid Films* **2008**, *516*, 5822-5828.

(7) Cairns, D. R.; Witte, R. P.; Sparacin, D. K.; Sachsman, S. M.; Paine,

D. C.; Crawford, G. P.; Newton, R. R. Strain-dependent electrical resistance of tin-doped indium oxide on polymer substrates. *Appl. Phys. Lett.* **2000**, *76*, 1425-1427.

(8) Cairns, D. R.; Crawford, G. P. Electromechanical properties of transparent conducting substrates for flexible electronic displays. *Proc. IEEE* **2005**, *93(8)*, 1451-1458.

(9) Chae, S. H.; Lee, Y. H. Carbon nanotubes and graphene towards soft electronics. *Nano Converg.* **2014**, *1*, 15.

(10) Kim, D. Y.; Kim, M. J.; Sung, G.; Sun, J. Y. Stretchable and reflective displays: materials, technologies and strategies. *Nano Converg.* **2019**, *6*, 21.

(11) Zhao, Y.; Kim, A.; Wan, G. X.; Tee, B. C. K. Design and applications of stretchable and self-healable conductors for soft electronics. *Nano Converg.* **2019**, *6*, 25.

(12) Lee, C.; Wei, X. D.; Kysar, J. W.; Hone, J. Measurement of the elastic properties and intrinsic strength of monolayer graphene. *Science* **2008**, *321*, 385-388.

(13) Kim, K. S.; Zhao, Y.; Jang, H.; Lee, S. Y.; Kim, J. M.; Kim, K. S.; Ahn, J. H.; Kim, P.; Choi, J. Y.; Hong, B. H. Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature* **2009**, *457*,

706-710.

(14) Pang, S. P.; Hernandez, Y.; Feng, X. L.; Mullen, K. Graphene as Transparent Electrode Material for Organic Electronics. *Adv. Mater.* **2011**, *23*, 2779-2795.

(15) Bang, K.; Chee, S. S.; Kim, K.; Son, M.; Jang, H.; Lee, B. H.; Baik, K. H.; Myoung, J. M.; Ham, M. H. Effect of ribbon width on electrical transport properties of graphene nanoribbons. *Nano Converg.* **2018**, *5*, 7.

(16) Lee, J.; Han, T. H.; Park, M. H.; Jung, D. Y.; Seo, J.; Seo, H. K.; Cho, H.; Kim, E.; Chung, J.; Choi, S. Y.; Kim, T. S.; Lee, T. W.; Yoo, S. Synergetic electrode architecture for efficient graphene-based flexible organic light-emitting diodes. *Nat. Comm.* **2016**, *7*, 11791.

(17) Liu, J. H.; Yi, Y. H.; Zhou, Y. H.; Cai, H. F. Highly Stretchable and Flexible Graphene/ITO Hybrid Transparent Electrode. *Nanoscale Res. Lett.* **2016**, *11*, 108.

(18) Won, S.; Jang, J. W.; Choi, H. J.; Kim, C. H.; Lee, S. B.; Hwangbo, Y.; Kim, K. S.; Yoon, S. G.; Lee, H. J.; Kim, J. H.; Lee, S. B. A graphene meta-interface for enhancing the stretchability of brittle oxide layers. *Nanoscale* **2016**, *8*, 4961-4968.

(19) Lee, S. J.; Kim, Y.; Hwang, J. Y.; Lee, J. H.; Jung, S.; Park, H.; Cho, S.; Nahm, S.; Yang, W. S.; Kim, H.; Han, S. H. Flexible Indium-Tin Oxide

Crystal on Plastic Substrates Supported by Graphene Monolayer. *Sci Rep-Uk* **2017**, *7*, 3131.

(20) Choi, H. J.; Kim, D. B.; Kim, M. H.; Lee, G. H.; Cho, Y. S. Quantitative analysis of improved bending fracture behavior of large-scale graphene monolayer-intervened flexible oxide thin films. *J. Mater. Chem. C* **2018**, *6*, 6125-6131.

(21) Seo, D.; Jeon, S.; Seo, S.; Song, I.; Kim, C.; Park, S.; Harris, J. S.; Chung, U. I. Fully transparent InGaZnO thin film transistors using indium tin oxide/graphene multilayer as source/drain electrodes. *Appl. Phys. Lett.* **2010**, *97*, 172106.

(22) D'Arsie, L.; Esconjauregui, S.; Weatherup, R.; Guo, Y. Z.; Bhardwaj, S.; Centeno, A.; Zurutuza, A.; Cepek, C.; Robertson, J. Stability of graphene doping with MoO_3 and I_2. *Appl. Phys. Lett.* **2014**, *105*, 103103.

(23) Kuruvila, A.; Kidambi, P. R.; Kling, J.; Wagner, J. B.; Robertson, J.; Hofmann, S.; Meyer, J. Organic light emitting diodes with environmentally and thermally stable doped graphene electrodes. *J. Mater. Chem. C* **2014**, *2*, 6940-6945.

(24) Meyer, J.; Kidambi, P. R.; Bayer, B. C.; Weijtens, C.; Kuhn, A.; Centeno, A.; Pesquera, A.; Zurutuza, A.; Robertson, J.; Hofmann, S. Metal Oxide Induced Charge Transfer Doping and Band Alignment of

Graphene Electrodes for Efficient Organic Light Emitting Diodes. *Sci Rep-Uk* **2014,** *4*, 5380.

(25) Song, W.; Kwon, S. Y.; Myung, S.; Jung, M. W.; Kim, S. J.; Min, B. K.; Kang, M. A.; Kim, S. H.; Lim, J.; An, K. S. High-mobility ambipolar ZnO-graphene hybrid thin film transistors. *Sci Rep-Uk* **2014**, *4*, 4064.

(26) Sanders, S.; Cabrero-Vilatela, A.; Kidambi, P. R.; Alexander-Webber, J. A.; Weijtens, C.; Braeuninger-Weimer, P.; Aria, A. I.; Qasim, M. M.; Wilkinson, T. D.; Robertson, J.; Hofmann, S.; Meyer, J. Engineering high charge transfer n-doping of graphene electrodes and its application to organic electronics. *Nanoscale* **2015,** *7*, 13135-13142.

(27) Han, K. S.; Kalode, P. Y.; Lee, Y. E. K.; Kim, H.; Lee, L.; Sung, M. M. A non-destructive n-doping method for graphene with precise control of electronic properties via atomic layer deposition. *Nanoscale* **2016,** *8*, 5000-5005.

(28) Li, X. S.; Zhu, Y. W.; Cai, W. W.; Borysiak, M.; Han, B. Y.; Chen, D.; Piner, R. D.; Colombo, L.; Ruoff, R. S. Transfer of Large-Area Graphene Films for High-Performance Transparent Conductive Electrodes. *Nano Lett* **2009**, 9, 4359-4363.

(29) Bae, S.; Kim, H.; Lee, Y.; Xu, X. F.; Park, J. S.; Zheng, Y.; Balakrishnan, J.; Lei, T.; Kim, H. R.; Song, Y. I.; Kim, Y. J.; Kim, K. S.;

Ozyilmaz, B.; Ahn, J. H.; Hong, B. H.; Iijima, S. Roll-to-roll production of 30-inch graphene films for transparent electrodes. *Nat. Nanotechnol.* **2010**, *5*, 574-578.

(30) Munoz, R.; Gomez-Aleixandre, C. Review of CVD Synthesis of Graphene. *Chem. Vapor Depos.* **2013**, *19*, 297-322.

(31) Cho, S. Y.; Kim, M.; Kim, M. S.; Lee, M. H.; Kim, K. B. Effect of Cu surface treatment in graphene growth by chemical vapor deposition. *Mater. Lett.* **2019**, *236*, 403-407.

(32) Kim, M.; Kim, K. J.; Lee, S. J.; Kim, H. M.; Cho, S. Y.; Kim, M. S.; Kim, S. H.; Kim, K. B. Highly Stable and Effective Doping of Graphene by Selective Atomic Layer Deposition of Ruthenium. *ACS Appl. Mater. Interfaces* **2017**, *9*, 701-709.

(33) Chan, J.; Venugopal, A.; Pirkle, A.; McDonnell, S.; Hinojos, D.; Magnuson, C. W.; Ruoff, R. S.; Colombo, L.; Wallace, R. M.; Vogel, E. M. Reducing Extrinsic Performance-Limiting Factors in Graphene Grown by Chemical Vapor Deposition. *ACS Nano* **2012**, *6*, 3224-3229.

(34) Liang, X. L.; Sperling, B. A.; Calizo, I.; Cheng, G. J.; Hacker, C. A.; Zhang, Q.; Obeng, Y.; Yan, K.; Peng, H. L.; Li, Q. L.; Zhu, X. X.; Yuan, H.; Walker, A. R. H.; Liu, Z. F.; Peng, L. M.; Richter, C. A. Toward Clean and Crackless Transfer of Graphene. *ACS Nano* **2011**, *5*, 9144-9153.

(35) Lee, S. M.; Kim, J. H.; Ahn, J. H. Graphene as a flexible electronic material: mechanical limitations by defect formation and efforts to overcome. *Mater Today* **2015**, *18*, 336-344.

(36) Kim, H. H.; Lee, S. K.; Lee, S. G.; Lee, E.; Cho, K. Wetting-Assisted Crack- and Wrinkle-Free Transfer of Wafer-Scale Graphene onto Arbitrary Substrates over a Wide Range of Surface Energies. *Adv Funct. Mater* **2016**, *26*, 2070-2077.

(37) Arnaudov, B.; Paskova, T.; Evtimova, S.; Valcheva, E.; Heuken, M.; Monemar, B. Multilayer model for Hall effect data analysis of semiconductor structures with step-changed conductivity. *Phys. Rev. B* **2003**, *67*, 045314.

(38) Lee, D. J.; Kwon, J. Y.; Lee, J. I.; Kim, K. B. Self-Limiting Film Growth of Transparent Conducting In2O3 by Atomic Layer Deposition using Trimethylindium and Water Vapor. *J. Phys. Chem. C* **2011**, *115*, 15384-15389.

(39) Ferrari, A. C.; Basko, D. M. Raman spectroscopy as a versatile tool for studying the properties of graphene. *Nat. Nanotechnol.* **2013**, *8*, 235-246.

(40) Cattani, M.; Vaz, A. R.; Wiederkehr, R. S.; Teixeira, F. S.; Salvadori, M. C.; Brown, I. G. Influence of electron scattering from morphological

granularity and surface roughness on thin film electrical resistivity. *Surf. Rev. Lett.* **2007**, *14*, 87-91.

(41) Bierwagen, O.; Choi, S.; Speck, J. S. Hall and Seebeck measurement of a p-n layer stack: Determining InN bulk hole transport properties in the presence of a strong surface electron accumulation layer. *Phys. Rev. B* **2012**, *85*, 165205.

(42) Petritz, R. L. Theory of an Experiment for Measuring the Mobility and Density of Carriers in the Space-Charge Region of a Semiconductor Surface. *Phys Rev* **1958**, *110*, 1254-1262.

(43) Beams, R.; Cancado, L. G.; Novotny, L. Raman characterization of defects and dopants in graphene. *J. Phys-Condens. Mat.* **2015**, *27*, 083002

(44) Hudaya, C.; Park, J. H.; Lee, J. K. Effects of process parameters on sheet resistance uniformity of fluorine-doped tin oxide thin films. *Nanoscale Res. Lett.* **2012**, *7*, 17,

Chapter 4.

Defect Engineering in CVD-graphene as a Copper Diffusion Barrier (Part II)

: Patching of defects in graphene by atomic layer deposition of Ruthenium for Cu metallization

4.1 Introduction

In the 60 years since the first integrated circuit (IC) was demonstrated, evolution of ground rule, supposed to Moore's law has enabled the era of silicon ultra-large-scale integration (ULSI) in Information revolution.[1,2] As technical demands grew, Copper (Cu) interconnect has been widely used in IC manufacturing because of its low electrical resistivity and better electromigration reliability than conventional Al.[3] However, aggressive dimensional scaling makes some crucial issues arise from Cu interconnect such as resistance scalability and electromigration reliability. Among them, one of the chief concerns is an increasing global interconnect resistance and following increase in RC delay. As dimension approaches to below 10 nm node, Cu interconnect resistivity has entered an exponential increase regime due to the increased scattering at the surface and grain boundary interfaces, and particularly non-ideal scaling of the Cu diffusion barrier for Cu. In Cu interconnect, barrier material is essential to prevent diffusion of Cu into the interlayer intermetallic dielectric (IMLD) materials that leads to degradation of device performance and failure with dielectric breakdown and short circuits between metal lines. lines occur, creating deep level traps in Si, which hinder reliability of interconnects. Ta/TaN liner/barrier film has been widely used as a Cu diffusion barrier for several decades due owing to no intermetallic compounds in Cu-Ta binary system,

high barrier performance of TaN.[4,5,6] However, considering rapid downscaling has progressed, Ta/TaN barrier layer would have met a scaling challenge owing to its failure at thicknesses below 3 nm.[7] From At this point of view, a new ultra-thin and reliable diffusion barrier urgently required.[1]

As an alternative for TaN barrier to response to the technology nodes,[8] sub 1 nm-thick diffusion barrier with good barrier performance still need to be developed.[2] Cu interconnects are fabricated via electroplating in damascene process, therefore highly uniform diffusion barrier should be formed directly on dielectric. Due to its narrow and deep three-dimensional architecture, a fabrication process based on self-limiting behavior would be desirable to form conformal barrier directly on the dielectric trenches.[3] Self-forming barrier like $MnSi_xO_y$ formed at interface between Cu and SiO2 during post-annealing of Cu-metal alloy has been reported as a self-limiting Cu barrier before,[9] however, Cu diffusion barrier property of this 1.2 nm-thick amorphous $MnSi_xO_y$ barrier couldn't completely prevent Cu diffusion into the dielectric material.[4] Furthermore, processing temperature for constructing Cu diffusion barrier should be compatible with current Back-end-of-line (BEOL) process with processing temperature close or below 450 ℃ not to damage the dielectric material and pre-deposited Cu lines at lower levels.[5]

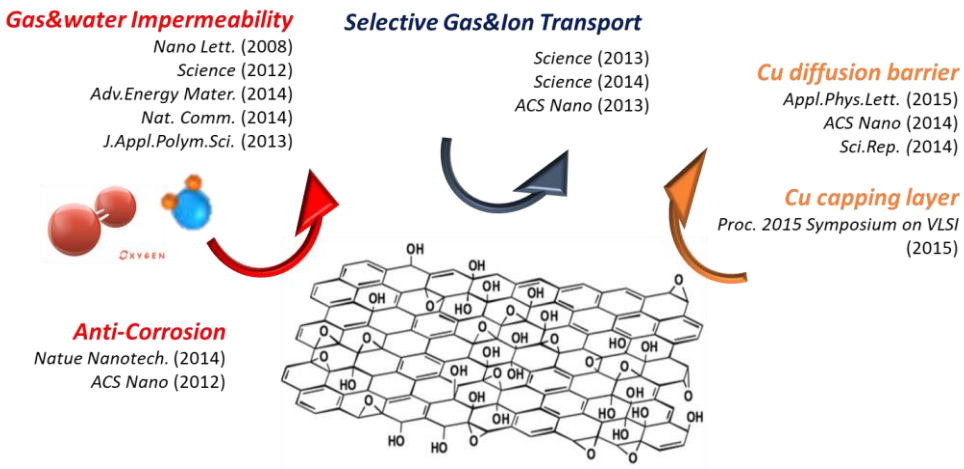


Figure 4-1. Graphene as an impermeable barrier layer for various applications.

Among the various candidates for the next generation Cu diffusion barrier, carbonaceous materials have been considered the constituent materials of the impermeable barrier. There are no Cu-C intermetallic compounds, when referring to the their binary phase diagram.[14] Especially, graphene, composed of a single layer of carbon atoms having in-plane sp2-bonds, has been suggested as a next generation Cu diffusion barrier because of its atomically thin thickness, high thermal and chemical stability, and superior atomic impermeability with extremely small geometrical pores of 0.064 nm, which even helium atom cannot pass through.[15, 16] Conventional thermal CVD graphene grown on a metal catalyst and polycrystalline graphene directly grown on dielectric can be suggested as a large-area

diffusion barrier for Cu interconnects.[17, 18, 19] However, the structural defects of graphene, which inevitably occur in the growth and post-transfer processes make is difficult to block mass transport.[20]

As mentioned above, research results of applying 2D materials as Cu diffusion barriers for motivation have started to be published in earnest from the mid-2010s. As shown in **table 4-1**, in the previous studies, high-quality CVD synthesis with large grain size was mainly utilized. In particular, in the case of graphene, effects such as Cu wire capping effect through reduction of Cu surface scattering and improvement of electromigration reliability have been reported in addition to Cu blocking performance.

Method	Growth Temperature	Barrier thickness	Barrier property	Ref
CVD on Cu foil & Transfer	900℃	1 nm (3 layers)	Thermal stability test [Cu/Si] Withstand up to 750℃	APL[6] (2014)
PECVD direct growth on SiO_2	550℃	5 nm	C-V measurement Withstand 50 min under 4 MV/cm, 400K	Nanoscale[7] (2017)
CVD on Cu foil & Transfer	1000℃	< 1 nm (2 layers)	MOS TDDB under 7 MV/cm, 470 times improvement – w/o barrier	Proc. IEEE[8] (2017)
CVD on Cu & Ni & Transfer	-	0.3 - 4 nm (1-3 layer)	MOS TDDB under 7 MV/cm, 100℃ 2L Gr (~0.8 nm) better than 4 nm of TaN	ACS Nano[9] (2015)
CVD on Cu, Ni & Transfer	1000℃	0.4 -10 nm (1L, MLG)	Thermal stability test [Cu/Si] & TDDB 10 um Grain SLG; withstand up to 900℃ 10 nm MLG~45 nm of TiN under 3 MV/cm, 225℃	Nanoscale[10] (2014)
CVD on Cu & Transfer	900℃	1L Gr & 1 nm of GO & rGO	Thermal stability test [Cu/Si] 1L Gr withstand up to 500℃, 30 min 1 nm of GO, rGO up to 400℃, 30 min	APL[11] (2015)

Table 4-1. Previous results on CVD graphene as a Cu diffusion barrier.

However, in order to utilize CVD graphene as a Cu diffusion barrier in the actual semiconductor wiring process, the following two critical issues need to be addressed. The first one is defects in graphene. Even in the case of graphene synthesized by CVD on a metal catalyst for high quality, vacancy and grain boundaries formed during the growth process exist, and in particular, micro-scale cracks occur during the transfer process. Considering the 2D nature of graphene, these defects should be the fast diffusion path of Cu. The second one is a process integration issue. The PMMA assisted wet transfer process or the roll-to-roll transfer process, which are widely being utilized method to transfer high quality CVD-graphene onto the substrate, cannot be applied to the intermetal dielectric substrate with a trench structure. Therefore, a new back-end process integration method that can conformally form a graphene barrier on the dielectric trench structure is required.

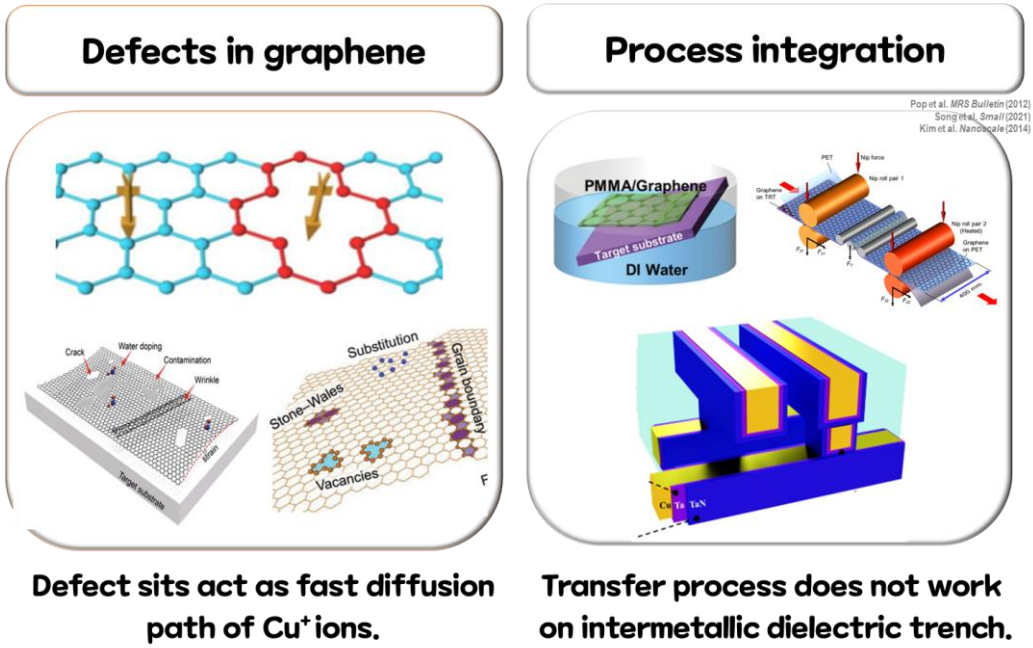


Figure 4-2. Key issues on CVD-graphene as a Cu diffusion barrier

As mentioned above, various types of defects exist in graphene, even in high quality CVD-grown graphene. Broadly classified, there are intrinsic defects such as grain boundary and vacancy formed by heterogeneous nucleation and growth on Cu foil, and defects such as micro or macro scale cracks and wrinkles formed during graphene transfer.

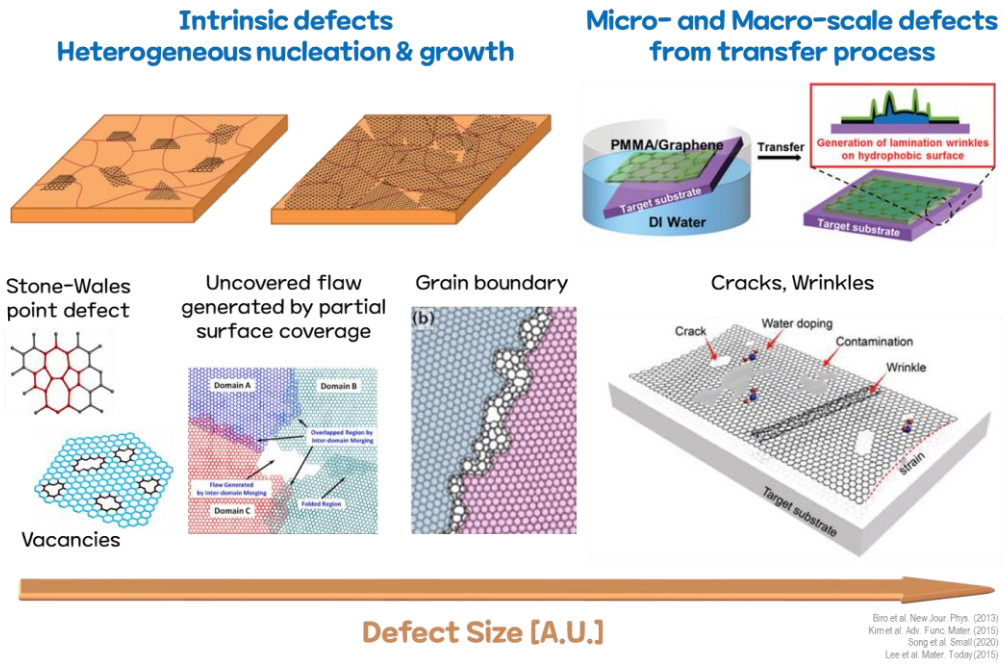


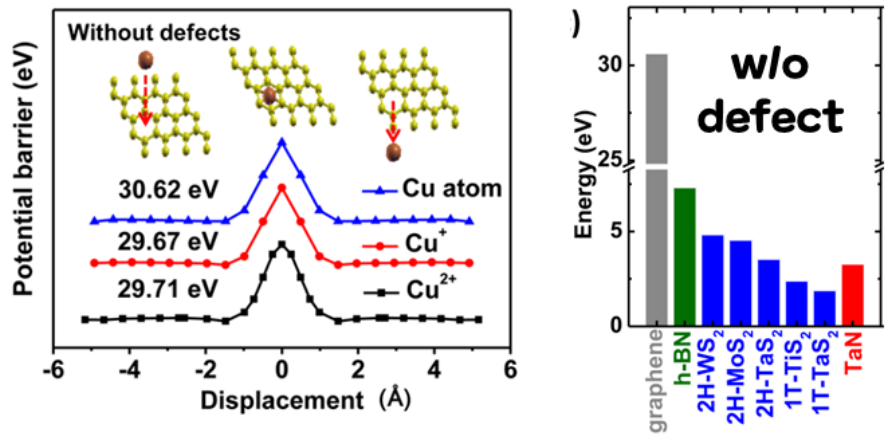
Figure 4-3. Various types of defects in CVD-graphene.

The results of previous studies on the effect of these defects on the penetration of Cu ions are as follows. The results in **Figure 4-4** are the results of the DFT calculation of the potential energy for Cu penetration in the defect site of graphene in a review paper published in 2020 by Zhihong Chen group of Purdue University and published in ACS Nano in 2014. First, the graph on the left is a potential energy landscape plotted by calculating the potential energy of the entire system according to the position of Cu after the displacement of the graphene sheet is set as 0. It can be seen that in the case

of defect-free perfect crystal graphene, it can pass through the hollow of the graphene hexagonal structure only after exceeding a very high potential energy barrier of 30 eV level.

On the other hand, in the case of a defective edge plane of graphene as shown in the **Figure 4-4**, the penetration potential barrier of graphene is rapidly lowered to 0.2 eV level, which is even compared to the potential energy of Cu migration in the TaN grain boundary experimentally measured in the existing TaN grain boundary.

✓ **In case of perfect crystal**



✓ **In case of divacancy & edge plane**

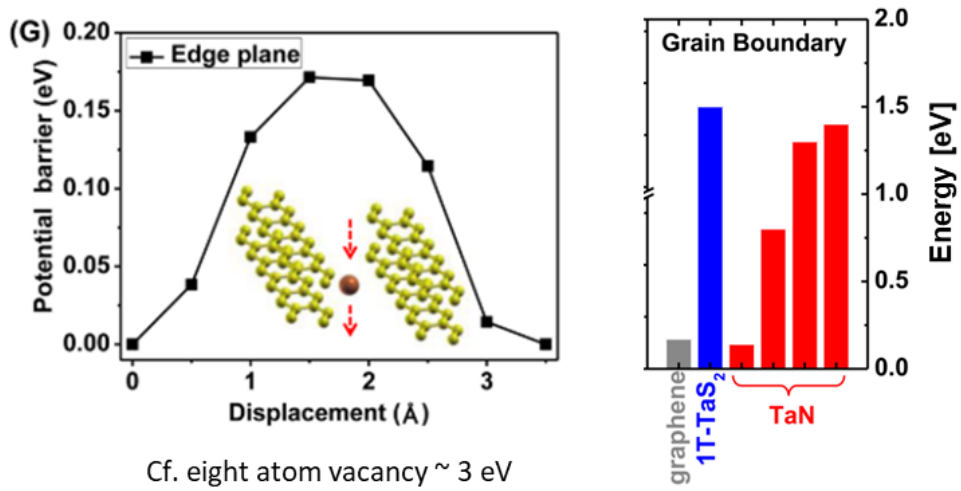


Figure 4-4. Activation energy for penetration of Cu ion through defects in graphene from heterogeneous nucleation and growth.

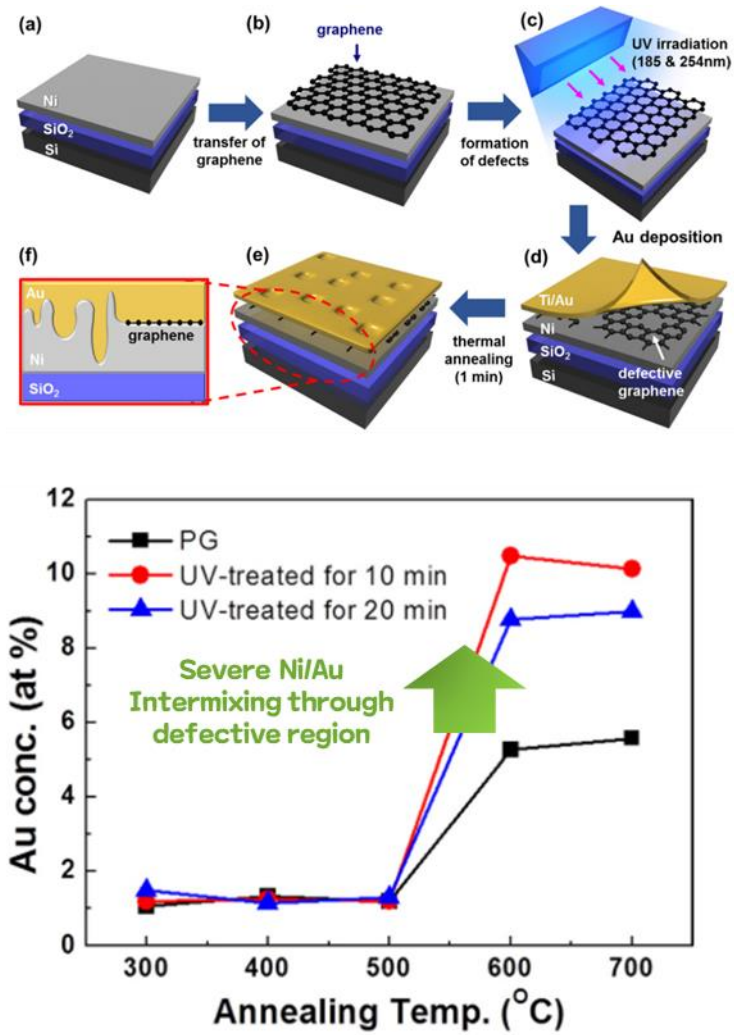


Figure 4-5. Micro- and Macro-scale defects from transfer process.

Figure 4-5 shows the content of using CVD graphene as a metal diffusion barrier at the Au/Ni interface. Here, we compared the barrier properties before and after defect formation after artificially forming microscale defects in graphene through UV radiation. As a result, it can be confirmed that the intermixing between Ni/Au was larger in graphene with microscale defects formed through UV treatment compared to pristine graphene during heat treatment at 600°C, resulting in higher Au concentration in Ni. Through these results, it can be predicted that the graphene grain boundary and vacancy will have a critical effect on Cu penetration.

4.2 Results and discussion

In order to directly check the effect of the grain boundary of graphene on Cu diffusion, the following experiment was conducted. After transferring graphene with various grain sizes from 17 to 58 um by tuning the CVD synthesis conditions, a Cu film of 40 nm was deposited by e-beam evaporation to form a Cu/graphene/Si structure. After that, through heat treatment, the failure temperature of the graphene barrier according to the graphene grain size was confirmed through XRD whether Cu silicide was formed. As a result of the experiment, Cu silicide formation could not be confirmed by XRD in graphene barriers of all grain sizes until heat treatment at 800°C, but Cu silicide peak was observed in graphene barriers with grain size of 17~42 um during 900°C heat treatment, compared to the graphene barrier with a lateral grain size of 58 um that Cu silicide peak did not appear.

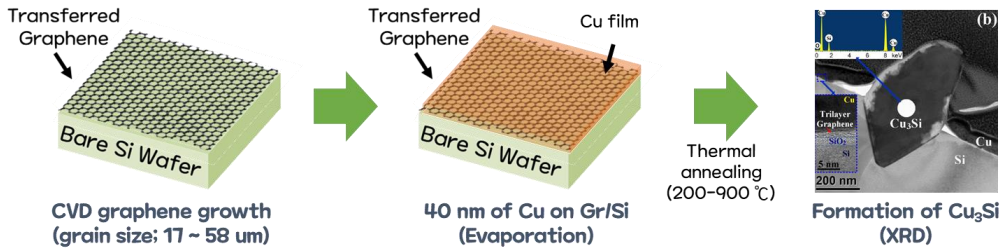


Figure 4-6. Experimental details to investigate barrier property by varying a grain size of CVD-graphene

Through these results, it was experimentally confirmed that the Cu barrier performance improved as the grain size of graphene increased, and the grain boundary of graphene is the most important factor in determining the barrier performance as a Cu diffusion barrier.[12]

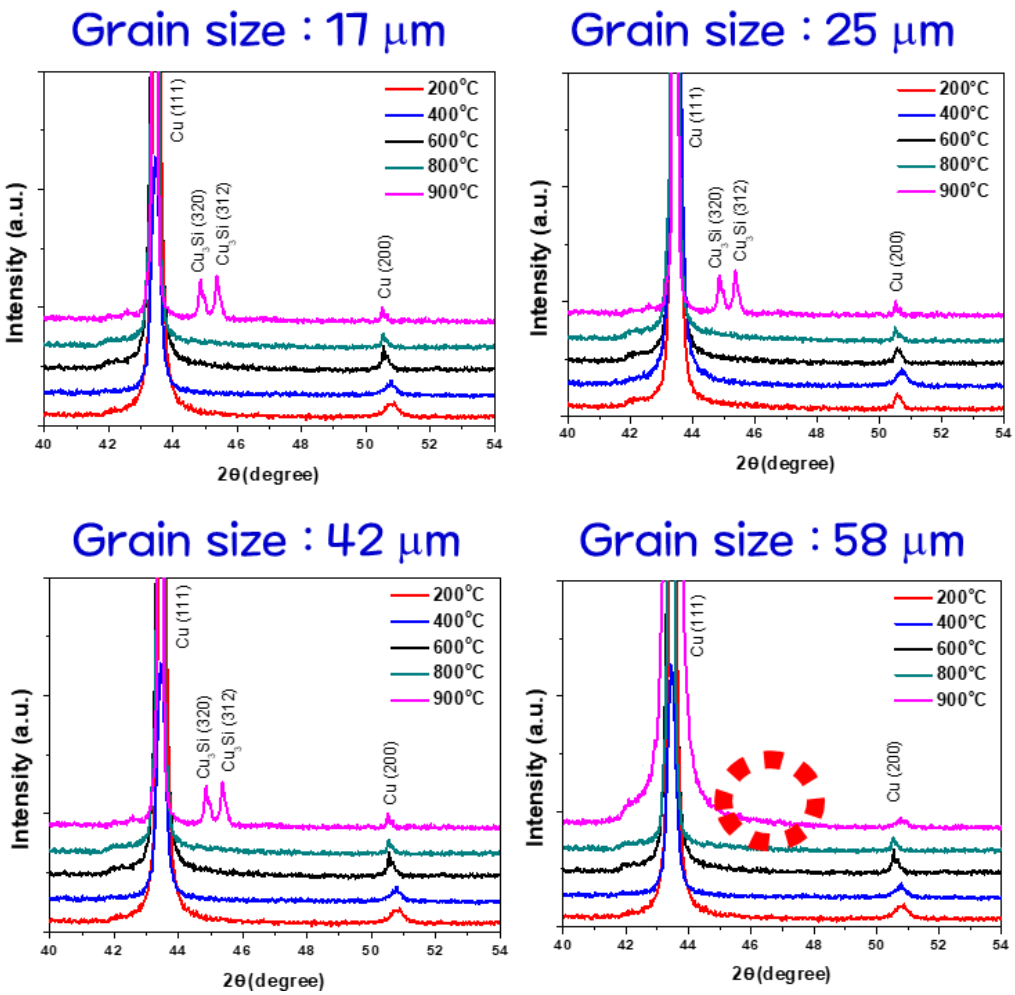


Figure 4-7. XRD characterization results for Cu/Graphene/Si structures after heat treatment

In this study, the atomic layer deposition (ALD) process on graphene has been applied to stuff defects such as grain boundaries that become the major diffusion path of Cu. When the ALD process is applied to graphene, it is deposited selectively only on defect sites, because the ALD precursor is selectively adsorbed only to defect sites where dangling bonds are present rather than adsorbed to the inert surface of graphene. This is already widely known through previous studies that applied metal ALD such as Pt and Ru as shown in the figure and oxide ALD such as Al_2O_3 and ZnO. As a result, the doping effect of graphene has been confirmed. Therefore, from the viewpoint of using graphene as a Cu diffusion barrier, we tried to stuff the graphene defects through the selective deposition behavior of ALD and improve the Cu blocking performance of graphene through defects.

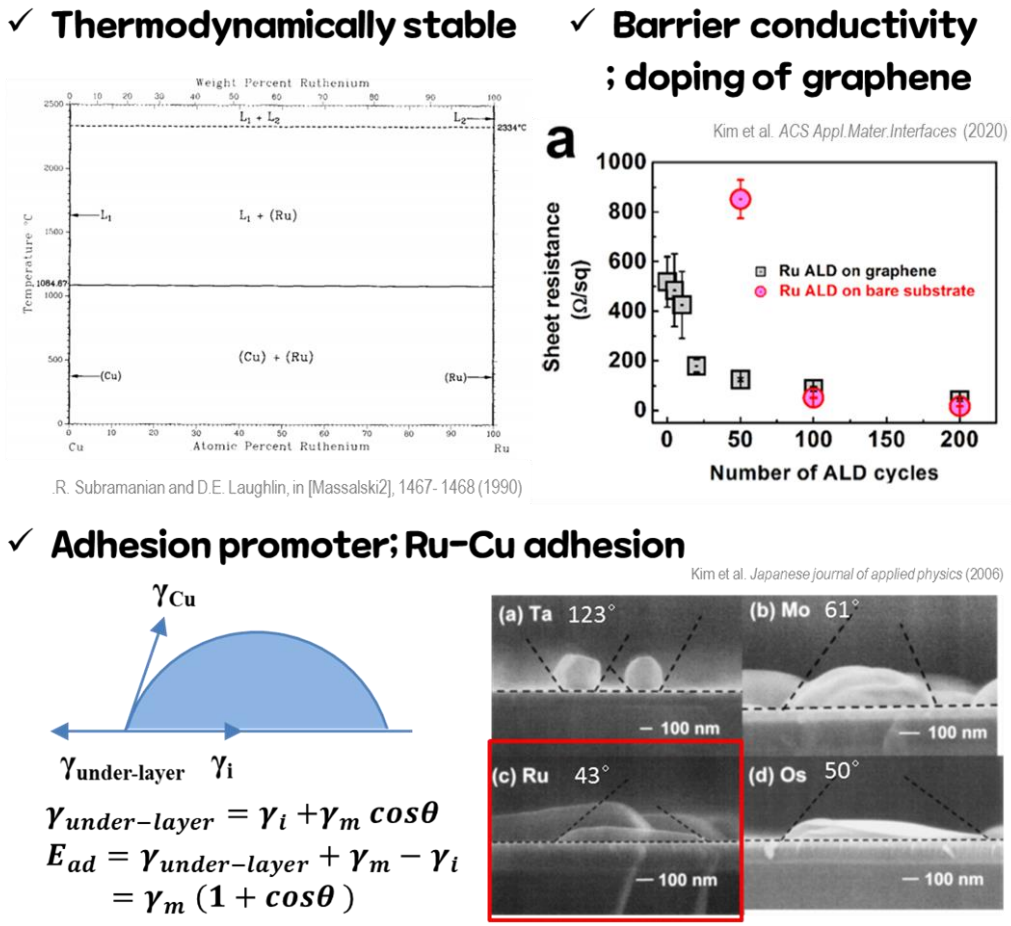
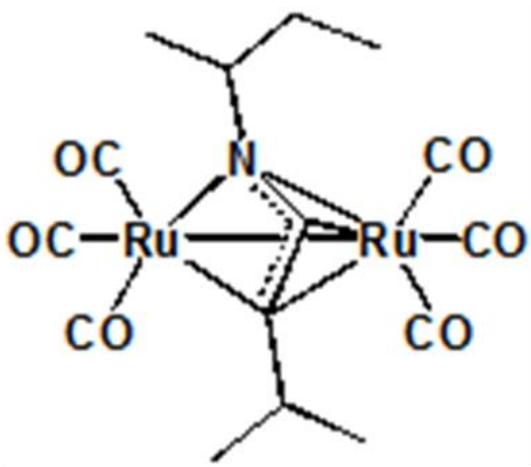


Figure 4-8. ALD materials selection: advantages of Ru as a defect-stuffing elements of CVD-graphene Cu diffusion barrier.

As an ALD deposition material for defect stuffing, Ru, which has the following advantages, was selected. First of all, in the binary phase diagram of Ru and Cu in **Figure 4-8**, it can be seen that Ru and Cu do not form an intermetallic compound, and they are thermodynamically stable due to their very low solubility. Also, as mentioned earlier, our laboratory has published the results of p-type doping of graphene by applying Ru ALD to graphene. **Figure 4-8** shows the sheet resistance of graphene according to the Ru ALD cycle, and it can be seen that the sheet resistance of graphene gradually decreases as the ALD cycle increases. As mentioned in the introduction, lowering the resistivity of the barrier itself is also important to lower the overall wire resistivity. Lastly, there is an adhesion issue with Cu. **Figure 4-8** shows the result of confirming the adhesion to Cu through the Cu wettability, that is, the contact angle, on various thin films such as Ta, Mo, Ru, and Os. As can be seen, it can be seen that Ru has a low contact angle of 43 degrees and has good adhesion with Cu. This is advantageous for securing Cu electromigration reliability, which will be discussed later.

As shown in the **Figure 4-9**, the Ru precursor used TANAKA's Rudic precursor, in which a buten-aminato ligand containing nitrogen and a buten-aminato ligand and a methylpropyl ligand containing six carbonyl groups on two metal-bonded rutheniums. As a thermal ALD, oxygen gas was used as a reactant at a substrate temperature of 220°C. This Ru ALD process

was carried out in the laboratory of Professor Soohyun Kim of Yeungnam University. The results of confirming the deposition pattern according to the Ru ALD cycle by SEM image are as follows. As previously reported,[13] it was confirmed that Ru particles were selectively deposited on defect sites such as grain boundaries of graphene.



Rudic, $C_{15}H_{17}NO_6Ru_2$

[[ruthenium,hexacarbonyl[μ-[(1,2-η)-3-methyl-N-(1-methylpropyl)-1-buten-1-aminato(2-)-κC2, κN1:κN1]]di-, (Ru–Ru)-]]

Figure 4-9. ALD-Ru precursor. Rudic ([[ruthenium,hexacarbonyl[μ-[(1,2-η)-3-methyl-N-(1-methylpropyl)-1-buten-1-aminato(2-)-κC2,κN1:κN1]] di-,(Ru-Ru)-]]

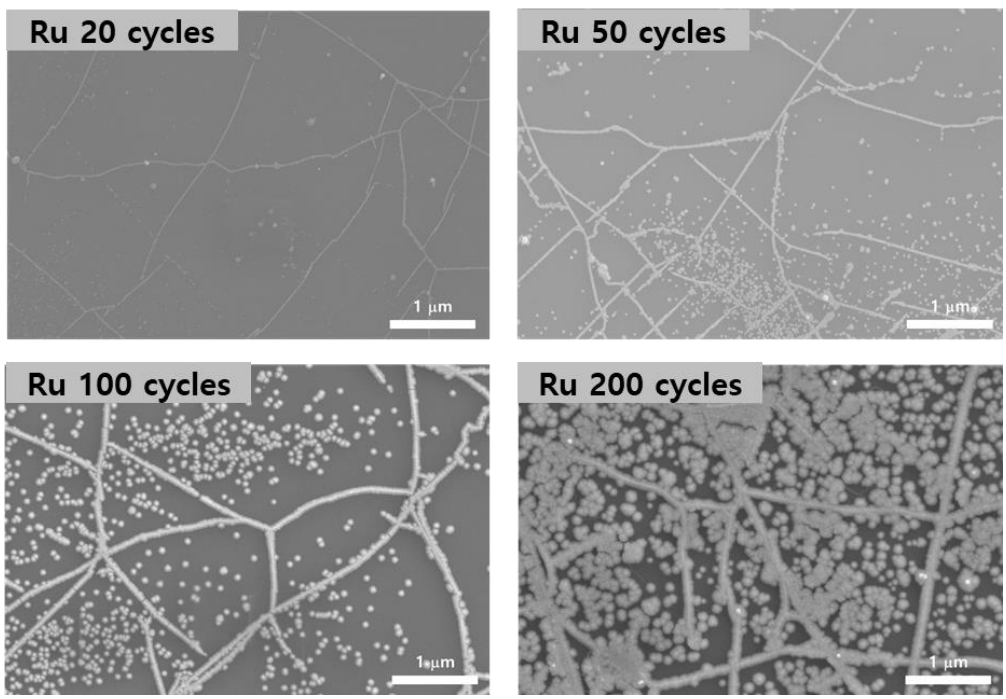


Figure 4-10. Selective deposition of Ru on graphene. SEM images of graphene after 20, 50, 100, and 200 cycles of Ru ALD

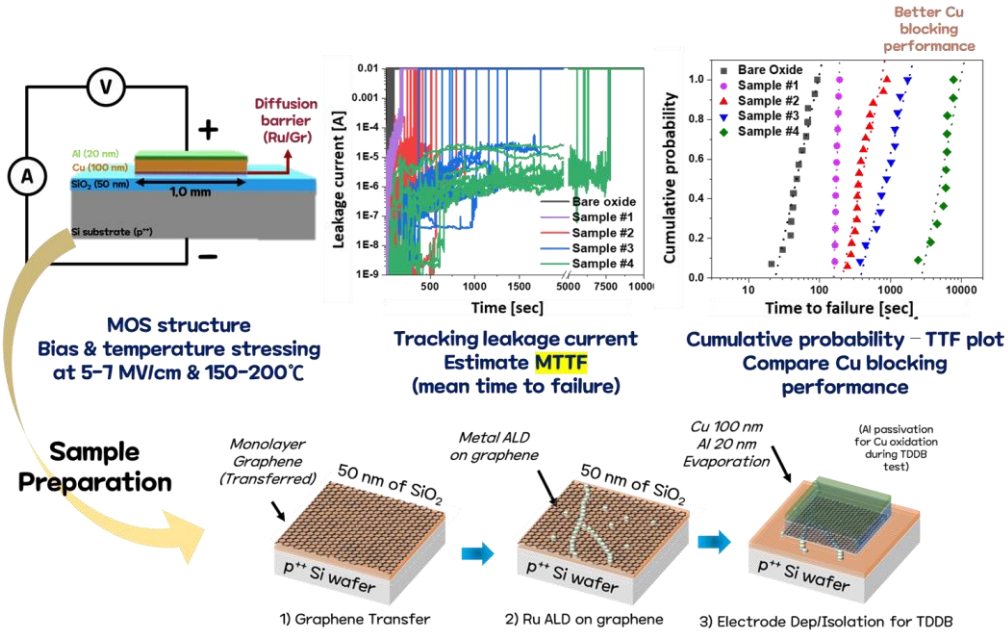


Figure 4-11. Brief introduction and sample preparation process for TDDB (time dependent dielectric breakdown) test

In order to check the Cu blocking performance of the graphene barrier stuffed with defects with Ru, the following time-dependent dielectric breakdown (TDDB) test was conducted. TDDB test is an abbreviation of time dependent dielectric breakdown, and after forming a MOS structure of Cu/barrier/silicon oxide/Si as shown in the **Figure 4-11**, it measures leakage current while applying an electric field at high temperature. When dielectric breakdown occurs in this process, a current path between the top and bottom is formed and the leakage current flows to the mA level, and this time is set

as time-to-failure. Repeat experiments for each barrier material, list them in the order of the shortest failure time, and plot them with the cumulative probability over time to get a plot like the one on the right. Through this cumulative plot, the time to failure between each barrier material can be intuitively compared, and the time-to-failure distribution can also be checked through the slope information.

Samples for this TDDB test were prepared as follows. After transferring graphene onto dry-oxidized 50 nm SiO_2 substrate, Ru ALD process was performed. After depositing 100 nm of Cu for TDDB test and 20 nm of Al for Cu passivation, the remaining graphene was removed through Oxygen RIE process for isolation between contact pads. In order to compare the Cu blocking performance of the graphene barrier before and after Ru ALD, the aforementioned TDDB test was conducted in an electric field of 6 MV/cm and a temperature of 200°C. As shown in **Figure 4-12**, compared to the bare graphene time to failure plot in red, it was confirmed that the time to failure of the Ru ALD post-processed samples was longer, which became longer as the Ru ALD cycle increased and the amount of Ru deposition increased. The results of comparing Time to failure through the box plot of the same data are shown on the right, and it was confirmed that the mean value of Time to failure increased by 427% from 589 seconds to 2524 seconds when Ru ALD 20 cycle was applied. Through these results, it was confirmed that the Cu

blocking performance of the graphene barrier could be improved by stuffing the grain boundary, which is the major diffusion path of Cu, with Ru.

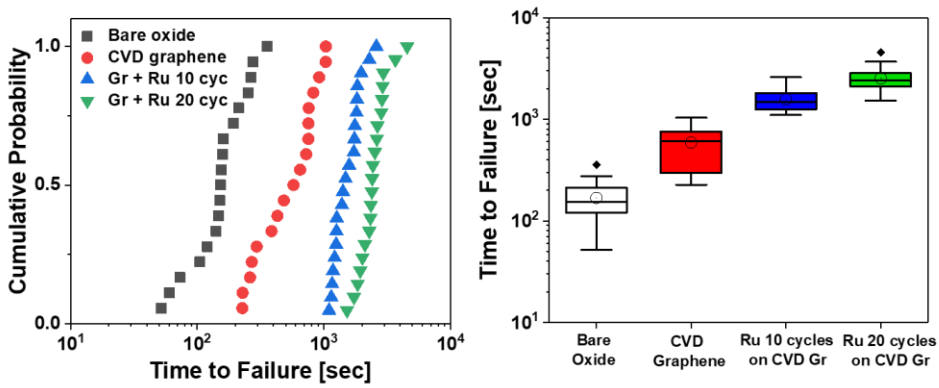


Figure 4-12. Preliminary TDDB results on graphene and defect-stuffed graphene.

In this study, we tried to proceed with a more detailed analysis through TDDB tests by temperature and electric field,[14] beyond simply checking the improvement of Cu blocking performance through a set of TDDB tests.[15] If the TDDB test is performed directly under normal device operating conditions of 0.5 to 1 MV/cm and 100°C, it may take months or years to collect device failure time data. Therefore, the TDDB test is conducted under an electric field that is much harsher than the actual device operating

condition, and it is extrapolated to the actual device operating condition by applying the time to failure field dependent model formula that matches each dielectric breakdown mechanism.[16] The exact dielectric breakdown mechanism under the TDDB test is still controversial, but if the mechanisms presented so far are broadly classified,[17] they can be classified into intrinsic and extrinsic as follows. Intrinsic breakdown refers to the dielectric breakdown mechanism by the breakage of SiO2 weak bonds[18] or electron tunneling in thin oxide without the influence of Cu ion diffusion or drift under TDDB test conditions.[19]

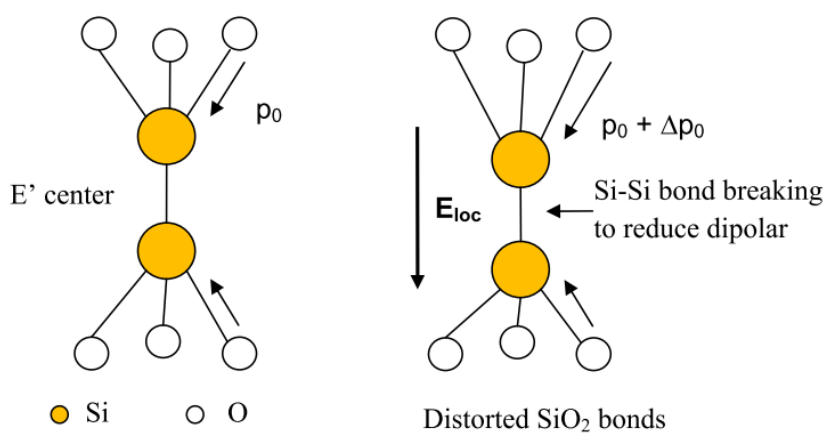


Figure 4-13. Typical example of intrinsic breakdown. Si-Si weak bond breaking to reduce dipolar moment under external E-field stress.

Figure 4-13 shows a typical example of intrinsic breakdown. The Si-Si bond formed in oxygen vacancy in SiO_2 is broken by an applied electric field, trap sites are formed, and dielectric failure occurs as these accumulate.[20]

$$TTF = Aexp\left(\frac{\Delta H_0 - aE}{k_b T}\right) : E\ model \qquad \text{(Eq 5-1)}$$

Here, ΔH is the activation energy for Si-Si bond breakage, and a is the field acceleration factor, including the permanent dipole moment of SiO_4 tetrahedral.

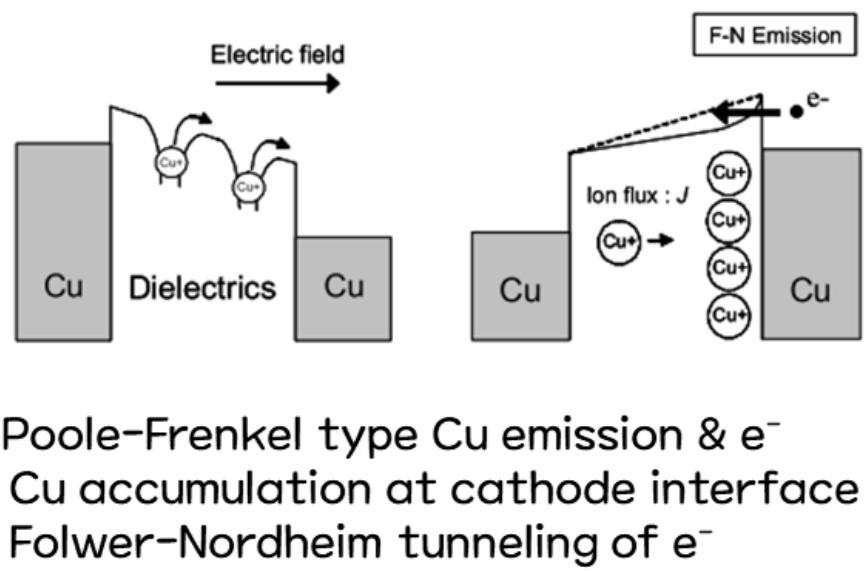


Figure 4-14. Typical example of extrinsic breakdown.[21] Accumulated Cu ions at cathode interface induces local E-field that results in Folwer-Nordheim tunneling of electrons.[22]

$$TTF = BE^{-1}\exp\left(-\frac{q}{k_bT}\left(\frac{q}{\pi\varepsilon_0 k}\right)^{\frac{1}{2}}\sqrt{E}\right): \sqrt{E}\ model \qquad \text{(Eq 5.2)}$$

Extrinsic breakdown refers to dielectric breakdown involving Cu ions.[23] **Figure 4-14** shows one of the examples of extrinsic breakdown mechanism,[24] and was presented in 2006 by suzumura of IMEC. Here, at the beginning of stressing, Cu ions at the interface migrate to trap sites in the dielectric through Poole Frenkel emission, and as these Cu accumulate at the cathode interface, the local field at the cathode and the dielectric interface increases.[25] This is a model that dielectric breakdown occurs as the slope of the energy band near the cathode interface becomes stiff due to this increase in the local field, and the effective barrier thickness of the electric Folwer-Nordheim tunneling from the cathode into the dielectric is reduced. In this case, the following field dependency model of TTF is constructed in which both the Poole-Frenkel emission of Cu ions and Folwer-Nordheim tunneling after Cu accumulation are involved.[26]

However, among the presented models, there was no content to establish and analyze a model for the 2-dimensional barrier like the conditions we tested, so we tried to establish a new field dependent model for the 2D barrier.[27] First, for justification of the model, we checked whether the dielectric breakdown in this experiment is extrinsic breakdown by Cu ions through the TOF-SIMS line profile of Cu ions before and after TDDB. As a

result of SIMS analysis, it was confirmed that the concentration of Cu ions in the SiO2 dielectric increased after TDDB, and through this, it was confirmed that it was an extrinsic breakdown. As shown in the TTF results in **Figure 4-12**, it can be seen that the time to failure increases significantly when the graphene barrier is applied and when the Ru ALD is applied.

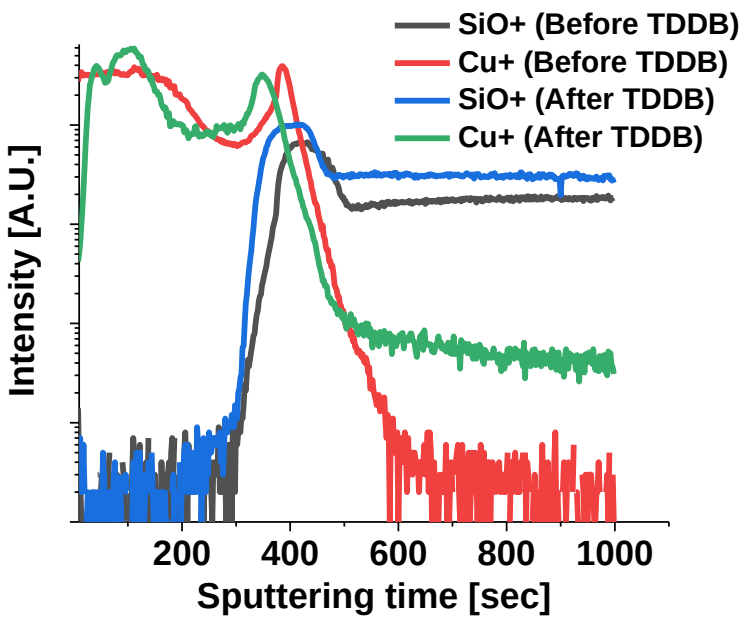


Figure 4-15. TOF-SIMS line profile for Cu+. Drift of Cu ion causes dielectric breakdown.

Based on the above results, the situation in which Cu ions overcome the potential barrier of the graphene barrier was analyzed by applying the 1-

D flux model.[28] Here, E_a is the activation energy of the graphene barrier, E_b is the activation energy of Cu ion migration in SiO_2, and it is assumed that E_a is very large compared to E_b. When a E-field is induced in the TDDB situation, the activation energy of Cu ion migration is reduced to $E_a - q\lambda E$, where λ is the effective barrier thickness of the potential barrier beyond graphene. The jumping frequency of Cu ions for the corresponding energy barrier and the corresponding flux can be expressed as follows by using the potential barrier values.

$$\Gamma_{net} = \Gamma_{right} - \Gamma_{left} = Aexp\left(-\frac{E_a - q\lambda E}{kT}\right) - Aexp\left(-\frac{E_a + q\lambda E}{kT}\right)$$

In the above equation, the first term refers to the diffusion term due to concentration gradient, and the second term refers to the drift component due to the electric field. Here, the x derivative and concentration time derivative of flux were matched by applying the continuity equation corresponding to Fick's second law. Therefore, the diffusion term is ignored. We also considered that dielectric failure cannot be observed when the temperature is raised without actually applying a field.

$$J(x,t) = [\frac{\partial C(x,t)}{\partial x}\lambda\Gamma_{right} + C(x,t)\Gamma_{net}]\lambda$$

$$-\frac{\partial C(x,t)}{\partial t} = \frac{\partial J(x,t)}{\partial x} = \frac{\partial^2 C(x,t)}{\partial x^2}\lambda\Gamma_{right} + \Gamma_{net}\lambda\frac{\partial C(x,t)}{\partial x}$$

$$\frac{\partial C(x,t)}{\partial t} = M(E)\frac{\partial C(x,t)}{\partial x}$$

Finally, by arranging the terms independent of position and time as M(E), and integrating this expression from time 0 to time to failure, it can be arranged as follows, Cu that crosses the potential barrier in the opposite direction under a very strong field Since the flux of ions is negligible, we can finally derive the relation between Time to failure, E field, and temperature as follows.

$$TTF(E) = \frac{Aexp\left(\frac{E_a}{kT}\right)}{exp\left(\frac{q\lambda E}{kT}\right) - exp(-\frac{q\lambda E}{kT})} = Aexp\left(\frac{E_a - q\lambda E}{kT}\right)$$

Based on the formula summarized in this way, after all the TDDB tests shown above were performed under the conditions of 150, 180, 200°C and applied electric field 5,6,7 MV/cm, the mean value was obtained and 9 points were obtained as follows. In the following ln(TTF) and 1/T plots, since

E_a and L are reflected in the slope value, the activation energy and effective barrier thickness values that match the temperature dependence slope values of each of the three electric fields of 5, 6, and 7 MV/cm were obtained.

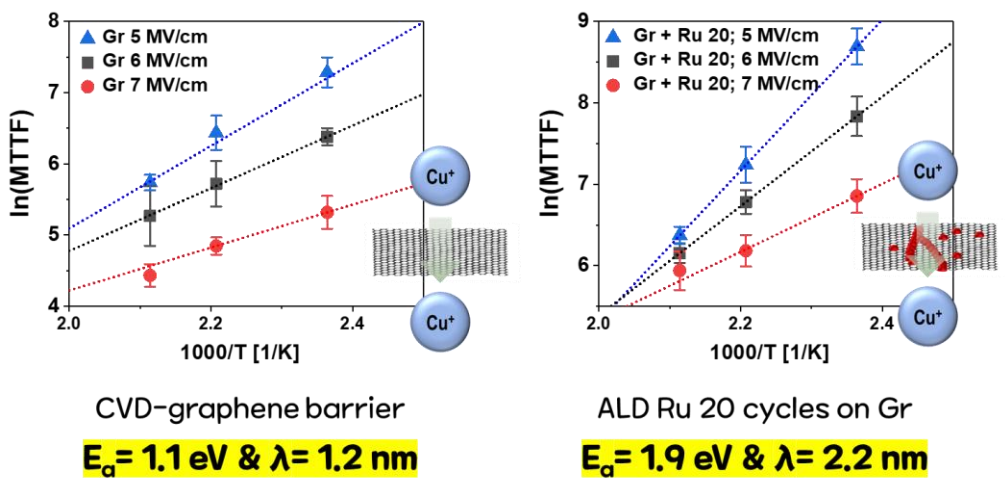


Figure 4-16. Implicating 1-D flux model to CVD-graphene barrier, and defected-stuffed graphene barrier. Proper values of activation energy and effective barrier thickness for each TDDB results are fitted.

As a result, in the case of the bare graphene barrier, it was confirmed that the slope value at the activation energy 1.1 eV effective barrier thickness 1.2 nm matches the slope value of the three lines best. In the case of the barrier subjected to Ru ALD 20 cycle, it was confirmed that the slope value at

the activation energy of 1.9 eV and the effective barrier thickness of 2.2 nm was the best fitting. According to these results, when Ru ALD is applied, the activation energy of Cu ions to pass through the defect site is increased as Ru is selectively deposited at the defect site that becomes the fast diffusion path of Cu, and as Ru is deposited, the activation energy at the defect site is increased. It was also confirmed that the effective barrier thickness increased.

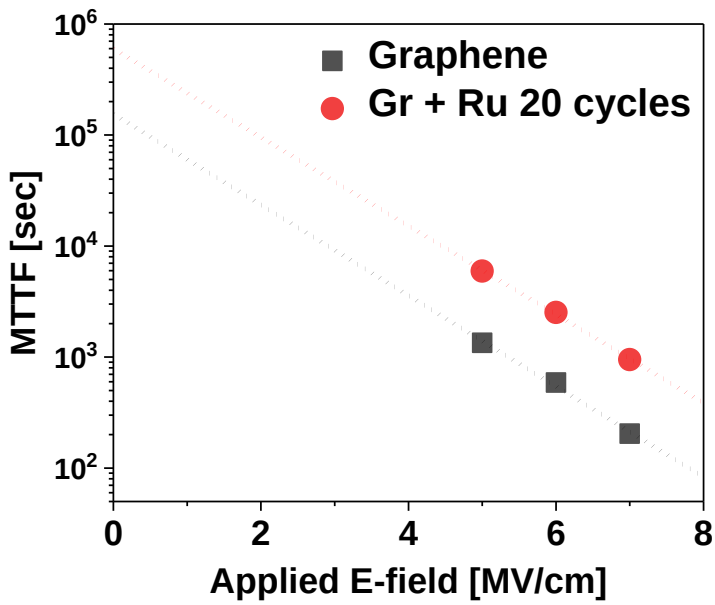


Figure 4-17. Extrapolating dielectric lifetime at 1 MV/cm and 150°C, which is normal device operating condition.

In addition, after plotting the TDDB results at 150°C according to the field for graphene and graphene to which Ru ALD 20 cycle was applied, as shown in **Figure 4-17**, the mean time to failure value at 1 MV/cm corresponding to the normal device operating condition was calculated before the MTTF. We compared it with extrapolation through the field dependency expression. As a result, it was confirmed that the dielectric lifetime of about 4 times longer in the barrier to which the Ru ALD 20 cycle was applied was extrapolated. In summary, by applying Ru ALD to graphene, Cu migration activation energy from 1.1eV to 1.9eV, effective barrier thickness increases from 1.2 to 2.2 nm, and dielectric lifetime improvement by 4 times under normal device operating conditions were confirmed. Through this, it was confirmed that Ru ALD improves the Cu blocking performance of the graphene barrier.

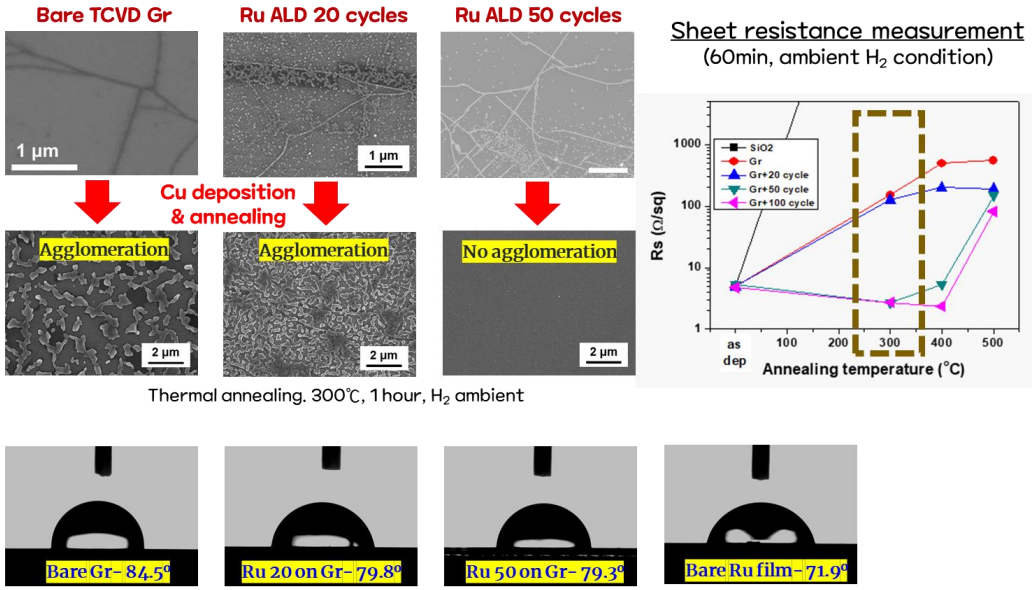


Figure 4-18. Electromigration reliability: Cu agglomeration test and water contact angle measurement on Ru-Graphene Cu diffusion barrier.

The results of comparing Cu Agglomeration behavior before and after Ru ALD are shown in **Figure 4-18**. In the case of bare graphene, Cu agglomeration after heat treatment at 300°C for 1 hour was confirmed through the SEM image, and a sharp increase in sheet resistance was confirmed. On the other hand, in the case of Ru ALD 50 cycle, the deposition amount of Ru, which has good adhesion with Cu, increased, and agglomeration did not occur even under the same heat treatment conditions. In conclusion, through this comparison of Cu agglomeration behavior, when

Ru ALD is applied, not only the aforementioned improvement in Cu blocking performance. In addition, the improvement of electromigration reliability can also be expected through the improvement of adhesion between Cu wiring and diffusion barrier.

4.3 Summary

In summary, by applying Ru ALD to graphene, it was confirmed that Ru was selectively deposited on defect sites that become the fast diffusion path of Cu, thereby stuffing defects. Accordingly, the improvement of Cu blocking performance was confirmed through TDDB test. The field dependent model in the TDDB system to which the 2D barrier is applied is presented through the 1D flux model. Through this, it was confirmed that the activation energy and effective barrier thickness of Cu migration were improved when Ru ALD was applied. Additionally, it was confirmed that the electromigration reliability of Cu and the conductivity of the barrier itself can also be improved when Ru ALD was applied.

References

(1) Zhao, R.; Lo, C. L.; Zhang, F.; Ghosh, R. K.; Knobloch, T.; Terrones, M.; Chen, Z. H.; Robinson, J. Incorporating Niobium in MoS2 at BEOL-Compatible Temperatures and its Impact on Copper Diffusion Barrier Performance. *Adv Mater Interfaces* **2019**, *6* (22).

(2) Lo, C. L.; Catalano, M.; Smithe, K. K. H.; Wang, L. H.; Zhang, S. J.; Pop, E.; Kim, M. J.; Chen, Z. H. Studies of two-dimensional h-BN and MoS2 for potential diffusion barrier application in copper interconnect technology. *Npj 2d Mater Appl* **2017**, *1*.

(3) Lo, C.; Zhang, K.; Robinson, J. A.; Chen, Z. BEOL compatible sub-nm diffusion barrier for advanced Cu interconnects. In *2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, 16-19 April 2018, 2018; pp 1-2.

(4) An, B. S.; Kwon, Y.; Oh, J. S.; Lee, M.; Pae, S.; Yang, C. W. Amorphous TaxMnyOz Layer as a Diffusion Barrier for Advanced Copper Interconnects. *Sci Rep-Uk* **2019**, *9*.

(5) Lo, C.; Smithe, K. K. H.; Mehta, R.; Chugh, S.; Pop, E.; Chen, Z. Atomically thin diffusion barriers for ultra-scaled Cu interconnects implemented by 2D

materials. In *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2-6 April 2017, 2017; pp MR-4.1-MR-4.4.

(6) Nguyen, B. S.; Lin, J. F.; Perng, D. C. 1-nm-thick graphene tri-layer as the ultimate copper diffusion barrier. *Appl Phys Lett* **2014**, *104* (8).

(7) Mehta, R.; Chugh, S.; Chen, Z. Transfer-free multi-layer graphene as a diffusion barrier. *Nanoscale* **2017**, *9* (5), 1827-1833..

(8) Lo, C.; Zhang, S.; Shen, T.; Appenzeller, J.; Chen, Z. BEOL compatible 2D layered materials as ultra-thin diffusion barriers for Cu interconnect technology. In *2017 75th Annual Device Research Conference (DRC)*, 25-28 June 2017, 2017; pp 1-2. (9) Li, L.; Chen, X. Y.; Wang, C. H.; Cao, J.; Lee, S.; Tang, A.; Ahn, C.; Roy, S. S.; Arnold, M. S.; Wong, H. S. P. Vertical and Lateral Copper Transport through Graphene Layers. *Acs Nano* **2015**, *9* (8), 8361-8367.

(10) Hong, J.; Lee, S.; Lee, S.; Han, H.; Mahata, C.; Yeon, H. W.; Koo, B.; Kim, S. I.; Nam, T.; Byun, K.; et al. Graphene as an atomically thin barrier to Cu diffusion into Si. *Nanoscale* **2014**, *6* (13), 7503-7511.

(11) Bong, J. H.; Yoon, S. J.; Yoon, A.; Hwang, W. S.; Cho, B. J. Ultrathin graphene and graphene oxide layers as a diffusion barrier for advanced Cu metallization. *Appl Phys Lett* **2015**, *106* (6).

(12) Oh, S.; Jung, Y.; Kim, J. Effects of defect density on ultrathin graphene-based metal diffusion barriers. *J Vac Sci Technol A* **2015**, *33* (6).

(13) Farmer, D. B.; Antunez, P. D.; Hopstaken, M.; Gunawan, O.; Han, S.-J. Patching of Lattice Defects in Two-Dimensional Diffusion Barriers. *ACS Applied Nano Materials* **2018**, *1* (7), 3068-3074.

(14) Degraeve, R.; Ogier, J. L.; Bellens, R.; Roussel, P. J.; Groeseneken, G.; Maes, H. E. A new model for the field dependence of intrinsic and extrinsic time-dependent dielectric breakdown. *Ieee T Electron Dev* **1998**, *45* (2), 472-481.

(15) Hwang, S. S.; Jung, S. Y.; Joo, Y. C. The electric field dependence of Cu migration induced dielectric failure in interlayer dielectric for integrated circuits. *J Appl Phys* **2007**, *101* (7).

(16) Achanta, R. S.; Plawsky, J. L.; Gill, W. N. A time dependent dielectric breakdown model for field accelerated low-k breakdown due to copper ions. *Appl Phys Lett* **2007**, *91* (23).

(17) McPherson, J. W.; Mogul, H. C. Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO2 thin films. *J Appl Phys* **1998**, *84* (3), 1513-1523.

(18) Snow, E. H.; Grove, A. S.; Deal, B. E.; Sah, C. T. Ion Transport Phenomena in Insulating Films. *J Appl Phys* **1965**, *36* (5), 1664-1673.

(19) McPherson, J. W. Time dependent dielectric breakdown physics - Models revisited. *Microelectron Reliab* **2012**, *52* (9-10), 1753-1760.

(20) Wong, T. K. S. Time Dependent Dielectric Breakdown in Copper Low-k Interconnects: Mechanisms and Reliability Models. *Materials* **2012**, *5* (9), 1602-1625.

(21) Chen, F.; Shinosky, M. A. Electron fluence driven, Cu catalyzed, interface breakdown mechanism for BEOL low-k time dependent dielectric breakdown. *Microelectron Reliab* **2014**, *54* (3), 529-540.

(22) Zhao, L.; Tőkei, Z.; Croes, K.; Wilson, C. J.; Baklanov, M.; Beyer, G. P.; Claeys, C. Direct observation of the 1/E dependence of time dependent dielectric breakdown in the presence of copper. *Appl Phys Lett* **2011**, *98* (3), 032107.

(23) Lee, S.; Oates, A. S. On the voltage dependence of copper/low-k dielectric breakdown. In *2015 IEEE International Reliability Physics Symposium*, 19-23 April 2015, 2015; pp 3A.3.1-3A.3.6.

(24) Ogden, S. P.; Xu, Y. M.; Yeap, K. B.; Shen, T.; Lu, T. M.; Plawsky, J. L. Charge transport model to predict dielectric breakdown as a function of

voltage, temperature, and thickness. *Microelectron Reliab* **2018**, *91*, 232-242.

(25) Palumbo, F.; Wen, C.; Lombardo, S.; Pazos, S.; Aguirre, F.; Eizenberg, M.; Hui, F.; Lanza, M. A Review on Dielectric Breakdown in Thin Dielectrics: Silicon Dioxide, High-k, and Layered Dielectrics. *Adv Funct Mater* **2020**, *30* (18).

(26) Wu, C.; Pedreira, O. V.; Leśniewska, A.; Li, Y.; Ciofi, I.; Tőkei, Z.; Croes, K. Insights into metal drift induced failure in MOL and BEOL. In *2018 IEEE International Reliability Physics Symposium (IRPS)*, 11-15 March 2018, 2018; pp 3A.1-1-3A.1-7.

(27) Wu, E. Y. Facts and Myths of Dielectric Breakdown Processes-Part II: Post-Breakdown and Variability. *Ieee T Electron Dev* **2019**, *66* (11), 4535-4545.

(28) Wu, E. Y. Facts and Myths of Dielectric Breakdown Processes-Part I: Statistics, Experimental, and Physical Acceleration Models. *Ieee T Electron Dev* **2019**, *66* (11), 4523-4534.

Chapter 5.

Self-limited Deposition of Sub 1-nm-thick Amorphous Carbon Layer as a Next Generation Cu Diffusion Barrier

This chapter is based on the accepted manuscript in

Advanced Materials, (2022)

5.1 Introduction

In the 60 years since the first integrated circuit (IC) was demonstrated, the evolution of ground rule, supposed to Moore's law has enabled the era of silicon ultra-large-scale integration (ULSI) in the Information revolution.[1-2] As technical demands grew, Copper (Cu) interconnect has been widely used in IC manufacturing because of its low electrical resistivity and better electromigration reliability than conventional Al.[3] In spite of the advantages of Cu interconnect, barrier material is essential to prevent diffusion of Cu into the intermetallic dielectric (IMD) materials that leads to degradation of device performance and failure with dielectric breakdown and short circuits between metal lines. Due to the relatively high electrical conductivity compared to Cu, the thickness of the barrier layer has been required to be minimized for lowering its portion in the barrier/Cu line, the contact resistance, and smaller resistance-capacitance delay. Ta/TaN film has been widely used as a Cu diffusion barrier for several decades owing to no intermetallic compounds in Cu-Ta binary system, high barrier performance.[4-6] However, considering rapid downscaling has progressed, Ta/TaN barrier would have met a scaling challenge owing to its failure to maintain high barrier performance at thicknesses below 3 nm.[7] At this point of view, a new ultra-thin and reliable diffusion

barrier urgently required. As an alternative for TaN barrier, self-forming barrier, $MnSi_xO_y$ layer formed at interface between Cu and SiO_2 has been reported.[8-9] However, Cu diffusion barrier property of this 1.2 nm-thick amorphous $MnSi_xO_y$ barrier couldn't completely prevent Cu diffusion into the dielectric material.[9]

Among the various candidates for the next generation Cu diffusion barrier, carbonaceous materials have been considered the constituent materials of the impermeable barrier due to no Cu-C intermetallic compounds in binary phase system.[10] Especially, single layer graphene has been suggested as a next-generation Cu diffusion barrier because of its atomically thin thickness, high thermal and chemical stability, and superior atomic impermeability with extremely small geometrical pores of 0.064 nm, which even helium atom cannot pass through.[11, 12] Conventional thermal CVD graphene grown on a metal catalyst and polycrystalline graphene directly grown on dielectric can be suggested as a large-area diffusion barrier for Cu interconnects.[13-15] However, the structural defects of graphene, which inevitably occur in the growth and post-transfer processes, make it difficult to block mass transport.[16] Therefore, ultra-thin amorphous carbon (a-C) layer without any grain boundaries directly grown on the substrate could be an alternative.[17] Furthermore, for compatibility with the current back-end-of-line (BEOL) process, processing temperature should be close or

below 450°C not to damage the dielectric material and pre-deposited Cu lines at lower levels.[18-21] Additionally, considering deposition of barrier layer onto dielectric trench in Cu damascene processing, adopting self-limiting process also would be an effective method to get conformal ultra-thin a-C diffusion barrier.

Here, a wafer-scale ultra-thin a-C layer was directly fabricated by introducing carbonization of PS grafted on the dielectric substrate. Uniform PS layer was grafted directly on a 4-inch SiO2/Si wafer with controlled thickness compared to the spin-casted hydroxyl group terminated polystyrene (PS-OH) on the substrate. The end-functionalized PS was grafted easily onto the substrate by the interfacial reaction between the end groups of PS and the substrate and un-grafted PS was removed after washing with solvent. This self-limiting behavior enables the achievement of uniform PS thin film on substrates, especially non-planar substrates like nanoparticles and trenches.[22-24] Formation of the interfacial bond via dehydration reaction between PS-OH and surface hydroxyl group of SiO_2 after grafting was identified by X-ray photoelectron spectroscopy (XPS). Because of this interfacial bond, PS layer of a certain thickness remained on SiO_2 when dissolved in a solvent. Also, as a second step, the additional thickness reduction was obtained through the carbonization of grafted PS. Through UV crosslinking and subsequent carbonization, ultra-thin a-C layer

directly formed on SiO_2 with thickness reduced to 1/10. The BEOL-compatible processing temperature of 400°C was adequate to carbonize grafted PS and induce the reduction of the thickness. The ultra-thin a-C layer directly fabricated on 4-inch SiO2/Si wafer exhibited a thickness of less than 2 nm with extreme uniformity, high thermal and chemical stability. By decreasing MW of PS-OH, the resultant thickness of a-C layer can be less than 1 nm, which can respond to further downscaling. To demonstrate the Cu diffusion barrier properties of ultra-thin a-C layer, the time-dependent dielectric breakdown test (TDDB) of underlying SiO_2 was investigated.

5.2 Experimental details

5.2.1 Self-limited grafting of PS-OH on SiO_2.

PS-OH (MW: 2.7 kg/mol, 13.5 kg/mol, and 59 kg/mol) (Polymer Source, Inc.) was dissolved in toluene (Sigma-Aldrich) with a concentration of 1.0 wt%. The PS-OH solution was spin-coated at 3000 rpm for 40 sec on SiO_2/Si wafer and then thermally reacted at 160°C for 12 hours in a vacuum oven (JEIO-TECH) to graft PS-OH on the surface of SiO_2 (native oxide for Si wafer). Unreacted PS-OH was washed off with toluene.

5.2.2 Carbonization of grafted PS

The grafted PS-OH thin film was cross-linked by UV light with a wavelength of 254 nm for 4 hours via a UV reactor (LZC-4V, Luzchem). The cross-linked PS-OH was carbonized in a quartz tube-type furnace to produce an ultra-thin a-C film directly on the SiO_2 substrate. The furnace was pumped down to 6×10^{-3} Torr, and then Ar gas (200 sccm, 5×10^{-1} Torr) was introduced to minimize oxidation. Heating was conducted at a ramp rate of 10 °C/min to reach the target temperature (400 °C-1000 °C) and held for 1 hour to carbonize the cross-linked PS-OH.

5.2.3 Fabrication of MOS structure

The a-C thin film was fabricated on 4-inch thermally grown SiO_2 50 nm/p++-type Si wafer by the method mentioned above. Carbonization was carried out at 460 ^oC to respond to the temperature requirements of BEOL process. Using shadow mask, 100 nm of Cu film with 20 nm of Al as a capping layer was evaporated as a top gate electrode in 100 μm × 100 μm square pads and then O_2 plasma was applied to etch underlying a-C layer. As a reference sample for diffusion barrier, 1nm-thick TaN_x was deposited with cluster type ALD (Atomic Premium, CN_1) with tert-butylimidotris-(diethylamido) tantalum [$(tBuN)(NEt_2)_3Ta$, TBTDET] as a precursor and H_2 gas as a reactant. One TaN_x ALD cycle consisted of TBTDET pulsing (2 sec) – purging (10 sec) – H2 pulsing (6 sec) – purging (10 sec). The deposition was conducted repeating 15 cycles at 300 ^oC with plasma power of 300 W.

5.2.4 Materials characterization

The film thickness of spin-casted PS-OH and grafted PS was measured by Ellipsometry (alpha-SE, J.A. Woollam Co.). Conformal deposition of PS grafted on SiO2 was investigated by using Ellipsometry, Field emission electron microscope (FE-SEM) (Verios 460, FEI). After

carbonization, a-C layer was characterized by Raman spectroscopy (Alpha300 M+, WITec GMbh, the wavelength of 488 nm), XPS (Thermo Scientific ESCALAB 250 Xi), AFM (Bruker Dimension Icon), and STEM. Structural characterizations with STEM HAADF and STEM EELS analysis were conducted using TEM (JEM-2100F, JEOL) with the operation voltage of 200 kV. For TEM sampling, Ti (20 nm) was deposited on the top of the sample as a protection layer during TEM sampling with PECS (Gatan model 682, Gatan) followed by covering carbon ink on the sample. FIB (Helios Nanolab 450, FEI) was used for TEM sampling using Ga+ ion beam with ion voltage, current, the incident angle of 30 kV, 2.5 nA, and 52° for rough milling specimen to move it to TEM grid. Fine milling was conducted with same Ga+ ion beam with 30 kV, 0.23 nA, and 51.2°~52.8°. Carbon EELS mapping was obtained in 20 nm ×14 nm region with holding 0.3 sec in 0.74 nm × 0.74 nm region as one frame for a-C layer (Mw: 60 kg/mol) and 9 nm ×9 nm region with holding 0.1 sec in 0.27 nm × 0.27 nm region as one frame for a-C layer (Mw: 13.5 kg/mol). The Cu diffusion barrier properties were measured using probe station with a semiconductor parameter analyzer (KEITHLEY 4200). under a stressing conditions of 5.0 – 7.0 MV/cm and the temperature of 150℃. The presence of Cu, Si and C along depth profile was conducted using TOF-SIMS (TOF-SIMS 5, IONTOF).

5.3 Results and discussion

5.3.1 Formation of ultrathin a-C layer

As shown in **Figure 5-1**, PS is composed of only C and H atoms in the repeating unit and readily decomposed above 450 °C. End-functional form of PS-OH can chemically interact with target substrate, including -OH, -COOH, -NH_2, -SH, and -Cl. Here, PS-OH dispersion with the extremely uniform M_w (average molecular weight of PS-OH polymer), such that polydispersity index (PDI) ~ 1.08, is commercially available with various average molecular weight of PS-OH. As illustrated in **Figure 5-2 and Figure 5-3**, PS-OH was spin-casted onto SiO_2/Si substrate and covalently grafted at 160 °C. Un-grafted polymers were subsequently spin-washed away with toluene solvent. Following carbonization process requires UV crosslinking and thermal annealing above 400 °C. Here, $PS_{2.7}$, $PS_{2.7}$-OH, $PS_{13.5}$, $PS_{13.5}$-OH, PS_{59}, and PS_{59}-OH stand for the M_n of 2.7 kg/mol, 13.5kg/mol, and 59 kg/mol, respectively.

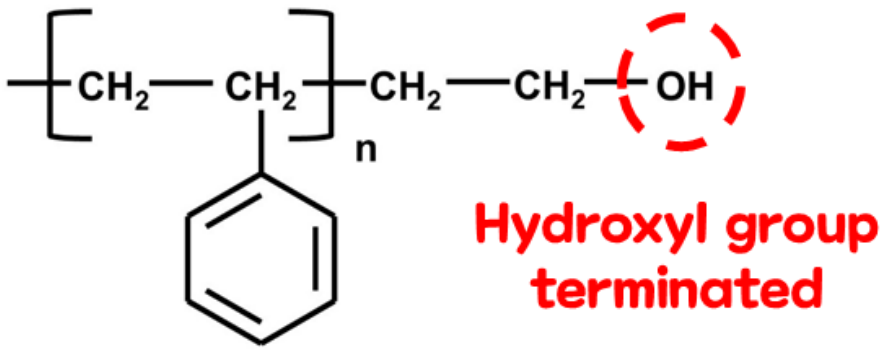


Figure 5-1. Monomer of hydroxyl group terminated PS. (PS-OH).

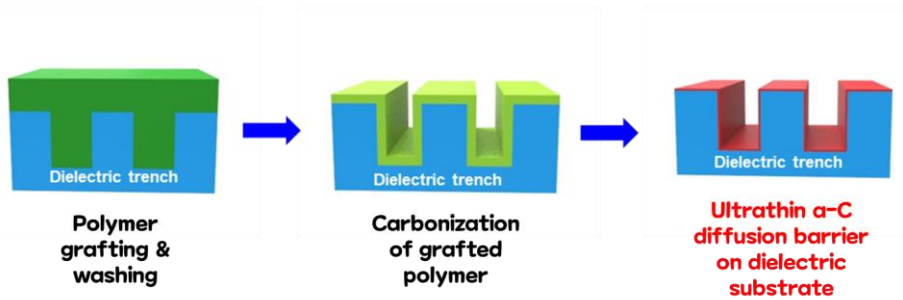


Figure 5-2. Schematic of formation of ultrathin a-C layer onto dielectric substrate. Grafting and subsequence carbonization of PS-OH coated onto dielectric trench substrate.

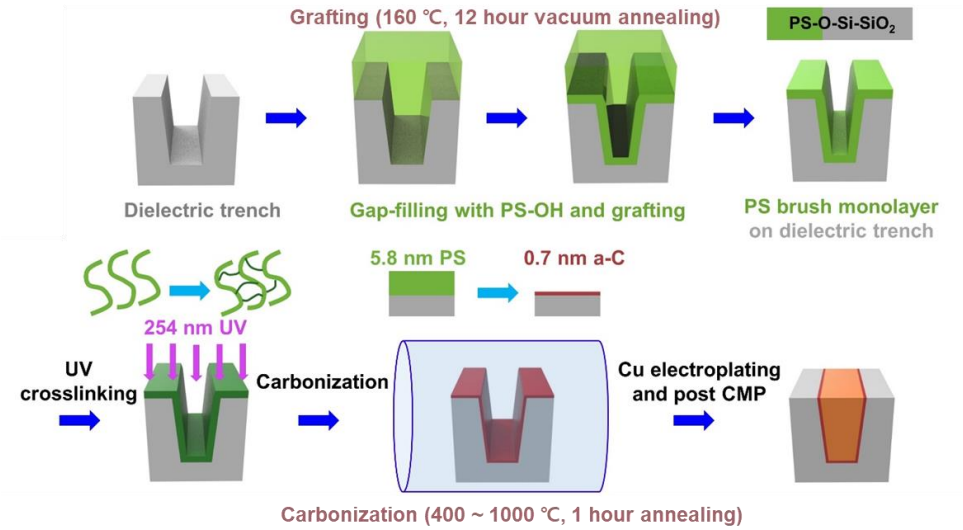


Figure 5-3. Detailed fabrication process of a-C layer on dielectric trench substrate.

Self-limited grafting of PS-OH over the large SiO_2 substrate were investigated by XPS and ellipsometry, as shown in **Figure 5-4**. For the surface-confined condensation of -OH [27, 28, 29, 30, 31], dehydration reaction occurs between the hydroxyl groups of PS-OH and SiO_2 surface. According to the XPS Si 2p spectrum as shown in Figure 5-4 (a), the spin-casted $PS_{13.5}$-OH on SiO_2/Si wafer showed a Si-O (Si^{4+}) bonding peak of SiO_2 at 103.6 eV with the surface Si-OH peak at 104.5 eV.[32] After grafting at 160 °C, the surface Si-OH peak was diminished and an additional peak was observed at 101.8 eV along with Si-O (Si^{4+}) bonding peak at 103.9 eV (Figure 5-4 (b)). This peak reflects a silicon alkoxy

bonding (Si-O-CH_2-CH_2-PS) by the hydrolysis reaction of PS-OH (PS-CH_2-CH_2-OH) with Si-OH.[33]

Thicknesses of the as spin-casted PS-OH and grafted PS (h_{gr}, PS remained after grafting and washing) on Si wafer were measured by ellipsometry according to the concentration and M_n of the PS-OH dissolved in toluene, as shown in **Figure 5-5**. The thickness increased from 32.0 ± 1.1 to 95.8 ± 1.5 nm for the concentration range from 1.0 to 2.5 wt% along with the viscosity increase of casting solution.[34] By contrast, after solvent spin-washing, h_{gr} remained almost constant at 18.2 ± 1.2 nm, revealing a self-limiting behavior. Similarly, uniform thicknesses of 12.0 ± 0.3 and 5.8 ± 0.2 nm were obtained for $PS_{13.5}$-OH and $PS_{2.7}$-OH, respectively.

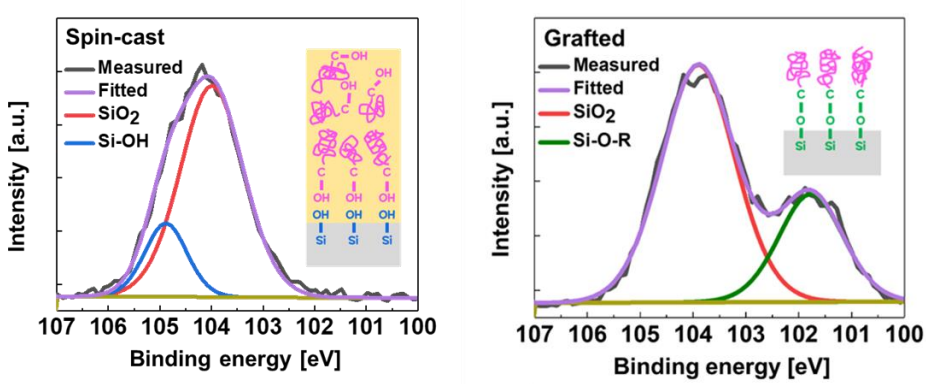


Figure 5-4. XPS Si 2p spectra of spin-cast PS-OH and grafted PS on SiO_2 surface.

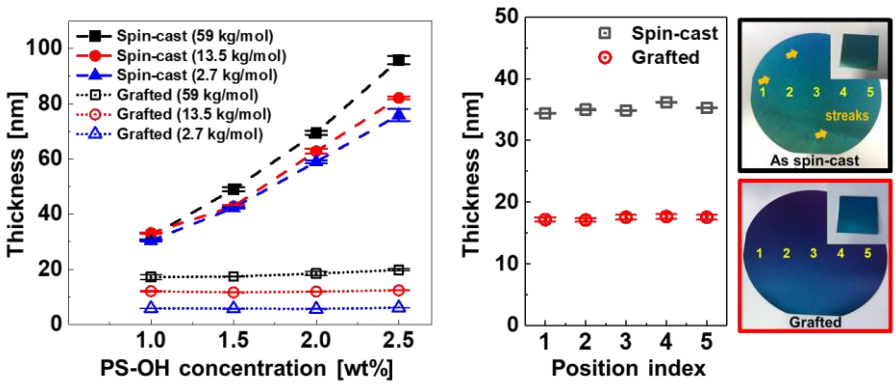
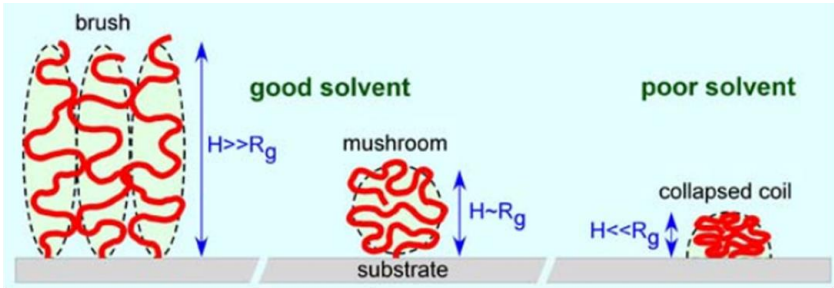


Figure 5-5 (a) Thickness variations of spin-cast and grafted PS brush layer with different molar weights and concentrations of PS-OH in the casting solution. (b) Thickness uniformity of surface-grafted PS brush layer and as spin-cast PS_{59}-OH over a 4-inch wafer. The inset shows grafted PS brush layer and as spin-cast PS_{59}-OH on square wafer slices.



M_n (kg/mol)	N	h_{gr} (nm)	R_g (nm)	$h_{gr}/(R_g)$	σ (chains/nm^2)	D (nm)
2.7	25	5.8	1.4	4.2	1.3	0.97
13.5	125	12.0	3.1	3.8	0.56	1.5
59	546	18.2	6.5	2.8	0.19	2.6

$$Rg = a(\frac{N}{6})^{\frac{1}{2}}, \sigma = \frac{h\rho N}{M_n}, D = \left(\frac{4}{\pi\sigma}\right)^{\frac{1}{2}}$$

For PS-OH, a=0.68 nm, ρ=1.04 g/cm^3

M_n; Molecular weight of PS-OH
h_{gr}; The thickness after grafting & washing
R_g; The radius of gyration
σ; Grafting density
D; The distance between grafted polymer

Figure 5-6. Grafting density of PS-OH on SiO_2 substrate. Brush-type of grafting geometry was evaluated by estimating h_{gr}/R_g values for each PS-OH with the molecular weight of 2.7, 13.5, and 59 kg/mol.

The h_{gr} value was compared with radius of gyration (R_g), grafting density (σ), and the distance between grafting sites (D) in **Figure 5-6**. Regardless of M_n, $h_{gr}/(2R_g)$ ratio was larger than 1, indicating the sufficiently dense grafting of PS-OH accompanied by the chain stretching of grafted PS.[35, 36] Besides, relatively low value of D compared with $2R_g$ also confirms a high density grafting of stretched chains rather than sparse grafting of mushroom-like chain-conformation.[37, 38, 39] As

M_n increases, the $h_{gr}/(2R_g)$ ratio gradually decreased, which is attributed to the decreased σ, as caused by the increased entropy penalty for chain stretching for long PS molecules.[35, 40]

We characterized the thickness uniformity of grafted PS at the 5 different points of 4-inch wafers, as shown in Figure 5-5 (SiO_2 300 nm/Si wafer was used for visualization). While as-casted PS-OH showed many streaks apparently, the spin-washed samples solely with grafted PS exhibited the uniform thickness of 17.2 ± 0.6 nm over the entire area. Edge beads, formed on square wafer slices, also disappeared. The resulting root mean square roughness (R_q) decreased from 6.4 to 0.52 nm after the solvent spin-washing process. The grafted PS_{59} clearly shows the XPS C1s spectrum with C-C/C-H bond at 284.8 eV and C-O bond at 286.0 eV along with π-π satellite peak at 290.9 eV originated from the aromatic rings of PS. Therefore, a uniform PS layer could be obtained over the 4-inch Si wafer through the self-limited behavior. For the possibility of 3D conformal coating, the similar grafting condition was applied to the non-planar 620 nm-height Si step as shown in **Figure 5-7**. Uniform and conformal coating of PS was also verified along the surface of Si steps.

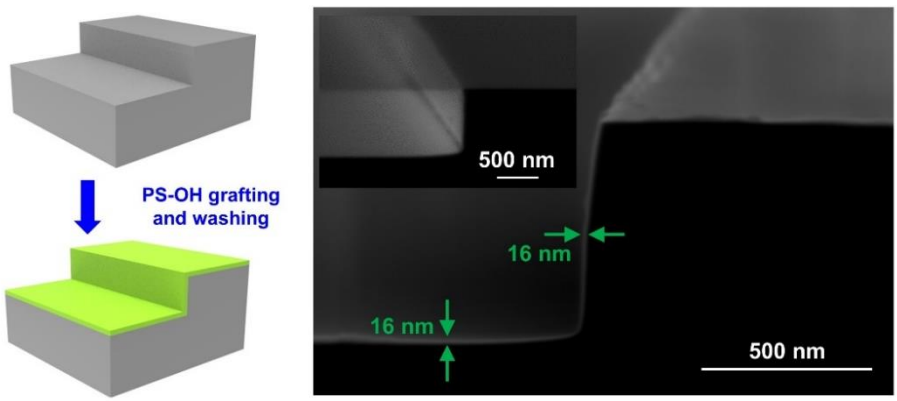


Figure 5-7. Schematic and cross-sectional SEM image of a Si step after grafting of PS1700 brush layer. Inset in the top left of the photograph is an SEM image of a bare Si step without the PS brush layer.

254 nm wavelength UV was irradiated on the PS thin film to prevent PS evaporation upon thermal decomposition. Under the deep UV irradiation, free radicals are generated in the backbone of polymer chains, and adjacent polymer chains with free radicals crosslink each other.[41, 42] Thus, the thermal stability of PS thin film was enhanced and the following high temperature treatment reliably yields an uniform a-C layer.[42, 43, 44, 45] We prepared area-selective UV irradiated samples with a shadow mask as shown in **Figure 5-8**. While unexposed region shows no Raman signals for a-C, UV-exposed regions exhibit the typical

signals for a-C, including G band (1594 cm^{-1}) and D band (1365 cm^{-1}) with the 0.60 of I_D/I_G ratio. The 2D band was was weakly detected due to the low degree of stacking, as shown in Figure 5-8. [46] Besides, the 210 cm^{-1} of broad full width half maximum (FWHM) for D band indicates a highly disordered structure with low contents of sp^2 clustered aromatic structures of carbon.[47, 48, 49]

According to the graphitization temperature, further evolution of Raman spectra was investigated, as shown in **Figure 5-9**. Interestingly, nearly identical Raman spectra appeared above 400 ^oC with the intensive G and D bands. While the principal decomposition of crosslinked PS proceeds from 400 to 500 ^oC,[50] no noticeable G or D band was detected below 350 ^oC. From 460 to 1000 ^oC, I_D/I_G ratio increased from 0.60 to 1.0, reflecting the increase of sp^2 clustered aromatic structures.[46] AFM characterization confirms that the thickness of grafted PS_{59} was mostly reduced up to 460 ^oC yet no more decrease even to 1000 ^oC. This indicates that atomic rearrangement without significant low of carbon in the range from 460 to 1,000 ^oC.

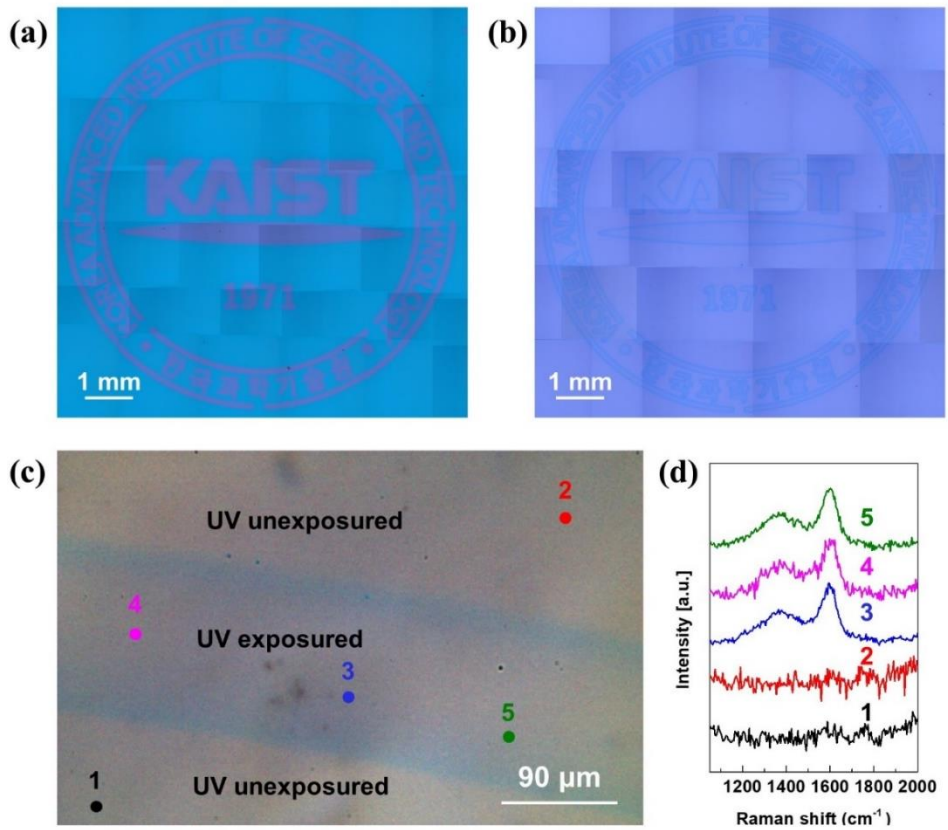


Figure 5-8. Carbonization of PS after selective UV irradiation. (a) Optical microscope image of (a) grafted PS_{59} brush layer after UV irradiation and (b) the same sample heated at 600 ℃. The purple area in (a) is exposed with UV 254 nm through shadow mask. (c) Optical microscope image of the selected area of (b), and (d) corresponding Raman spectra of the marked positions.

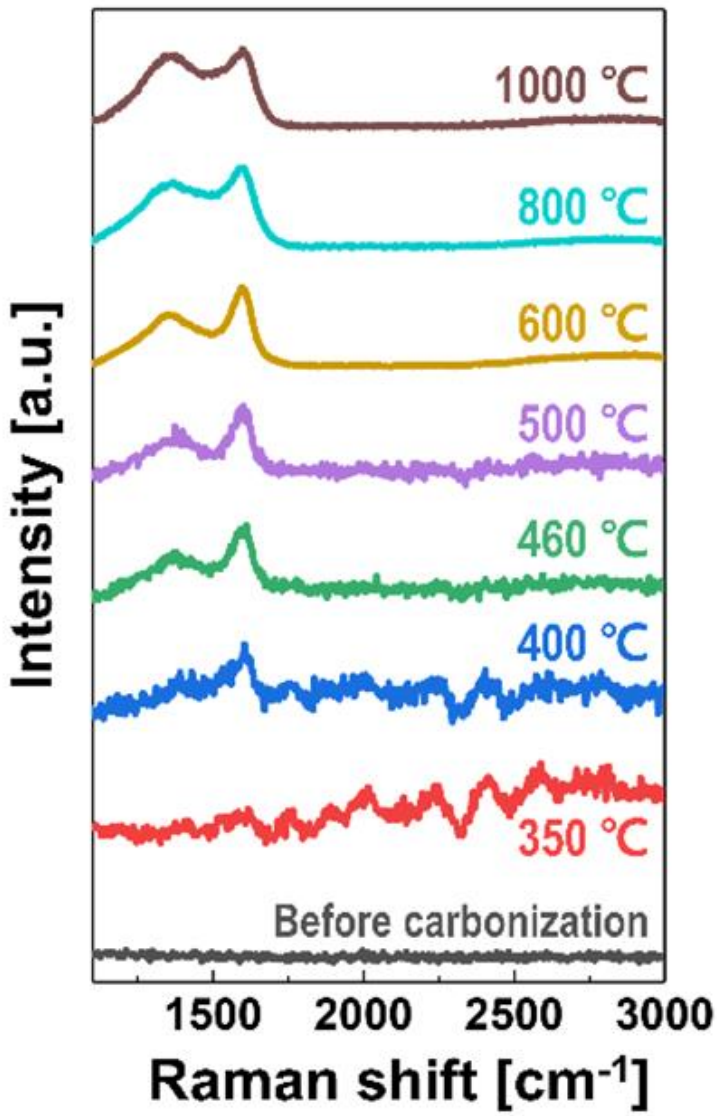


Figure 5-9. Raman spectrum of a-C layer from the grafted PS_{59} on SiO_2/Si substrate according to the carbonization temperature. Characteristic D band (1365 cm^{-1}) and G band (1594 cm^{-1}) were observed from 400 °C

Figure 5-10 shows the XPS C1s spectrum of a-C synthesized at 460 °C. The deconvolution of C 1s peak reveals four different peaks at 284.2 (79.60 %), 285.3 (9.29 %), 286.3 (7.83 %) and 288.2 eV (3.13 %), which correspond to sp^2 C=C, sp^3 C-C, C-O and C=O, respectively.[51] Compared to the as-grafted PS, the π-π satellite peak (290.9 eV) decreased from 4.62 to 1.92%. XPS C1s spectra were further obtained according to the heating temperatures. Crosslinked PS grafted onto SiO_2/Si substrate shows high contents of C-O (286.5 eV, 21.0%) and C=O (288.6 eV, 30.4 %) from –COOH groups. Oxidative degradation of grafted PS occurs simultaneously by the UV crosslinking under atmospheric condition.[52] The π-π satellite peak decreased due to the photocleavage of phenyl ring along with the oxidation of PS.[53] After heating to 350 °C, the contents of C-O and C=O bonds decreased to 17.1and 12.6 %, respectively, due to decarbonylation.[50] The heating from 400 to 1000 °C increased the sp^2 C=C bond content from 69.7 to 77.2 %. Overall, a-C layer can be synthesized over a wide temperature window from 400 to 1000 °C with various bonding configurations while the layer thickness remains constant.

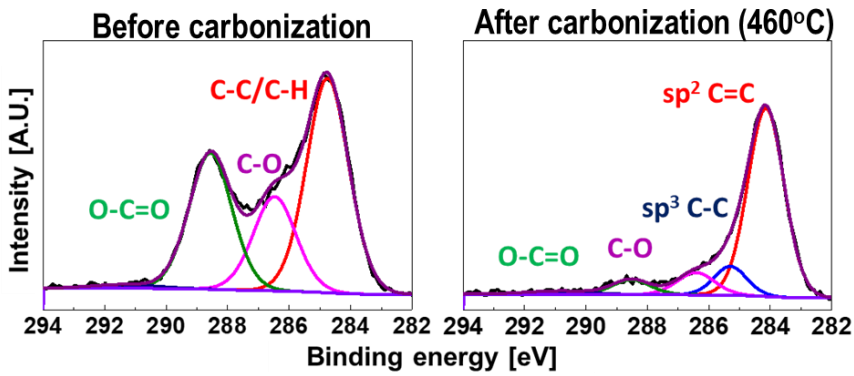


Figure 5-10. XPS C 1s spectra of the grafted and UV cross-linked PS_{59}-OH on SiO_2 substrate and that of a-C layer.

Additionally, plan-view TEM image of 460 °C -carbonized $PS_{2.7}$ clearly shows the absence of long-range order without any lattice fringes and holes, as shown in **Figure 5-11**. The corresponding fast Fourier transformed (FFT) image with a halo pattern also convinces that crosslinked PS was successfully transformed into a-C layer. Noteworthy that even after severe ultra-sonication in N-Methyl-2-Pyrrolidone (NMP) for 12 hours, Raman spectra of a-C layer on SiO_2 substrate does not change significantly, as shown in **Figure 5-10**. A strong adhesion between a-C and SiO_2, presumably involved with some chemical bindings, endows the excellent stability against harsh ultra-sonication condition. The surface roughness of a-C layer was also characterization by AFM. The a-C layers prepared by $PS_{2.7}$-OH, $PS_{13.5}$-OH and PS_{59}-OH

revealed ultra-smooth surfaces with R_q of 0.26, 0.19, and 0.23 nm, respectively, without any pinhole, hillock and uncovered regions over the entire scan area of 20 × 20 μm^2.

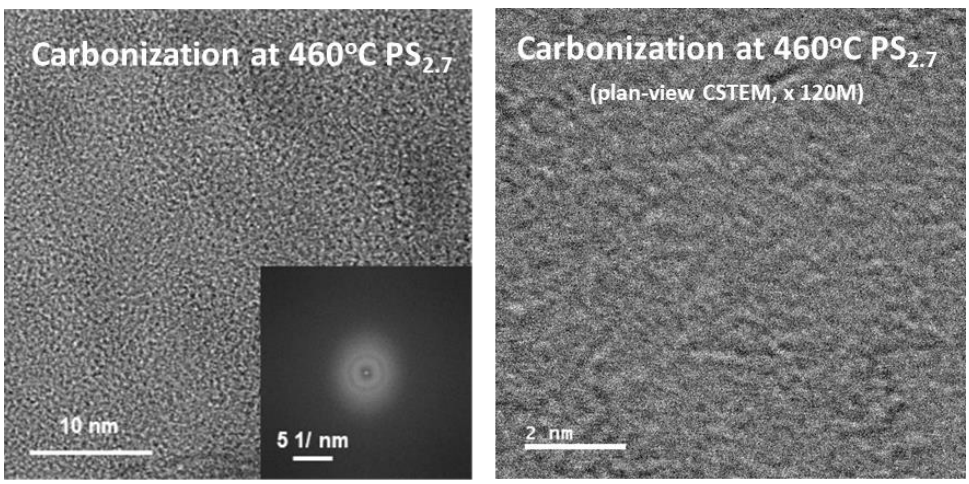


Figure 5-11. Plan-view TEM image and following CS-TEM image of a-C layer, which fabricated by grafting and carbonization of $PS_{2.7}$-OH polymer on SiO_2 substrate.

Different with thin film agglomeration of metal on SiO_2/Si substrate,[54] the ultra-smooth surface of a-C layer seems to be attributed to low surface energy and low diffusion coefficient of a-C layer with high melting point not causing thin film agglomeration of a-C and forming a-C islands on SiO_2/Si substrate.[54-56]

Figure 5-12 presents the thicknesses of a-C layers from the different M_n values of PS-OH. Upon carbonization, thickness of the grafted $PS_{2.7}$ layer sharply decreased down to 1 nm-level. From the STEM high angle annular dark-field (HAADF) micrographs and Carbon EELS analysis, the thicknesses were measured to be 0.70 ± 0.15, 1.25 ± 0.16, and 1.67 ± 0.14 nm for the a-C layers converted from grafted $PS_{2.7}$, $PS_{13.5}$, and PS_{59}, respectively. Regardless of the Mn of PS-OH, the thickness of a-C reduced down to approximately 10% of the thickness of grafted PS. Note that the STEM HAADF contrast and Carbon EELS signal of a-C layers were faded up measurements, due to ultrathin thicknesses and amorphous character of samples. Fortunately, further analysis, including AFM and XRR measurements, complements the STEM results, as shown in **Figure 5-13, and Figure 5-14**. Notably, the thinnest layer consistently exhibited the thickness below 1 nm, such that 0.70 nm, 0.67 nm, and 0.89 nm from STEM, AFM, and XRR, respectively.

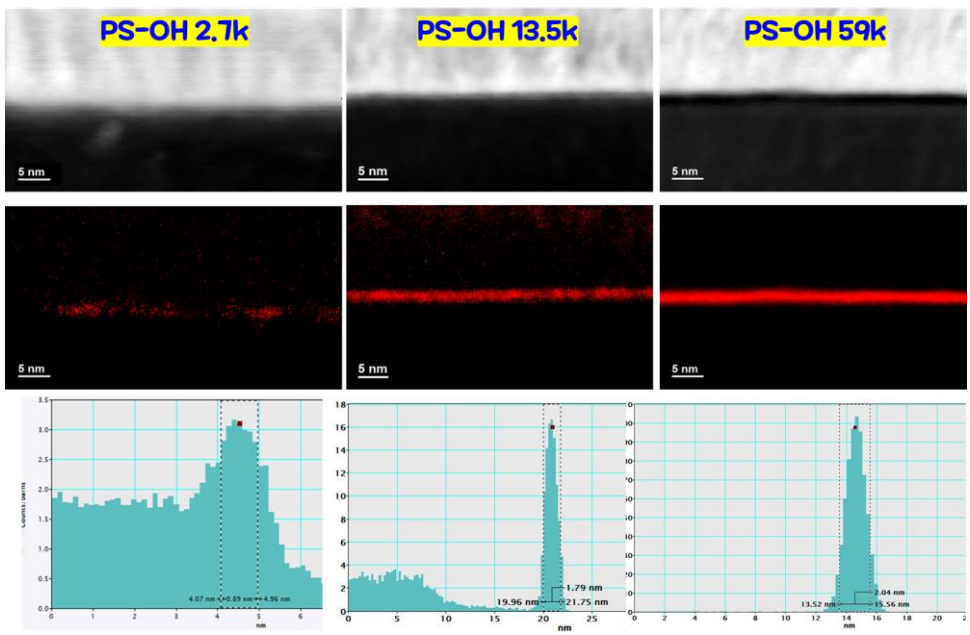


Figure 5-12. The thickness of a-C layer by varying the Mn of PS-OH. HAADF, Carbon EELS mapping and intensity line profile

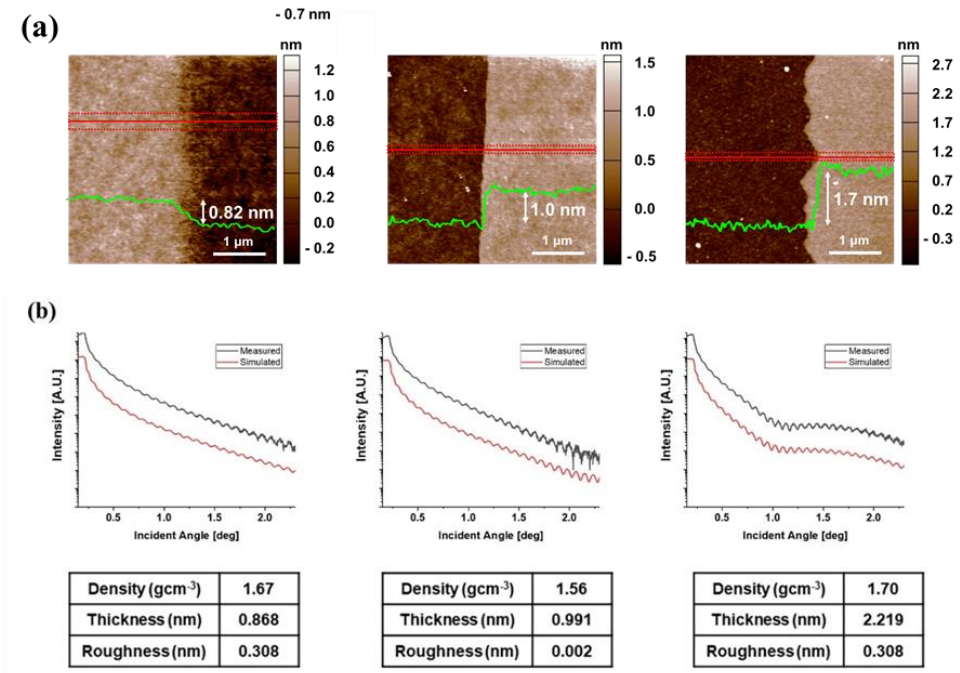


Figure 5-13. AFM and XRR results on the thickness of a-C layers.

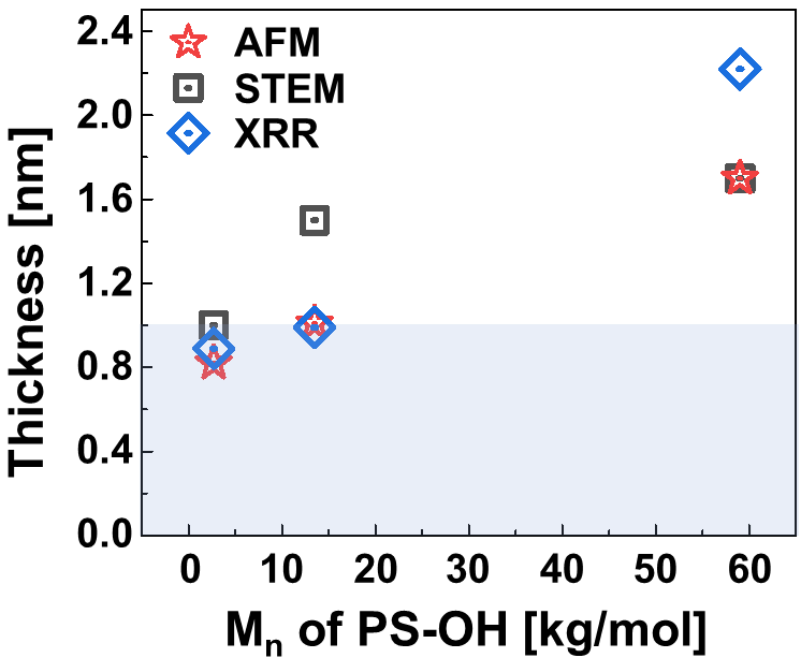


Figure 5-14. Summary on the thickness evaluation results by various characterization methods, such that TEM, AFM, and XRR.

5.3.2 Cu blocking performance of a-C layer

The reliability of the a-C layer as a Cu diffusion barrier was investigated by time-dependent-dielectric breakdown (TDDB) measurements with a simple metal-oxide-semiconductor (MOS) capacitor structure, as shown in **Figure 5-15**. Here, the applied electric field enforces Cu ions to migrate into SiO_2 dielectric by Poole-Frenkel tunneling, while facilitating the bond breakage of SiO_2[57, 58] (See Method section for the details of MOS device fabrication). Under 6.0 MV/cm and 150 ℃ of bias temperature stressing (BTS) condition, time-to-failure behaviors of a-C layers with various thicknesses (*i.e.*, 460 ℃ carbonized $PS_{2.7}$, $PS_{13.5}$, PS_{59} grafted on SiO_2/Si wafer with the thicknesses of 0.70, 1.25 and 1.67 nm, as confirmed by STEM) and 1.0 nm of TaN_x film, deposited by Atomic Layer Deposition (ALD), were straightforwardly compared. Figure 5-15 shows the measured leakage current traces of MOS capacitors and corresponding cumulative probabilities of dielectric breakdown against stressing time. Obviously, a-C layers successfully blocked the diffusion of Cu ions towards the underlying SiO_2 dielectric, enhancing the dielectric lifetime compared to the barrier-free bare oxide. A time-of-flight secondary ion mass spectroscopy (TOF-SIMS) detects no further Cu diffusion even after 2000 sec of BTS in the case of MOS device with the 1.67 nm-thick a-C layer. Statistical distribution of time-to-failure and the following

estimation of the mean-time-to-failure (MTTF) present that the MTTFs for the a-C layers with 0.70, 1.25, and 1.67 nm thicknesses were improved by 11, 29, and 149 times, respectively, compared to the bare oxide (53.7 sec). This thickness dependency of Cu blocking performance is also clearly shown in **Figure 5-16**. By contrast, 1.0 nm-thick conventional TaN_x Cu diffusion barrier showed only 3.7 times increase from the bare oxide. Even the thinner a-C layer with 0.70 nm thickness exhibited 3.3 times longer MTTF (575.6 sec) than the 1.0 nm-thick TaN_x (174.5 sec). These results strongly suggest that the a-C layer offers highly enhanced Cu blocking performance compared conventional TaN_x barrier.

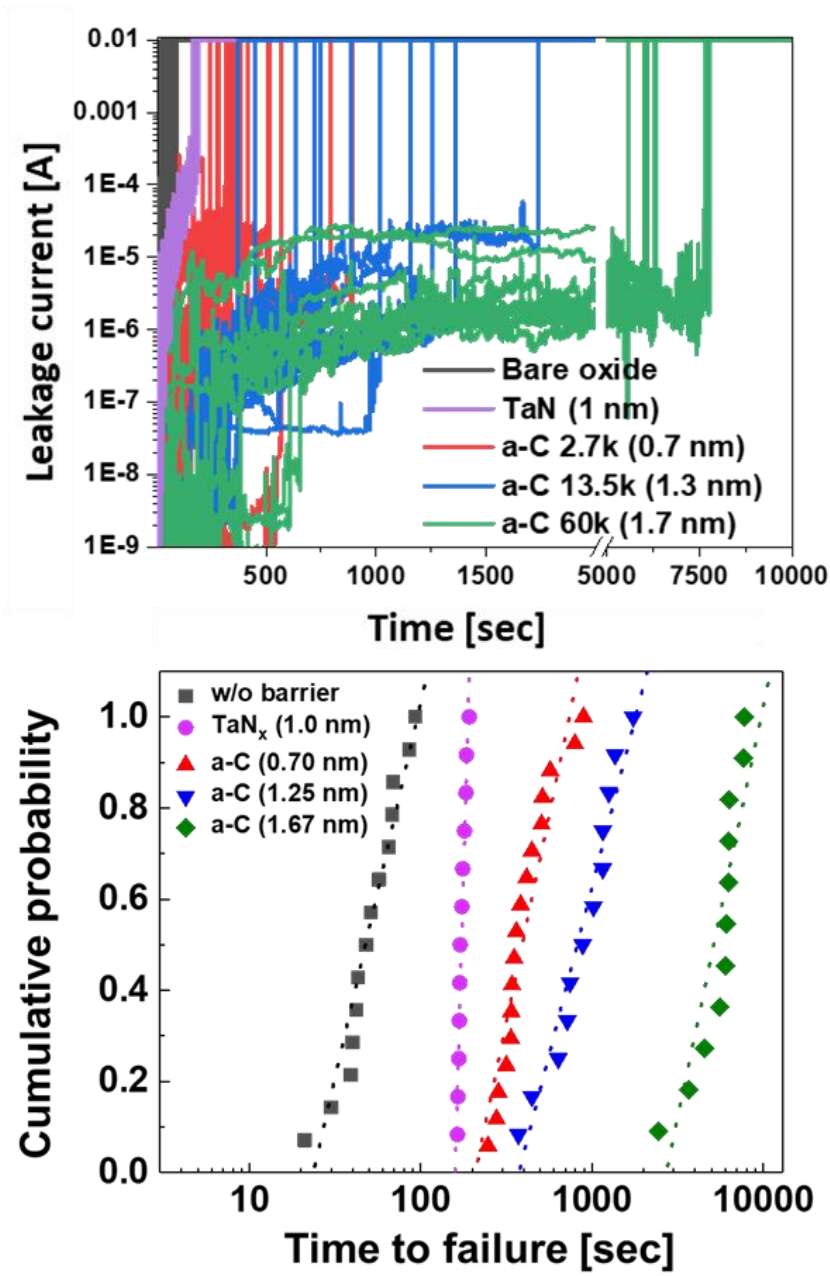


Figure 5-15. Typical TDDB results under 150°C and 5 MV/cm test condition.

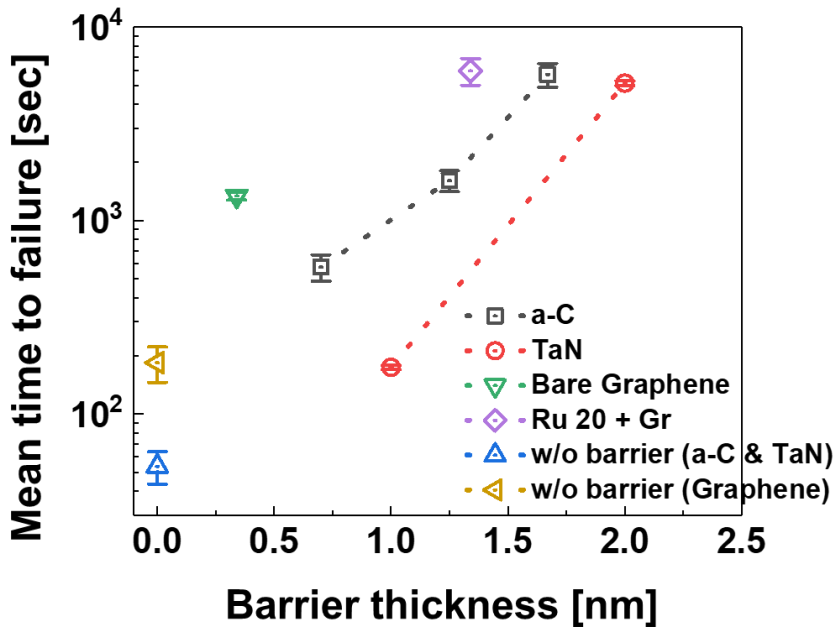


Figure 5-16. Mean-time-to-failure of various kinds of Cu diffusion barrier, including a-C, CVD-graphene and defect-stuffed graphene by Ru ALD, and a-C layer with the barrier thicknesses.

Finally, electric field dependent TDDB testing was further conducted to predict the MTTF of a-C layers at normal device operating condition (1 MV/cm).[59, 60, 61] Among many dielectric reliability models, $\sqrt{E}$ and 1/E models were accepted, which have been developed to predict Cu ion-induced dielectric failure.[62, 63, 64] The predicted lifetimes of MOS devices with the a-C thicknesses of 0.70, 1.25, and 1.67 nm were estimated as 2.8×10^6, 4.9×10^7, and 4.4×10^7 sec, respectively, while 1.0

nm-thick TaN_x exhibited 8.1×10^4 sec by $\sqrt{E}$ model. Besides, estimated device lifetimes by 1/E model exhibited 1.3×10^{17}, 3.3×10^{19}, 6.5×10^{22}, and 3.1×10^{13} sec for 0.70, 1.25, 1.67 nm thick a-C layers, and 1.0 nm of TaN_x layer, respectively. These results confirm that device lifetime of 0.70-nm-thick a-C diffusion barrier is expected to be 34 times ($\sqrt{E}$ model) or 4000 times (1/E model) longer than 1.0 nm-thick conventional TaN_x barrier.

Obviously, this superior barrier property of sub-1-nm a-C layer should to be attributed to its large-area uniform amorphous phase without grain boundary. Grain boundaries within a crystalline diffusion barrier are well-known to act as the primary diffusion path of Cu ions, even more critical at nanoscale ultrathin thickness.[65] Typical PEALD-TaN_x films grown from *tert*-butylimidotris-(diethylamido) tantalum (TBTDET) precursor and hydrogen reactant are highly polycrystalline.[65, 66] Therefore, the sub-1-nm of TaN_x barrier would suffer from the leakage of Cu ions through grain boundaries,[67, 68] By contrast, our amorphous diffusion barrier is free from such leakage pathways for Cu diffusion. Atomic diffusivity in amorphous phase is known to be typically orders of magnitude lower than the polycrystalline counterparts. Noteworthy that amorphous ALD-TaN_x film can also be deposited employing a metal halide Ta precursor. However, barrier failure temperature of the amorphous TaN_x barrier sharply decreases

due to easy low temperature crystallization of ultrathin thickness below 5 nm.[69, 66, 70, 71]

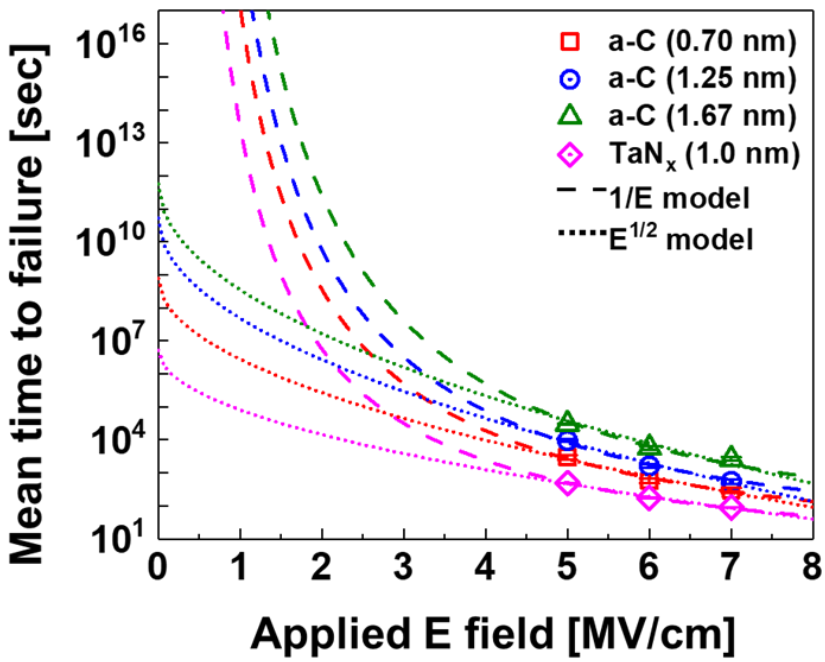


Figure 5-17. Extrapolation of dielectric lifetime under normal device operating condition. 1/E model and square root E model are introduced to extrapolate mean-time-to-failure of a-C and TaN Cu diffusion barriers.

[sec]	√E model	1/E model
TaN 1 nm	8.1×10^{4}	3.1×10^{13}
a-C 0.70 nm	2.8×10^{6}	1.3×10^{17}
a-C 1.25 nm	4.4×10^{7}	3.3×10^{19}
a-C 1.67 nm	4.9×10^{7}	6.5×10^{22}

Table 5-1. Extrapolated mean-time-to-failure of a-C and TaN Cu diffusion barriers by 1/E model and square root E model.

Apart from amorphous nature, the superior barrier performance of a-C layer should be more fundamentally understood, particularly considering the small geometric size of Cu ions. Zhao *et al.* have reported that eight-atom vacancy (0.25 nm^2) in graphene has a low adsorption energy so as to allow Cu atoms to penetrate through the basal plane.[72] Therefore, the typical porosity within a-C layer is insufficiently to physical block the diffusion of Cu ions. Here, the atomic level intimate interaction between Cu^+ ions and a-C layer should be the primary factor for the Cu diffusion barrier performance. It has been reported that -COOH terminated self-assembled monolayer (SAM)

immobilized Cu shows a strong interaction between -COOH and Cu^+ at the Cu/SAM interface.[73, 74] Under our BTS situation without ultrahigh-vacuum state, Cu^+ ions are readily generated from the chemical oxidation of Cu with ambient O_2 gases and moisture and diffuse toward SiO_2/Si under an electric field.[75, 76] Meanwhile, the moisture could be readily adsorbed onto a-C layer in the presence of the residual amount of oxygen functional group after UV irradiation and carbonization process. With the adsorbed moisture, - COOH group can be deprotonated to yield negative charged carboxylate ($-COO^-$) groups.[77, 78] The strong electrostatic interaction between Cu^+ ion and $-COO^-$ within a-C layer can greatly hamper the drift of Cu^+ ion and thereby increase TDDB lifetime. Indeed, the surface charge of a-C layer was measured to be -18.2 mV at pH of 7.0, while the original SiO_2 layer exhibits relatively low negative value of -9.0 mV at the same pH. Overall, our ultra-thin a-C layers perform superior Cu diffusion barrier properties taking advantage of its amorphous nature as well as intimate strong electrostatic binding of Cu^+ ions.

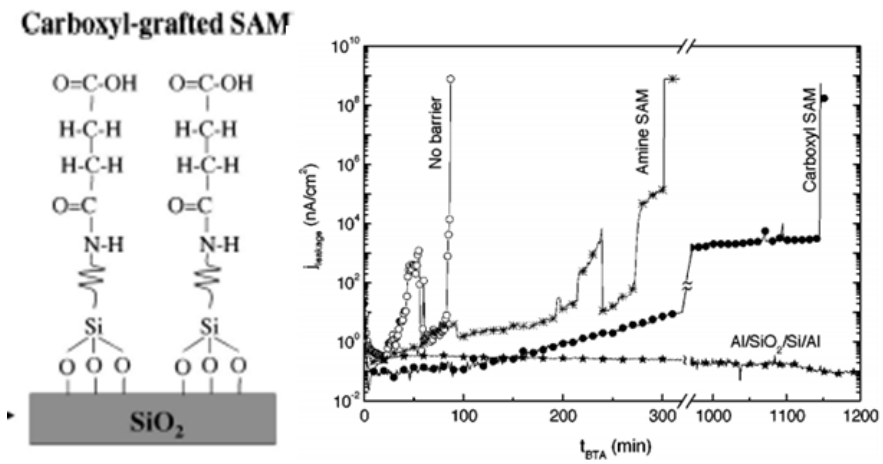


Figure 5-18. Surface functional group of SAM could play a major role for blocking Cu ions. Ref

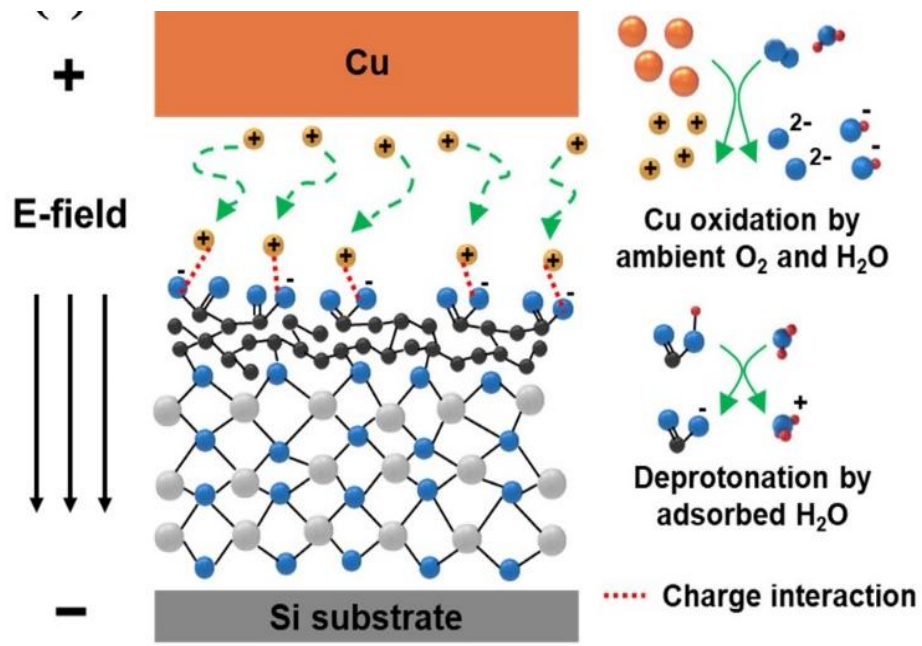


Figure 5-19. Origin of superior Cu blocking performance of a-C layer

5.4 Summary and Conclusion

A reliable method for preparing a conformal amorphous carbon (a-C) layer with a thickness of 1-nm-level, was tested as a possible Cu diffusion barrier layer for next-generation ultrahigh density semiconductor device miniaturization. A polystyrene brush of uniform thickness was grafted onto 4-inch SiO2/Si wafer substrates with 'self-limiting' chemistry favoring such a uniform layer. UV crosslinking and subsequent carbonization transformed this polymer film into an ultrathin a-C layer without pinholes or hillocks. The uniform coating of nonplanar regions or surfaces is also possible. The Cu diffusion "blocking ability" was evaluated by time-dependent dielectric breakdown (TDDB) tests using a metal-oxide-semiconductor (MOS) capacitor structure. A 0.82 nm-thick a-C barrier gave TDDB lifetimes 3.3× longer than that obtained using the conventional 1.0 nm-thick TaNx diffusion barrier. In addition, this exceptionally uniform ultrathin polymer and a-C film layers hold promise for selective ion permeable membranes, electrically and thermally insulating films in electronics, slits of angstrom-scale thickness, and when appropriately functionalized, as a robust ultrathin coating with many other potential applications.

References

(1) Ellmer, K. Past Achievements and Future Challenges in the Development of Optically Transparent Electrodes. *Nat. Photonics* **2012,** *6*, 809-817.

(2) Dawar, A.; Joshi, J. Semiconducting Transparent Thin Films: Their Properties and Applications. *J. Mater. Sci.* **1984,** *19*, 1-23.

(3) Cao, W.; Li, J.; Chen, H.; Xue, J. Transparent Electrodes for Organic Optoelectronic Devices: A Review. *J. Photonics Energy* **2014,** *4*, 040990.

(4) Mizuhashi, M. Electrical Properties of Vacuum-Deposited Indium Oxide and Indium Tin Oxide Films. *Thin Solid Films* **1980,** *70*, 91-100.

(5) Song, J. I.; Park, J. S.; Kim, H.; Heo, Y. W.; Lee, J. H.; Kim, J. J.; Kim, G. M.; Choi, B. D. Transparent Amorphous Indium Zinc Oxide Thin-Film Transistors Fabricated at Room Temperature. *Appl. Phys. Lett.* **2007,** *90*, 022106.

(6) Taylor, M. P.; Readey, D. W.; van Hest, M. F. A. M.; Teplin, C. W.; Alleman, J. L.; Dabney, M. S.; Gedvilas, L. M.; Keyes, B. M.; To, B.; Perkins, J. D.; Ginley, D. S. The Remarkable Thermal Stability of Amorphous In-Zn-O Transparent Conductors. *Adv. Funct. Mater.* **2008,** *18*, 3169-3178.

(7) Park, S. Y.; Song, J. H.; Lee, C. K.; Son, B. G.; Lee, C. K.; Kim, H. J.; Choi, R.; Choi, Y. J.; Kim, U. K.; Hwang, C. S.; Kim, H. J.; Jeong, J. K. Improvement in Photo-Bias Stability of High-Mobility Indium Zinc Oxide Thin-Film Transistors by Oxygen High-Pressure Annealing. *IEEE Electron Device Lett.* **2013,** *34*, 894-896.

(8) Kim, H.; Choi, D.; Park, S.; Park, K.; Park, H. W.; Chung, K. B.; Kwon, J. Y. Impact of Bias Stability for Crystalline InZnO Thin-Film Transistors. *Appl. Phys. Lett.* **2017,** *110,* 232104.

(9) Sheng, J.; Lee, H. J.; Oh, S.; Park, J. S. Flexible and High-Performance Amorphous Indium Zinc Oxide Thin-Film Transistor Using Low-Temperature Atomic Layer Deposition. *ACS Appl. Mater. Interfaces* **2016,** *8*, 33821-33828.

(10) Oh, S.; Yang, B. S.; Kim, Y. J.; Oh, M. S.; Jang, M.; Yang, H.; Jeong, J. K.; Hwang, C. S.; Kim, H. J. Anomalous Behavior of Negative Bias Illumination Stress Instability in an Indium Zinc Oxide Transistor: A Cation Combinatorial Approach. *Appl. Phys. Lett.* **2012,** *101*, 092107.

(11) Ramamoorthy, K.; Kumar, K.; Chandramohan, R.; Sankaranarayanan, K. Review on Material Properties of IZO Thin Films Useful as Epi-n-TCOs in Opto-Electronic (SIS Solar Cells, Polymeric LEDs) Devices. *Mater. Sci. Eng., B* **2006,** *126*, 1-15.

(12) Lee, D. J.; Kwon, J. Y.; Kim, J.; Kim, K. J.; Cho, Y. H.; Cho, S. Y.; Kim, S. H.; Xu, J.; Kim, K. B. Ultrasmooth, High Electron Mobility Amorphous In-Zn-O Films Grown by Atomic Layer Deposition. *J. Phys. Chem. C* **2014,** *118*, 408-415.

(13) Yaglioglu, B.; Yeom, H. Y.; Beresford, R.; Paine, D. C. High-Mobility Amorphous In2O3-10 wt %ZnO Thin Film Transistors. *Appl. Phys. Lett.* **2006,** 062103.

(14) Faber, H.; Das, S.; Lin, Y. H.; Pliatsikas, N.; Zhao, K.; Kehagias, T.; Dimitrakopulos, G.; Amassian, A.; Patsalas, P. A.; Anthopoulos, T. D. Heterojunction Oxide Thin-Film Transistors with Unprecedented Electron Mobility Grown from Solution. *Sci. Adv.* **2017,** *3* , e1602640.

(15) Gomes, L.; Marques, A.; Branco, A.; Araujo, J.; Simoes, M.; Cardoso, S.; Silva, F.; Henriques, I.; Laia, C. A. T.; Costa, C. IZO Deposition by RF and DC Sputtering on Paper and Application on Flexible Electrochromic Devices. *Displays* **2013,** *34*, 326-333.

(16) Leenheer, A. J.; Perkins, J. D.; van Hest, M. F. A. M.; Berry, J. J.; O'Hayre, R. P.; Ginley, D. S. General Mobility and Carrier Concentration Relationship in Transparent Amorphous Indium Zinc Oxide Films. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2008,** *77*, 115215.

(17) Morales-Masis, M.; Nicolas, S. M. D.; Holovsky, J.; Wolf, S. D.; Ballif, C. Low-Temperature High-Mobility Amorphous IZO for Silicon Heterojunction Solar Cells. *IEEE J. Photovoltaics* **2015,** *5*, 1340-1347.

(18) Naghavi, N.; Marcel, C.; Dupont, L.; Rougier, A.; Leriche, J.-B.; Guéry, C. Structural and Physical Characterisation of Transparent Conducting Pulsed Laser Deposited InO–ZnO Thin Films. *J. Mater. Chem.* **2000,** *10*, 2315-2319.

(19) Yan, Y.; Pennycook, S. J.; Dai, J.; Chang, R. P. H.; Wang, A.; Marks, T. J. Polytypoid Structures in Annealed In2O3–ZnO Films. *Appl. Phys. Lett.* **1998,** *73*, 2585.

(20) Haming, M.; Issanin, A.; Walker, D.; von Seggern, H.; Jagermann, W.; Bonrad, K. Interrelation between Chemical, Electronic, and Charge Transport Properties of Solution-Processed Indium-Zinc Oxide Semiconductor Thin Films. *J. Phys. Chem. C* **2014,** *118*, 12826-12836.

(21) Tetzner, K.; Isakov, I.; Regoutz, A.; Payne, D. J.; Anthopoulos, T. D. The Impact of Post-Deposition Annealing on the Performance of Solution-Processed Single Layer In2O3 and Isotype In2O3/ZnO Heterojunction Transistors. *J. Mater. Chem. C* **2017,** *5*, 59-64.

(22) Wang, C. L.; Liu, X. Q.; Xiao, X. H.; Liu, Y. L.; Chen, W.; Li, J. C.; Shen, G. Z.; Liao, L. High-Mobility Solution-Processed Amorphous

Indium Zinc Oxide/In2O3 Nanocrystal Hybrid Thin-Film Transistor. *IEEE Electron Device Lett.* **2013,** *34*, 72-74.

(23) George, S. M. Atomic Layer Deposition: An Overview. *Chem. Rev.* **2010,** *110*, 111-131.

(24) Sonsteby, H. H.; Fjellvag, H.; Nilsen, O. Functional Perovskites by Atomic Layer Deposition - An Overview. *Adv. Mater. Interfaces* **2017,** *4*, 1600903.

(25) Mackus, A. J. M.; Schneider, J. R.; MacIsaac, C.; Baker, J. G.; Bent, S. F. Synthesis of Doped, Ternary, and Quaternary Materials by Atomic Layer Deposition: A Review. *Chem. Mater.* **2019,** *31*, 1142-1183.

(26) Miikkulainen, V.; Leskelä, M.; Ritala, M.; Puurunen, R. L. Crystallinity of Inorganic Films Grown by Atomic Layer Deposition: Overview and General Trends. *J. Appl. Phys.* **2013,** *113*, 021301.

(27) Sanctis, S.; Krausmann, J.; Guhl, C.; Schneider, J. J. Stacked Indium Oxide/zinc Oxide Heterostructures as Semiconductors in Thin Film Transistor Devices: a Case Study Using Atomic Layer Deposition. *J. Mater. Chem. C* **2018,** *6*, 464-472.

(28) Kim, D.; Nam, T.; Park, J.; Gatineau, J.; Kim, H. Growth Characteristics and Properties of Indium Oxide and Indium-Doped Zinc Oxide by Atomic Layer Deposition. *Thin Solid Films* **2015,** *587*, 83-87.

(29) Krausmann, J.; Sanctis, S.; Engstler, J.; Luysberg, M.; Bruns, M.; Schneider, J. J. Charge Transport in Low-Temperature Processed Thin-Film Transistors Based on Indium Oxide/Zinc Oxide Heterostructures. *ACS Appl. Mater. Interfaces* **2018,** *10*, 20661-20671.

(30) Illiberi, A.; Katsouras, I.; Gazibegovic, S.; Cobb, B.; Nekovic, E.; van Boekel, W.; Frijters, C.; Maas, J.; Roozeboom, F.; Creyghton, Y.; Poodt, P.; Gelinck, G. Atmospheric Plasma-Enhanced Spatial-ALD of InZnO for High Mobility Thin Film Transistors. *J. Vac. Sci. Technol., A* **2018,** *36*, 04F401.

(31) Elam, J. W.; Sechrist, Z. A.; George, S. M. ZnO/Al2O3 Nanolaminates Fabricated by Atomic Layer Deposition: Growth and Surface Roughness Measurements. *Thin Solid Films* **2002,** *414*, 43-55.

(32) Sintonen, S.; Ali, S.; Ylivaara, O. M. E.; Puurunen, R. L.; Lipsanen, H. X-ray Reflectivity Characterization of Atomic Layer Deposition Al2O3/TiO2 Nanolaminates with Ultrathin Bilayers. *J. Vac. Sci. Technol., A* **2014,** *32*, 01A111.

(33) Chaaya, A. A.; Viter, R.; Baleviciute, I.; Bechelany, M.; Ramanavicius, A.; Gertnere, Z.; Erts, D.; Smyntyna, V.; Miele, P. Tuning Optical Properties of Al2O3/ZnO Nanolaminates Synthesized by Atomic Layer Deposition. *J. Phys. Chem. C* **2014,** *118*, 3811-3819.

(34) Mullings, M. N.; Hagglund, C.; Tanskanen, J. T.; Yee, Y.; Geyer, S.; Bent, S. F. Thin Film Characterization of Zinc Tin Oxide Deposited by Thermal Atomic Layer Deposition. *Thin Solid Films* **2014,** *556*, 186-194.

(35) Ho, M. Y.; Gong, H.; Wilk, G. D.; Busch, B. W.; Green, M. L.; Lin, W. H.; See, A.; Lahiri, S. K.; Loomans, M. E.; Raisanen, P. I.; Gustafsson, T. Suppressed Crystallization of Hf-Based Gate Dielectrics by Controlled Addition of Al2O3 Using Atomic Layer Deposition. *Appl. Phys. Lett.* **2002,** *81*, 4218.

(36) Zhilova, O. V.; Pankov, S.; Sitnikov, A. V.; Kalinin, Y. E.; Kashirin, M. A.; Makagonov, V. A. Optical and Electrical Properties of Thin-Film Hetero-Structures of the In2O3-ZnO System. *Mater. Res. Express* **2019,** *6*, 086330.

(37) Raghavan, R.; Bechelany, M.; Parlinska, M.; Frey, D.; Mook, W. M.; Beyer, A.; Michler, J.; Utke, I. Nanocrystalline-to-Amorphous Transition in Nanolaminates Grown by Low Temperature Atomic Layer Deposition and Related Mechanical Properties. *Appl. Phys. Lett.* **2012,** *100*, 191912.

(38) Hagglund, C.; Grehl, T.; Tanskanen, J. T.; Yee, Y. S.; Mullings, M. N.; Mackus, A. J. M.; Maclsaac, C.; Clemens, B. M.; Brongersma, H. H.; Bent, S. F. Growth, Intermixing, and Surface Phase Formation for Zinc

Tin Oxide Nanolaminates Produced by Atomic Layer Deposition. *J. Vac. Sci. Technol., A* **2016,** *34*, 021516.

(39) Chang, S. L.; Takoudis, C. G. Growth Behavior and Structural Analysis of Atomic Layer Deposited SnxTi1-xOy Films. *J. Vac. Sci. Technol., A* **2018,** *36*, 01A121.

(40) Li, D. H.; Zhai, C. H.; Zhou, W. C.; Huang, Q. H.; Wang, L.; Zheng, H.; Chen, L.; Chen, X.; Zhang, R. J. Effects of Bilayer Thickness on the Morphological, Optical, and Electrical Properties of Al2O3/ZnO Nanolaminates. *Nanoscale Res. Lett.* **2017,** *12*.

(41) Schiøtz, J.; Di Tolla, F. D.; Jacobsen, K. W. Softening of Nanocrystalline Metals at Very Small Grain Sizes. *Nature* **1998,** *391*, 561-563.

(42) Kwon, J. Y.; Lee, D. J.; Kim, K. B. Review Paper: Transparent Amorphous Oxide Semiconductor Thin Film Transistor. *Electron. Mater. Lett.* **2011,** *7*, 1-11.

(43) Hosono, H. Ionic Amorphous Oxide Semiconductors: Material Design, Carrier Transport, and Device Application. *J. Non-Cryst. Solids.* **2006,** *352*, 851-858.

(44) Lany, S.; Zunger, A. Dopability, Intrinsic Conductivity, and Nonstoichiometry of Transparent Conducting Oxides. *Phys. Rev. Lett.* **2007,** *98, 045501.*

(45) Martins, R.; Barquinha, P.; Pimentel, A.; Pereira, L.; Fortunato, E. Transport in High Mobility Amorphous Wide Band Gap Indium Zinc Oxide Films. *Phys. Status Solidi A* **2005,** *202*, R95-R97.

Chapter 6.

Summary and Conclusion

System scaling enabled by Moore's scaling is increasingly challenged by such a manufacturing issues and corresponding physical limitations of dimension scaling. Traditionally, dimensional scaling had been adequate to bring PPA (power-performance-area) merits, such as higher speed, higher density, lower power. A major portion of semiconductor device manufacturing is devoted to continue dimensional scaling, and these scaling targets have driven the industry toward a number of major technological innovations, including material and process changes such as high-k dielectrics and strain enhancement at field-effect transistor level. In case of interconnect scalability, maintaining control of interconnect resistance and electromigration and time-dependent-dielectric-breakdown limits has been emerged as major issues for manufacturing process. Especially, non-ideal scaling of the Cu diffusion barrier and corresponding reliability limits hinders further improvement in PPA of logic devices.

At this point of view, besides conventional Ta(N) 3D Cu diffusion barrier, alternative two-dimensional (2D) materials, including graphene, hexagonal-boron-nitride (h-BN), and transition-metal-dichalcogenides (TMDs), which exhibit atomic-level-thickness, research has been carried out to evaluate 2D materials as a Cu diffusion barrier replacement in the past few years. Previous results have suggested that 2D materials have promising Cu diffusion barrier

properties, which encourages integrating these novel materials to the state-of-the-art technologies. However, several key issues, such as defect modulation and back-end-of-line (BEOL) process integration issues, still hinder implicating of 2D materials as a Cu diffusion barrier. In this dissertation, we cover the opportunities and challenges of 2D carbon-based materials as a Cu diffusion barrier, and address a way to process integration for semiconductor manufacturing. These challenges are divided into 1) defect modulation of chemical vapor deposition (CVD) graphene and 2) BEOL process integration of carbon-based materials.

In chapter 2-4, we covered modulation of micro- and nanometer scale defects in CVD-graphene by various approaches. In chapter 2-3, we developed novel hybrid transparent conducting electrode (TCE) materials with significantly improved areal uniformity by hybridization of chemical vapor deposition (CVD) grown graphene and ALD grown thin film.

In chapter 2, we investigated the effects of bilayer period of atomic layer deposition of In-Zn-O transparent conducting oxide thin film. Here, the bilayer period is defined as the total number of ALD cycles in one supercycle. Unlike other deposition methods, the layer-by-layer deposition manner of ALD can make both well-blended homogeneous film and multilayered structure of binary sublayers. In this aspect, the

bilayer period of ALD determines whether deposited film exhibits a well-blended or layered structure, and makes enormous discrepancies in phase evolution and following the physical properties of the film. In particular, we deposited ALD-IZO films by varying the bilayer period from 10 to 200 cycles, while fixing the other ALD process parameters, such as a cycle ratio of In-O: Zn-O and the total number of ALD cycles. Throughout investigating the growth rate and cation ratio with increasing the bilayer period, we indicated the retarded adsorption of Zn precursor on its counter surface. More importantly, as the bilayer period increased, we examined the phase transition from well-blended amorphous IZO to the layered structure of In-rich and Zn-rich sublayers with the appearance of nanocrystalline In_2O_3 bixbyite. Intensive plan-view and cross-sectional TEM measurements revealed the microstructure evolution along with the bilayer period. Finally, the increase in resistivity coming from a decrease in both mobility and charge carrier density along with the bilayer period was discussed, combining the change in metal composition and microstructure evolution.

In chapter 3, we propose the way to compensate microscale defects in CVD-graphene by hybridization of CVD-graphene and transparent conducting oxide thin film, which is ALD-In_2O_3 in this case based on the results from above chapter. In this work, we prepared

graphene-In_2O_3 bilayer (GI-bilayer) and systematically investigated its electrical and optical properties. By comparing bare graphene and In_2O_3, the GI-bilayer showed improved electrical properties, but also complemented disadvantages of each material. For example, excellent areal-uniformity of the electrical properties (standard deviation of sheet resistance: 12 Ω/sq) of GI-bilayer (7 × 7 cm^2) clearly demonstrated that non-uniformity of CVD graphene is well compensated by homogeneously deposited In_2O_3 underlayer. Interestingly, both holes and electrons act as a major charge carrier in GI-bilayer and each electrical transport behaviors were analyzed by Hall effect measurement and supported by theoretical model. As a result, the electrical properties of graphene were indeed improved by increasing the concentration of the charge carrier. *P*-type doping of graphene was also experimentally confirmed by Raman spectroscopy and ultraviolet photoelectron spectroscopy analysis.

In chapter 4, atomic layer deposition (ALD) of Ru on CVD-graphene is introduced to patch defects in CVD-graphene, and following Cu blocking performance was evaluated by time-dependent-dielectric-breakdown (TDDB) test. ALD-Ru on CVD graphene shows selective deposition behavior, namely stuffing defects in graphene, and this defect stuffed CVD-graphene shows greater Cu blocking performance. Novel E-model was proposed based on 1-D flux model and implicated to

estimate activation energy and effective barrier thickness for Cu^+ ion to pass through the graphene diffusion barrier. In addition, electromigration (EM) reliability and enhancement in electrical conductivity of barrier itself are also investigated by agglomeration behavior of Cu on the barrier film, and evaluating surface energy.

Finally, in chapter 5, ultrathin amorphous carbon layer with the thickness of sub-1-nm is proposed as a next generation Cu diffusion barrier. This study focuses on the BEOL process integration issue of carbon-based materials. Conformal deposition of amorphous carbon layer on dielectric substrate was accomplished by grafting and following carbonization of hydroxyl group terminated polystyrene (PS-OH) polymer. Carbonization conducted under BEOL compatible temperature of below 460°C resulted in uniform 1-nm-thick amorphous carbon layer on SiO_2 substrate. Time-dependent-dielectric-breakdown (TDDB) test evaluated that this amorphous carbon layers exhibited superior Cu blocking performance than conventional TaN diffusion barrier under the thickness of 2 nm regime. Extrapolation of dielectric lifetime under normal device operating condition (~ 1 MV/cm, 100~150 °C) showed that this novel amorphous carbon layer is expected to exhibit 3-5 order of longer time to failure compared to conventional ALD-TaN diffusion barrier.

요약 (국문초록)

IC 집적회로가 무어의 법칙에 따라 점차 고집적화 됨에 따라, front-end 의 트랜지스터 영역은 물론 IC 소자 내 back-end 인터커넥트의 배선폭도 수십 nm 이하로 급격히 줄어들게 되었다. 이로 인해 인터커넥트 단의 RC delay 가 크게 증가하여 현재는 IC 소자 전체의 latency 를 결정하는 요소로 거론되고 있다. 따라서 차세대 로직 소자의 지속적인 미세화를 위해서는 높은 수준의 전류를 지연없이 전달할 수 있는 새로운 형태의 인터커넥트 구조 및 소재의 개발이 반드시 요구된다 할 수 있다.

현재 대부분의 반도체 소자 양산공정에 적용되고 있는 구리 인터커넥트 구조는 1990 년대 중반 IBM 에서 최초로 제시되었으며, 현행 5 nm technology node 는 물론 4 nm technology node 이하의 차세대 공정에서도 꾸준히 활용될 전망이다. 구리 인터커넥트 구조는 필연적으로 구리 확산방지막을 요구하게 되는데, 이는 구리가 인접한 실리콘 혹은 절연층으로의 높은 확산계수를 가지고 확산되기 때문이다. 인터커넥트 구조의 배선폭이 급격하게 감소함에 따라 기존에 구리 확산방지막으로 활용되던 수 nm 수준의 TaN 박막이 그 한계를 맞이하게 되었고, 원자 한 층 수준의 두께를 가지는 이차원 물질들이 기존 TaN 박막을 대체할 수 있는 차세대 구리 확산방지막으로 제시되고 있다. 그 중에서도 그래핀의 경우 탄소 원자의 반데르발스 반지름을 고려할 때

외부 분자가 통과할 수 있는 구조적 포어 지름이 0.064 nm 수준에 불과하여 높은 구리 확산방지 특성을 기대할 수 있으며, 이차원 물질의 특성 상 원자 한 층 수준의 매우 얇은 두께를 가진다. 또한 구리와 화합물을 형성하지 않음과 동시에 극히 낮은 용해도를 가지고 있으며, 투명전극으로 활용될 만큼 낮은 비저항을 가지고 있어 차세대 구리 확산방지막으로써 큰 장점을 가진다고 할 수 있다. 본 논문에서는 이러한 그래핀의 실제 구리 확산방지막 적용을 위한 결함제어, 그리고 반도체 공정 적합성이 확보된 1 nm 수준의 비정질 탄소막의 증착 및 그 구리 확산방지 특성에 대해 논하였다.

제 2 장 ~ 제 4 장에서는 그래핀에 존재하는 마이크로 혹은 매크로 수준의 결함제어 및 그 응용에 대해 논하였다. 비교적 높은 수준의 결정성을 가지는 것으로 알려진 화학기상증착법을 통해 합성된 그래핀 박막의 경우에도 그 합성과 전사 과정에서 정공, 결정립계, 균열 등 다양한 형태의 결함을 가지게 된다. 이러한 그래핀 내 결함들은 그래핀의 이차원 구조를 고려할 때, 구리의 빠른 확산경로가 되어 구리 확산방지 특성을 저해하게 된다.

제 2 장에서는 원자층증착법을 통해 Indium 기반 투명전극의 증착에 대해 연구하였다. 원자층증착법의 주요한 공정 파라미터 중 하나인 이중층 주기 (bilayer period)에 따른 IZO(In-Zn-O) 박막의 물성을 평가하였다. 제 3 장에서는 이러한 Indium 기반 산화물 박막과 그래핀 층의 복합체를 형성하여, 그래핀 내 존재하는 다양한 형태의 결함을 제어하였다. 이러한 결함제어과정을 통해 4 인치 수준의 대면적

상에서 매우 높은 면저항 균일도를 가지는 그래핀 기반 투명전극을 제조할 수 있음을 확인하였다.

제 4 장에서는 그래핀에 Ru (Ruthenium) 원자층증착법을 적용함으로써 그래핀의 결함부분에만 Ru 을 선택적으로 증착시켰으며, 이를 통해 그래핀의 결함을 제어하였다. Ru 으로 결함이 치유된 그래핀의 구리 확산방지 특성이 향상되는 것을 TDDB (time-dependent dielectric breakdown) 테스트를 통해 확인하였으며, 이차원 물질이 적용된 TDDB 시스템 상에서의 field dependent model 을 1D flux model 을 통해 제시하였다. 이를 통해 Ru 원자층증착법 적용시 구리가 그래핀 박막을 통과하는데 필요한 활성화에너지와 유효 확산방지막 두께가 증가함을 규명하였다. 추가적으로 Ru 으로 결함이 치유된 그래핀 확산방지막의 전기전진(electromigration) 신뢰성과 확산방지막 자체의 전도도 향상을 확인하였다.

제 5 장에서는 그래핀의 반도체 공정 적합성을 개선하기 위해 고분자의 그래프팅(grafting)과 탄화(carbonization)을 활용하여 1 nm 수준의 비정질 탄소막 증착 공정을 제시하였다. 그 결과 2.7 kg/mol 의 분자량을 가지는 폴리스타일렌 (Polystyrene)의 그래피팅 및 탄화를 통해 두께 0.8 nm 수준의 균일한 비정질 탄소막 구리 확산방지막을 인터커넥트 트렌치 구조에 형성할 수 있음을 확인하였다. 이렇게 합성된 비정질 탄소막의 구리 확산방지 특성을 TDDB 테스트를 통해 확인한 결과, 2 nm 이하의 두께에서 기존 TaN 확산방지막에 비해 더욱 뛰어난 구리 확산방지 특성을 가짐을 규명하였다.

주요어: Cu interconnect, Metallization, Diffusion barrier, Barrier Metal, Graphene, Amorphous carbon, Atomic layer deposition (ALD)

학번: 2015-20850

List of Publications

Papers

- **Sangbong Lee**, Minsu Kim, Seong-Yong Cho, Do-Joong Lee, Hyun-Mi Kim, Ki-Bum Kim. "Electrical properties of graphene/In_2O_3 bilayer with remarkable uniformity as transparent conducting electrode." *Nanotechnology* 31.9 (2019): 095708.

- **Sangbong Lee,#** Yun-Ho Kang,# Min-Sik Kim, Hyerin Lee, Yeong-Ho Cho, Minsu Kim, Tae-Sik Yoon, Hyun-Mi Kim, Ki-Bum Kim._"Effect of the Bilayer Period of Atomic Layer Deposition on the Growth Behavior and Electrical Properties of the Amorphous In–Zn–O Film." *ACS Applied Materials & Interfaces* 12.35 (2020): 39372-39380. (Supplementary cover figure)

- Yun-Ho Kang,# **Sangbong Lee,#** Youngwoo Choi, Won Kyung Seong, Kyu Hyo Han, Jang Hwan Kim, Hyun-Mi Kim, Seungbum Hong, Sun Hwa Lee,* Rodney S. Ruoff,* Ki-Bum Kim,* and Sang Ouk Kim* "Large-area Uniform 1-nm-level Amorphous Carbon Layers from 3D Conformal Polymer Brushes. A "Next-generation" Cu Diffusion Barrier?" *Advanced Materials* (2022) (Accepted)

- Kyungmin Jo, **Sangbong Lee**, Sang-Min Kim, Jung Bin In, Seung-Mo Lee, Jae-Hyun Kim, Hak-Joo Lee, Kwang-Seop Kim. "Stacked bilayer graphene and redox-active interlayer

for transparent and flexible high-performance supercapacitors." *Chemistry of Materials* 27.10 (2015): 3621-3627.

- Sejeong Won, Jae-Won Jang, Hyung-Jin Choi, Chang-Hyun Kim, **Sangbong Lee**, Yun Hwangbo, Kwang-Seop Kim, Soon-Gil Yoon, Hak-Joo Lee, Jae-Hyun Kim, Soon-Bok Lee. "A graphene meta-interface for enhancing the stretchability of brittle oxide layers." *Nanoscale* 8.9 (2016): 4961-4968.

- Min-Sik Kim, Minsu Kim, Suyeon Son, Seong-Yong Cho, **Sangbong Lee**, Dong-Kwan Won, Jaechul Ryu, Inseob Bae, Hyun-Mi Kim, Ki-Bum Kim "Sheet resistance analysis of interface-engineered multilayer graphene: mobility versus sheet carrier concentration." *ACS applied materials & interfaces* 12.27 (2020): 30932-30940.

- Minsu Kim, Shunichi Nabeya, Seung-Min Han, Min-Sik Kim, **Sangbong Lee**, Hyun-Mi Kim, Seong-Yong Cho, Do-Joong Lee, Soo-Hyun Kim, Ki-Bum Kim "Selective Atomic Layer Deposition of Metals on Graphene for Transparent Conducting Electrode Application." *ACS applied materials & interfaces* 12.12 (2020): 14331-14340.

- Min-Sik Kim, Ki-Ju Kim, Minsu Kim, **Sangbong Lee**, Kyu Hyun Lee, Hyeongkeun Kim, Hyun-Mi Kim, Ki-Bum Kim "Cu oxidation kinetics through graphene and its effect on the electrical properties of graphene." *RSC Advances* 10.59 (2020): 35671-35680.

Award

- **STAM Young Scientist Award 2018**, Science and Technology of Advanced Materials. The 14th UT-SNU-TU Student workshop in Beijing, China

Patents

- 김기범, 김현미, 조영호, **이상봉** "투명전극" 10-2019-0069085 (대한민국)
- 김기범, 김상욱, 강윤호, **이상봉** "탄소막 형성 방법" 10-2021-0031173 (대한민국)
- 김기범, **이상봉** "펠리클 구조체 제조 방법 및 그에 따라 제조된 펠리클 구조체" 10-2021-0059890 (대한민국)

Conferences

- **Sangbong Lee**, et al. "Enhanced stretchability of transparent graphene electrode", ICAMD (2013)
- **Sangbong Lee**, et al. "Restoring carrier mobility of defective CVD-graphene by atomic stitching." NCC2016 (2016)
- **Sangbong Lee**, et al. "Flexible and transparent electrode properties of graphene/Indium oxide bilayer structure." ENGE 2018 (2018)
- **Sangbong Lee**, et al. "Solid-state nanopore and its application for high throughput protein-protein interaction screening." IDS-08 (2019)
- **Sangbong Lee**, et al. "Graphene/Indium oxide composite as a transparent conducting electrode." 2019 E-MRS Fall meeting (2019)