Ph.D. Dissertation

Design of High-Speed Power-Efficient Transmitter Systems with Bandwidth Extension Techniques

대역폭 증대 기술을 이용한 전력 효율적 고속 송신 시스템 설계

by

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February, 2022

Department of Electrical and Computer Engineering
College of Engineering
Seoul National University

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이 논문을 공학박사 학위논문으로 제출함
2022 년 2 월

서울대학교 대학원
전기·정보공학부
도 형 록

도형록의 박사 학위논문을 인준함
2022 년 2 월

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부위원장 _____ (인)

위 원 _____ (인)

위 원 _____ (인)

위 원 _____ (인)

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A Dissertation Submitted to the Department of
Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy
at
SEOUL NATIONAL UNIVERSITY

February, 2022

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Abstract

The high-speed interconnect at the datacenter is being more crucial as 400 Gb Ethernet standards are developed. At the high data rate, channel loss requires bandwidth extension techniques for transmitters, even for short-reach channels. On the other hand, as the importance of east-to-west connection is rising, the data center architectures are switching to spine-leaf from traditional ones. In this trend, the number of short-reach optical interconnect is expected to be dominant. The vertical-cavity surface-emitting laser (VCSEL) is a commonly used optical modulator for short-reach interconnect. However, since VCSEL has low bandwidth and nonlinearity, the optical transmitter also needs bandwidth-increasing techniques. Additionally, the power consumption of data centers reaches a point of concern to affect climate change. Therefore, this thesis focuses on high-speed, power-efficient transmitters for data center applications. Before the presenting circuit design, bandwidth extension techniques such as fractionally-spaced feed-forward equalizer (FFE), on-chip transmission line, inductive peaking, and T-coil are mathematically analyzed for their effectiveness.

For the first chip, a power and area-efficient pulse-amplitude modulation 4 (PAM-4) transmitter using 3-tap FFE based on a slow-wave transmission line is presented. A passive delay line is adopted for generating an equalizer tap to overcome the high clocking power consumption. The transmission line achieves a high slow-wave factor of 15 with double floating metal shields around the differential coplanar waveguide. The transmitter includes 4:1 multiplexers (MUXs) and a quadrature

clock generator for high-speed data generation in a quarter-rate system. The 4:1 MUX utilizes a 2-UI pulse generator, and the input configuration is determined by qualitative analysis. The chip is fabricated in 65 nm CMOS technology and occupies an area of 0.151 mm^2. The proposed transmitter system exhibits an energy efficiency of 3.03 pJ/b at the data rate of 48 Gb/s with PAM-4 signaling.

The second chip presents a power-efficient PAM-4 VCSEL transmitter using 3-tap FFE and negative-k T-coil. The phase interpolators (PIs) generate fractionally-spaced FFE tap and correct quadrature phase error. The PAM-4 combining 8:1 MUX is proposed rather than combining at output driver with double 4:1 MUXs to reduce serializing power consumption. T-coils at the internal and output node increase the bandwidth and remove inter-symbol interference (ISI). The negative-k T-coil at the output network increases the bandwidth 1.61 times than without T-coil. The VCSEL driver is placed on the high VSS domain for anode driving and power reduction. The chip is fabricated in 40 nm CMOS technology. The proposed VCSEL transmitter operates up to 48 Gb/s NRZ and 64 Gb/s PAM-4 with the power efficiency of 3.03 pJ/b and 2.09 pJ/b, respectively.

Keywords : PAM-4 transmitter, 4:1 multiplexer(MUX), fractionally-spaced feed-forward equalizer(FFE), slow-wave transmission line, T-coil, VCSEL CMOS transmitter, push-pull driver

Student Number : 2016-20891

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Chapter 1

Introduction

1.1 Motivation

The data center has been a nucleus of the overall industry as the demand for high-tech ICT such as artificial intelligence, internet-of-things, cloud computing, and autonomous vehicles rapidly increases. The hyperscale data center, which has over 5,000 servers, is estimated to grow +87% from 2015 to 2020 [1.1]. The global data center traffic also boosts more than triples at the same period, as shown in Fig. 1.1. The previous user-centric computing is alternating to cloud-centric computing of the data center. This paradigm shift is a natural result since data processing and storage requirements are skyrocketing, making it inefficient for individuals to own their equipment. Video streaming account for an overwhelming percentage of 60.6% in the global application traffic category [1.2]. The 4K resolution movie has dozens

of gigabytes volume, which is too large for personal storage. These make Netflix the most significant data traffic provider beating even YouTube, as shown in Fig. 1.2. These data traffic trend accelerates the increment of data centers.

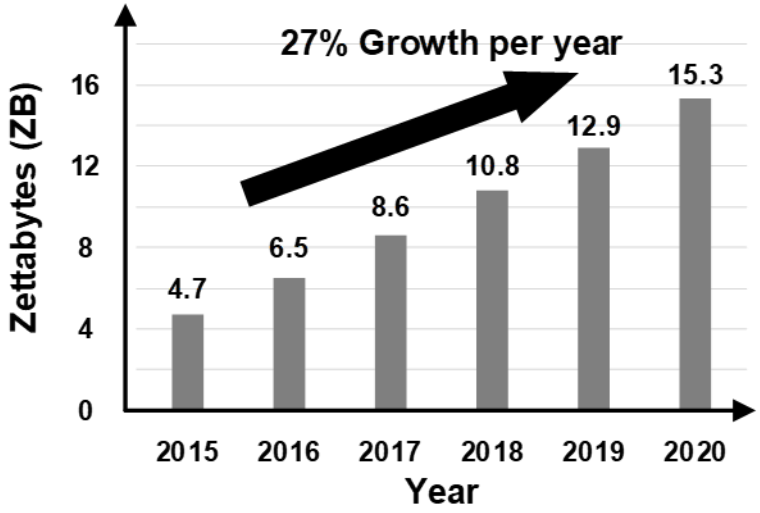


Fig. 1.1 Data center traffic growth [1.1]

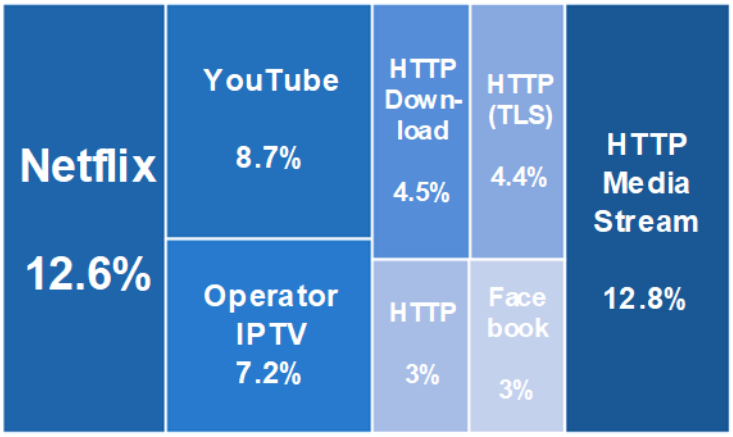


Fig. 1.2 Global application traffic share in 2019 [1.2]

At the same time, climate system change is concerned with impacting real-life shortly [1.3]-[1.5]. Increasing electricity usage is crucial for climate change, and the proportion of data centers is already over 1% of overall electricity consumption [1.5]-[1.8]. The carbon emission of the data center is about 0.3% of the broad emission. However, this proportion is expected to rise rapidly because of the internet traffic explosion. In the worst-case scenario, ICT will use as much as half of global electricity, and data center usage will account for one-third of it in 2030. Seeing the international data center energy-use trends in [1.7], the improvement of energy efficiency such as lowering power usage effectiveness (PUE) or increasing data center infrastructure was inadequate to data service demands rise. While the storage capacity and data center traffic increase 26 times and 11 times, PUE and the number of servers per workload fall to 0.75 times and 0.19 times, respectively. In response to these problems, 54% of the data center organizations are preparing for climate

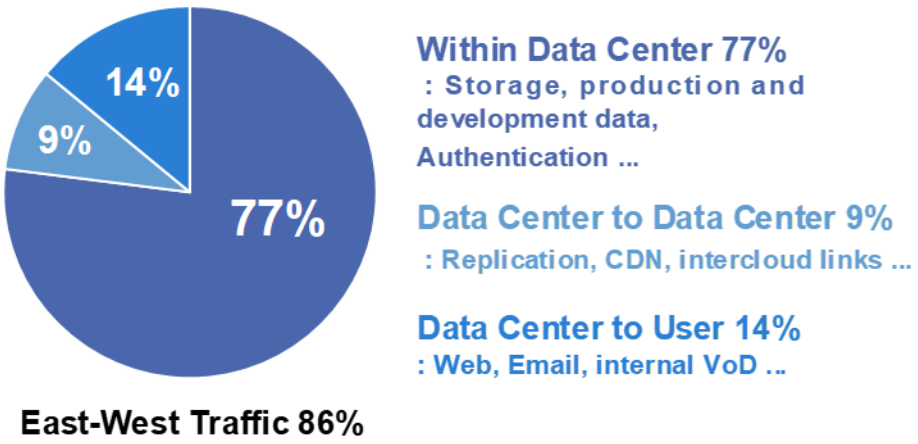


Fig. 1.3 Global data center traffic by destination in 2020 [1.1]

change by re-evaluating the cooling system or reporting sustainability [1.9]. However, because the fundamental problem is power consumption and heat dissipation of the server, the technology development of a power-efficient system is more important to suppress climate change.

Back to the data center trends, the data traffic occurs within and without the data center. Though networked devices are predicted to be 29.3 billion in 2023 [1.10], the east-west traffic accounts for the majority in the data center, as shown in Fig. 1.3. This fact reminds us that the interface in the data center is still essential compared to long-haul optical interface or wireless communication.

Meanwhile, the data rate per pin is also crucial to overall power efficiency as well as low power consumption. For this reason, the four-level pulse-amplitude modulation (PAM-4) is adopted to high data rate standards both for the electrical interface and optical interface [1.11]-[1.13]. The multi-level modulation allows a higher data throughput both for low-bandwidth lossy electrical channels and optical modulation devices. Equalization, especially feed-forward equalization (FFE), is also widely adopted for the high-speed transmitter. However, the FFE harms the power efficiency of the transmitter system by increasing circuit complexity. In this thesis, the high-speed PAM-4 transmitters for the electrical and optical interface are proposed with FFE and other bandwidth extension techniques for enhanced power efficiency. The transmission-line-based FFE is offered for the electrical transmitter to reduce clocking power and increase output node bandwidth. The fractionally-spaced tap FFE and negative-k T-coil are adopted for the VCSEL transmitter to compensate for low VCSEL bandwidth. The proposed transmitters achieve a high data rate and advanced power efficiency compared to state-of-the-art circuits.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, the backgrounds of the data center architectures and bandwidth extension techniques are presented. A comparison of conventional data center architecture and advanced spine-leaf architecture is provided. And, the bandwidth extension techniques with passive element and FFE are presented. The analyses of fractionally-spaced FFE, on-chip transmission line, inductor, and T-coil are discussed.

In Chapter 3, a 48 Gb/s PAM-4 electrical transmitter with FFE based on an on-chip transmission line is presented. The proposed slow-wave coplanar waveguide is designed in a floating double-shielded form to obtain sufficient group delay. And the design consideration on single-ended current mode 4:1 multiplexer is introduced with a qualitative analysis. Then, the circuit implementation is explained, and the measurement results are shown.

In Chapter 4, a 64 Gb/s PAM-4 VCSEL transmitter is presented. First, the design considerations for a power-efficient system are discussed about serializer and driver scheme. Then, the circuit implementation is explained, and the measurement results are shown.

Chapter 5 summarizes the proposed works and concludes this thesis.

Chapter 2

Background of High-Speed Interface

2.1 Overview

The data bandwidth for the wireline interface has grown exponentially to respond to the explosive global data traffic increment. The interface system is constrained by the physical size as well as by the bandwidth. Therefore the interface standards are adopting a higher per-lane data rate and PAM-4 rather than low-speed multi-lane. This high per-lane data rate demand appears in various wireline applications such as memory, backplane, rack-to-rack, and LAN [2.1], as shown in Fig. 2.1. The demanding transfer rate almost doubles every four years from low-speed DRAM interface, DDR, to high-speed CEI. When seeing from a data center architectural point of view, the high per-lane data rate allows less interconnect such as copper cable and

active optical cable (AOC) between chip-to-chip, chip-to-module, server-to-server, and server-to-switch. For the electrical interface, the low per-lane data rate with multi-lane has problems on the number of pad limitation or crosstalk. The additional optical modules and optical devices produce cost and packaging space problems for the optical interface of server-to-server and server-to-switch interconnect.

On the other hand, the high per-lane data rate requires the in-circuit bandwidth extension techniques or channel loss compensating equalization. These techniques have trade-offs with power consumption. Therefore, effective power-saving and bandwidth-boosting methods are crucial to lowering overall power usage effectiveness (PUE).

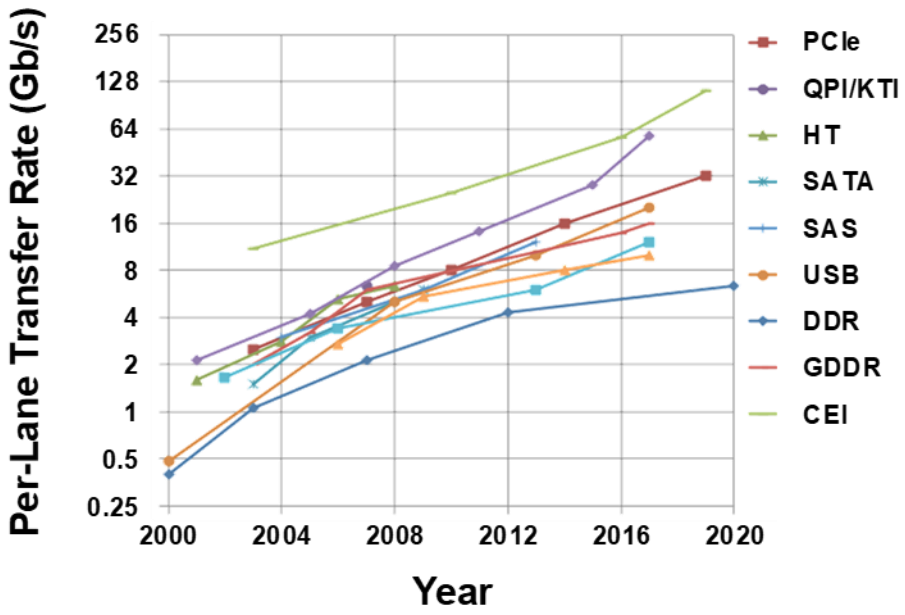


Fig. 2.1 Per-lane transfer rate trend of interface standards [2.1]

This chapter will deal with the data center architecture and short-reach standards to describe the importance of the following chapters. After that, the power-efficient bandwidth extension techniques by passive elements and fractionally-spaced FFE are presented with mathematical analyses.

2.2 Basis of Data Center Architecture

A data center is a facility that centralizes ICT equipment and operations to store, process, and disseminate the data. The data center infrastructure includes servers, storage systems, switches, and routers. The traditional 3-tier architecture is illustrated in Fig. 2.2. The 3-tier architecture is the most common, consisting of the edge layer (access layer), the aggregation layer, and the core layer [2.2]. The aggregation switches facilitate many server nodes with a loop-free topology. The interconnect consists of copper cable, AOC based on multi-mode fiber (MMF), and single-mode

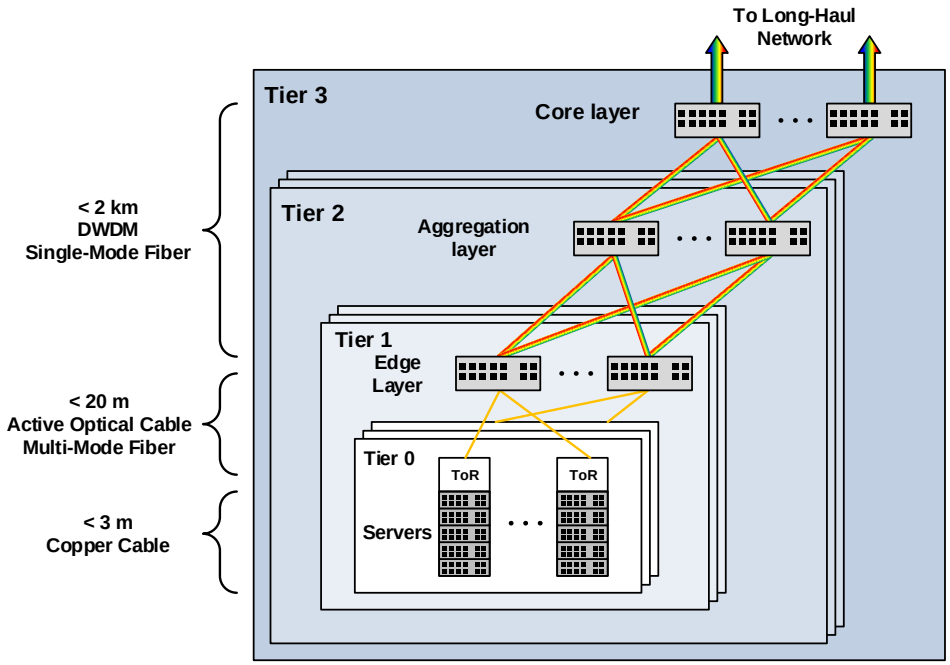


Fig. 2.2 Conventional 3-tier data center architecture

fiber (SMF) according to tier and physical length. Comparing the number of each cable type, copper cable and AOC are dominant because of dense server-to-server connection. The data communication is primarily within one rack, and only one-tenth of the data traffic is sent out of the rack. As mentioned in Chapter 1, since east-west data communication has been emphasized rather than north-south, the 3-tier architecture loses competitiveness.

Recently, the 2-tiered spine-and-leaf architecture is considered better than the conventional one because of its aptness for east-west traffic. In spine-and-leaf architecture, every leaf switch connects to every spine switch. The data traffic always crosses the same number of devices for server-to-server communication to enhance the performance of the east-west data path [2.3]. The performance would not degrade much if one of the top spine switches failed since other switches could share the workload. In the implementation, top-of-rack (ToR) plays a role of leaf aggrega-

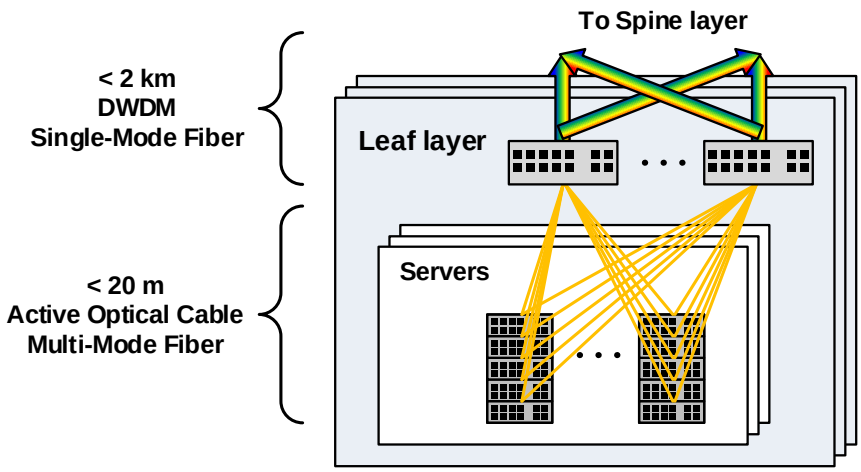


Fig. 2.3 Future candidate of spine-and-leaf data center architecture

tion switch in leaf layer. The interconnect between servers and ToR typically consists of copper cable, which is less than 5 meters. In [2.4], the advanced spine-and-leaf is discussed, as shown in Fig. 2.3. The lossy copper cable and latency-adding ToR switch are removed. The AOC, which has been the dominant media even before, is now more important.

2.3 Short-Reach Interface Standards

As the data rate rises, ultra-high-speed link standards are published to cope with the industrial demands [1.11]-[1.13]. The organizations such as IEEE and OIF developed interoperable interface standards for electrical and optical 400 Gb/s communication. Fig. 2.4 shows the CEI-112G application for short-reach electrical interface [2.5]. The targets of interconnecting reach are from 25 mm of package channel to long distance with two connectors between backplanes or cable. PAM-4 is adopted by most applications for low channel loss and circuit bandwidth. The data equalization and forward error correction (FEC) compensate channel loss and achieve a

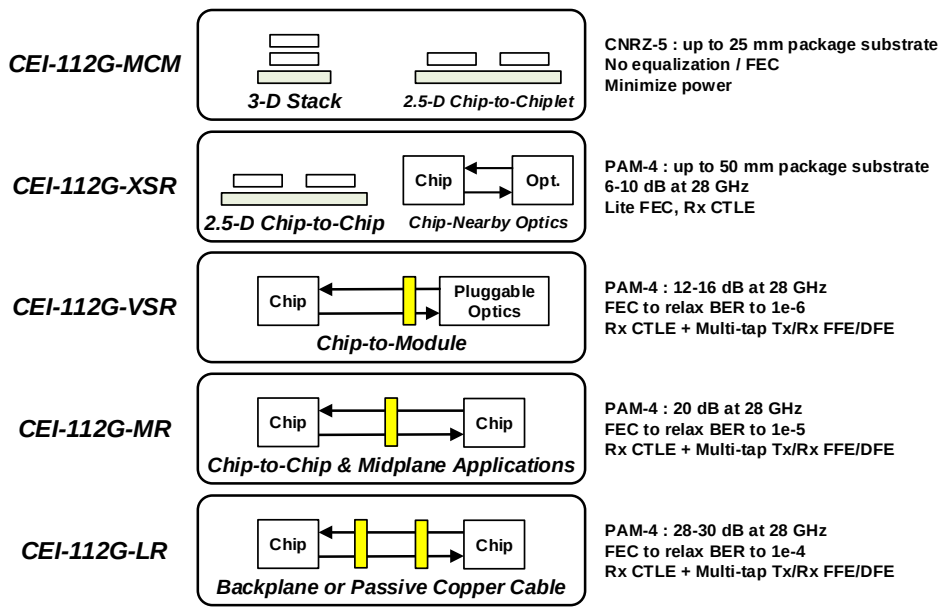


Fig. 2.4 OIF CEI-112G development application space [2.5]

low bit error rate (BER). Since the relatively-short interfaces within server and intra-rack are based on the copper medium, the electrical links are still important even for the future spine-and-leaf architecture data center.

For the short-reach optical interface, IEEE defines 400GBASE-SR16, and 400GBASE-SR8 for 100 m reach 400Gb/s Ethernet standard [1.11][1.12] which use sixteen parallel strands of fiber each at 25 Gb/s NRZ and eight parallel strands of fiber each at 50 Gb/s PAM-4. The optical standards have a low per-lane data rate, although channel loss and dispersion are negligible under 100 m for MMF. The reason is in the optical device, especially in transmitters. Optical modulation devices are used in short-reach interconnect such as Mach-Zehnder modulator, microring modulator, and vertical-cavity surface-emitting laser (VCSEL). Mach-Zehnder modulator has a wide bandwidth. However, it has high operating voltage and a too big package area. The Microring modulator has a wide bandwidth and very compact package area, and the operating voltage is sufficient to be driven by CMOS technology. However, it should be fabricated in an expensive photonic IC. Lastly, VCSEL has a meager cost by wafer process and reasonable package area. It has disadvantages on high operating voltage, low bandwidth, and nonlinearity. Nevertheless, VCSEL is the most common device for the optical modulator for its cost competitiveness. The BiCMOS process is usually utilized for the VCSEL driver to deal with the operating voltage and bandwidth.

The optical interconnect in the server is mainly utilized by pluggable optics. It can be conveniently used by plugging the server rack back without re-configuring the chip or chip package. However, as seen in Fig. 2.4, the pluggable optics module is placed far from the host chip, with a channel loss of 12-16 dB and a reflective

connector. Corresponding to this problem, on-board optics and co-packaged optics are proposed, as shown in Fig. 2.5 [2.6][2.7]. On-board optics moves the connector into the board from the edge. Though the PCB trace is shortened, the channel loss remains, requiring an equalization and data recovery. Co-packaged optics replaces

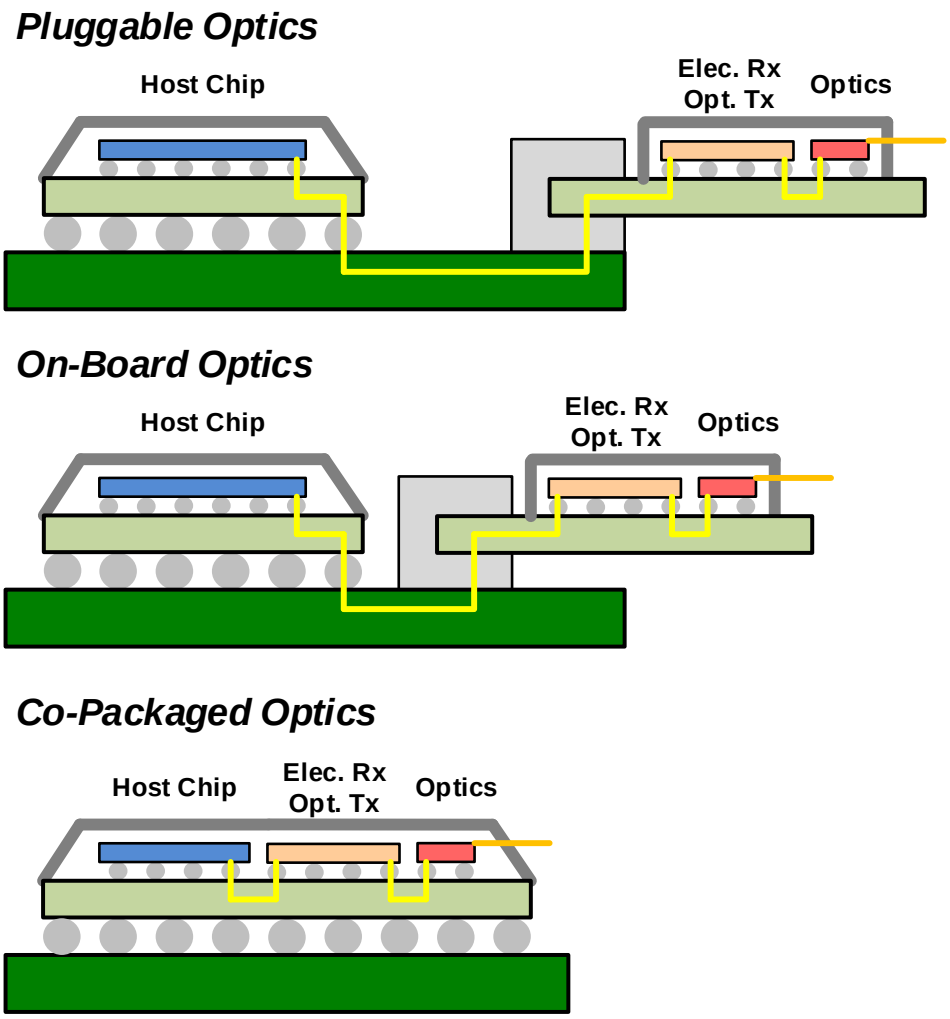


Fig. 2.5 Development of chip-to-optical module interconnect

the connector by integrating optical transceiver and optical devices into the package of the host chip, and thereby the interconnect is shortened to XSR standard. Furthermore, if the transceiver is fabricated in CMOS technology, same with the host ASIC, the overall system except photonic devices is monolithically designed as described in Fig. 2.6. The fully integrated system would remove the power-hungry electrical transceiver to realize a power-efficient data center.

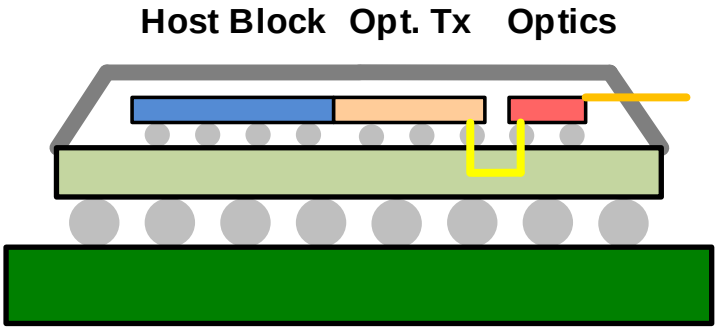


Fig. 2.6 Future candidate of electrical-to-optical interconnect

2.4 Analyses of Bandwidth Extension Techniques

2.4.1 Fractionally-Spaced FFE

The feed-forward equalization, FFE, is commonly used in the transmitter to compensate for channel loss or low interconnect bandwidth. The general block diagram of FFE is shown in Fig. 2.7. There are N pre-taps and M post-taps in the block diagram. The output *y[n]* is expressed as follows.

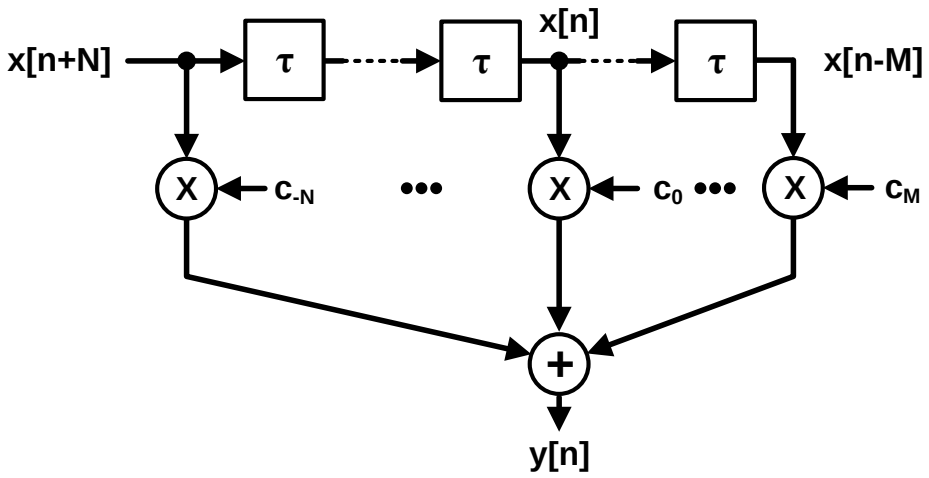


Fig. 2.7 FFE block diagram

$$y[n] = \sum_{i=-N}^{M} c_i x[n-i]$$
$$where \sum_{i=-N}^{M} |c_i| = 1 \tag{2.1}$$

The summation of FFE coefficients is normalized to one by the driver amplitude limitation. When this input-output relationship is written in the s-domain, the transfer function is expressed as (2.2).

$$\mathrm{H}(s) = Y(s)/X(s) = \sum_{i=-N}^{M} c_i e^{-s*i\tau} \tag{2.2}$$

The tap interval τ is usually a 1-unit interval (UI), which is the symbol width of the data. The serializing clock can quickly produce the 1-UI time delay. The frac-

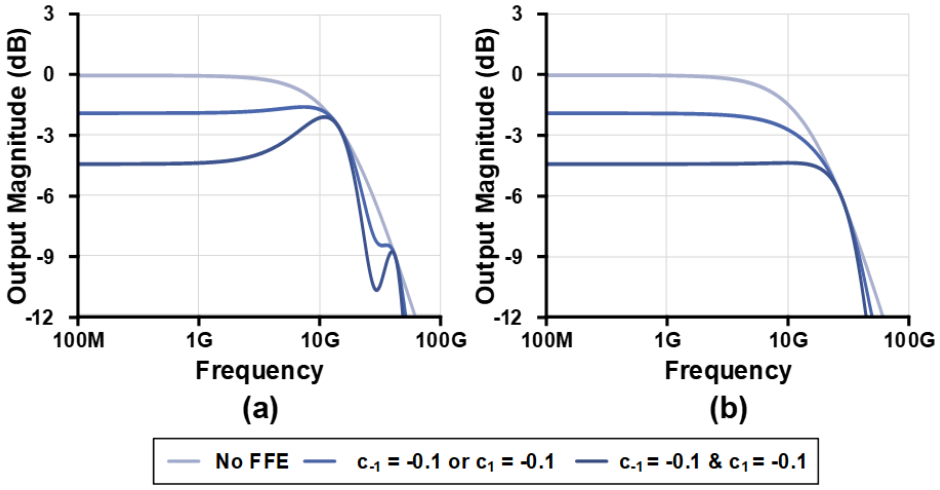


Fig. 2.8 AC-response of FFE for RC load (a) 1-UI tap (b) 0.5-UI tap

tionally-spaced FFE is also used for broader bandwidth [2.8]-[2.12]. The AC-response of the conventional and fractionally-spaced FFE is shown in Fig. 2.8. The output load is a termination resistor with 400 fF of a capacitor. Because the FFE term in (2.2) has peakings at every $1/\tau i$ Hz, the output magnitude is de-emphasized from DC to $1/\tau i$ Hz. In the same principle, fractionally-spaced FFE has wider de-emphasizing range. As seen in Fig. 2.8, the 3-dB bandwidth in the flat gain condition is wider for 0.5-UI tap FFE. However, the AC-response graph does not show inter-symbol-interference (ISI) characteristics. It is hard to separate the effect of pre-tap and post-tap since the exponential term seems equal in magnitude output.

A single-bit-response (SBR) analysis helps find the proper FFE coefficient better than AC-response. An example of the SBR and FFE is presented in Fig. 2.9. The

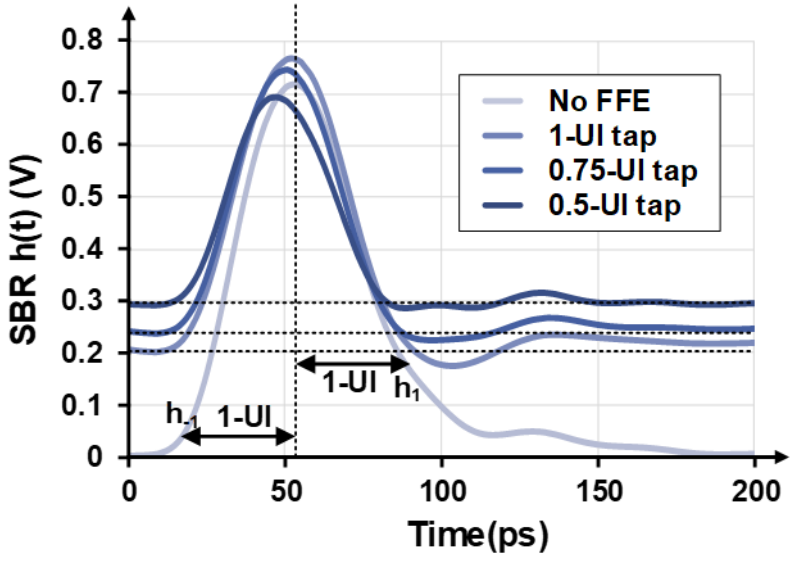


Fig. 2.9 28 Gb/s Single-bit-response with various FFE tap interval

number of taps is one for pre- and post-tap each. The tap coefficients of *k*-UI tap FFE are set to remove 1st pre-cursor and post-cursor, and they can be calculated by the following equation (2.3). The original SBR function is *h(t)* which its main-cursor is at t=0, and the symbol width is normalized to one.

$$\begin{bmatrix} C_{-k} \\ C_0 \\ C_k \end{bmatrix} = \begin{bmatrix} h\big(-(1-k)\big) & h(-1) & h\big(-(1+k)\big) \\ h(k) & h(0) & h(-k) \\ h\big((1+k)\big) & h(1) & h\big((1-k)\big) \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \tag{2.3}$$

The coefficients in (2.3) are not normalized since the matrix does not include en-

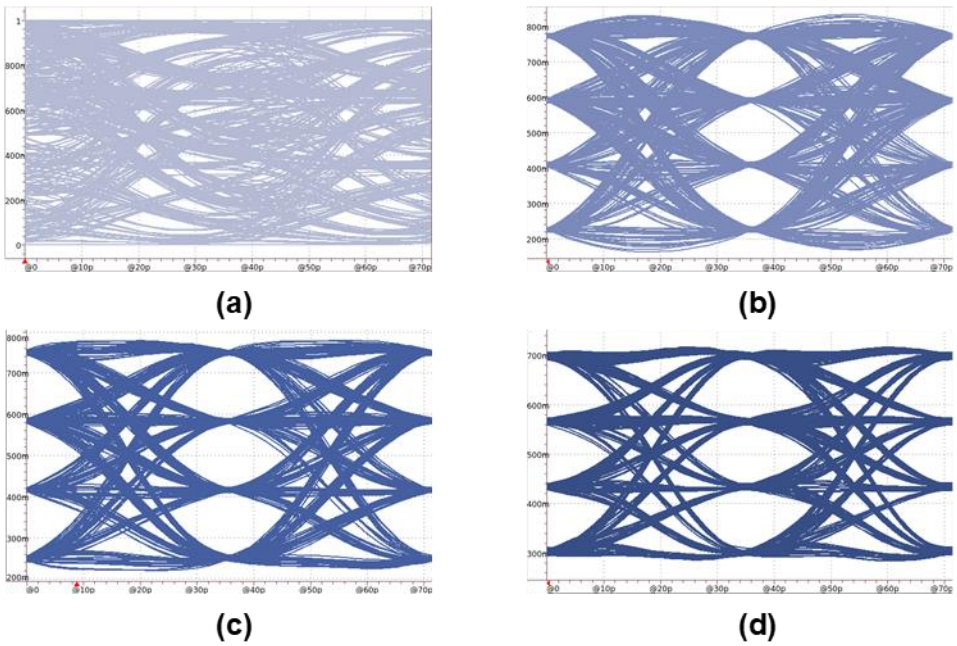


Fig. 2.10 56 Gb/s PAM-4 eye diagram of 3-tap FFE

(a) no FFE (b) 1-UI tap (c) 0.75-UI tap (d) 0.5-UI tap

tire cursors. The eye diagram of each FFE type with proper coefficients is presented in Fig. 2.10. The simulation is implemented in PAM-4 rather than NRZ since it is more vulnerable to data-dependent jitter (DDJ). As seen in the eye diagrams, the eye height is open with the cursor-removing FFE coefficients. For the eye width, short-tap interval FFE has an advantage in removing DDJ. The measurements of center eye width are 0.515 UI, 0.588 UI, and 0.615 UI for Fig. 2.10(b), (c), and (d), respectively. Since the eye width is hard to be equalized at a receiver, the fractionally-spaced FFE is efficient to lower the bit error rate as the data rate increase.

2.4.2 Transmission Line

The on-chip transmission line is often used as a distributed amplifier for RF application [2.13][2.14]. As the data rate of the wireline application also increases, utilizing a transmission line is considered the circuit design option.

Fig. 2.11 shows a distributed N-stage amplifier. The complex propagation constant of the transmission line is expressed in (2.4).

$$\gamma = \sqrt{(R_0 + j\omega L_0)(G + j\omega C_0)}$$

$$= j\omega\sqrt{L_0 C_0}\sqrt{1 - j\left(\frac{R_0}{\omega L_0} + \frac{G_0}{\omega C_0}\right)}$$

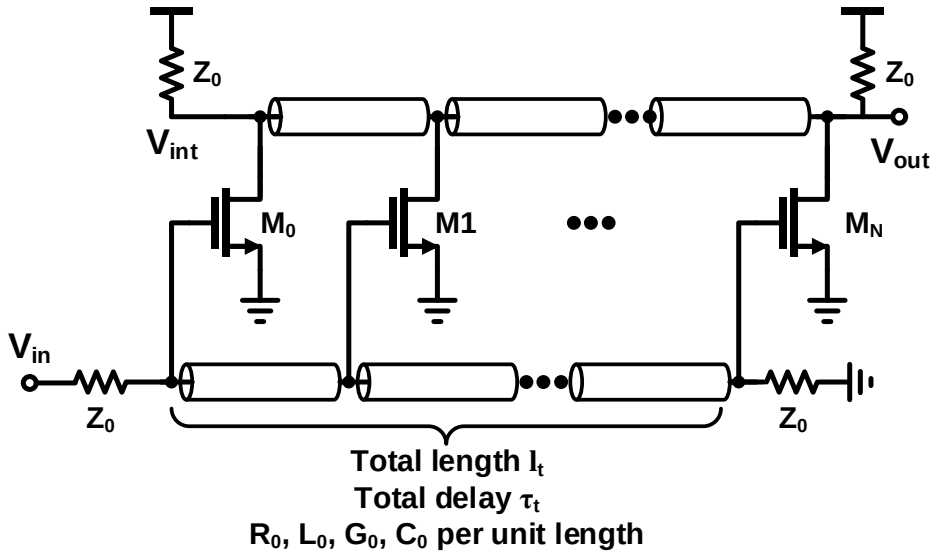


Fig. 2.11 Distributed amplifier with transmission line

$$\cong j\omega\sqrt{L_0C_0}\left(1-\frac{j}{2}\left(\frac{R_0}{\omega L_0}+\frac{G_0}{\omega C_0}\right)\right)=\alpha+j\beta$$

$$\text{where } \alpha\cong\frac{1}{2}\left(\frac{R_0}{Z_0}+GZ_0\right),\beta=\omega\sqrt{L_0C_0},Z_0=\sqrt{L_0/C_0} \tag{2.4}$$

Assuming the gate capacitance of the transistor, C_{GS}, is uniformly distributed over a length l_t, the characteristic impedance Z_0 is written as follows:

$$Z_0=\sqrt{\frac{L_0}{C_0+nC_{GS}/l_t}}\cong\sqrt{\frac{L_0}{nC_{GS}/l_t}} \tag{2.5}$$

The output gain is derived as (2.6) if the attenuation constant α is negligible. The gate-source capacitance C_{GS} is approximated to $(2/3)C_{OX}WL$.

$$A_{v,out}=\frac{1}{4}ng_m\sqrt{\frac{L_0}{nC_{GS}/l_t}}$$

$$=\frac{n}{4}\mu_nC_{OX}\frac{W}{L}(V_{GS}-V_{th})\sqrt{\frac{L_0}{nC_{GS}/l_t}}$$

$$\cong\frac{3}{8}\frac{\mu_n}{L^2}(V_{GS}-V_{th})\sqrt{\frac{nC_{GS}}{l_t}L_0l_t^2}$$

$$\cong\frac{3}{8}\frac{\mu_n}{L^2}(V_{GS}-V_{th})\tau_t \tag{2.6}$$

The amplifier gain is proportional to the transmission delay, τ_t. The transmission line also cancels the transistor input capacitance by distribution of lumped elements,

thus extending the bandwidth. Meanwhile, the voltage gain at V_{int} is derived in the same way.

$$A_{v,int} = \frac{1}{4}\left(\sum_{i=0}^{n} e^{-s\frac{2\tau_t}{n}i}\, g_{m,i}\right)\sqrt{\frac{L_0}{nC_{GS}/l_t}} \tag{2.7}$$

If the transconductances $g_{m,i}$ are biased differently as $c_i \frac{3}{2}\frac{\mu_n}{L^2} C_{GS}$, the circuit using V_{int} as output behaves as FFE driver as shown in (2.8) [2.15][2.16]. In this case, the bandwidth extension effect still remains.

$$A_{v,int} = \left(\sum_{i=0}^{n} e^{-s\frac{2\tau_t}{n}i}\frac{c_i}{n}\right)\frac{3}{8}\frac{\mu_n}{L^2}\tau_t \tag{2.8}$$

In reality, the attenuation constant α is not negligible because the resistance of the transmission line and output resistance of the transistor act as R_0 and G_0, respectively. Therefore, considering the attenuation, the FFE gain $A_{v,int}$ is expressed as follows:

$$A_{v,int} = \left(\sum_{i=0}^{n} e^{-s\frac{2\tau_t}{n}i}\left(\frac{c_i}{n}e^{-\frac{2\alpha l_t}{n}i}\right)\right)\cdot\frac{3}{8}\frac{\mu_n}{L^2}\tau_t \tag{2.9}$$

The attenuation of the input and output line can be compensated by an increment of corresponding FFE coefficient c_i. Therefore, the bandwidth extension by absorbing gate capacitance into the transmission line is still valid in this case.

2.4.3 Inductor

The bandwidth extension by inductive peaking in an amplifier has been used for a long time [2.17]-[2.20]. The inductive peaking provides wide bandwidth without the additional power consumption and design complexity. Inductors in a current-mode (CM) driver are utilized both for capacitive load and terminated load. Plus, it is placed either shunt or series way against the load. Fig. 2.12 shows CM drivers with two types of inductive peaking. C_D and Z_L correspond to driver output capacitance and load impedance, respectively. The load impedance is capacitive for pre-driver or terminated for output driver.

$$\begin{aligned} Z_L &= 1/sC_L && \text{(capacitive load)} \\ \text{or } & R||(1/sC_L) && \text{(terminated load)} \end{aligned} \tag{2.10}$$

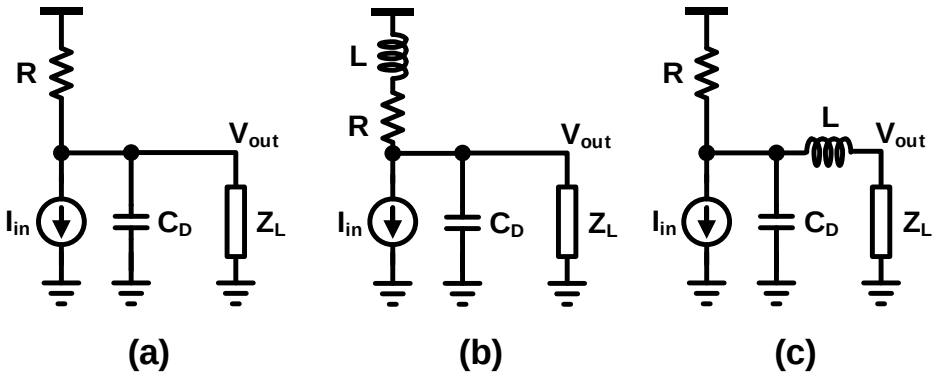


Fig. 2.12 CM driver (a) without inductor (b) with shunt peaking

(c) with series peaking

For shunt peaking, the load capacitance and driver capacitance are merged into one capacitance, namely $C = C_D + C_L$, and the transfer function is derived as follows:

$$Z_{T,cap}(s) = V_{out}/I_{in} = -R \cdot \frac{1 + k_L\left(\frac{s}{\omega_0}\right)}{1 + \frac{s}{\omega_0} + k_L\left(\frac{s}{\omega_0}\right)^2} \tag{2.11}$$

$$Z_{T,term}(s) = -\frac{R}{2} \frac{1 + k_L\left(\frac{s}{\omega_0}\right)}{\left(1 + \frac{(1+k_L)}{2}\left(\frac{s}{\omega_0}\right) + \frac{k_L}{2}\left(\frac{s}{\omega_0}\right)^2\right)} \tag{2.12}$$

where $\omega_0 = 1/RC$, which is 3-dB bandwidth without the inductor and termination resistor and $k_L = L/R^2C$. As seen (2.11) and (2.12), the shunt peaking extends the bandwidth by adding zero at R/L. In other words, the current insertion to the induc-

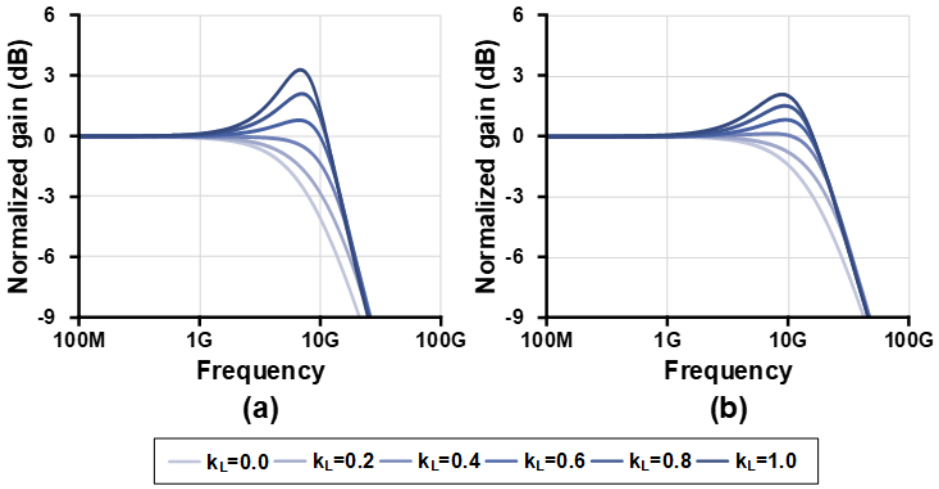


Fig. 2.13 Gain magnitude response with shunt peaking

(a) for capacitive load (b) for terminated load

tor is delayed by the induced voltage. Thereby the driven current charges the load firstly. The normalized gain magnitude responses for some examples of shunt inductors are shown in Fig. 2.13. The circuit elements *R*, *C* are set to 50 and 400 fF to have the bandwidth at 8 GHz and 16 GHz for capacitive and terminated load, respectively.

As the inductance rise, zero at *R/L* and low damping factor produce over-peaking, widening the 3-dB bandwidth. However, for wide-band operation, the over-peaking that affects ISI should be refrained. Phase delay analysis is functional than time-consuming transient simulation to estimate the optimum inductance for the minimum ISI [2.21]. Since the power spectral density of N-bit, f_d data rate PRBS pattern under f_d is a set of impulses at every $f_d/(2^N-1)$ in an envelopment of $1/f_d$ period $sinc^2$ function, the measurement range for phase delay is under f_d. Fig. 2.14 shows the

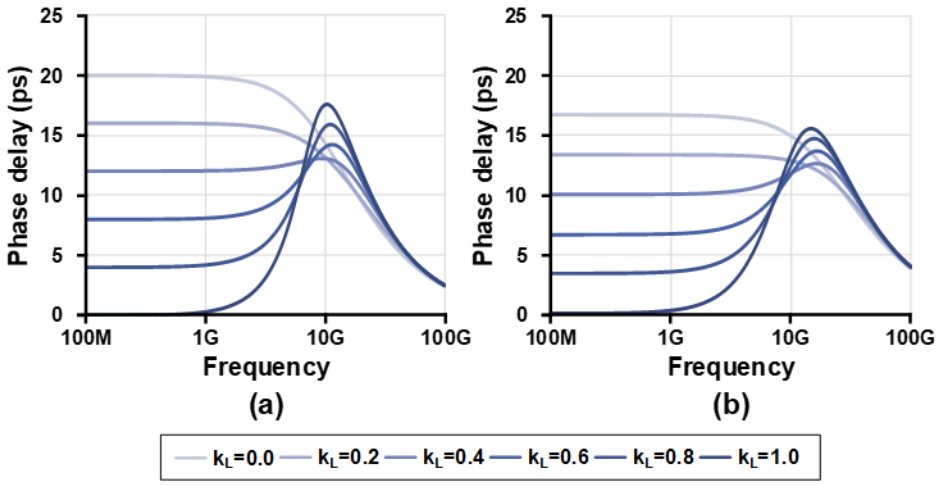


Fig. 2.14 Phase delay response with shunt peaking

(a) for capacitive load (b) for terminated load

simulation result of phase delay. The phase delay deviation among the interest frequency range is minimized around k_L = 0.4. Meanwhile, the 3-dB bandwidth maximization condition is separate from the ISI minimization condition. The bandwidth extension ratio (BWER) is maximized to 1.84 when $k_L = (\sqrt{2}/2)$ and maximally flat gain with BWER = 1.72 is achieved when $k_L = (\sqrt{2} - 1)$ for capacitive load [2.17]. The eye diagram comparison of the maximum bandwidth and minimum ISI is shown in Fig. 2.15. The 3-dB bandwidth maximization condition differs from the ISI minimizing condition, unlike the maximally flat one. The phase delay characteristic gently varies for the flat condition compared to others since the complex pole and zero compensate each other.

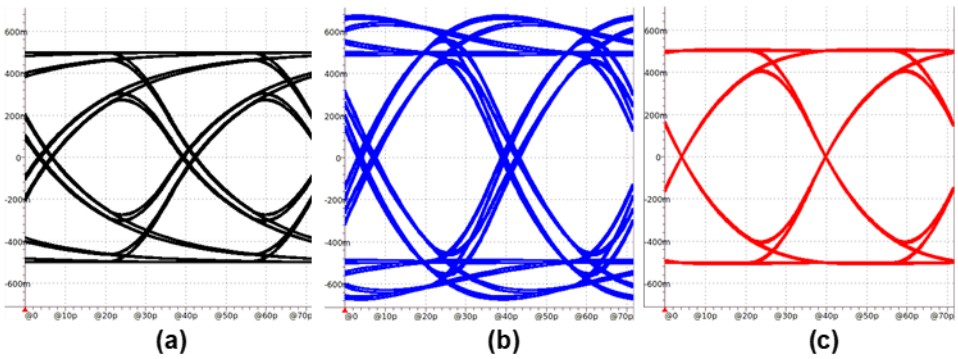


Fig. 2.15 28 Gb/s eye diagram for shunt peaking and capacitive load
(a) without inductor (b) maximum 3-dB bandwidth (c) minimum ISI

The transfer function is more difficult to analyze for series peaking in Fig. 2.12(c) due to increased denominator order. For simplicity, $k_C = C_D/(C_D+C_L)$ are introduced. The transfer function is derived as (2.13) and (2.14).

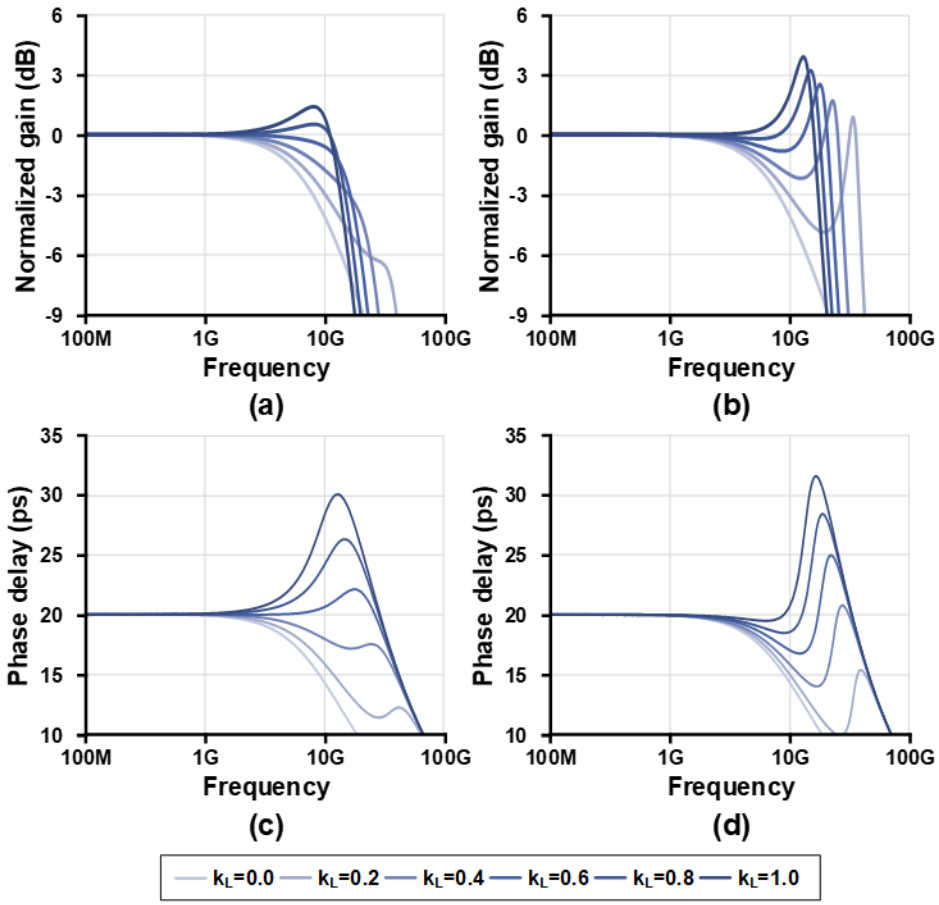


Fig. 2.16 AC response with series peaking for capacitive load.

Normalized gain magnitude for (a) $k_C = 0.25$ and (b) $k_C = 0.5$

Phase delay for (c) $k_C = 0.25$ and (d) $k_C = 0.5$

$$Z_{T,cap}(s) = \frac{-R}{1 + \frac{s}{\omega_0} + k_L(1-k_C)\left(\frac{s}{\omega_0}\right)^2 + k_L k_C(1-k_C)\left(\frac{s}{\omega_0}\right)^3} \quad (2.13)$$

$$Z_{T,term}(s) = \frac{-R/2}{1 + \frac{(1+k_L)}{2}\frac{s}{\omega_0} + \frac{k_L}{2}\left(\frac{s}{\omega_0}\right)^2 + \frac{k_L k_C(1-k_C)}{2}\left(\frac{s}{\omega_0}\right)^3} \quad (2.14)$$

The 3rd order transfer function can have a ripple in its magnitude response due to the coexistence of real pole and complex pole. The peaking from the under-damping term helps the extension of the bandwidth. The maximum 3-dB bandwidth when k_C = 0.5 is wider than the case of k_C = 0.25 as shown in Fig. 2.16(a) and (b). However, it also harms the phase delay characteristic, as shown in Fig. 2.16(c) and (d). Same as the shunt peaking, the inductance should be selected near the condition of maximally flat rather than maximum bandwidth. The eye diagrams of the ISI minimizing

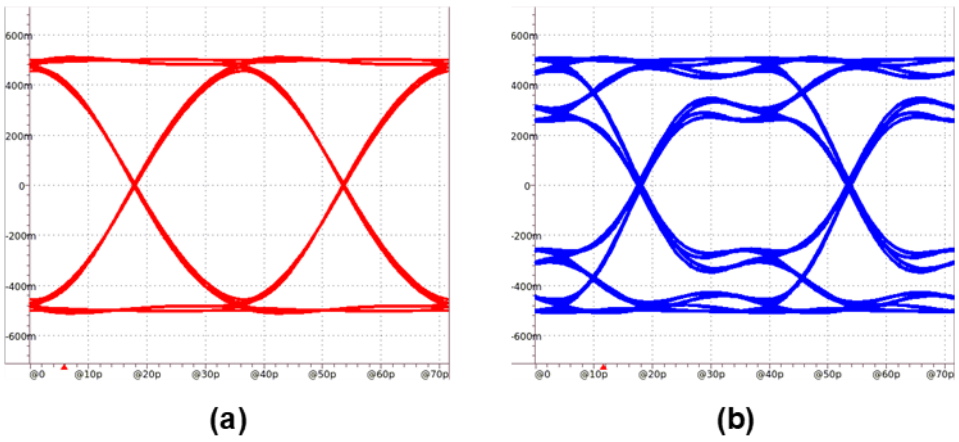


Fig. 2.17 28 Gb/s eye diagram for series peaking and capacitive load. k_L is set for minimum ISI. (a) k_C = 0.25 and k_L = 0.5 (b) k_C = 0.5 and k_L = 0.2

condition are shown in Fig. 2.17 for the case of k_C = 0.25 and k_C = 0.5. The eye diagram is clearly open for the low driver capacitance case, whereas a closed and uneven diagram is achieved for the high-k_C case. This trapezoidal and ringing eye diagram occurs by high-frequency peaking that produces the 3rd order harmonic term. Since this eye distortion is inevitable, the driver output capacitance should be reduced as much as possible.

The output characteristic is much better for the terminated load in Fig. 2.18 due to the higher damping factor. The over-peaking at the high-order harmonic band is reduced, resulting from low phase delay deviation. In this case, the circuit designer chooses the inductance considering the trade-off among fast transition, ringing, ISI, and eye height. Examples of the inductance choice are simulated in Fig. 2.19. The wrong choice of inductance could induce excessive ringing, closed eye height by trapezoidal waveform and closed eye width by phase delay deviation.

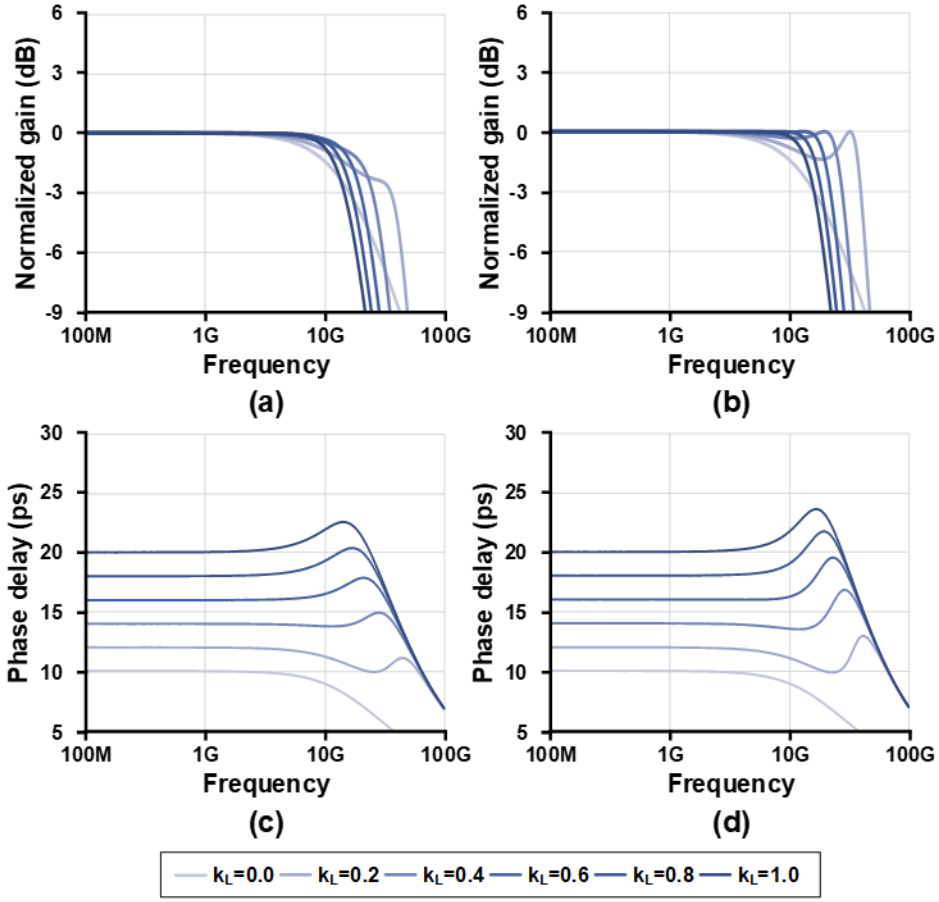


Fig. 2.18 AC response with series peaking for terminated load.

Normalized gain magnitude for (a) k_C = 0.25 and (b) k_C = 0.5

Phase delay for (a) k_C = 0.25 and (b) k_C = 0.5

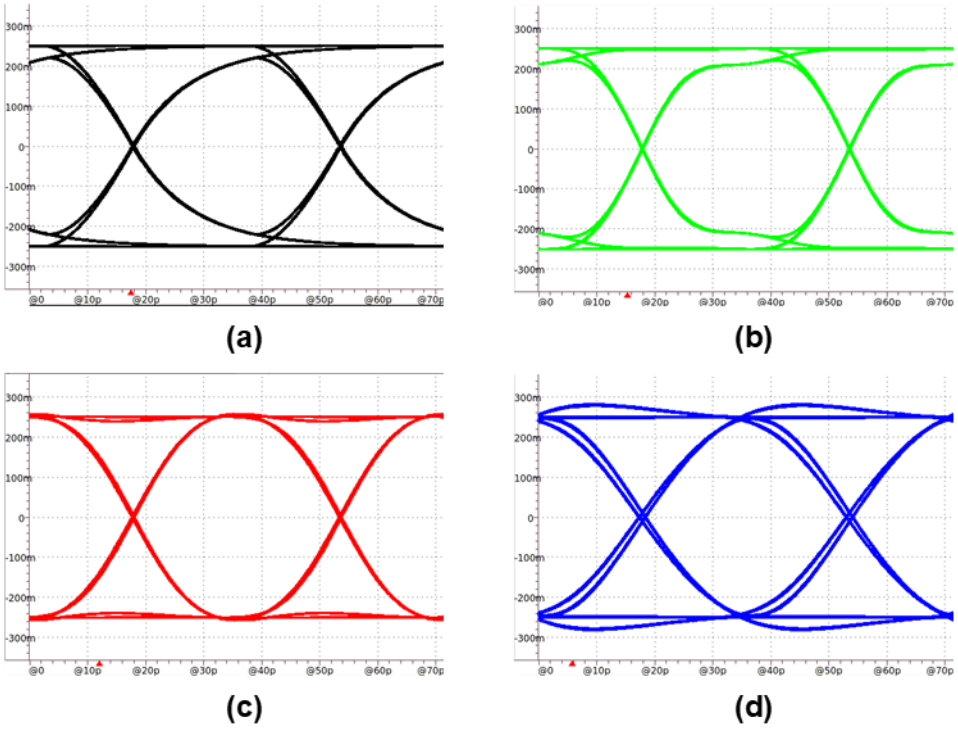


Fig. 2.19 28 Gb/s eye diagram for series peaking and terminated load. k_C = 0.25.

(a) Without inductor (b) k_L = 0.15. (c) k_L = 0.35 (d) k_L = 0.8

2.4.4 T-coil

The bandwidth extension analysis of T-coil was treated as a trade secret by Tektronix engineers for many years. However, it is used in various applications in wireline interface systems today [2.17],[2.20],[2.22]-[2.30]. It is known to be able to extend bandwidth wider than inductive peaking if appropriately analyzed. The circuit expression of T-coil is illustrated in Fig. 2.20, where $L_1 = L, L_2 = bL$, and $m = k_m\sqrt{L_1L_2}/L = k_m\sqrt{b}$. The equivalent impedance after Y-Δ conversion is expressed as follows.

$$Z_1 = \frac{s(1+m)L}{1+s^2(1+b+2m)LC_B}$$

$$Z_2 = \frac{s(b+m)L}{1+s^2(1+b+2m)LC_B}$$

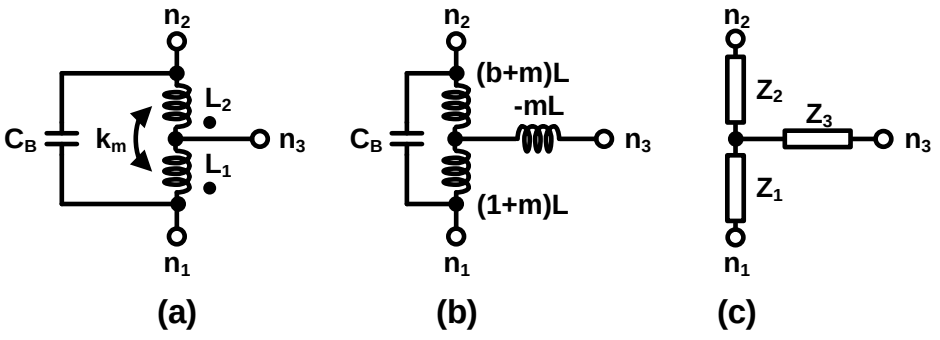


Fig. 2.20 Equivalent circuit expression of T-coil (a) basic expression (b) equivalent expression (c) Y-Δ conversed expression

$$Z_3 = \frac{s(1+b+2m)L}{1+s^2(1+b+2m)LC_B} - smL \tag{2.15}$$

The placement of T-coil is classified into two categories, the same as the placement of the inductor. The first method uses the middle node, n_3, as an output node, as shown in Fig. 2.21. For convenience, this placement of T-coil is called shunt T-coil in this chapter. For simplicity, assume the driver capacitance, C_D, is ignored and the load impedance is capacitive, *1/sC*. Then, the transimpedance Z_T is derived as follows [2.25]:

$$Z_T(s) = -R\frac{N(s)}{D(s)}$$

$$N(s) = 1 + k_L(b+m)\left(\frac{s}{\omega_0}\right) + k_B k_L(1+b+2m)\left(\frac{s}{\omega_0}\right)^2$$

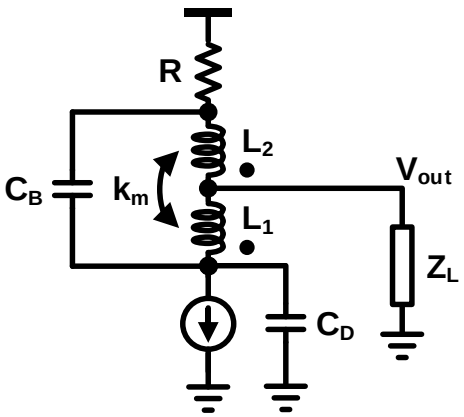


Fig. 2.21 T-coil shunt placement for current mode driver

$$D(s) = 1 + \left(\frac{s}{\omega_0}\right) + k_L\left(b + k_B(1 + b + 2m)\right)\left(\frac{s}{\omega_0}\right)^2 + k_B k_L(1 + b + 2m)\left(\frac{s}{\omega_0}\right)^3 + k_B k_L^2(b - m^2)\left(\frac{s}{\omega_0}\right)^4 \quad (2.16)$$

where $k_B = C_B/C, k_L = L/R^2C,$ and $\omega_0 = 1/RC$. The exact transfer function considering C_D is expressed to 5th order, however not written for few analytic meanings. As mentioned in the previous sub-chapter, the coexistence of multiple poles and zeros degrades the ISI performance regardless of bandwidth. The transfer function becomes more suitable for a wide-band application and easy to handle if this 5th order transimpedance equation is reduced to 3rd order. By the following condition (2.17), the transimpedance can be written as:

$$k_B = \frac{(b - m^2)(1 - k_C)}{(1 + b + 2m)^2}$$
$$k_L = \frac{(1 + m)(1 - k_C)}{(b + m)(1 + b + 2m)} \quad (2.17)$$

k_m	b	m	k_B	k_L	BWER
0.3	1.05	0.31	0.13	0.36	2.78
0.4	0.90	0.38	0.11	0.41	2.94
0.5	0.73	0.43	0.08	0.17	3.15
0.6	0.57	0.45	0.06	0.58	3.43

Table 2.1 Example of design parameter for shunt T-coil and capacitive load

$$Z_T(s) = -R\frac{1}{1 + p\left(\frac{s}{\omega_0}\right) + q\left(\frac{s}{\omega_0}\right)^2 + r\left(\frac{s}{\omega_0}\right)^3}$$

$$\text{where } p = 1 - (b+m)k_L,$$
$$q = k_L(-m + (1+2m)k_C + (b+m)^2 k_L),$$
$$\text{and } r = \frac{(b-m^2)(1-k_C)k_C k_L}{(1+b+2m)} \tag{2.18}$$

where $C_D = k_C C$ and $Z_L = 1/s(1-k_C)C$. When k_C=0, in the same word, ignoring driver capacitance, the transimpedance is expressed in 2nd order as follows.

$$Z_T(s) = -R\frac{1}{1 + 2\zeta\left(\frac{s}{\omega_n}\right) + \left(\frac{s}{\omega_n}\right)^2}$$

$$\text{where } \omega_n = (1+b+2m)\sqrt{\frac{b+m}{(1+m)(b-m^2)}}\omega_0$$
$$\text{and } \zeta = \frac{1}{2}\sqrt{\frac{(b+m)^3}{(1+m)(b-m^2)}} \tag{2.19}$$

Though the minimum ISI condition should be found with the phase delay analysis, the maximally flat gain condition, which is equivalent with $\zeta = 1/\sqrt{2}$, is analyzed for its similarity. Table 2.1 shows some reasonable design parameters and BWER for shunt T-coil with maximally flat gain. Since the 3rd order transimpedance equation (2.18) is generally not factorized, the T-coil design is accompanied by a numerical method for a given circuit environment such as R, C, and k_C.

The same methodology is adopted for terminated load, $R||1/s(1-k_C)C$. The 3rd order reducing condition, transimpedance, and design parameters at the maximally flat condition for k_C = 0 are expressed in (2.20) to (2.22) and Table 2.2.

$$k_B = \frac{(b-m^2)(1-k_C)}{(1+b+2m)(2+b+3m)}$$

$$k_L = \frac{(1+m)(1-k_C)}{(b+2m)(1+b+2m)} \tag{2.20}$$

$$Z_T(s) = -R\frac{1}{2+p\left(\frac{s}{\omega_0}\right)+q\left(\frac{s}{\omega_0}\right)^2+r\left(\frac{s}{\omega_0}\right)^3}$$

$$where\ \ p = 1-(b+2m)k_L,$$

$$q = k_L(-m+(2+2m)k_C+(b+m)(b+2m)k_L),$$

$$and\ \ r = \frac{(b-m^2)(1-k_C)k_Ck_L}{(1+b+2m)} \tag{2.21}$$

$$k_C = 0:\ \ Z_T(s) = -\frac{R}{2}\frac{1}{1+2\zeta\left(\frac{s}{\omega_n}\right)+\left(\frac{s}{\omega_n}\right)^2}$$

$$where\ \ \omega_n = (1+b+2m)\sqrt{\frac{b+2m}{(1+m)(b-m^2)}}\omega_0$$

$$and\ \ \zeta = \frac{1}{4}\sqrt{\frac{(b+m)^2(b+2m)}{(1+m)(b-m^2)}} \tag{2.22}$$

The T-coil can also be employed for the cancellation of ESD capacitance at the

k_m	b	m	k_B	k_L	BWER
0.3	2.30	0.46	0.09	0.11	2.16
0.4	2.03	0.57	0.07	0.12	2.27
0.5	1.72	0.66	0.06	0.14	2.40
0.6	1.37	0.7	0.04	0.16	2.57

Table 2.2 Example of design parameter for shunt T-coil and terminated load

output pad. The ESD diode with large capacitance is placed at a middle node, n_3, and the driver is placed at the same node or the opposite node to output pad, n_1, as described in Fig. 2.22. For convenience, this placement of T-coil is called series T-coil in this chapter. The series T-coil is utilized for optimization of return-loss by hiding the large capacitance. Firstly, the case of Fig. 2.22(a) is discussed. The load Z_L is $R||\frac{1}{s(1-k_C)C}$ and C_{ESD}+C_D is expressed to k_CC. In this formation, the output impedance Z_{OUT} is described as follows.

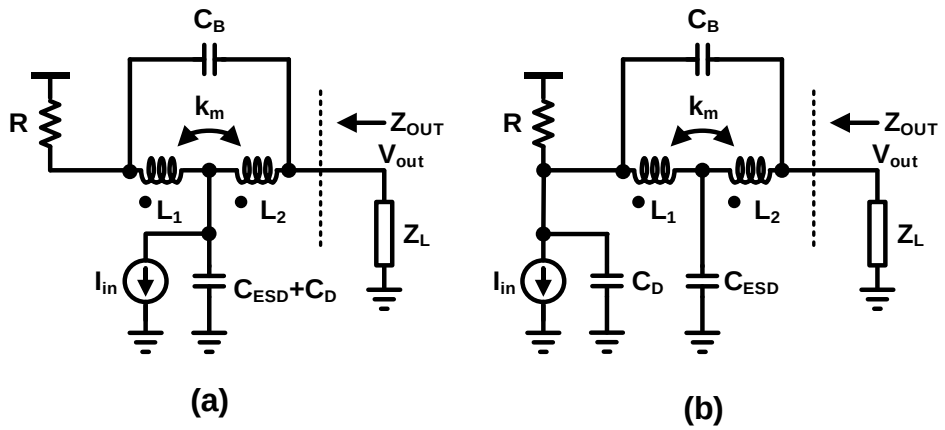


Fig. 2.22 T-coil series placement for ESD capacitor cancellation

(a) driver at n_3 (b) driver at n_1

$$Z_{OUT}(s) = R\frac{N_{ZOUT}(s)}{D_{ZOUT}(s)}$$

$$N_{ZOUT}(s) = 1 + (1+b+2m)k_L\left(\frac{s}{\omega_0}\right) + \left((1+b+2m)k_B + bk_C\right)k_L\left(\frac{s}{\omega_0}\right)^2 + (b-m^2)k_Ck_L^2\left(\frac{s}{\omega_0}\right)^3 + (b-m^2)k_Bk_Ck_L^2\left(\frac{s}{\omega_0}\right)^4$$

$$D_{ZOUT}(s) = 1 + k_C\left(\frac{s}{\omega_0}\right) + \left((1+b+2m)k_B + k_C\right)k_L\left(\frac{s}{\omega_0}\right)^2 + (1+b+2m)k_Bk_Ck_L\left(\frac{s}{\omega_0}\right)^3 + (b-m^2)k_Bk_Ck_L^2\left(\frac{s}{\omega_0}\right)^4 \quad (2.23)$$

Note that, with the design parameter of (2.24), the output impedance Z_{OUT} is perfectly matched to R in a universal frequency range.

$$b = 1$$
$$k_B = \frac{(1-m)}{4(1+m)}k_C$$
$$k_L = \frac{k_C}{2(1+m)} \quad (2.24)$$

In this case, the transimpedance is reduced to 3rd order without zero as (2.25).

$$Z_T(s) = -\frac{R}{2}\frac{1}{\left(1+\frac{1-k_C}{2}\left(\frac{s}{\omega_0}\right)\right)\left(1+\frac{k_C}{2}\left(\frac{s}{\omega_0}\right)+\frac{1-m}{4(1+m)}k_C^2\left(\frac{s}{\omega_0}\right)^2\right)} \quad (2.25)$$

For a given k_C, the circuit designer can choose k_m, considering the trade-off between output bandwidth and the ISI. There are some examples of output eye diagrams in Fig. 2.23. The overall capacitance C is set to 600 fF in this case.

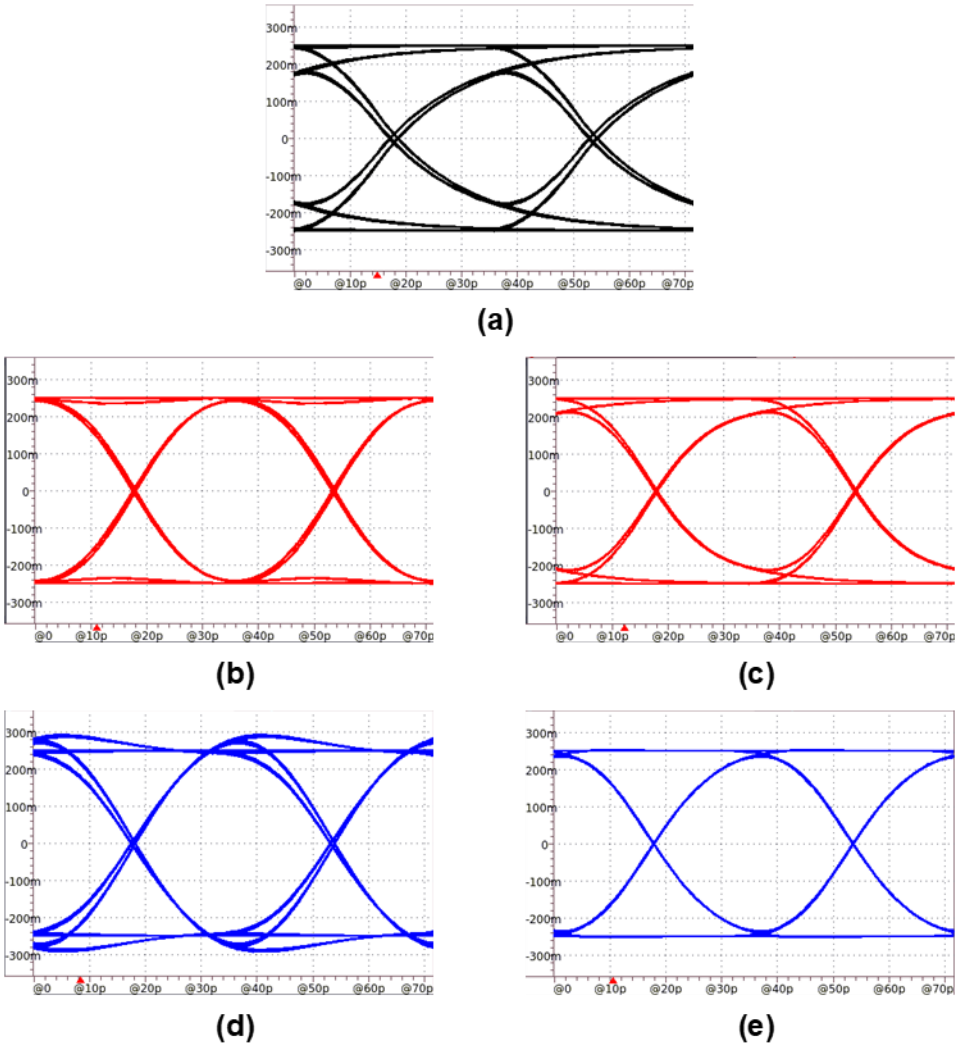


Fig. 2.23 28 Gb/s eye diagram for middle node driving series T-coil.

(a) without T-coil (b) k_C = 0.3 and k_m = -0.2 (c) k_C = 0.3 and k_m = 0.2

(d) k_C = 0.6 and k_m = 0.1 (e) k_C = 0.6 and k_m = 0.4

Meanwhile, the general formulas for transfer function and output impedance of Fig. 2.22(b) are complicated without any assumptions. Therefore, the driver capacitance C_D is ignored at first for simplicity. By definition of $C_{ESD} = k_E C$, the return-loss optimization condition is the same as the previous one (2.24). The transfer function Z_T is expressed as follows at that condition.

$$Z_T(s) = -\frac{R}{2}\frac{1}{1+\frac{1-k_E}{2}\left(\frac{s}{\omega_0}\right)}\frac{1-\frac{k_E}{2}\left(\frac{s}{\omega_0}\right)+\frac{1-m}{4(1+m)}k_E^2\left(\frac{s}{\omega_0}\right)^2}{1+\frac{k_E}{2}\left(\frac{s}{\omega_0}\right)+\frac{1-m}{4(1+m)}k_E^2\left(\frac{s}{\omega_0}\right)^2} \tag{2.26}$$

The first term corresponds to a pole from output load capacitance. The second term is the all-pass 2nd order function. Thereby the output bandwidth is determined by only output load capacitance. However, the phase delay characteristic is not always suitable for wide-band applications. Therefore, though an all-pass term is in the transfer function, the design of series T-coil should be accomplished carefully. Some examples of the simulation with series T-coils are shown in Fig. 2.24. In this case, the driver capacitance, C_D, is set to 100 fF considering the realistic circuit environment. The ESD capacitance C_{ESD} is set to $k_E C$, and the load capacitance is set to $(1-k_E)C$, where C = 500 fF.

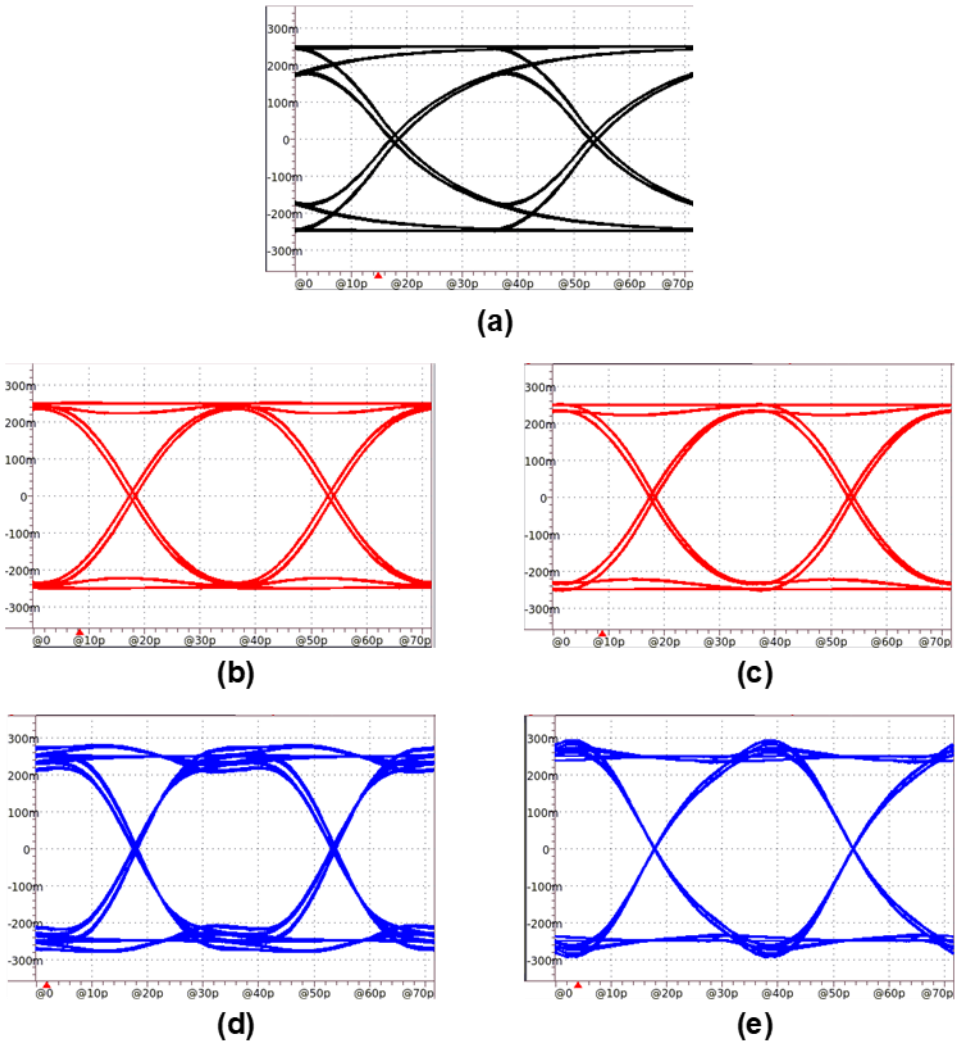


Fig. 2.24 28 Gb/s eye diagram for opposite node driving series T-coil.

(a) without T-coil (b) k_E = 0.3 and k_m = 0.3 (c) k_E = 0.3 and k_m = 0.6

(d) k_E = 0.6 and k_m = 0.3 (e) k_E = 0.6 and k_m = 0.6

Chapter 3

Design of 48 Gb/s PAM-4 Electrical Transmitter in 65 nm CMOS

3.1 Overview

A power-hungry equalization scheme such as a feed-forward equalizer (FFE) is required to compensate for high channel loss. Typical FFEs exploit flip-flops or latches to generate 1-UI taps that consume significant power due to clock distribution. This type of power consumption has been a dominant factor in power usage as the data rate increases. This type of power consumption has been a dominant factor in power usage as the data rate increases. It can even reach up to 50 % of the overall chip power consumption [3.1].

Alternatively, employing a passive delay line rather than flip-flops or latches is another option for power reduction. In [3.2], both active and passive delay paths generate FFE taps for an accurate delay and consume lower power for delay ele-

ments. Transmitters using only passive delay lines are also presented, which use an LC-ladder filter [3.3] and a transmission line in SiGe BiCMOS technology [3.4]. As the data rate increases, the required area of the passive delay element becomes lower, becoming a favorable option.

Furthermore, using passive delay elements for FFE tap generation has another advantage in the system configuration [3.3]. Fig. 3.1 compares the structure of the

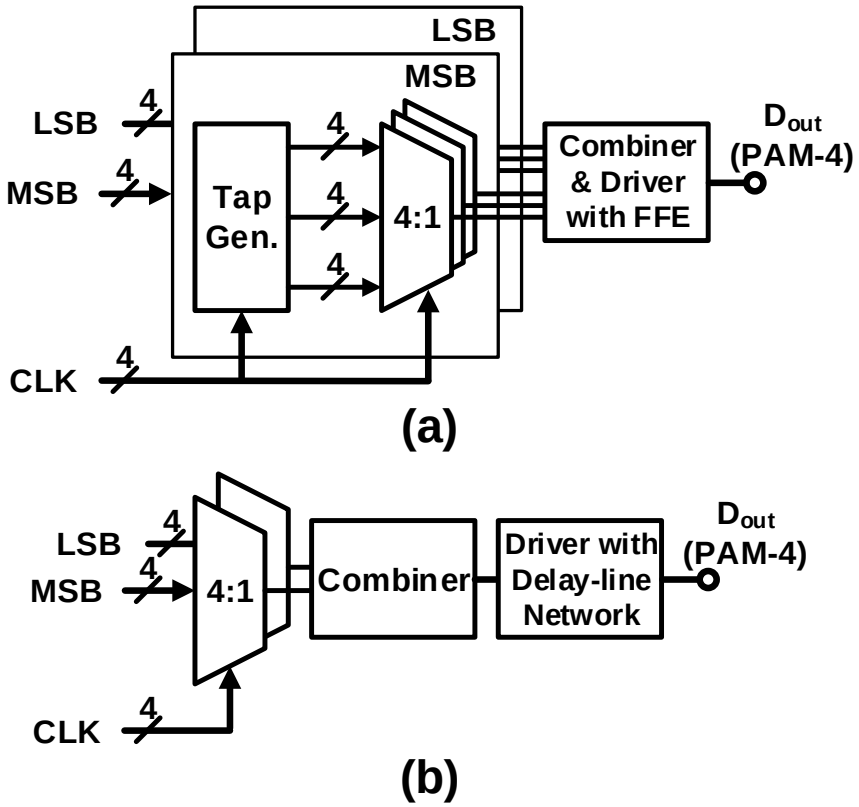


Fig. 3.1 Block diagrams of quarter-rate PAM-4 transmitter with 3-tap FFE. (a) Clock-based tap generating system. (b) Passive-delay-line-based tap generating system.

clock-based and passive-delay-line-based quarter-rate transmitter with a 3-tap FFE. In Fig. 3.1(a), the number of power-hungry multiplexer (MUX) pairs is the same as FFE taps. To make matters worse, as the data rate is raised, the required number of taps also increases, and the MUX consumes high power. On the other hand, unlike an active delay element, a passive element incurs less power consumption. Thus, FFE taps can be increased without consuming higher power, as shown in Fig. 3.1(b). Also, it is hard to employ the structure of Fig. 3.1 (b) to clock-based tap generating system because high-speed data after 4:1 MUX is difficult to be regenerated by clocked elements.

This chapter is organized as follows. First, we present the design of the proposed FFE with a double-shielded coplanar waveguide (DS-CPW) [3.5]. Next, the design consideration on the 4:1 multiplexer is followed. Then, the overall architecture of the 48 Gb/s PAM-4 transmitter with the FFE is described. Lastly, we discuss the measurement results of the implemented transmitter.

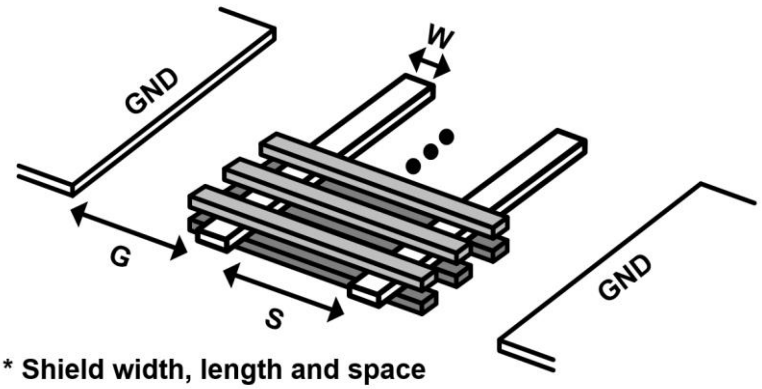
3.2 FFE Based on Double-Shielded Coplanar Waveguide

3.2.1 Basic Concept

Unlike an active delay line, a passive delay line requires physical area between each tap. Since a longer delay needs a larger size, an area reduction scheme is inevitable to lay the overall system out in a good chip area. The proposed FFE exploits three approaches. Firstly, the area efficiency is enhanced by adopting a slow-wave transmission line as a delay element. Significantly, the shielded coplanar waveguide(S-CPW) has been widely used to achieve a considerable reduction in wavelength on RF applications. In [3.6], the S-CPW technique is also applied in a bulk CMOS process with a high-quality factor owing to a narrow metal strip. Secondly, the delay line is split into the input and the driver's output, as shown in Fig. 3.1(b). It is similar to a distributed amplifier using transmission lines on both input and output. The FFE driver has an output node on the same side as the input node. By this separation, the total length of the FFE is halved. Lastly, a sub-UI interval tap is used in this work to shorten the entire run length. Applying the sub-UI tap has advantages not only in area occupation but also in equalizer performance. Since 1-UI tap FFE boosts the Nyquist frequency gain, the compensation frequency range is narrow under low channel bandwidth circumstances. In that case, fractionally-spaced FFE can be effective for bandwidth increasing despite lower equalization gain.

3.2.2 Proposed Double-Shielded Coplanar Waveguide

The structure of the differential DS-CPW proposed in this work is shown in Fig. 3.2. M7 and M5 are utilized as floating metal shields instead of the top metal to obtain a large slow-wave factor due to higher unit length capacitance. The slow-wave factor, S-parameters, and characteristic impedance (Z_0) are simulated by sweeping each physical dimensions in a 3-D electromagnetic simulator. The width of the signal metal, W, is set wide enough to ensure a high slow-wave factor defined as the ratio of the speed of light and the EM-wave in the waveguide. The metal density for the shield is maximized for the same reason, but the duty cycle of the shield *(SW / (SW + SS))* is set as 50 % to minimize conductive loss and eddy current loss [3.7].



Parameters	W	G	S	SW	SL	SS
Value	4 μm	40 μm	20 μm	0.1 μm	38 μm	0.1 μm

Fig. 3.2 Proposed differential double-shielded coplanar waveguide.

Since the slow-wave factor and Z_0 have a trade-off relation with W, optimal W is found as 4 µm. Also, the signal metal space, S, is set to 20 µm to obtain enough inductance per unit length.

The simulation results of these RF characteristics are shown in Fig. 3.3. The slow-wave factor increases by 45% as a single metal shield is placed to a non-shielded CPW. When both metal shields are applied, the slow-wave factor becomes 91% larger than the non-shielded waveguide, which means a 52% reduction in the run-length. Each transmission line runs either 220 µm or 250 µm, to achieve a consistent group delay of 12.5 ps with a different slow-wave factor for different types of terminations. In Fig. 3.3(c), Z_0 decreases significantly with the metal shield due to added capacitance between two signal lines. Decreased Z_0 requires low termination resistance, which incurs more significant power consumption. However, overall power consumption is reduced by the passive delay element. The insertion loss is also degraded by more than 0.01 dB per 10 µm at 20 GHz. However, the total insertion loss of full-length double-shielded line is not significant to deteriorate the driver's performance.

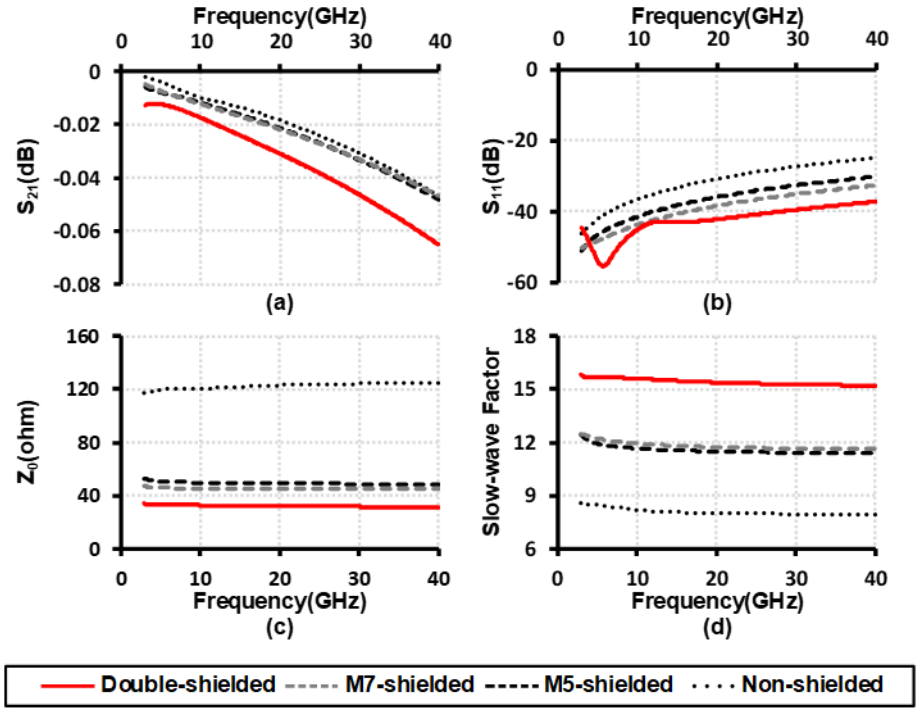


Fig. 3.3 3-D EM simulation results of frequency characteristics of 10 μm length coplanar waveguides. (a) Insertion loss S_{21}. (b) Return loss S_{11}. (c) Differential characteristic impedance Z_0. (d) Slow-wave factor.

3.3 Design Consideration on 4:1 MUX

Before the output driver, the 4:1 MUX operates at the highest data rate in the overall system. To avoid interference from floating nodes, 1-UI pulse generators are used with a current-mode MUX [3.8] and a voltage-mode MUX [3.9]. In [3.1], for compensation of using 3-stacked transistors for 1-UI pulse generation, additional transistors are used to remove floating nodes. However, a 1-UI pulse generator is hard to design with devices with limited bandwidth. This work employs the 2-UI pulse generator with a 2-stacked CML-based structure to compensate for this problem, as shown in Fig. 3.4 [3.10]. The details of the operation in the 2-UI pulse generator and 4:1 MUX are illustrated in Fig. 3.5. First, the data signal D_I is retimed by the quadrature clock CLK_I and converted to 2-UI-wide RZ data, M_I. Another quadrature clock CLK_Q passes the buffer to be delayed clock signal Φ_Q. Then, M_I is over-

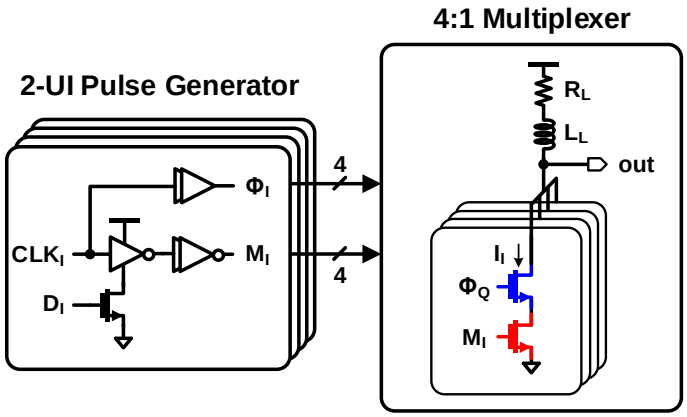


Fig. 3.4 Schematics of 4:1 MUX with 2-UI pulse generator.

lapped with Φ_Q to produce 1-UI current pulse, I_I. Other current pulses are generated with corresponding data and clocks to make the multiplexed output.

In this implementation, there are four cases of input configuration for the 4:1 MUX; the 2-UI data signal *M* is applied to upper transistor or lower one, and the input of the upper transistor rises first or later than the input of lower one. Fig. 3.6 shows 4:1 MUX output for these cases. When the input of upper transistor leads the input of lower ones, the ISI of output is significantly worsened as can be seen in Fig. 3.6(c) and (d). In the case of Fig. 3.6(c) and (d), if the output is sequential '1', stored charge at the floating node produce down-ripple. If the output is sequential '0', the upper transistors turn off earlier than the turning-on of the next lower transistors because of high source voltage, which produces up-ripple. For Fig. 3.6(b), only one upper transistor input falls at the end of '01' pattern which disturbs fully pushing-up whereas there are always two upper transistor inputs rising and falling respectively in the case of Fig. 3.6(a). The case of Fig. 3.6(c) is slightly worse than (d) since the

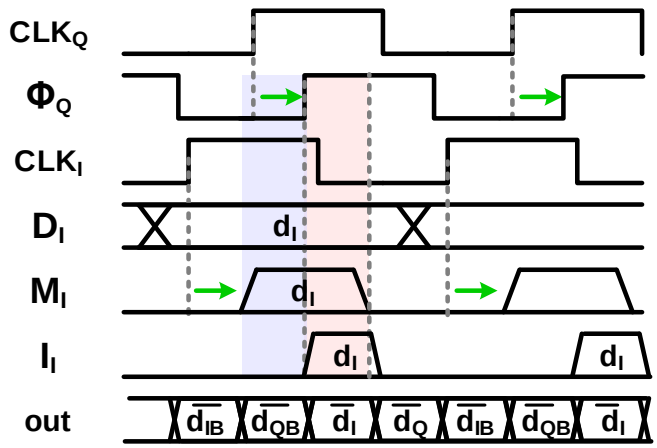
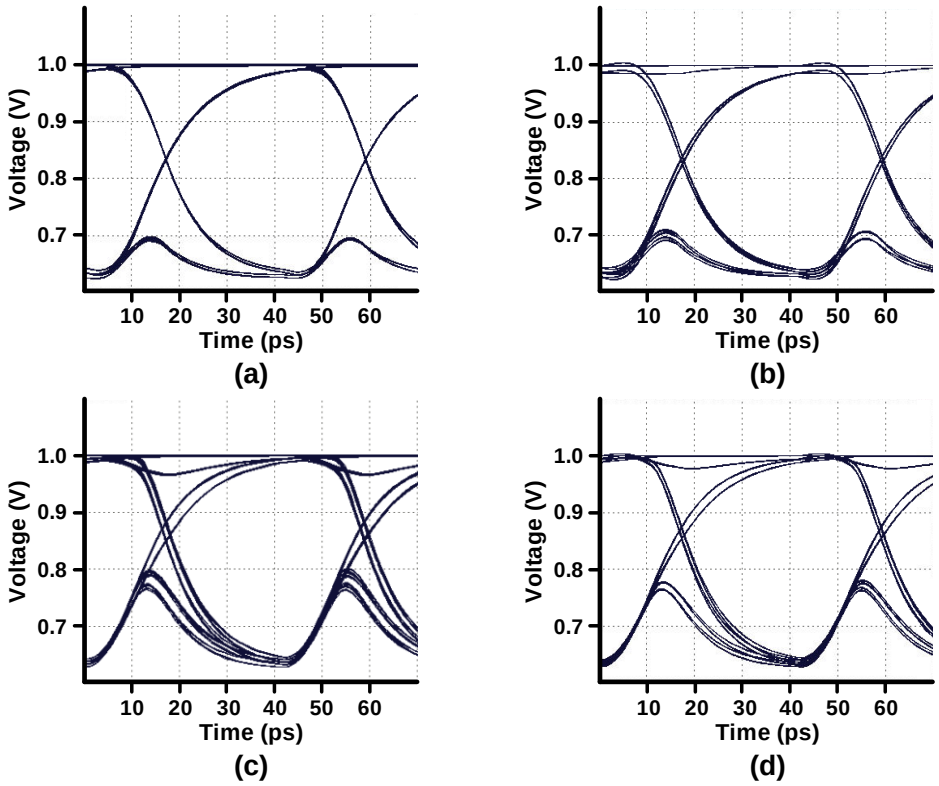


Fig. 3.5 Waveform of 4:1 MUX inputs and output.



	M at lower TR	M at upper TR
Upper TR input rise later	(a)	(b)
Upper TR input rise first	(c)	(d)

Fig. 3.6 Eye diagram of 4:1 serializer according to input configuration.

The case (a) is the same condition with Fig. 3.4.

internal node voltage varies with 4-UI former data.

3.4 Proposed PAM-4 Electrical Transmitter

The overall design of the proposed transmitter system is shown in Fig. 3.7. The data signals after 4:1 MUX are converted to differential rather than single-ended for better SNR. External clock is divided by 2 to operate MSB/LSB PRBS-7 generators and 8:4 serializers. A quadrature clock generator (QCG) based on an active polyphase filter is adopted for the quarter-rate system, as shown in Fig. 3.8. Compared with a passive polyphase filter, the active one has advantages in robustness and frequency range [3.1], [3.11]-[3.14]. Four stages of phase corrector are cascaded in an

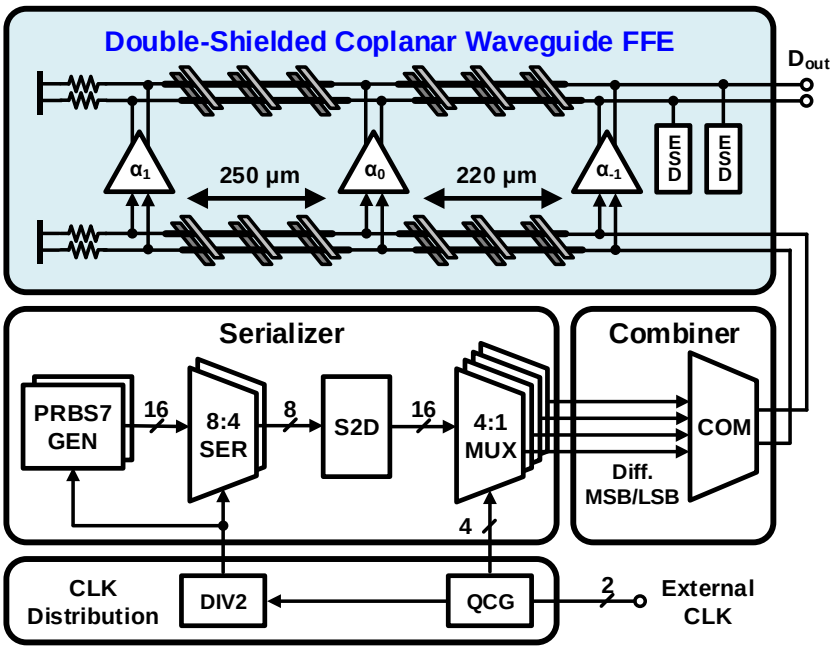


Fig. 3.7 Overall architecture of the proposed PAM-4 transmitter with DS-CPW FFE.

open-loop way to obtain a wide correction range of frequency. The simulated quadrature clock error is shown in Fig. 3.9.

4:1 MUXs shown produce serialized MSB/LSB data with 2 UI-wide data gated

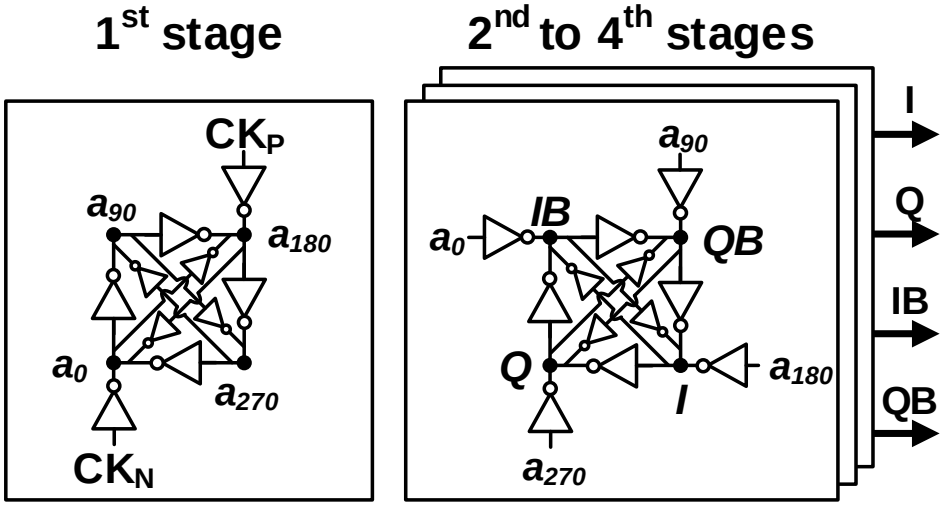


Fig. 3.8 Active polyphase filter based quadrature clock generator.

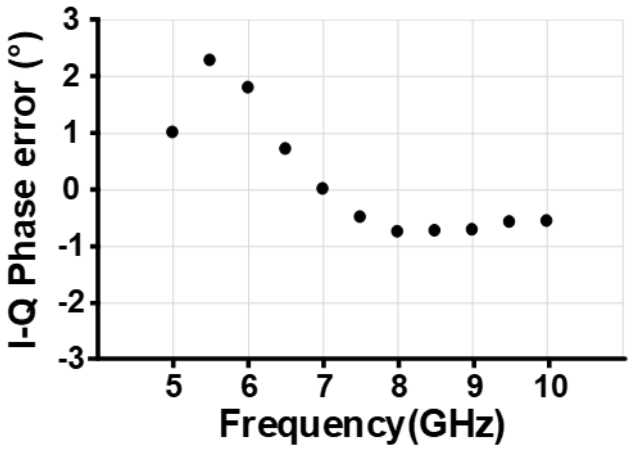


Fig. 3.9 Quadrature phase error of QCG output I-Q

with corresponding quadrature clock. A combiner is composed of parallel current-mode logic (CML) drivers. The current source of the MSB path is about two times larger than that of the LSB path. The current ratio is adjusted for improved level mismatch ratio (R_{LM}) induced by the nonlinearity of the output driver. The modulation type can be changed to NRZ by turning off the LSB current in the combiner. The output driver with FFE is also implemented in CML, and the transmission lines are attached at the drain and gate node. The inner end of the output transmission line is connected to a shunt terminated resistor, and the other end is connected to the output pad with electrostatic discharge (ESD) protection diodes. An external current input controls each tap coefficient. For bandwidth boosting, shunt peaking inductors are used at the 4:1 MUXs, the combiner, and the output node.

The data-dependent jitter (DDJ) results from data modulation and the load condition [3.15]. To verify the robustness of the DS-CPW delay, group delay and jitter variations against the process variation are simulated as illustrated in Fig. 3.10. The

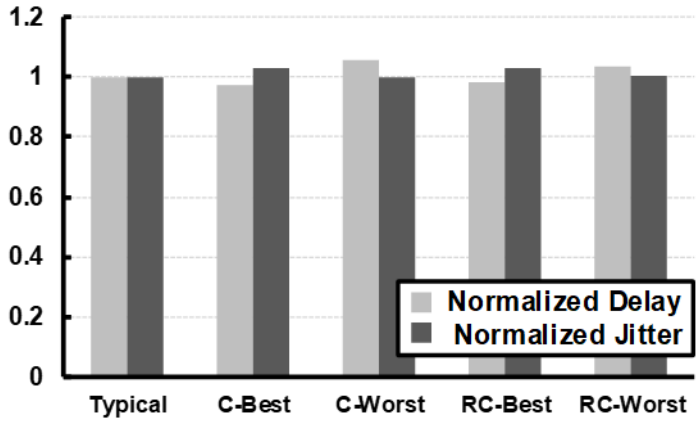


Fig. 3.10 Simulation results of process variation in proposed waveguide.

process corners of the metal and the dielectric layer are classified as C-Best/Worst and RC-Best/Worst according to parasitic capacitance and RC constant. The cases of C-Best and RC-Best exhibit less group delay than the typical case by the lower capacitance. In contrast, the other cases have a longer group delay. The delay variation is from 97% to 105%. On the other hand, since the termination of waveguides is optimized to the typical case, DDJ increases in different corners. For the data rate of PAM-4 48 Gb/s, DDJ increases by 3% in the C-Best case and RC-Best cases.

3.5 Measurement

The proposed PAM-4 transmitter with DS-CPW FFE is fabricated in 1P9M 65 nm CMOS technology. Fig. 3.11 shows a die photomicrograph. The DS-CPW occupies 0.113 mm^2 which corresponds to 74% of the overall area. The test chip is wire-bonded to PCB for verifying the transmitter performance. Fig. 3.12 presents the measurement setup. Anritsu MP1800A signal analyzer inputs a differential clock to the DUT. The transmitter output passes through an FR4 PCB channel, and the eye diagram is observed by Tektronix MSO 73304DX real-time mixed-signal oscilloscope with a P7313SMA differential probe. We used two channels for FFE measurement, which are shown in Fig. 3.13. The insertion losses are measured to 6.5 dB at 10 GHz and 14.8 dB at 12 GHz for channel 1 and 2, respectively. Since the NRZ

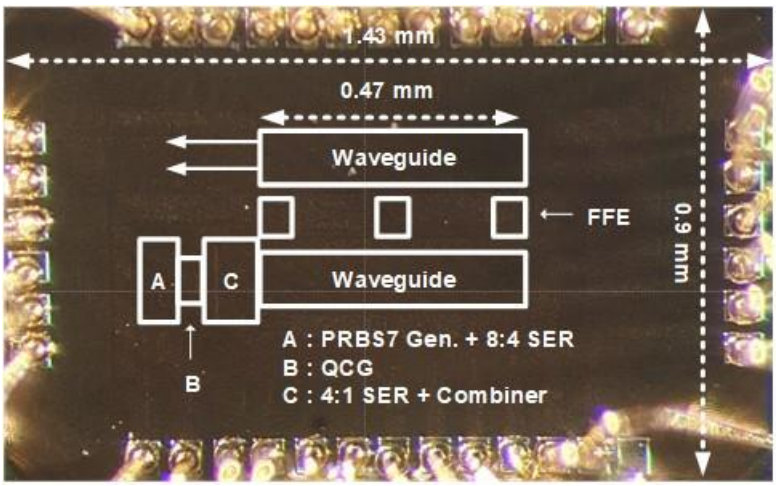


Fig. 3.11 Chip photograph and block description

data is less susceptible to jitter, the output eye diagram is measured with a harsher channel condition.

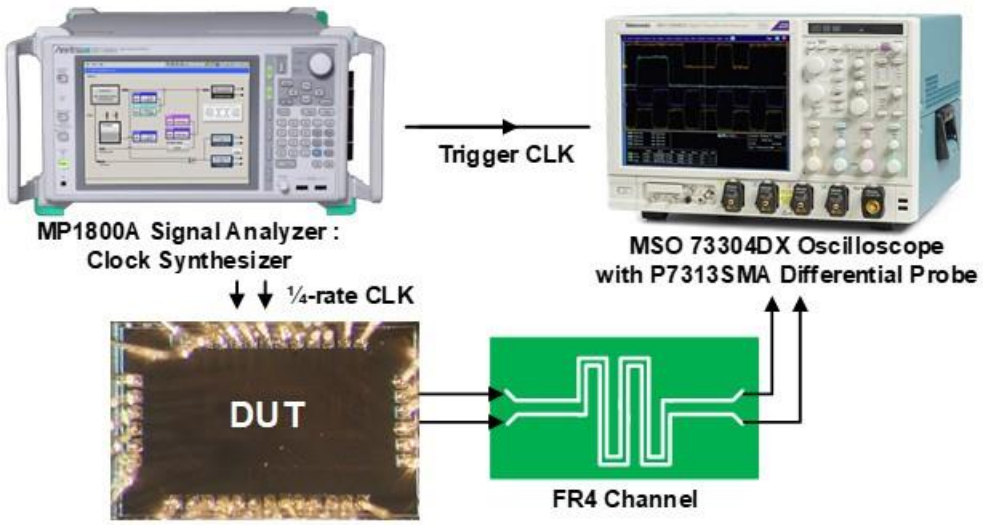


Fig. 3.12 Measurement setup

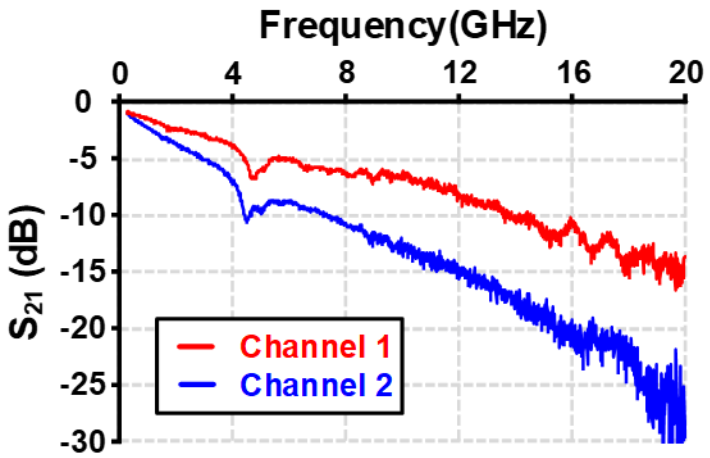


Fig. 3.13 Channel loss measurement

Fig. 3.14 presents PAM-4 eye diagrams for 24 Gb/s and 48 Gb/s measured without applying any de-embedding of the channel. For this measurement, a lossy channel is not added except for the 2 cm PCB trace. No FFE tap coefficient is enabled in this measurement, and the transmitter delivers a peak-to-peak differential output voltage swing of 252 $mV_{pp,diff}$ and 236 $mV_{pp,diff}$. The power efficiency is 3.03 pJ/b at the data rate of 48 Gb/s with PAM-4.

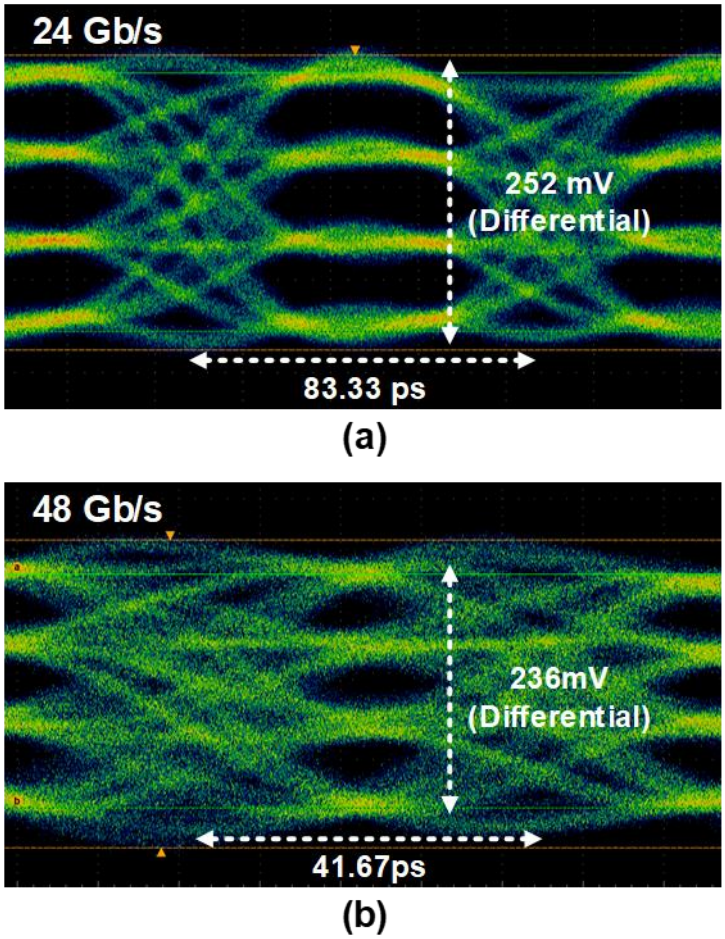


Fig. 3.14 Measured PAM-4 eye diagram without channel (a) 24 Gb/s (b) 48 Gb/s

Fig. 3.15 shows measured PAM-4 48 Gb/s eye diagrams after passing channel 1 without and with FFE. The measured output voltage swing is 105 $mV_{pp,diff}$ with the R_{LM} of 98%. The tap coefficients are (pre, main, post) = (-0.08, 0.8, -0.12). The measured NRZ 24 Gb/s eye diagram with channel 2 is shown in Fig. 3.16. The tap coefficients are (pre, main, post) = (-0.09, 0.57, -0.34). The power breakdown for 48

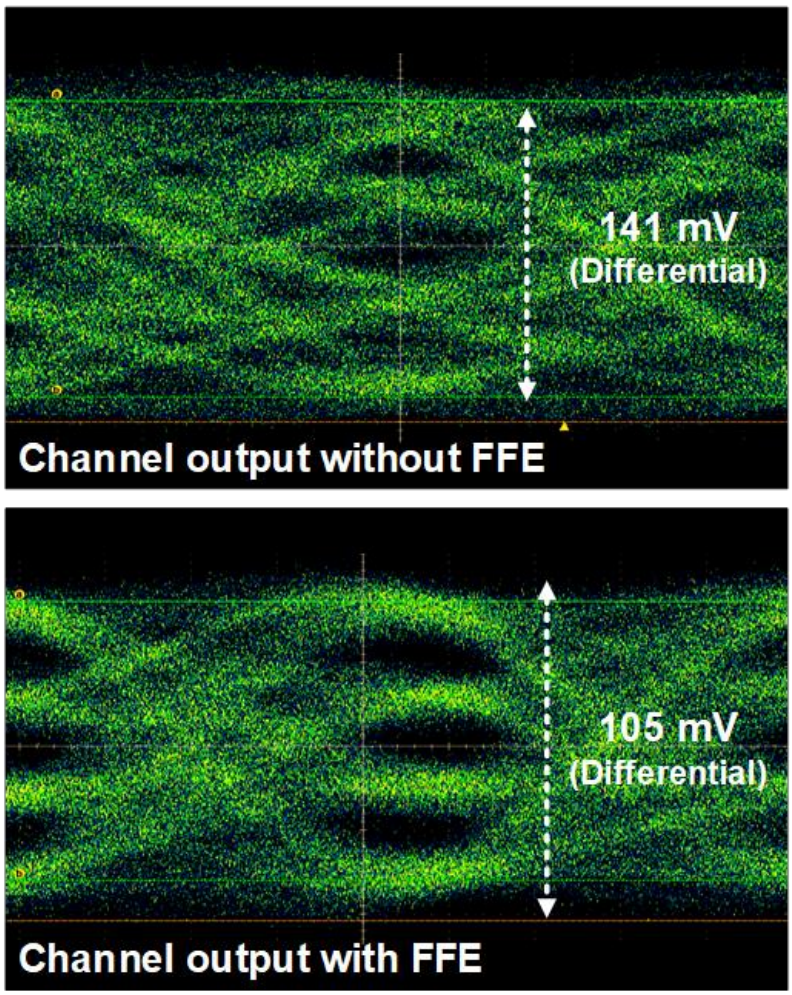


Fig. 3.15 Measured PAM-4 differential eye diagrams at 40 Gb/s with channel 1.

Gb/s PAM-4 operation is described in Fig. 3.17. The clock distribution power is as low as 10.5%, owing to the elimination of clocking in tap generation.

Table 3.1 summarizes the performance comparison of transmitters using similar technology. The transmitters fabricated in 65 nm CMOS technology are compared with power and area efficiency, and the proposed design shows competitive numbers. Compared with [3.4], which uses SiGe technology but has the FFE structure similar

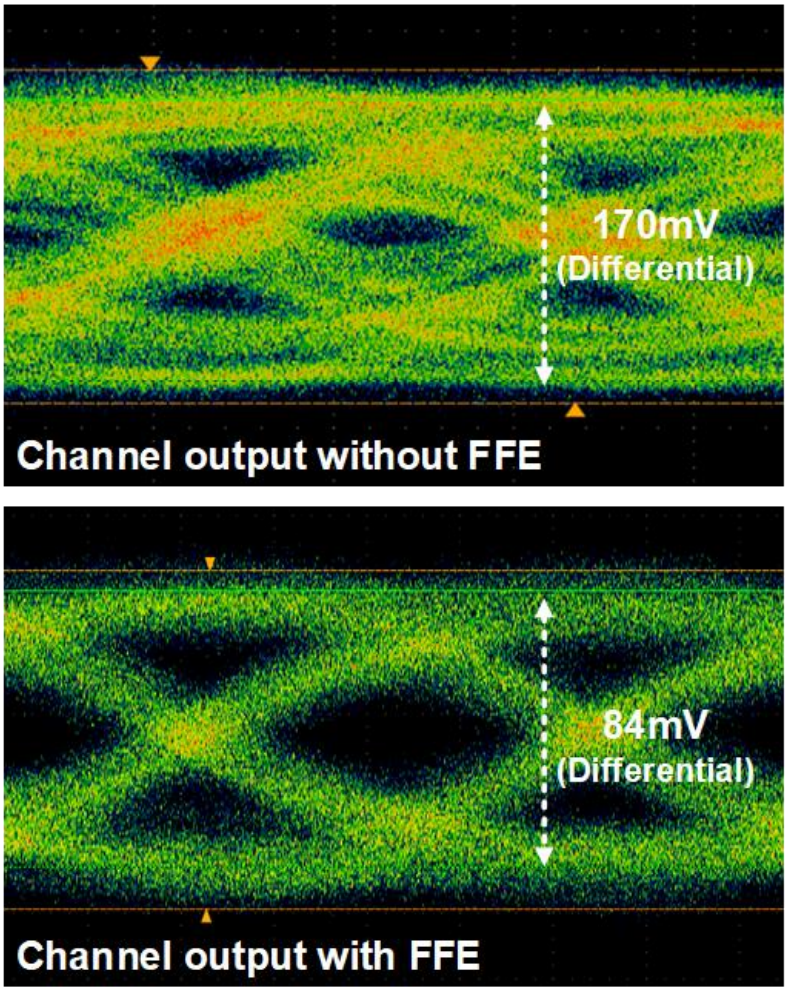


Fig. 3.16 Measured NRZ differential eye diagrams at 24 Gb/s with channel 2.

to the proposed scheme, a significant advantage is apparent. The proposed PAM-4 transmitter with DS-CPW FFE achieves state-of-the-art power and area efficiency compared to the other transmitters in the same scaling technology.

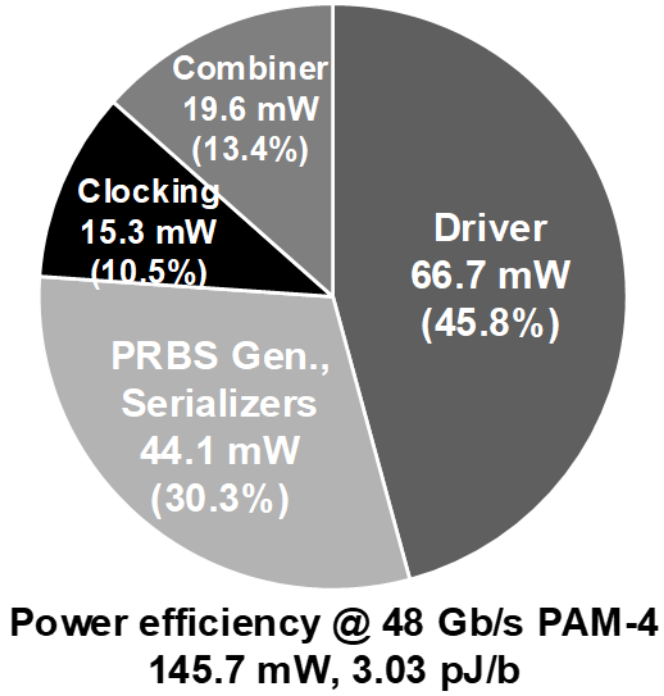


Fig. 3.17 Power breakdown of the proposed transmitter

Table 3.1 Performance comparison of transmitters with FFE

	MWCL'09 [3.4]	JSSC'10 [3.2]	JSSC'15 [3.3]	TCAS2'19 [3.14]	JSSC'15 [3.16]		JSSC'17 [3.17]	TCAS1'19 [3.18]	This work
Technology	130 nm SiGe	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS		65 nm CMOS	65 nm CMOS	**65 nm CMOS**
FFE structure	5-tap Microstrip	7-tap Active + LC-ladder	4-tap Active + LC-ladder	3-tap Flip-Flop	3-tap Flip-flop + Distributed Amp.		4-tap Latch	5-tap Latch + Active	**3-tap DS-CPW**
Data Rate (Gb/s)	84 (NRZ)	40 (NRZ)	64.5 (NRZ)	28 (NRZ)	62 (PAM-4)	61 (NRZ)	50 (NRZ)	10 (NRZ)	**48 (PAM-4)**
Chip Area (mm^2)	6.16	4.0	0.35	0.23	1.14	2.1	0.6	0.0071	**0.151**
Power (mW)	750	80	199	195	290	450	145	46	**146**
FoM1 (pJ/b)	8.93	2†	3.1	6.95	4.83*	7.35*	3.6	4.6†	**3.03**
FoM2 (mm^2/Gb/s)	0.0733	0.1	0.00543	0.00821	0.0184*	0.0344*	0.012	0.00071	**0.00315**

*** With PLL** **† Driver only**

Chapter 4

Design of 64 Gb/s PAM-4 Optical Transmitter in 40 nm CMOS

4.1 Overview

For the optical interface, the electro-optical transmitter chip designed in the CMOS process has been proposed rather than the BiCMOS process as technology advances. On the other hand, vertical-cavity surface-emitting laser (VCSEL) has been a popular candidate for the optical modulation device of the 400 GbE interconnect because of its cost and packaging efficiency [4.1]-[4.9]. However, the high operating voltage, nonlinear effects, and low bandwidth are problems to be overcome by the VCSEL driver to transmit high-speed PAM-4 data. Therefore, the pattern-detecting equalization is proposed [4.3], [4.5]-[4.7] to compensate for the nonlineari-

ty. The driver combines MSB and LSB data by designing each driver strength differently to produce PAM-4 output [4.3], [4.5], [4.9]. However, pattern detection requires power-consuming additional blocks. In addition, the combining at the driver needs an additional pre-driver and increases driver drain capacitance which lowers the bandwidth.

This chapter presents a 64 Gb/s PAM-4 VCSEL transmitter for 400 GbE with 3-tap fractionally-spaced asymmetric feed-forward equalizer fabricated in 40 nm CMOS technology [4.10]. The quarter-rate system and the PAM-4 combining 8:1 multiplexer are employed for clocking power reduction. In addition, the fractionally-spaced FFE and combining-ahead scheme compensate for low bandwidth. The proposed chip achieves a power efficiency of 2.09 pJ/b at 64 Gb/s.

4.2 Design Consideration of Optical Transmitter

The proposed transmitter system is designed to have broad bandwidth with low power consumption. There are several design considerations to achieve it. Firstly, the serializer can be operated in half-rate or quarter-rate. A full-rate clocking is excluded due to excessively high frequency for CMOS technology. The half-rate clocking requires delay matching buffers to fit the narrow timing margin in the final serializer. The quarter-rate clocking is more relaxed from the timing constraint owing to halved frequency. Additionally, the quarter-rate system consumes less power than half-rate one, though a doubled clock phase, because of halved frequency and less buffers [4.11]. The complex 4:1 MUX architecture and lowered bandwidth at the MUX output by self-loading drain capacitance [3.17] are solved by circuit design. There is also an option for the placement of the PAM-4 combining circuit. The MSB and LSB data are often combined at driver output because of driver linearity. The driver controls R_{LM} by bias control of MSB/LSB segments. However, combining at driver still has linearity problem due to VCSEL nonlinearity and requires power-hungry 4:1 MUX each for MSB and LSB paths. The combining-ahead scheme, namely combining at 4:1 MUX, reduces this power consumption by halving the number of 4:1 MUX. The driver and VCSEL linearity can be compensated simultaneously if there is a linearity control block in the MUX.

There are also design options in the VCSEL driver structure. The two types of differential VCSEL driver is illustrated in Fig. 4.1(a) and (b). The differential scheme drives both anode and cathode of the VCSEL [4.8], and the pseudo-differential scheme drives only anode or cathode with differential driver [4.1]-[4.7].

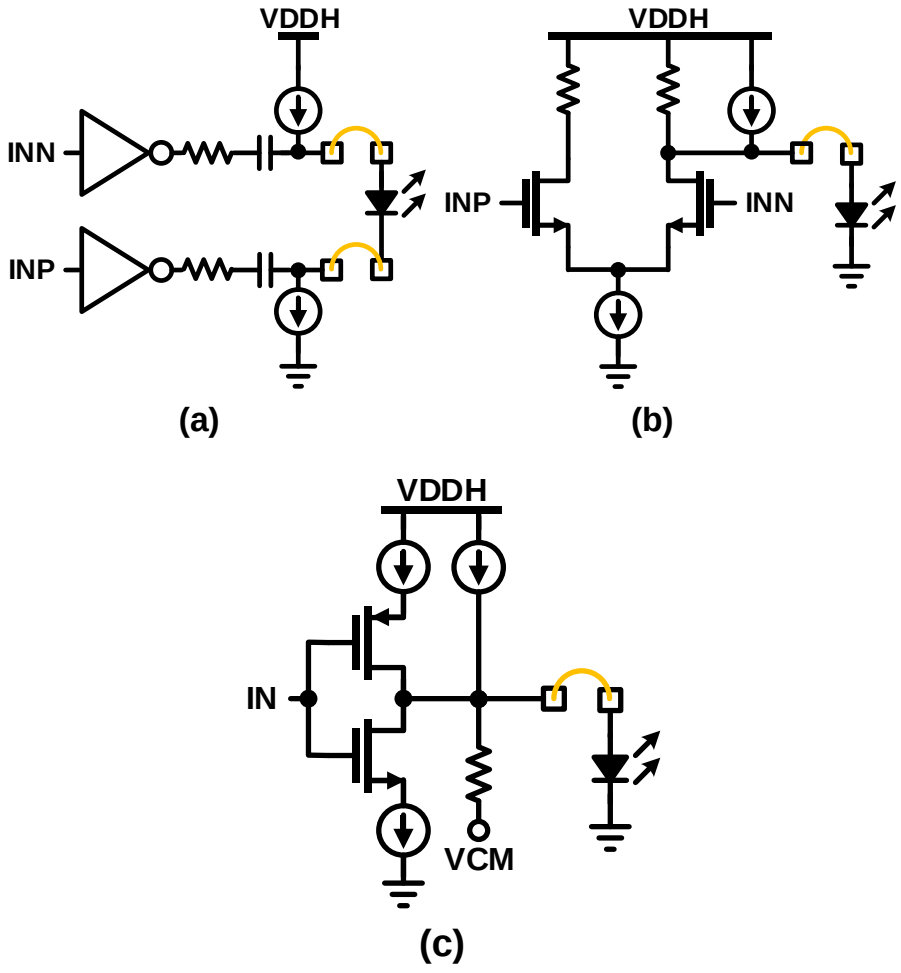


Fig. 4.1 VCSEL driver scheme (a) differential VM (b) pseudo-differential CM

(c) Single-ended push-pull

These types reduce the pre-driver power noise by differential input. However, the former suffers from common level noise by high DC impedance at both anode and cathode. The latter has low driver power efficiency than the former one because of the driver DC current. Fig. 4.1(c) shows a single-ended push-pull VCSEL driver. It alleviates the drawback of the differential drivers by common-cathode and push-pull driving [4.12]—also, the single-ended halves the power consumption at pre-driver. The single-ended push-pull scheme is power-efficient among the presented drivers for both pre-driver and output driver.

4.3 Proposed PAM-4 VCSEL Transmitter

The overall block diagram of the proposed VCSEL transmitter system is illustrated in Fig. 4.2. The external clock is forwarded to the quadrature clock generator (QCG) for quarter-rate clocking. Two pairs of phase interpolators (PI) produce two quadrature clocks for the sub-UI tap generation. The PRBS-7 generators produce MSB and LSB data, respectively, to emulate data input from the host chip. The 4-UI serialized data are retimed at the sub-UI tap generator by CLK_{main} for main-tap and CLK_{FFE} for pre/post-tap. The retimed MSB and LSB data are finally serialized to a

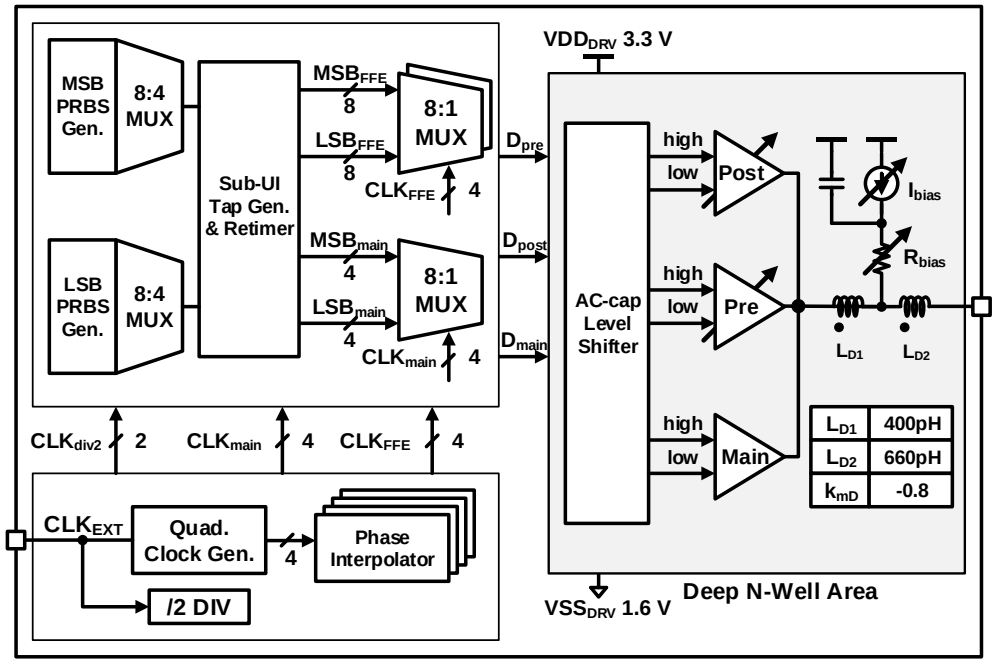


Fig. 4.2 Overall architecture of the proposed PAM-4 VCSEL transmitter.

PAM-4 data stream in the 8:1 MUXs, which perform as a pre-driver. The serialized data passes the AC-cap-based level shifter to drive the VCSEL, which operates at high voltage. The asymmetric FFE driver and T-coil network compensate for the nonlinearity and overcome the low bandwidth of VCSEL.

A quadrature clock generator based on an active polyphase filter is adopted for the quarter-rate system, as shown in Fig. 3.8. The remained phase error from PVT variation or layout mismatch is corrected by 128-code PIs shown in Fig. 4.3. The timing margin between 8:4 MUX and the tap generator is also secured by employing PIs. Since VCSEL has low bandwidth due to large diode capacitance and rate-equation, fractionally-spaced feed-forward equalization (FFE) is utilized. It has benefits over conventional 1-UI FFE at reducing PAM-4 switching jitter. The sub-UI tap generation is implemented by another set of quadrature clocks, CLK_{FFE}, from an

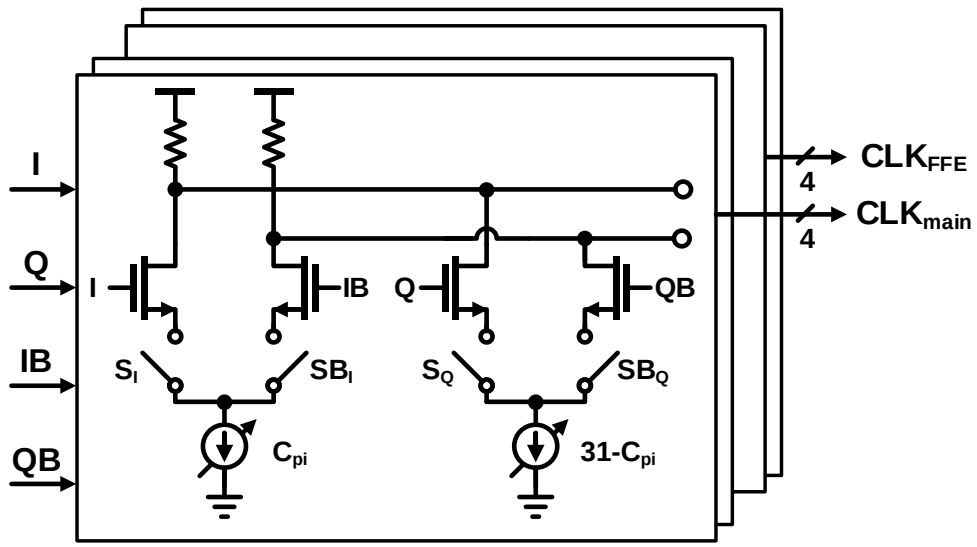


Fig. 4.3 Phase interpolator

additional pair of PI with a 0.125-period interval from CLK_{main}.

The retimer for the quarter-rate clock is illustrated in Fig. 4.5. The retimer is composed of C^2latches rather than flip-flops to reduce clock load. At first, each data from 8:4 MUX is aligned with CLK_0 and re-aligned with the corresponding clock. Since the transition of D' should be in the floating period of D_{ret}, an additional latch is required to D_{in}<2,3>. The main-tap, pre-tap, post-tap data are generated in separate retimer that operate with CLK_{main}, CLK_{FFE}, and 90-degree-shifted CLK_{FFE}, respectively.

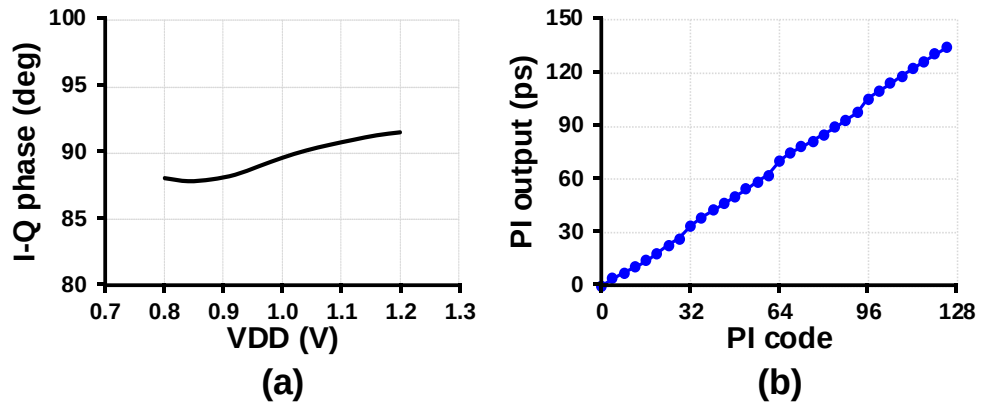


Fig. 4.4 Simulation Result of quadrature clock generator and phase interpolator (a) I-Q phase error according to VDD variation (b) PI output location according to input code

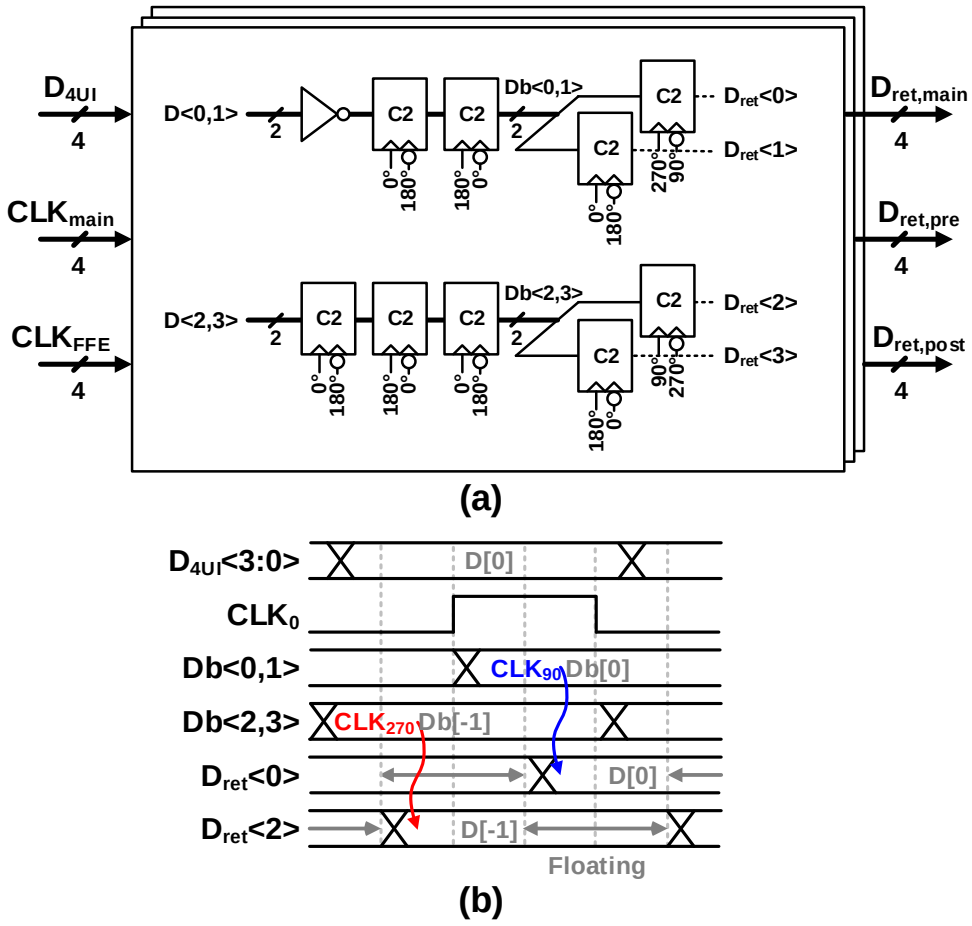


Fig. 4.5 (a) Schematic of tap generator / retimer. CLK_{main} is used for main-tap and CLK_{FFE} is used for pre/post tap. (b) Timing diagram, and (c) C^2Latch schematic.

Before 8:1 serializing, the retimed 4-UI width MSB and LSB data are gray-encoded and curved to 1-UI pulse as shown in Fig. 4.6(a). The MSB and LSB are encoded to gray code D_{01}, D_{11}, and D_{10} to effectively adjust the level separation mismatch ratio (R_{LM}). The logic for D_{00} is omitted since the corresponding MUX output is VDD. Up to one of D_{01}, D_{11}, and D_{10} is data 1 in a quadrature-phase by the gray code logic. And then, each data passes NAND logic with matching clocks to be carved to 1-UI data pulse. D_{main} passes the logic with $CLK_{main,}$ and D_{pre} and D_{post} pass the logic with CLK_{FFE}. The timing diagram of the 1-UI pulse generator is shown in Fig. 4.7. The data $D_{01,0}$, aligned to CLK_0, passes the AND gate with CLK_{90} to be a 2-UI pulse data. And then, passes the AND gate again with the delayed CLK_{180} to be 1-UI pulse data, $D_{01,0,1UI}$. The exact process applies to other data. In the source-less CML stage, quadrature sets of NMOSs for D_{01}, D_{11}, and D_{10} are connected to R_L through T-coil, as shown in Fig. 4.8. The width of 1-UI pulse data is crucial to this structure since it affects the output ripple at the data transition. The short pulse occurs up-ripple, whereas the long pulse occurs down-ripple. The pulse width is determined by the transistor size of NAND, which is illustrated in Fig. 4.6(b). Each dimension of the transistors is determined by consideration of fan-out and pulse width. Since the order of NAND input is set, some transistors in NANDs can be omitted. To obtain PAM-4 linearity, the NMOS width of the CML stage is determined to be 3.8 μm, 8.48 μm, and 15.36 μm for D_{01}, $D_{11,}$ and D_{10}, respectively.

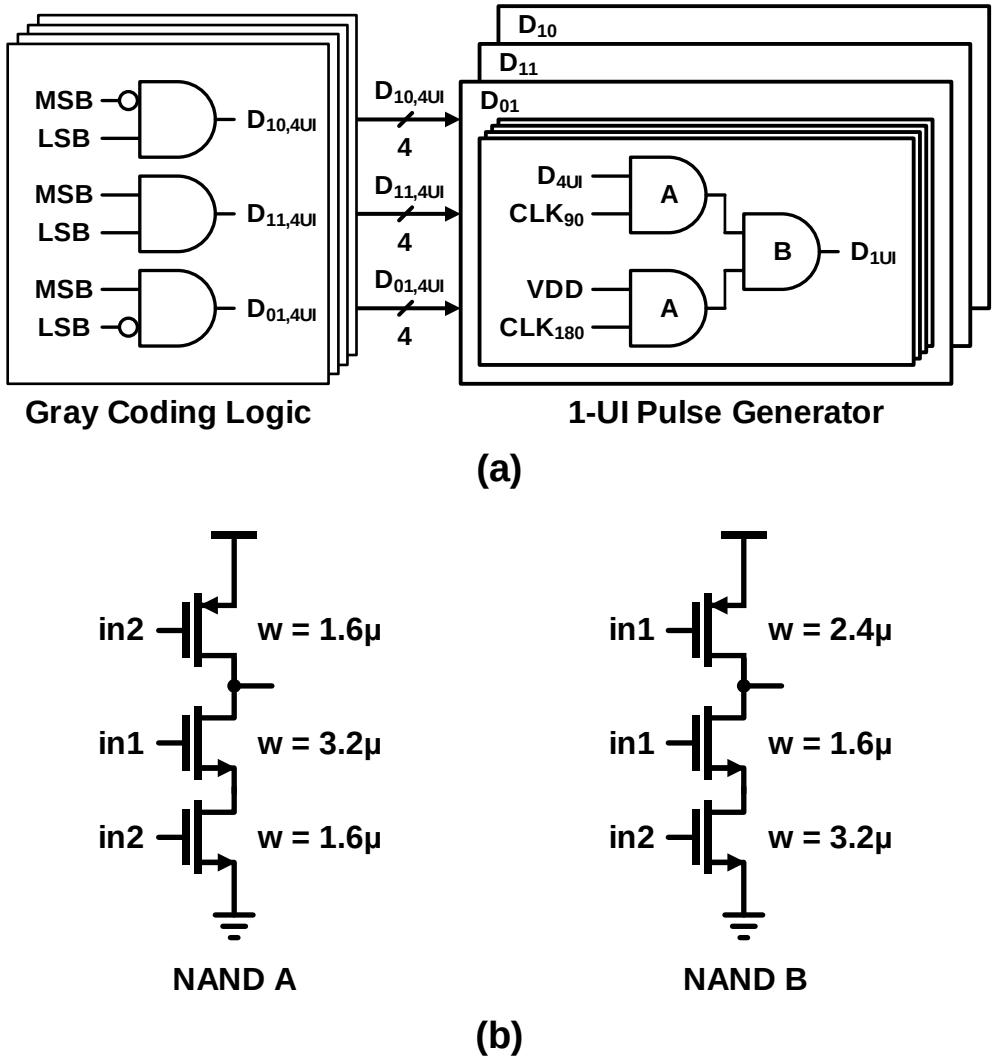


Fig. 4.6 (a) Circuit of 1-UI pulse generator in 8:1 MUX

(b) NANDs in 1-UI pulse generator

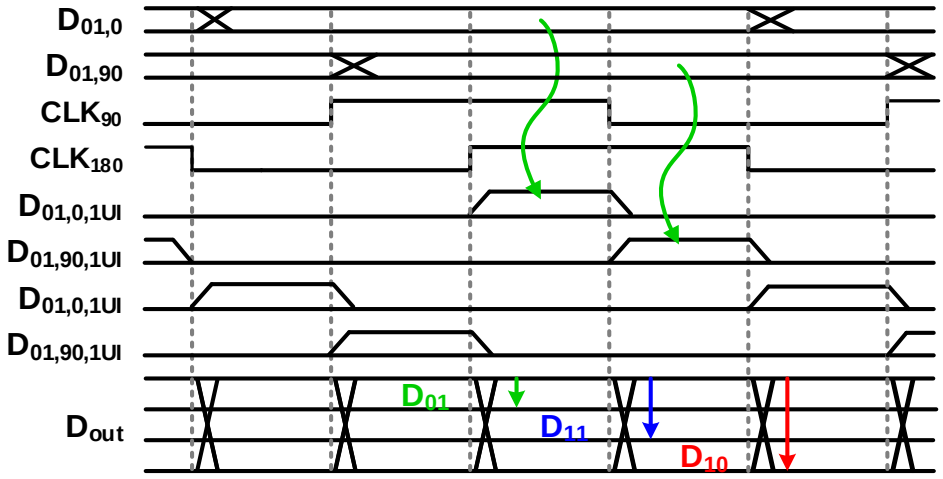


Fig. 4.7 Timing diagram of 1-UI pulse generator and 8:1 MUX

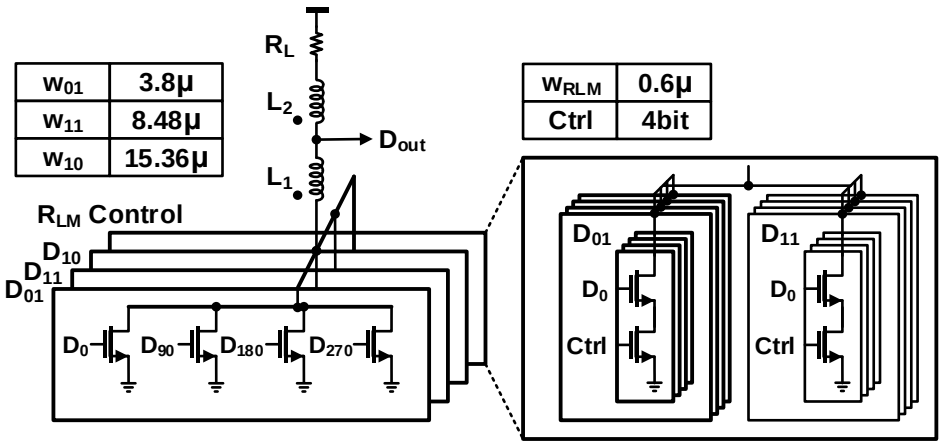


Fig. 4.8 Circuit of the source-less CML stage in 8:1 MUX. The data inputs are outputs of 1-UI pulse generator.

In the R_{LM} control block, the effective transistor width for input D_{01} and D_{11} is digitally controlled to ensure the R_{LM} of VCSEL output considering both the driver and VCSEL nonlinearity without the bias control at the driver. The width can be controlled with a 4-bit thermometer code to have five voltage levels. Fig. 4.9 shows the simulated eye diagram with R_{LM} control code sweep. The output voltage levels for D_{01} and D_{11} are independently adjusted to ± 25 mV. Thus, the control range is sufficient to compensate for the driver and VCSEL nonlinearity.

The bandwidth of 8:1 MUX is narrow because of the significant driver size though the current-mode logic structure has wider bandwidth than the CMOS structure. Lowering the load resistance of CML is constrained by the power consumption and output voltage swing. We applied T-coil at the MUX output to extend the bandwidth without additional power consumption. The T-coil in the MUX is designed in top-metal M10 and M9 to have 160 pH and 70 pH with the mutual coefficient of 0.22, as shown in Fig. 4.10. The T-coil parameters are decided by numerical

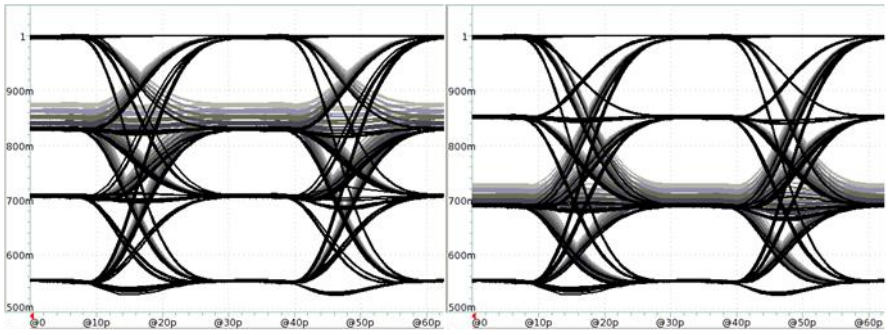
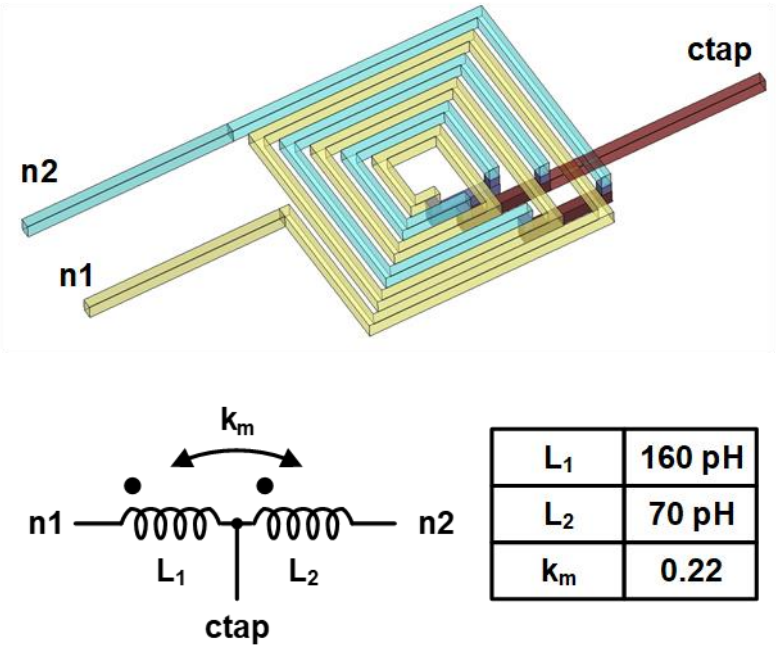


Fig. 4.9 Simulated eye diagram of 8:1 MUX output at 64 Gb/s PAM-4 with RLM control block code sweep (a) Sweeping D01 control code (b) Sweeping D11 control code

method to maximize the bandwidth and minimize the jitter, as described in Chapter 2. Fig. 4.11 is the simulation results of the 8:1 MUX output eye diagram at 64 Gb/s PAM-4 without and with the T-coil. Without the T-coil, the output bandwidth is insufficient that the middle eye width is 18.1 ps, and the output voltage is not entirely settled in a unit interval. Applying the T-coil, the central eye width is increased to 23.7 ps, and the eye height is entirely open.

The VCSEL driver adopts a high VSS domain for low power by isolated deep-N-well area as described in Fig. 4.12Fig. 4.13. VDD_{DRV} and VSS_{DRV} are 3.3 V and 1.6 V, respectively, to provide an operating range of VCSEL and prohibit the transistor voltage stress. The cascode devices can be removed by utilizing high VSS, which consumes the output voltage headroom. The pre/main/post PAM-4 data pass through



L_1	160 pH
L_2	70 pH
k_m	0.22

Fig. 4.10 Layout and inductance of T-coil in 8:1 MUX

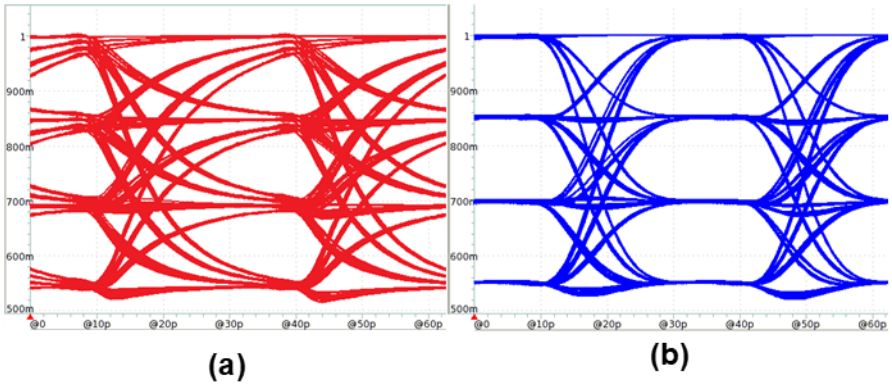


Fig. 4.11 Simulated eye diagram of 8:1 MUX (a) Without T-coil (b) With T-coil

the AC-coupled high-pass filter, which controls the common voltage level of PMOS/NMOS for each driver. The driver works in push-pull current mode operating in saturation region by the level shifter. At the current bias block, the shunt load resistor R_{bias} helps to extend the bandwidth for the current mode driver. It is difficult for a push-pull driver to place a load resistor without an additional regulator or voltage source since it affects the output common level, which is especially important to the VCSEL driver. An AC-ground capacitor solves the common level problem by being placed parallel with the VCSEL bias current source.

On the other hand, the pad capacitance C_p degrades the bandwidth, which can be compensated by shunt peaking and series peaking inductors. The proposed driver uses a reverse-turn T-coil that provides shunt peaking to R_{bias} and series peaking to C_p to save the inductor area. The overall small-signal model of the driver-VCSEL interconnect is described in Fig. 4.13. Though the push-pull driver operates in a saturation region, the output resistance should be considered due to its large size. The electrical model of the VCSEL consists of pad capacitance, C_{vcin}, series mirror re-

sistance R_s, diode junction capacitance C_{vcout}, and diode small-signal resistance R_{vc}. The layout and equivalent circuit of the T-coil are shown in Fig. 4.14. The T-coil for the output network is designed to have a negative mutual coefficient by reverse-turn at the center tap. The negative-k T-coil provides both shunt and series peaking. The T-coil value is 400 pH for L_{D1} and 660 pH for L_{D2} with the mutual coefficient of -0.8. The designed inductance and mutual coefficient make one part of T-coil inductance to zero, and other parts to be 400 pH of shunt inductance, L_{sh}, and 260 pH of series inductance, L_{se}. The bandwidth extension by the proposed T-coil is described in Fig. 4.15. The VCSEL diode input current, proportional to VCSEL optical power, gets wider bandwidth with the load resistance R_{bias} and T-coil. The 3dB bandwidth increases 1.61 times to 22.8 GHz from 14.2 GHz. The phase delay is also widely flattened by proposed design.

The push-pull strength of the pre/post driver is independently controlled with a 4-bit binary code. The asymmetric control of the FFE driver compensates for the nonlinear rise/fall characteristic of VCSEL.

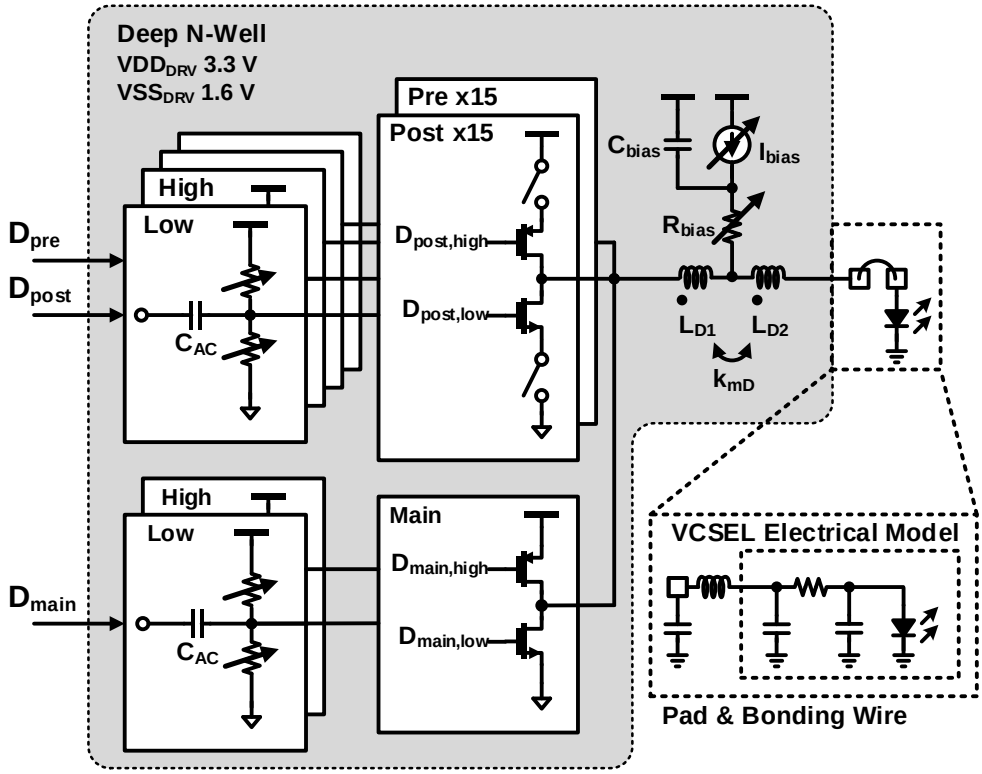
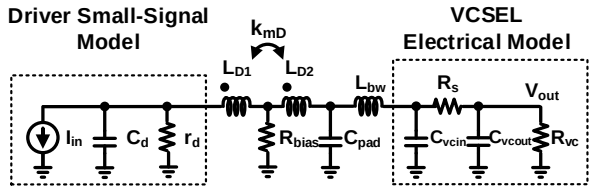


Fig. 4.12 Circuit of proposed VCSEL driver on deep-N-well area



r_d	115 Ω	C_{pad}	110 fF
C_d	192 fF	L_{bw}	500 pH
L_{D1}	400 pH	C_{vcin}	25 fF
L_{D2}	660 pH	R_s	33 Ω
k_{mD}	-0.8	C_{vcout}	300 fF
R_{bias}	40 Ω	R_{vc}	61 Ω

Fig. 4.13 Small-signal model of the VCSEL driver output network

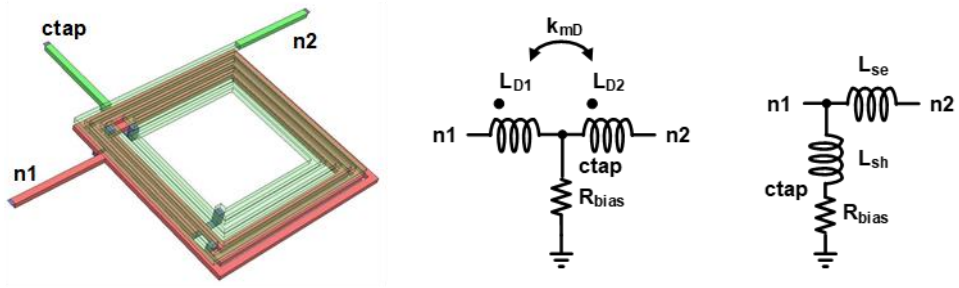


Fig. 4.14 Layout and equivalent circuit of the proposed T-coil

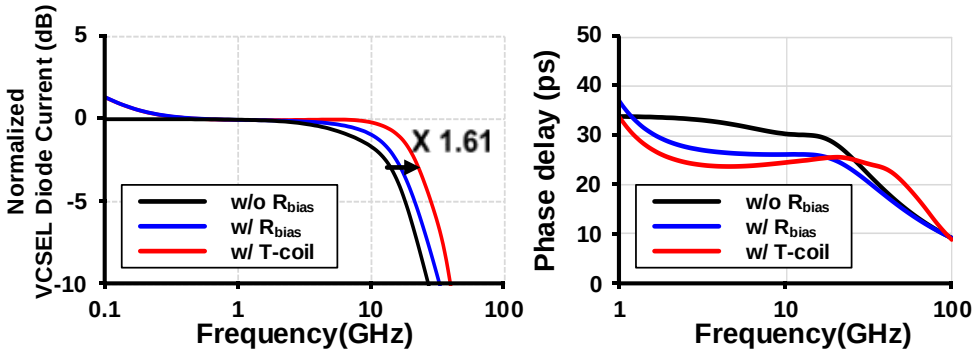
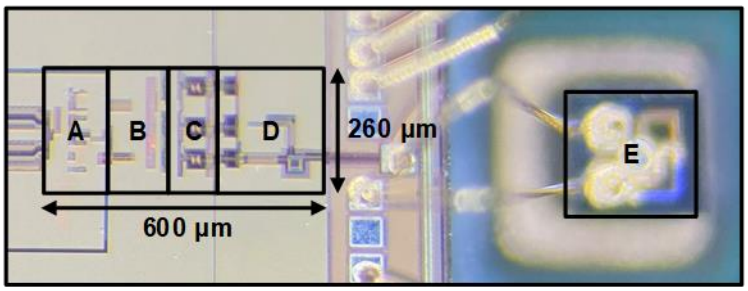


Fig. 4.15 AC-response of VCSEL current input

4.4 Measurement

The proposed VCSEL transmitter system is fabricated in 40 nm CMOS technology, and 18 GHz bandwidth 850 nm wavelength VCSEL is wire-bonded to the driver output. The transmitter system occupies 0.156 mm^2, including T-coils, as shown in Fig. 4.16. The measurement setup is illustrated in Fig. 4.17. The clock synthesizer in Anritsu MP1800A produces a quarter-rate clock and sampling trigger for Keysight DCA-X86100D optical oscilloscope. The differential quarter-rate clocks are input to the test board through the SMP connector. The VCSEL output is coupled to OM2 bare-fiber to be scoped by the equipment. The optical power loss occurs in the process of VCSEL-fiber direct coupling. The 3 dBm of loss is de-



	Block Description	Area(μm^2)	Power(mW)
A	QCG & PI	35100	56.4
B	PRBS Gen. & Tap Gen.	31200	10.1
C	8:1 Mux	28600	36.5
D	VCSEL Driver	61100	30.6
E	18 GHz BW VCSEL	62500	-

Fig. 4.16 Die micrograph

embedded to OMA (optical modulation amplitude) measurement results [4.1].

The measured NRZ eye diagrams are shown in Fig. 4.18. By using T-coil, a wide opening is measured at 28 Gb/s without FFE. The OMA is measured to 4.13 dBm, and the extinction ratio(ER) is measured to 5.26 dB. However, the data 0 level is a bit closed because of the nonlinearity. The asymmetric FFE compensates for this by using only the PMOS driver. The normalized FFE coefficient for NRZ 28 Gb/s is $[P_{main}/N_{main}, P_{pre}/N_{pre}, P_{post}/N_{post}]$ = [1/2.7, 0.78/0, 0.52/0]. The maximum data rate is measured to 48 Gb/s. The closed eye diagram is open with the coefficient of [1/1.3, 0.87/0.53, 0/0]. With FFE, the OMA is measured to 1.00 dBm and 0.85 dBm for 28 Gb/s and 48 Gb/s, respectively. The overall system's power consumption is measured to 113.8 mW and 145.2 mW, which correspond to 4.06 pJ/bit and 3.03 pJ/bit. The measured PAM-4 eye diagrams are shown in Fig. 4.19. Since PAM-4 is more

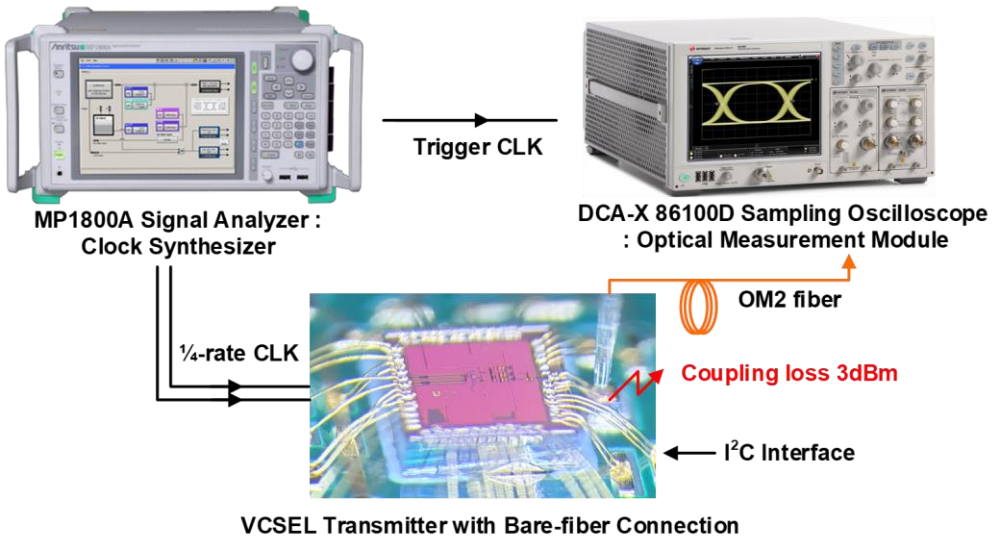


Fig. 4.17 Measurement setup

vulnerable to nonlinearity, the eye diagram is closed without FFE. With the sufficient coefficient and bias current, the PAM-4 output can be measured. For 56 Gb/s measurement, the coefficients are [1/2.1, 0.65/0, 0.43/0] and [1/1.3, 0.25/0.20, 0.25/0.20] and the eye openings are 2.76 dBm and 2.02 dBm for Fig. 4.19(b) and (c), respectively. For 64 Gb/s, the PAM-4 eye is entirely closed without FFE, unlike the case of 56 Gb/s. With the coefficient of [1/1.2, 0.57/0.09, 0.57/0.09], eye opening of 0.32 dBm is obtained for 64 Gb/s. The power consumption is measured to 125.6 mW and 133.6 mW for 56 Gb/s and 64 Gb/s, corresponding to 2.24 pJ/bit and 2.09 pJ/bit. The R_{LM} for PAM-4 measurement is over 94%, which is the requirement of IEEE802.3bs and CEI-56G [1.11][1.13], by linearity control block in 8:1 MUX. The comparison with the recent VCSEL transmitter fabricated in CMOS technology is presented in Table 4.1. The proposed transmitter operates in the highest data rate both for NRZ and PAM-4. The power efficiency is also measured as the best figure owing to 8:1 multiplexing and bandwidth extension techniques.

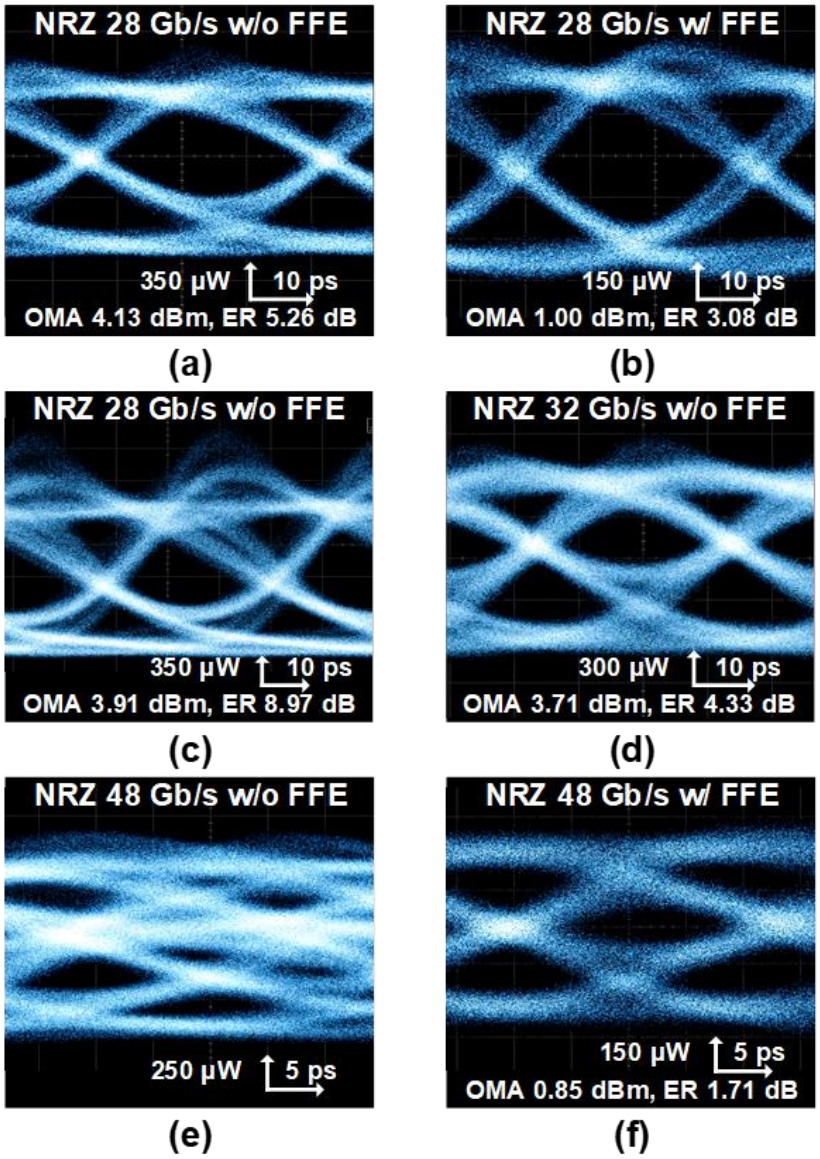


Fig. 4.18 NRZ eye diagram measurement. (a) 28 Gb/s without FFE (b) 28 Gb/s with FFE (c) 28 Gb/s without FFE, low current bias (d) 32 Gb/s without FFE(e) 48 Gb/s without FFE (f) 48 Gb/s with FFE

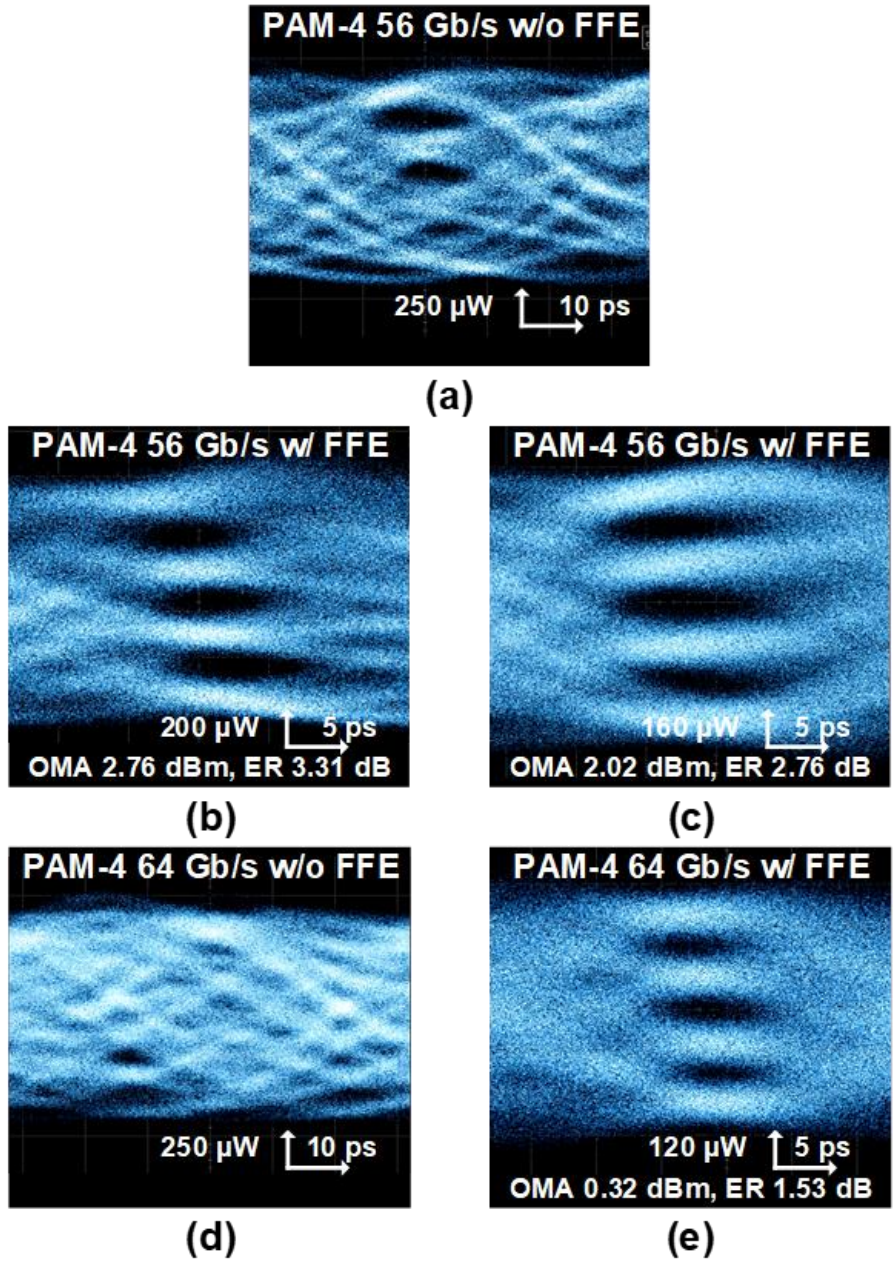


Fig. 4.19 PAM-4 eye diagram measurement. (a) 56 Gb/s without FFE (b)-(c) 56 Gb/s with

Table 4.1 Performance comparison of state-of-the-art VCSEL transmitters

	JSSC'18 [4.1]	PTL'18 [4.3]	OFC'19 [4.5]	SOVC'19 [4.9]		This work	
Technology	14 nm	65 nm	40 nm	65 nm		40 nm	
VCSEL BW (GHZ)	15	11	16	20		18	
Clock rate	Half-rate	Half-rate	Half-rate	Quarter-rate		Quarter-rate	
Clock Source	Forwarded Clock	Forwarded Clock	CDR	PLL		Forwarded Clock	
Equalization Technique	0.5-UI 3-tap	2.5-tap DAC	Pattern Pulsed	Asym. 1-UI 3-tap		Asym. 0.5-UI 3-tap	
Area (mm^2)	0.088	0.2	-	0.278		0.156	
Data Rate (Gb/s)	NRZ 32	PAM-4 50	PAM-4 50	NRZ 44	PAM-4 64	**NRZ 48**	**PAM-4 64**
OMA (dBm)	1.23*	3	0.22	3.33*	3.98*	0.85*	0.32*
FoM (pJ/b)	3.28	5.12	7.6	3.65	2.69	**3.03**	**2.09**

*** Coupling loss de-embedded**

Chapter 5

Conclusions

In this dissertation, the transmitter systems for short-reach interface in data center applications are proposed. As the data rate increase, power-efficient bandwidth extension techniques are required to compensate low bandwidth of the electrical channel and optical device. The proposed transmitters utilized fractionally-spaced FFE, transmission line, inductor, and T-coil to achieve power-efficient and high-bandwidth systems. The first chip is a 48 Gb/s PAM-4 electrical transmitter with FFE based on a double-shielded coplanar waveguide. A passive delay element is adopted for FFE tap generation rather than using a clock element or an active delay element to reduce clocking power consumption. In addition, the proposed technique also helps to minimize power-hungry serializer blocks. The area efficiency, which is the drawback of using a passive delay element, is significantly improved by a sizeable slow-wave factor owing to double metal shields above and below the waveguide. The structure and input configuration of the 4:1 MUXs are designed to avoid data-

dependent capacitive couplings or charge injections. A prototype chip is fabricated in 65 nm CMOS technology. The transmitter achieves a data rate of 48 Gb/s PAM-4 with a power efficiency of 3.03 pJ/b while occupying the chip area of 0.151 mm^2.

The second chip presents a 64 Gb/s PAM-4 VCSEL transmitter in 40 nm CMOS for co-package optics. The fractionally-spaced 3-tap asymmetric FFE, AC-grounded shunt resistor, and negative-k T-coil network are used for compensation of the low bandwidth of VCSEL. T-coils are also designed at the internal circuit considering bandwidth-limiting capacitance at the driver input. In addition, the system utilizes the quarter-rate clocking, 8:1 MUX, and high VSS driver to improve power efficiency. These efforts have advanced the state-of-the-art VCSEL transmitter data rate of 64 Gb/s and power efficiency of 2.09 pJ/b.

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초 록

400Gb 이더넷 표준이 개발됨에 따라 데이터 센터의 고속 상호 연결이 더욱 중요해지고 있다. 높은 데이터 속도에서의 채널 손실에 의해 단거리 채널의 경우에도 송신기에 대한 대역폭 확장 기술이 필요하다. 한편, 데이터 센터 내 동-서 연결의 중요성이 높아지면서 데이터 센터 아키텍처가 기존의 아키텍처에서 스파인-리프로 전환되고 있다. 이러한 추세에서 단거리 광학 인터커넥트의 수가 점차 우세해질 것으로 예상된다. 수직 캐비티 표면 방출 레이저(VCSEL)는 일반적으로 단거리 상호 연결을 위해 사용되는 광학 모듈레이터이다. VCSEL 은 낮은 대역폭과 비선형성을 가지고 있기 때문에, 광 송신기도 대역폭 증가 기술을 필요로 한다. 또한, 데이터 센터의 전력 소비는 기후 변화에 영향을 미칠 수 있는 우려 지점에 도달했다. 따라서, 본 논문은 데이터 센터 응용을 위한 고속 전력 효율적인 송신기에 초점을 맞추고 있다. 회로 설계를 제시하기 전에, 부분 간격 피드-포워드 이퀄라이저 (FFE), 온칩 전송선로, 인덕터, T-코일과 같은 대역폭 확장 기술을 수학적으로 분석한다.

첫 번째 칩은 저속파 전송선로를 기반으로 한 3-탭 FFE 를 사용하는 전력 및 면적 효율적인 펄스-진폭-변조 4(PAM-4) 송신기를 제시한다. 높은 클럭 전력 소비를 극복하기 위해 이퀄라이저 탭 생성을 위해 수동소자 지연 라인을 채택했다. 전송 라인은 차동 동일평면도파관 주위에 이중 플로팅 금속 차폐를 사용하여 15 의 높은 전달속도 감쇠를 달성한다. 송신기에는 4:1 멀티플렉서(MUX)와 4-위상 클럭 생성기가 포함되어 있다. 4:1 MUX 는 2-UI 펄스 발생기를 사용하며, 정성 분석에 의해 입력 구성

이 결정된다. 이 칩은 65 nm CMOS 기술로 제작되었으며 0.151 mm^2의 면적을 차지한다. 제안된 송신기 시스템은 PAM-4 신호와 함께 48 Gb/s의 데이터 속도에서 3.03 pJ/b의 에너지 효율을 보여준다.

두 번째 칩에서는 3-탭 FFE 및 역회전 T-코일을 사용하는 전력 효율적인 PAM-4 VCSEL 송신기를 제시한다. 위상 보간기(PI)는 부분 간격 FFE 탭을 생성하고 4-위상 클럭 오류를 수정하는 데 사용된다. 직렬화 전력 소비를 줄이기 위해 출력 드라이버에서 MSB와 LSB를 두 개의 4:1 MUX를 통해 결합하는 대신 8:1 MUX를 통해 PAM-4로 결합하는 회로가 제안된다. 내부 및 출력 노드에서 T-코일은 대역폭을 증가시키고 기호 간 간섭(ISI)을 제거한다. 출력 네트워크에서 역회전 T-코일은 T-코일이 없는 경우보다 대역폭을 1.61 배 증가시킨다. VCSEL 드라이버는 양극 구동 및 전력 감소를 위해 높은 VSS 도메인에 배치된다. 이 칩은 40 nm CMOS 기술로 제작되었다. 제안된 VCSEL 송신기는 각각 3.03pJ/b 와 2.09pJ/b 의 전력 효율로 최대 48Gb/s NRZ 와 64Gb/s PAM-4 까지 작동한다.

주요어 : PAM-4 transmitter, 4:1 multiplexer(MUX), fractionally-spaced feed-forward equalizer(FFE), slow-wave transmission line, T-coil, VCSEL CMOS transmitter, push-pull driver

학 번 : 2016-20891