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Interface Phenomena Analysis in Dual-Stacked Structure and Synaptic Current Modeling of Oxide Thin-Film Transistors

이중 산화물 박막 트랜지스터의 계면 현상 분석과 시냅틱 박막 트랜지스터의 드레인 전류 모델링

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이 논문을 공학박사학위 논문으로 제출함.

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Abstract

Interface Phenomena Analysis in Dual-Stacked Structure and Synaptic Current Modeling of Oxide Thin-Film Transistors

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Thin-film transistors (TFTs) have been used as the switching devices in the field of display. Recently, existing flat-panel display devices are changing transparently and flexibly. Accordingly, an oxide semiconductor (OS) having all of these characteristics has been spotlighted as a channel layer of TFTs, and continuous research has been conducted. Indium-gallium-zinc oxide (IGZO) is actively used as a channel layer in

TFTs due to its stable off-current characteristics and an ideal threshold voltage close to 0 V. However, despite their excellent off-state properties, IGZO TFTs are limited by low field-effect mobility ($\sim$10 $cm^2/V \cdot s$), which critically affects display resolution and power consumption. To solve this problem, the dual-stacked TFTs using dual OS layers have been introduced. They improve field-effect mobility from the two-dimensional gas (2DEG) effect formed at the interface of the junctioned OSs. However, despite the remarkable improvement in field-effect mobility (30–60 $cm^2/V \cdot s$), the off-current characteristics still become a problem.

Herein, the dual-stacked TFTs with ultra-high field-effect mobility ($\sim$80 $cm^2/V \cdot s$) are implemented while maintaining excellent off characteristics such as an ideal threshold voltage close to 0 V and a high on-off current ratio ($>10^9$). To visually represent the conduction mechanism, the induced areas such as gate bias-induced area (GBIA), electrode bias-induced area (EBIA), band offset-induced area (BOIA), and BOIA-induced area (BIA) are newly proposed. Equivalent circuit modeling and the transmission line method are also introduced for more precise verification. In-situ analysis is conducted using these methods to confirm that confined electrons exist at the interface of OSs and contribute to the current flow. This is powerful evidence to understand the conduction mechanism in the dual-stacked TFTs, and it will provide new design rules for high-performance OS-based TFTs.

Synaptic devices that emulate human brain have attracted much attention for brain-inspired neuromorphic system. Especially, synaptic TFTs have emerged with the advantages of simultaneous signal processing and information storage. However, the electrical conditions with synaptic performance have been set only with repeated experimental measurements so far because it is complicated to process excitatory postsynaptic current (EPSC) which changes over time.

Herein, the single-pulse-driven synaptic EPSC (SPSE) model is analytically proposed. This is the first model to represent the EPSC that changes over time and can simulate EPSC of the synaptic devices under the given TFT-operating conditions. SPSE model can characterize quantified parameters, meaning the capacitive effect and the synaptic windows, depending on the electrical conditions applied to TFTs. The various gate insulators such as SiO_2 and ion-gel are used to verify the feasibility of SPSE model. This model enables the estimation of energy consumption, which can potentially be utilized to compare the energy cost of EPSC. The SPSE model will provide a guideline to design the suitable operating conditions for better synaptic performance based on comprehensive understanding the EPSC of a synaptic device.

Keywords: thin-film transistors, field-effect mobility, conduction mechanism, equivalent circuit, synaptic devices, excitatory postsynaptic current, drain current model, capacitive effect, synaptic window, energy consumption

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Contents

List of figures

Chapter 1

Chapter 2

List of tables

Chapter 2

Chapter 3

Chapter 1

Introduction

1.1 Overview

Thin-film transistors (TFTs) used as switching devices in the field of display control current supplied to light-emitting devices such as organic light-emitting diode (OLED) or micro light-emitting diode (LED) [1-4]. Therefore, it is essential to improve the performance of TFTs especially in the high-resolution display industry [5,6]. Recently, the importance of the fourth industrial revolution is increasing. Accordingly, new material technologies have been commercialized for various electronic products such as next-generation displays, memory devices, energy storage devices, and power generators [7-9]. In particular, oxide semiconductors (OSs) are attracting much attention as important candidates that can overcome the limitations of Si-based materials [1,10,11,12]. The OS typically has an energy band gap of less than 3 eV, and energy injection above this energy band gap allows the electrons to move against an internal electric field, resulting in current flow [1,12]. Therefore, the OSs are widely used as a channel layer of TFTs because current can be controlled by voltage regulation. OS-based TFTs are transparent and they can be fabricated at low temperature, so it is possible to process on transparent and flexible substrates such as plastic or polyimide [1,12].

Indium-gallium-zinc-oxide (IGZO) has been widely used as a channel layer of TFTs in the display industry because of low leakage current and ideal threshold

voltage formed close to 0 V [11-13]. However, it is difficult to apply IGZO TFTs to high-resolution displays due to their relatively low field-effect mobility (～10 $cm^2/V \cdot s$). To improve this, there have been various studies such as various types of doping [14,15], material changes [16-18], and OS film reinforcement [19,20]. In particular, the introduction of advanced vacuum deposition equipment such as atomic layer deposition (ALD) and pulsed layer deposition (PLD) significantly improved the field-effect mobility (～70 $cm^2/V \cdot s$) [21-24]. However, these methods require relatively high temperature processes (>400 ℃), making it difficult to apply such TFTs fabricated in this way to next-generation devices on flexible substrates. It is very challenging to enhance the field-effect mobility while maintaining stable off-current characteristics under low temperature processes (<300 ℃).

Dual-stacked OS-based TFTs have been considered as potential candidates to solve these problems. In dual-stacked structure, the electrons confined to the interface of OSs bent by band offset form the two-dimensional gas (2DEG), which affects current conduction [25-28]. The fundamental parameters of TFTs and more details of the dual-stacked structure are provided in chapter 1.

Synaptic devices that mimic the human brain have attracted much attention for brain-inspired neuromorphic system. Particularly, synaptic TFTs have been

proposed to obtain the advantage of simultaneous signal processing and information storage by emulating synaptic weight modulation with both drain and gate voltage (V_{DS} and V_{GS}) change [29-32]. The general purpose of developing synaptic TFTs is to improve the linearity of excitatory postsynaptic current (EPSC), the drain current (I_{DS}), accumulated in the sequential voltage pulses and to maintain the long-term plasticity (LTP) as long as possible. There have been many studies on synaptic performance improvement, mechanism identification, or demonstration of new applications [33-35]. However, most synaptic conditions have been obtained through repetitive experiments so far. This is because there was no suitable model for synaptic TFTs. Although it is valuable and important to extract the synaptic conditions through some experiments, comprehensive understanding of fundamental synaptic characteristics should be preceded for better research. There have been several studies that intuitively use fitting equation with exponential terms to calculate the pair-pulse facilitation (PPF) index [36,37]. Although it is a simple and reasonable method to represent EPSC shape of synaptic TFTs, there is a limitation to bridge the EPSC with the operating conditions of synaptic TFTs such as V_{DS}, V_{GS}, and other synaptic information. Thus, a comprehensive EPSC model is required to specifically describe the characteristics of the EPSC when a single V_{GS} pulse is applied.

More details of the synaptic TFTs are also provided in chapter 1.

In chapter 2, I newly propose the working mechanism in dual-stacked OS structure, and based on this, I develop dual-stacked OS-based TFTs with improved performance; high field-effect mobility (~ 80 $cm^2/V \cdot s$), ideal threshold voltage near 0 V, high on–off current ratio (>10^9), and good stability at bias stress. Four newly defined induced areas are introduced to verify the conduction mechanism more clearly such as gate bias-induced area (GBIA), electrode bias-induced area (EBIA), band offset-induced area (BOIA), and BOIA-induced area (BIA). Equivalent circuit modeling and transmission line method (TLM) are also used for more accurate verification. It is confirmed that the electrons confined at the interface of OSs exist and actually affect the flow of current. This is powerful evidence to understand the conduction mechanism in dual-stacked OS-based TFTs, and it will provide new design rules for high-performance OS-based TFTs. This work has been published as "Analysis of Interface Phenomena for High-Performance Dual-Stacked Oxide Thin-Film Transistors via Equivalent Circuit Modeling" by C. Im, J. Kim, N.-K. Cho, J. Park, E. G. Lee, S.-E. Lee, H.-J. Na, Y. J. Gong, and Y. K. Kim, *ACS Appl. Mater. Interfaces* 13, 51266-51278 (2021) [38].

In chapter 3, I newly propose an analytical model that emulates the EPSC of

synaptic TFTs, and named as a single-pulse-driven synaptic EPSC (SPSE) model. This model has four newly defined parameters; lumped responsive time-delaying constant ($\langle\tau\rangle_{rp}$), lumped relaxed time-delaying constant ($\langle\tau\rangle_{rx}$), responsive ratio constant (γ_{rp}), and relaxed ratio constant (γ_{rx}). Time-delaying constants quantify the capacitive effect associated with LTP and ratio constants quantify the synaptic window associated with short-term plasticity (STP). Moreover, EPSC increases after a single V_{GS} pulse, which is describe as a change in threshold voltage (ΔV_{TH}). All parameters depend on the electrical condition applied to synaptic TFTs. The various gate insulators such as SiO_2 and ion-gel are used to validate the feasibility of SPSE model. This model enables the estimation of energy consumption, which can potentially be utilized to fairly compare the energy cost of EPSC. The SPSE model will provide a guideline to design the suitable operating conditions for better synaptic performance based on a comprehensive understanding of the EPSC of synaptic devices. This work has been published as "Excitatory Postsynaptic Current Model for Synaptic Thin-Film Transistors" by C. Im, J. Kim, J. H. Lee, M. Jin, H. Lee, J. Lee, J. C. Shin, C. Lee, Y. S. Kim, and E. Lee, *J. Appl. Phys.* 132, 044503 (2022) [39].

Finally, in chapter 4, the overall conclusions and the potentials of these dissertations are summarized.

1.2 Oxide TFTs: characteristics and electrical parameters

TFTs are three-terminal transistors consisting of gate electrode, channel layer, and source-drain electrodes. In particular, the channel layer has the greatest influence on the electrical characteristics of TFTs because current conduction actually occurs in the channel layer. Si-based materials have been widely used as the channel layer in the field of display [40]. Low-temperature polycrystalline silicon (LTPS) has replaced hydrogenated amorphous silicon (a-Si:H) having low field-effect mobility under 1 $cm^2/V \cdot s$. LTPS has become mainstream based on ultrahigh field-effect mobility above 100 $cm^2/V \cdot s$ [41]. However, high cost processes are required and it is not easy to implement the uniform and large-scaled layer. It is also difficult to apply to next-generation display devices due to its lack of transparency and flexibility. Above all, the biggest problem is that the leakage current occurs because it is not stable in the off state.

OS is emerging as an alternative to solving these problems. In particular, it has superior off-current characteristics compared to Si-based semiconductors, which significantly reduces power consumption [1,11,13]. This is a very big advantage as a switching device. It also has little difference in electrical characteristics according to phase change. Silicon-based semiconductor with covalent bonds combines in four directions under the influence of sp^3 hybrid orbitals. In the

crystalline state, electrons can easily move along the combined bonds. However, in the amorphous state, electrons are difficult to move easily due to the disturbed electron pathway [1,11,13]. It causes a significant degradation in the field-effect mobility. On the other hand, OS with ionic bonds is composed of overlapping metal ns orbitals. This overlap is not greatly affected by structural distortion, so movement of the electrons is not significantly suppressed [1,11,13].

The accumulation of electrons is main source in the operation of n-type OS-based TFTs. In more detail, the electrons are accumulated at an interface between gate insulator and channel layer when a positive bias is applied to gate electrode . Such electrons move from source (low potential) to drain (high potential) by an electric field applied between source-drain electrodes, thereby contributing to current conduction [1,11,13]. At this time, the amount of accumulated electrons is related to the current flow, that is, field-effect mobility, depending on the bias applied to each electrode, or the inherent properties of materials. On the other hand, the electrons are depleted at an interface between gate insulator and channel layer when a negative bias is applied to gate electrode. This suppresses the current flow from drain electrode to source electrode. Threshold voltage (V_{TH}) refers to a point at which current starts to flow by the accumulated electrons. When V_{GS} is smaller than V_{TH}, the electrons are depleted at the bottom of the channel layer,

so I_{DS} does not flow. However, I_{DS} can flow by accumulated electrons when V_{GS} is larger than V_{TH}. At this time, I_{DS} equation can be defined differently for the linear region and saturation region as follows.

- Linear region: $V_{GS} - V_{TH} > V_{DS}$

$$I_{DS,lin} = \frac{W}{L}\mu_{lin}C_i\left\{(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right\} \quad (1)$$

- Saturation region: $V_{GS} - V_{TH} < V_{DS}$

$$I_{DS,sat} = \frac{W}{2L}\mu_{sat}C_i(V_{GS} - V_{TH})^2 \quad (2)$$

where W is the channel width, L is the channel length, C_i is the areal capacitance of gate insulator, μ_{lin} is the field-effect mobility in the linear region, and μ_{sat} is the field-effect mobility in the saturation region. Figure 1. 1a shows the trend of I_{DS} in linear and saturation regions of TFTs.

The main electrical parameters of TFTs are extracted from the transfer curve as shown in Figure 1. 1b. A brief description of each parameter is as follows [1].

- Field-effect mobility (***μ***)

Field-effect mobility represents the mobility of the electrons or holes under the

external bias, and is obtained from Equations (1) and (2).

$$\mu_{lin} = \frac{L}{WC_iV_{DS}}\frac{\partial I_{DS,lin}}{\partial V_{GS}} \tag{3}$$

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS,sat}}}{\partial V_{GS}}\right)^2 \tag{4}$$

- On/off current ratio ($\boldsymbol{I_{on/off}}$)

This is simply defined as the ratio of the minimum to the maximum I_{DS} as shown in Figure 1. 1b. The minimum I_{DS} is usually given by the gate leakage current (I_{GS}) or the noise in the measuring process and the maximum I_{DS} depends on the materials themselves such as channel and gate insulator layer.

- Subthreshold swing (SS)

Subthreshold swing means the inverse of the maximum slope of the $\log(I_{DS})$ in transfer curve of TFTs as shown in Figure 1. 1b. As the slope of I_{DS} is close to ∞, the transition is faster to the turn-on state. Therefore, it is more suitable for switching devices as SS, the reciprocal of slope, is close to zero. SS is obtained as follows.

$$SS = \left(\frac{\partial\log(I_{DS})}{\partial V_{GS}}\bigg|_{max}\right)^{-1} \tag{5}$$

- Turn-on voltage ($\boldsymbol{V_{on}}$)

Turn-on voltage is the V_{GS} at which I_{DS} starts to increase as shown in Figure 1. 1b.

- Threshold voltage ($\boldsymbol{V_{TH}}$)

Threshold voltage corresponds to the V_{GS} in which electrons are accumulated at an interface between gate insulator and channel layer. . Threshold voltage can be determined using linear extrapolation of the square root of drain current ($\sqrt{I_{DS}}$) versus gate voltage (V_{GS}) as shown in Figure 1. 1b.

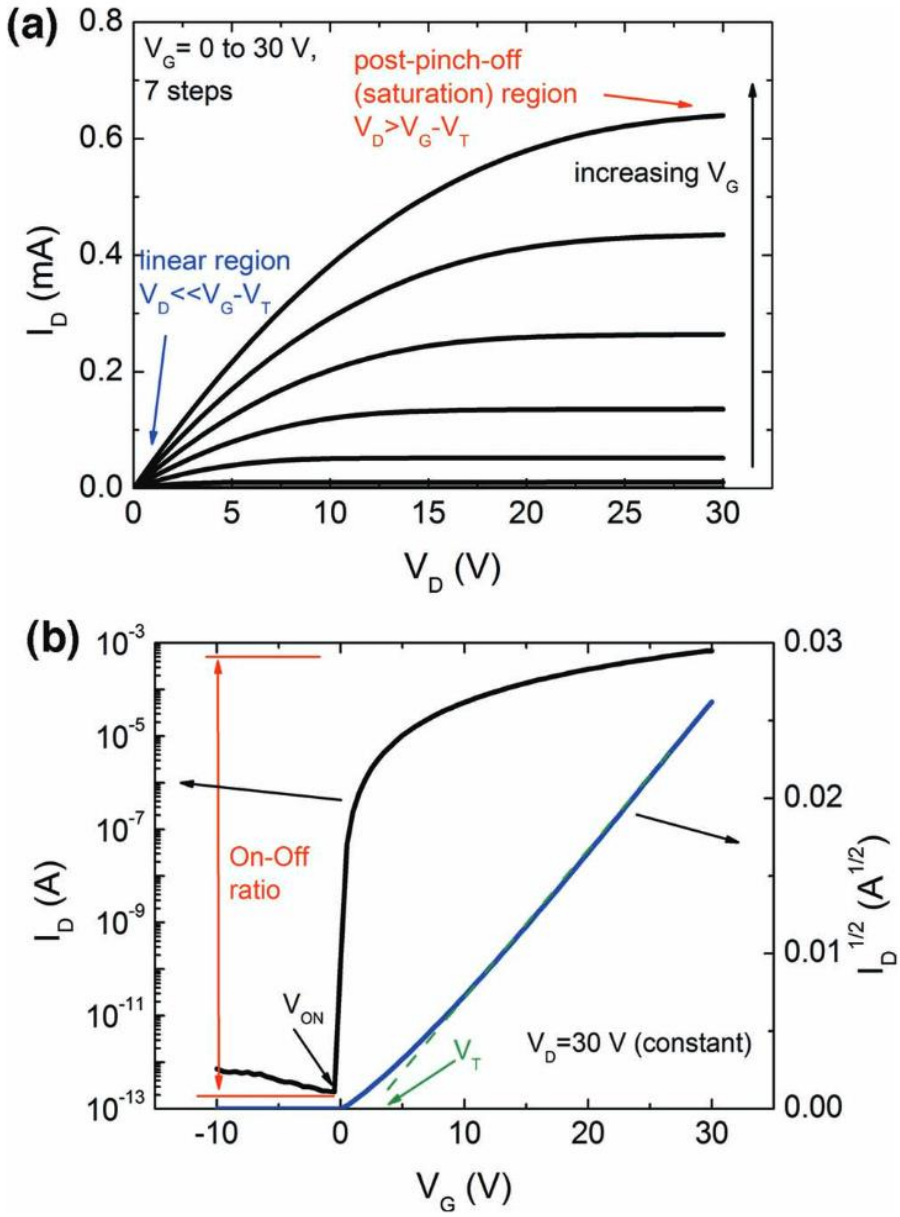

Figure 1. 1 Typical (a) output and (b) tranfer characteristics of a n-type oxide TFT [1]. Reproduced with permission of Ref. 1. Copyright 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

1.3 Dual-stacked TFTs

There are several important parameters for TFTs, but among them, the improvement of field-effect mobility, which is the most suitable for representing the performance of TFTs has been most actively studied such as various types of doping, material changes, structural changes, and surface treatment. However, there is a limit to using a single channel layer alone. To address this problem, the dual-stacked OS-based TFTs have been proposed. 2DEG is the major phenomenon to improve the field-effect mobility in dual-stacked OS-based TFTs [25-28]. It provides additional charge carriers, which dramatically improves field-effect mobility. However, off-current characteristics such as V_{TH} and I_{on} are inversely degraded. The trade-off relation between field-effect mobility and off-current characteristics is the biggest problem to be solved. 2DEG is well known, but the obvious mechanisms for improving field-effect mobility have not yet been clearly addressed.

1.4 Synaptic TFTs

Most modern computers adopt the von Neumann architecture with central processing unit (CPU), memory, and program structure. Various tasks could be processed in this architecture by replacing software without rearranging hardware. However, the development of machine learning and deep learning required tremendous data, which led computers to process more tasks than before. Such excessive tasks could cause the processing delays in CPU because all commands are processed sequentially on only one bus (a passage that connects memory and CPU). This phenomenon is called the von Neumann bottleneck [42,43]. Synaptic devices that emulate human brain are emerging as an alternative to overcome this problem. Human brain shows parallel and power efficient data processing with a high speed on a large scale. Especially, synapses are basic structures that transmit electrical or chemical signals from one neuron to another. These signals are selectively controlled by the connection strength between preneurons and postneurons, that is, the synaptic weight. Synapses are strengthened only when a lot of information is transmitted steadily through the synapses, otherwise they are weakened. This characteristic, synaptic plasticity, is a biological process in which synaptic activity causes changes in synaptic weight and is considered as a main principle of learning and memory [44]. It is generally divided into STP to support

computations and LTP to provide a physiological basis for learning and memory [45]. They are represented by excitatory postsynaptic current (EPSC) generated when the stimulus arrives at the presynaptic membrane [46].

Unlike typical TFTs, which require non-hysteresis and large current on/off ratio, synaptic TFTs basically require wide hysteresis (it refers to a phenomenon in which the drain current does not return to the starting point and falls to another value when the gate bias moves periodically or within the range). This is because the purpose of use is different. Typical TFTs, which are mainly used for switching purposes in the display industry, require fast on/off switching time and have to maintain the same current value under the same electrical conditions. However, synaptic TFTs require a wide hysteresis, which means that drain current accumulates. This corresponds to a synaptic TFTs that aim to memory characteristics. Therefore, in synaptic TFTs, the degree of the current accumulated by the stimulus, *i.e.*, the synaptic weight, is more important than the absolute field-effect mobility, which is an important factor in typical TFTs.

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Chapter 2

Conduction Mechanism for High-Performance Dual-Stacked Thin-Film Transistors

2.1 Introduction

New material technologies are emerging for commercialization in various electronic components such as next-generation displays, memory devices, energy storage devices, and power generators. In particular, ‘oxide electronics’ based on oxide semiconductor (OS) materials exceed the limit of amorphous Si [1,2]. Because the potential of OSs is significant, it can be used in various applications in the future. The OS has an energy band gap less than approximately 3 eV, allowing electrons to move through the energy band gap, which causes current to flow [3]. Accordingly, the OSs are widely used in switching devices because the current can be controlled by voltage regulation. OS-based thin film transistors (TFTs) are transparent and can be fabricated at low temperature, so they can be processed on transparent and flexible substrates such as plastic and polyimide [4-8]. OSs are in the spotlight as an active layer of TFTs because they are low cost and transparent, and research continues to this day [1,9]. Based on these characteristics, OS-based TFTs have been applied as switching devices to organic light-emitting diode (OLED) suitable for applications such as virtual reality (VR) and augmented reality (AR) [10,11]. With this transparency and low cost as well as high electrical performances, OS-based TFTs will be widely applied to many wearable devices [12].

Indium-gallium-zinc-oxide (IGZO) is commonly used as an active layer of TFTs due to low leakage current in the off state and an ideal threshold voltage formed near 0 V [1,12,13]. However, since it causes excessive power consumption and limits high-resolution displays due to low field-effect mobility (~10 $cm^2/V \cdot s$), it is difficult to apply them to next-generation displays, so improvement is needed. Although there have been many studies such as various types of doping [14-17], material changes [18-25], and OS films reinforcement [26-29], there have been limitations as a single OS-based TFT due to low field-effect mobility. In recent years, some atomic layer deposition (ALD) methods for channel layer deposition have been largely developed based on the advantages of sophisticated atomic control. Using this ALD technique, a study with ultra-high field-effect mobility (~70 $cm^2/V \cdot s$) has been reported [30-32]. However, these methods require a relatively high temperature (> 400 ℃) process, and thus it is difficult to apply them to next-generation devices using flexible substrates. Improving OS-based TFTs with high field-effect mobility through the low temperature process (<300 ℃) is very challenging task.

To address this problem, dual-stacked OS-based TFTs have been considered potential candidates for improving field-effect mobility [33-39]. However, it still has insufficient field-effect mobility (30~60 $cm^2/V \cdot s$), considerably low on-off

current ratio ($<10^6$), undesirable threshold voltage away from 0 V, or unstable reliability caused by bias stress. When the threshold voltage is formed far from 0 V and the on-off ratio is low, power consumption occurs even in the off state, and reliability problems such as degradation of the display devices may occur. Improve these things with high field-effect mobility is very difficult. Above all, the main bottleneck for applying OS-based dual-stacked TFTs to actual applications is a lack of a comprehensive understanding of conduction mechanisms, which hinders practical applications in the display industry.

Here, I newly present the exact role of the dual-stacked OSs consisting of the channel layer at the bottom and the buffer layer at the top in TFTs in the low temperature process (250 ℃) [40]. I also demonstrated the high performance dual-stacked OS-based TFTs with very high field-effect mobility, ideal threshold voltage near 0 V, high on-off current ratio, and stable reliability under bias stress. InO_x with high field-effect mobility was used as the channel layer, and IGZO with excellent off-state characteristics was used as the buffer layer. In more detail, when a gate bias is applied, the InO_x at the bottom of the dual-stacked OS supplies the accumulated electrons to the source-drain electrodes in an on-state, and the IGZO at the top of the dual-stacked OS reduces a leakage current in an off-state, thereby forming a threshold voltage near 0 V. The core of this mechanism is the

‘induced area’ derived from the dual-stacked OS interface. Due to the connection between the induced areas, electrical performances were significantly improved for a very high field-effect-mobility (~80 $cm^2/V \cdot s$), an ideal threshold voltage near 0 V, a low subthreshold swing (SS) value (<0.5 $V \cdot dec^{-1}$), and a very high current on-off ratio (>10^9). Furthermore, the stability of dual-stacked OS-based TFTs was maintained under positive bias stress (PBS) and negative bias stress (NBS). As a result, dual-stacked OS-based TFTs showed little threshold voltage shift of 2.62 V and 1.72 V in PBS and NBS, respectively, similar to the results of a single IGZO TFT.

First of all, I proposed a novel conduction mechanism and analyzed the interface phenomena in the dual-stacked OS using the newly defined concept of induced area. When bias is applied or OSs are connected, an induced areas are always formed at the interface, and the connection between these induced areas can explain the conduction mechanism. Based on the interactions between these induced areas, a conduction mechanism of dual-stacked OS-based TFTs has been newly developed.

For more quantitative analysis, the equivalent circuit model was also applied to dual-stacked OSs in TFT. Each resistance constituting an equivalent circuit was extracted from a transmission line method (TLM). Specifically, contact resistance

and bulk resistance in each single OS (InO_x and IGZO) were extracted, and based on this, it is possible to confirm in detail the current flow in the dual-stacked OS. As the process of current conduction can be specifically identified through this mechanism verified through the equivalent circuit, it is possible to implement a dual-stacked OS-based TFTs with remarkably improved characteristics. In addition, they show great potential for the next-generation display industry.

2.2 Fabrication of dual-stacked TFTs

Figure 2. 1a shows the schematic diagram of a dual-stacked OS-based TFT composed of a channel layer at the bottom and a buffer layer at the top. The field-effect mobility was improved by using InO_x as the channel layer, and the stability at an ideal threshold voltage near to 0 V, a high on-off ratio, a low off current level, and bias stress was ensured by using IGZO as the buffer layer. It is essential to design an optimal structure that can utilize both the advantages of InO_x and IGZO by identifying the exact mechanism. These OSs were deposited by radio-frequency (RF) sputtering at room temperature. After that, rapid thermal annealing (RTA) was carried out immediately after deposition of OSs. This RTA method is most effective compared to other annealing methods such as annealing in tube furnace and annealing in glove box, and detailed results are shown in Figure 2. 2 and Table 2. 1.

A TEM image of a TFT device with a dual-stacked OS is shown in Figure 2. 1b. In the image, it can be seen that the thickness of InO_x is 9.86 nm and the thickness of IGZO is 30.24 nm, which is similar to the optimal thicknesses of 10 nm and 30 nm, respectively. In addition, atomic components were extracted using a high-resolution transmission electron microscopy (HR-TEM) to ensure that each layer was properly formed (Figure 2. 1c). As expected, it could be verified through the

distribution of atomic components, such as In, Ga, Zn and O, that InO_x and IGZO were well formed. The depth profile of the TEM including each component (In, Ga, and Zn) was shown to clearly confirm the thickness (Figure 2. 3). In order to evaluate the crystallinity of the InO_x and IGZO thin films, X-ray diffraction (XRD) analysis was also performed as shown in Figure 2. 4. The XRD pattern shows (222) crystalline orientation at the InO_x film but amorphous at the IGZO film.

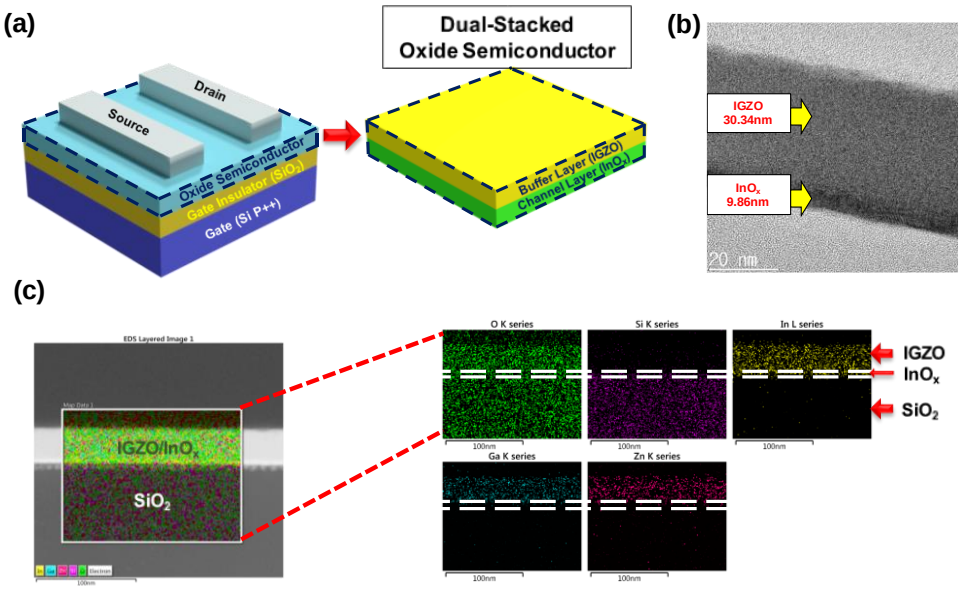

Figure 2. 1 Schematic diagram of a dual-stacked OS-based TFT and cross sectional images. (a) Dual-stacked OS-based TFT composed of InO_x as a channel layer and IGZO as a buffer layer. (b) Cross-sectional TEM images of a dual-stacked OS-based TFT. (c) TEM image mapping that represents atomic dispersion. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

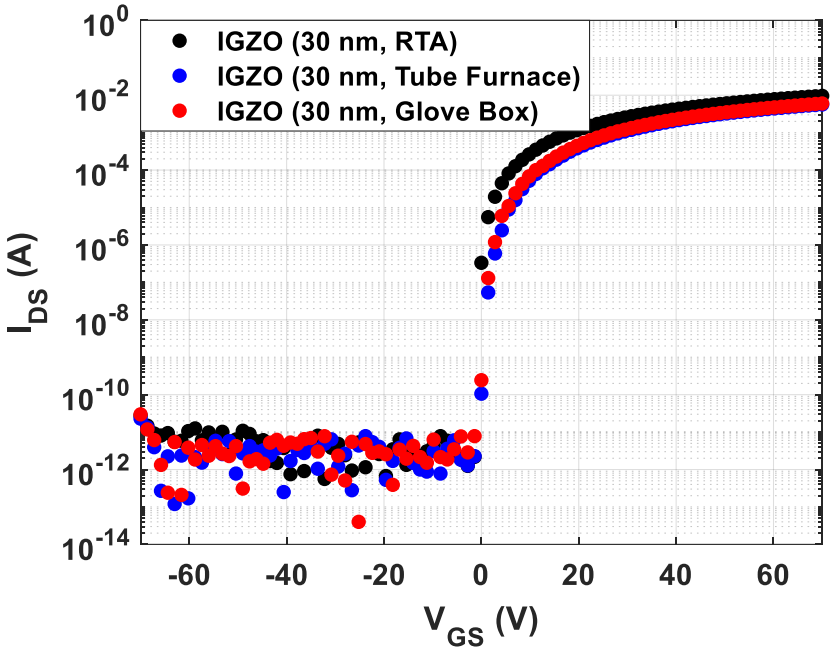

Figure 2. 2 Transfer curves of the single IGZO TFTs under the same conditions (250 ℃, 90 s) of annealing methods: RTA, annealing in tube furnace, and annealing in glove box (V_{DS} = 20V). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

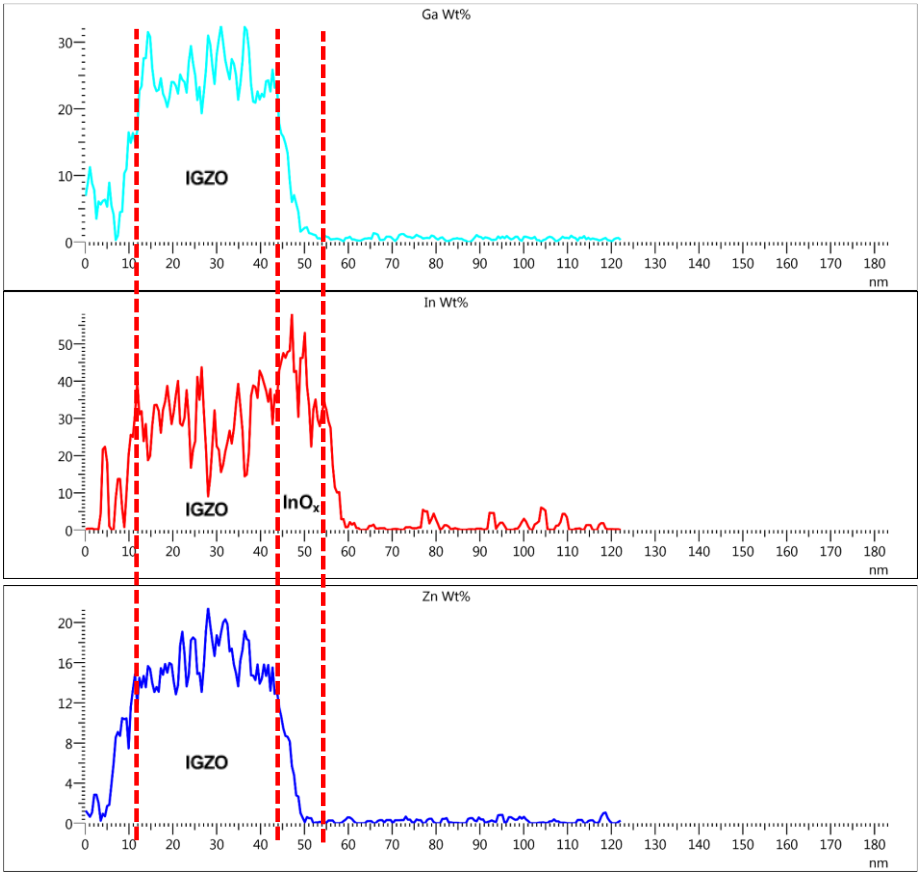

Figure 2. 3 The depth profile (wt%) of the TEM that represents each component (In, Ga, and Zn). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

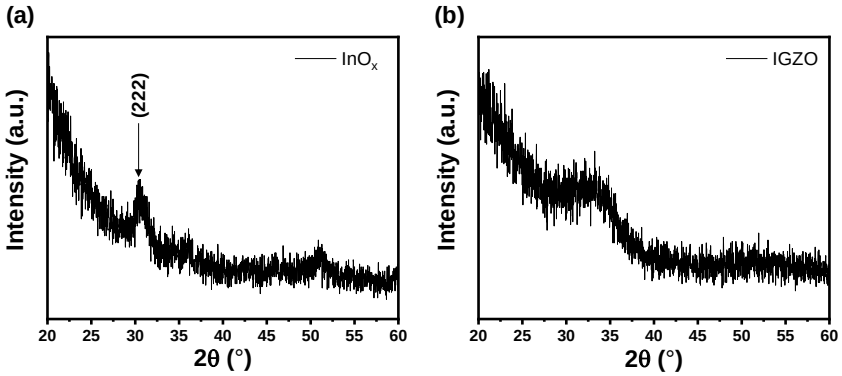

Figure 2. 4 XRD analysis of (a) InOx (10 nm) and (b) IGZO (30 nm) films. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Annealing Conditions / Parameters	RTA	Tube Furnace	Glove Box
Field-Effect Mobility ($cm^2/V \cdot s$)	19.85	17.24	16.82
I_{on}/I_{off}	$>10^9$	$>10^9$	$>10^9$
Subthreshold Swing ($V \cdot dec^{-1}$)	0.29	0.51	0.53
Threshold Voltage (V)	1.12	5.26	5.74

Table 2. 1 Electrical parameter values for the single IGZO TFTs according to the annealing methods under the same conditions (250 ℃ for 90 s): RTA, annealing in tube furnace, and annealing in glove box. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.3 Electrical characteristics of TFTs

Figure 2. 5a shows the transfer curves of three types of OS-based TFTs. The red one and the blue one are single OS-based TFTs consisting of InO_x and IGZO, respectively. The thickness of InO_x and IGZO are 10 nm and 30 nm, respectively. And the pink one is a dual-stacked OS-based TFT composed of InO_x and IGZO. In dual-stacked OS, the thickness of InO_x and IGZO is 10 nm and 30 nm, respectively, the same thickness as that of a single InO_x TFT and IGZO TFT. Their optimized thicknesses were determined based on the performance according to the thickness of a single InO_x layer and a single IGZO layer respectively. Details can be found in Figure 2. 6, Table 2. 1, and Table 2. 2.

For a single InO_x TFT, a relatively high on-state current level provides excellent field-effect mobility [34,41,42]. However, the off-state current level is also high, which can lead to excessive power consumption and poor switching signals in the circuits. In addition, a single InO_x TFT represents a negative shift turn-on voltage away from 0 V, resulting in additional power consumption. Given all of this, it is difficult to utilize the single InO_x TFTs in display industries that require accurate switching system. For a single IGZO TFT, it shows low off-state current level of 1 pA (10^{-12} A) and turn-on voltage near 0 V. They play an important role in preventing leakage currents [1,4,7,8]. For this critical reason, OS-based TFTs

with both InO_x and IGZO advantages are needed, and they can be realized through dual-stacked OS-based TFT using InO_x and IGZO as channel layer at the bottom and buffer layer at the top, respectively. A dual-stacked TFT represents a low off-state current level and an ideal turn-on voltage near 0 V, similar to a single IGZO TFT. It also indicates a high on-state current level of at least 10 mA (10^{-2} A) at gate bias of 70 V similar to a single InO_x TFT. It is more clearly shown in the inset of Figure 2. 5a.

Important electrical parameters representing the performance of the TFTs include field-effect mobility, threshold voltage, SS value, and current on-off ratio, and they can be extracted from the transfer curve shown in Figure 2. 5a [1,4]. In case of field-effect mobility, as shown in the left y-axis of Figure 2. 5b, it was calculated using the following linear mobility equation:

$$\mathrm{I}_{DS} = \mu C_i \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right), \quad (2.\ 1)$$

where μ is the field-effect linear mobility, C_i is the capacitance of the gate insulator, W is the channel width, and L is the channel length. A single InO_x TFT and a dual-stacked TFT showed very high field-effect mobility of 77.01 $cm^2/V \cdot s$ and 74.38 $cm^2/V \cdot s$ respectively. On the other hand, a single IGZO TFT showed relatively low field-effect mobility of 19.62 $cm^2/V \cdot s$. For the threshold voltage, as shown in the right y-axis of Figure 2. 5b, it was calculated by fitting

a straight line with the square root plot of I_{DS} versus V_{GS} as shown in Equation 2. 1. A single IGZO TFT and a dual-stacked OS-based TFT represented threshold voltage of 1.12 V and 4.36 V respectively. On the other hand, InO_x TFT showed a threshold voltage of -21.81 V, which showed a negative shift away from 0 V. The threshold voltage can be determined using linear extrapolation of the square root of the drain current ($\sqrt{I_{DS}}$) versus the gate voltage (V_{GS}) [4]. Figure 2. 6 shows three types of threshold voltages by linear extrapolation. In the case of SS, as shown in the left y-axis of Figure 2. 5c, it was calculated in reverse order of the maximum slope of the transfer characteristic:

$$SS = \left(\frac{dlog(I_{DS})}{dV_{GS}} \Big|_{max} \right)^{-1}. \quad (2.\ 2)$$

The single IGZO TFT and the dual-stacked OS-based TFT showed very low SS values with 0.28 V·dec^{-1} and 0.47 V·dec^{-1}, respectively. On the other hand, a single InO_x TFT manifested a slightly higher SS value of 2.42 V·dec^{-1}, and thus, the slope of the transfer curve close to the turn-on voltage was high. In the case of the on-off current ratio, as shown in the right y-axis of Figure 2. 5c, both the single IGZO TFT and the dual-stacked OS-based TFT showed a very high on-off current ratio over 10^9. On the other hand, a single InO_x TFT showed a low on-off current ratio of about 10^5.

When the above results are considered, the dual-stacked OS-based TFTs showed

the most prominent characteristics. It is noteworthy that the field-effect mobility and off-state characteristics (threshold voltage and current on-off ratio), which have been considered trade-offs, have simultaneously improved [43,44]. This is due to the induced area formed at the interface of the OSs because of electron confinement by band-offset, which is a key point of the working mechanism, in the newly proposed dual-stacked OS-based TFTs.

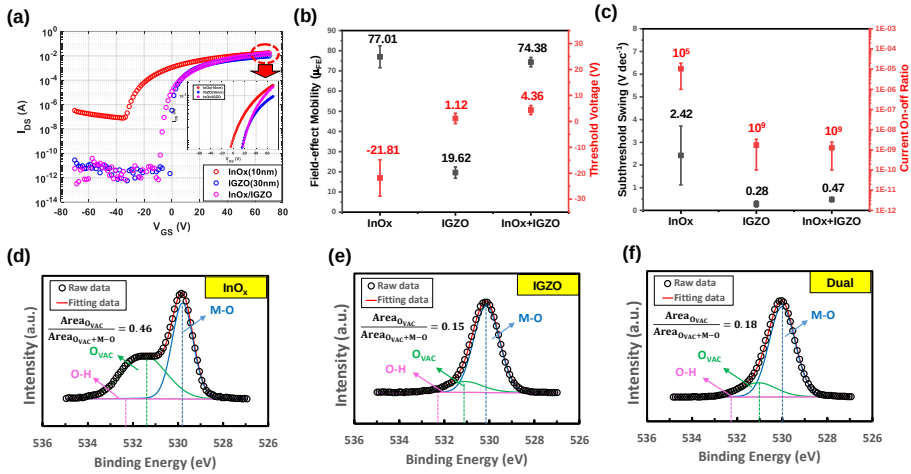

Figure 2. 5 Transfer curves, electrical properties, and X-ray photoelectron spectroscopy (XPS) analysis. (a) Transfer curves for a single InO_x TFT, a single IGZO TFT, and a dual-stacked OS-based TFT (V_{DS} = 20V). Inset: Zoom in region of the on-state current. Electrical characteristics extracted from the transfer curves : (b) field-effect mobility (black), threshold voltage (red), (c) subthreshold voltage (black), and current on-off ratio (red). O 1s XPS analysis for (d) a single InO_x TFT, (e) a single IGZO TFT, and (f) a dual-stacked OS-based TFT. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

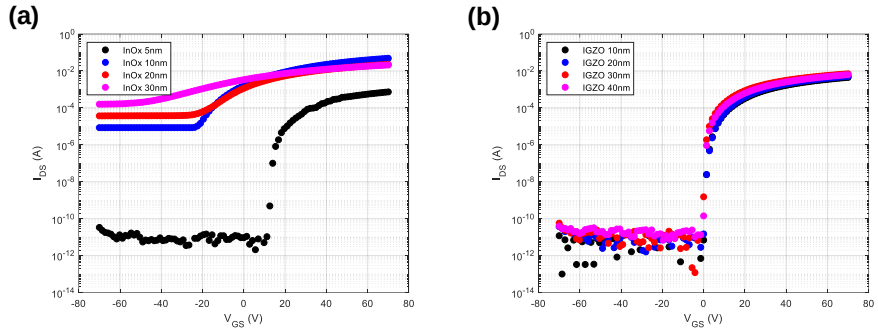

Figure 2. 6 Transfer curves according to the thickness of OS. (a) Transfer curves of a single InO_x TFTs according to the thickness (5, 10, 20, and 30 nm). (b) Transfer curves of a single IGZO TFTs according to the thickness (10, 20, 30, and 40 nm). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

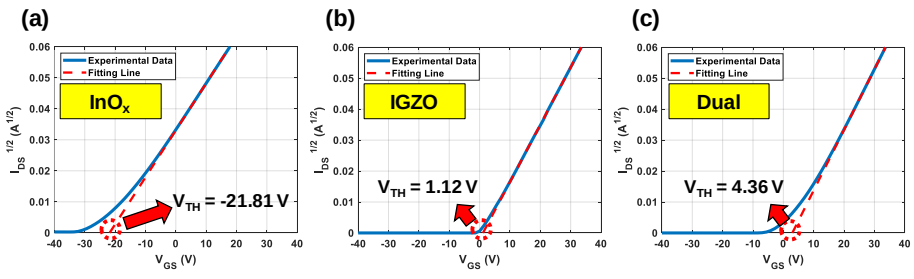

Figure 2. 7 Transfer curves of $\sqrt{I_{DS}}$ versus V_{GS} to extract threshold voltage using linear extrapolation for (a) a single InO_x TFT, (b) a single IGZO TFT, and (c) a dual-stacked OS-based TFT. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Thickness / Parameters	5 nm	10 nm	20 nm	30 nm
Field-Effect Mobility ($cm^2/V \cdot s$)	3.21	70.09	64.20	43.81
I_{on}/I_{off}	$>10^9$	$>10^4$	$>10^2$	$>10^2$
Subthreshold Swing ($V \cdot dec^{-1}$)	0.52	6.72	13.47	32.87
Threshold Voltage (V)	19.72	-18.38	-22.50	-38.95

Table 2. 2 The values of the electrical parameters in single InO_x TFTs according to the thickness (5, 10, 20, and 30 nm). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Parameters \ Thickness	10 nm	20 nm	30 nm	40 nm
Field-Effect Mobility ($cm^2/V \cdot s$)	15.49	17.23	20.64	20.54
I_{on}/I_{off}	$>10^8$	$>10^9$	$>10^9$	$>10^8$
Subthreshold Swing ($V \cdot dec^{-1}$)	0.39	0.44	0.43	0.37
Threshold Voltage (V)	5.46	5.57	1.59	2.59

Table 2. 3 The values of the electrical parameters in single IGZO TFTs according to the thickness (10, 20, 30, and 40 nm). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.4 Analysis of oxygen vacancy and energy bandgap in OSs

XPS measurements were performed to identify the oxygen vacancies in InO_x and IGZO constituting the dual-stacked OS-based TFTs. For more accurate measurements, etching process was performed a thickness of 1/3 to 1/2 before the measurement was started. This eliminates measurement noise that may appear on the material surface. Figure 2. 5d-5f show the chemical changes in the O 1s spectrum of three types of TFTs measured by X-ray photoelectron spectroscopy (XPS). For further analysis, the O 1s spectrum was fitted by the Gaussian-Lorentzian function. For a single InO_x TFT shown in Figure 2. 5d, the O 1s spectrum could be divided into three peaks centered at 532.2, 531.3, and 529.8 eV, corresponding to a oxygen bond of the hydroxide (O-H bond), the oxygen vacancy (O_{vac}), and metal-oxide bond without oxygen vacancy (M-O bond), respectively [28,45]. For a single IGZO TFT shown in Figure 2. 5e, the O 1s spectrum could be divided into three peaks centered at 532.2, 531.1, and 530.1 eV. Also, for dual-stacked OS-based TFT shown in Figure 2. 5f, the O 1s spectrum could be divided into the three peaks centered at 532.2, 531.0, and 530.0 eV. O_{vac} / (O_{vac} + M-O bond) area ratios used to verify the oxygen vacancy effects are 0.46 (single InO_x TFT), 0.15 (single IGZO TFT), and 0.18 (dual-stacked OS-based TFT) [26]. A single IGZO TFT and a dual-stacked OS-based TFT exhibit

very low area ratios, which are expected to affect improved off-state characteristics such as threshold voltage and current on-off ratio excluding field-effect mobility. Oxygen vacancies typically supply conductive carriers, but they act as carrier traps and cause instability in the electrical transport [46,47]. These trap sites are closely related to the SS of the oxide semiconductors. The higher the trap site, the higher the SS value, and the lower the trap site, the lower the SS value [48,49]. This is consistent with the trend of the data shown in Figure 2. 5b and 5c.

It is widely known that the reduction in oxygen vacancy means that the carrier density decreases and thus the electron mobility decreases [50]. However, the dual-stacked TFT showed high field-effect mobility similar to that of a single InO_x TFT, although the oxygen vacancy was low. This means that there are charge carriers that can be involved in current conduction except for oxygen vacancies. Such charge carriers exist at the interface of the OSs in TFTs because of electrons confined by band-offset.

To clearly check the existence of confined electrons at the interface of OSs and understand the mechanism of current conduction, it is important to understand the energy band structure diagram of OSs in TFTs. To explain this, ultraviolet-visible spectroscopy (UV-vis) and ultraviolet photoelectron spectroscopy (UPS)

measurements were performed. First, the optical band gap energy of the InO_x and IGZO films were calculated based on the UV-vis measurement data as shown in Figure 2. 8, respectively [51]. Then, the energy gap difference from the valence band maximum (VBM) to the Fermi energy level and the work function was extracted from the UPS measurement data as shown in Figure 2. 8b. Based on these data, the energy band gap structure of the dual-stacked OS composed of InO_x and IGZO was drawn as shown in Figure 2. 8c [52]. It was described in equilibrium. Electrons are confined in the induced area bent by the band-offset and play a very important role in current conduction as the charge carriers in a dual-stacked OS-based TFTs.

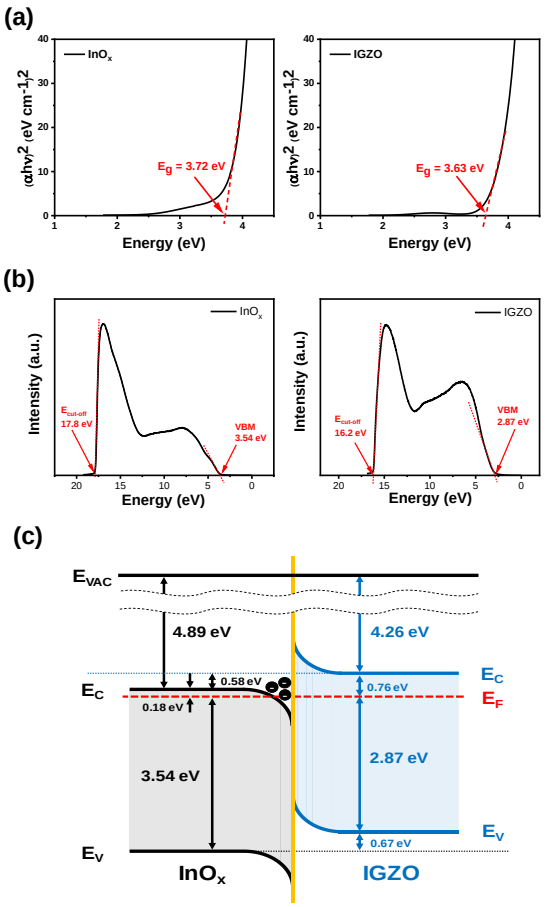

Figure 2. 8 Optical analysis and energy band diagrams of a dual-stacked OS-based TFT. (a) The PL spectrum calculated from UV-vis data of the InO_x and IGZO films. (b) UPS spectrum showing cut-off and VBM energy of InO_x and IGZO films. (c) An energy band diagram of a dual-stacked OS-based TFT based on (a) and (b). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.5 Conduction mechanism in a single OS-based TFTs

Theoretical studies on the conduction mechanisms in the single OS-based TFTs have been studied a lot so far, and specific theories such as electron accumulation or depletion at the boundary between semiconductor and gate insulator have been established [1,3,12]. However, the exact conduction mechanisms in dual-stacked OS-based TFTs have not yet been reported. In this study, I present a new types of conduction mechanism that can be applied to both single OS-based TFTs and dual-stacked OS-based TFTs. The key is the overlap between the induced areas due to electrons confined by the band-offset.

Figure 2. 9a-9h show the conduction mechanisms of accumulation mode and depletion mode in a single OS-based TFT. When V_{GS} is higher than threshold voltage, electrons are accumulated on the surface of the oxide semiconductor adjacent to gate insulator and current flows, which is called accumulation mode. When V_{GS} is lower than threshold voltage, electrons are depleted on the surface of the oxide semiconductor adjacent to gate insulator and no current flows, which is called depletion mode. First of all, the induced area by the gate bias is formed at the bottom of OS layer adjacent to the gate insulator, which is named as gate-bias-induced area (GBIA). And another area induced by the source-drain bias is formed at the top of OS layer adjacent to the source-drain electrodes, which is

named as electrode-bias-induced area (EBIA). These two areas are defined when V_{GS} and drain voltage (V_{DS}) are applied. Based on these, Figure 2. 9a shows GBIA and EBIA in accumulation mode of single OS-based TFT. When positive gate bias is applied, electrons accumulate at GBIA (red area) of OS layer as shown in the top image of Figure 2. 9a. As gate bias increases, GBIA becomes larger and this makes electron accumulate more. EBIA (green area) also becomes larger as source bias increases and this means that the deeper area is affected by source-drain bias.

GBIA and EBIA are always formed together and they can be divided into three cases depending on the thickness of OS layer. First, as shown in Figure 2. 9b, it is the case that OS layer is included in GBIA. As these two areas are connected, electrons accumulated in GBIA can be involved in current flow from source to drain in EBIA. As the thickness of OS layer increases in the range of GBIA, the field-effect mobility increases proportionally because OS layer overlaps more with GBIA where the electrons are accumulated. Second, as shown in Figure 2. 9c, it is the case that OS layer is included in the combined area of EBIA and GBIA. Even in this case, since GBIA and EBIA are connected, the electrons accumulated in GBIA can be involved in current flow from source to drain in EBIA. Since GBIA is already included within OS layer, all electrons accumulated

in GBIA can always be involved even if the thickness of OS layer increases. Thus, it represents maximum field-effect mobility, and this quantity remains unchanged. Third, as shown in Figure 2. 9d, it is the case that OS layer is not included in the combined area of EBIA and GBIA. In this case, the electrons accumulated in GBIA cannot be involved in current flow because GBIA and EBIA are not connected, so dual-stacked OS-based TFTs represent the bulk characteristics of EBIA where current flows directly.

The tendency in the depletion mode is similar to the accumulation mode. When applying gate and source-drain bias in TFT, GBIA and EBIA are formed as accumulation mode as shown in Figure 2. 9e. However, there is a difference that electrons are depleted in GBIA, unlike accumulated electrons in accumulation mode. GBIA and EBIA are always formed together and they can be divided into three cases depending on the thickness of OS layer, as the above mentioned accumulation mode. First, as shown in Figure 2. 9f, it is the case that the OS layer is included in the GBIA. In this case, there is little current flow from source to drain regardless of the thickness of OS layer because electrons are depleted in GBIA. Second, as shown in Figure 2. 9g, it is the case that the OS is included in the combined area of EBIA and GBIA. Even in this case, there is little current flow from source to drain due to the effects of the depleted electrons in GBIA

connected to EBIA. Even if the thickness of OS layer increases, there is still little current flow as long as EBIA is connected to GBIA with depleted electrons. Third, as shown in Figure 2. 9h, it is the case that the OS is not included in the combined area of EBIA and GBIA. In this case, since GBIA and EBIA are not connected, the current flow is not affected by the depleted electrons in GBIA but only affected by the characteristics of the bulk area in EBIA. This tendency is similar to accumulation mode shown in Figure 2. 9d.

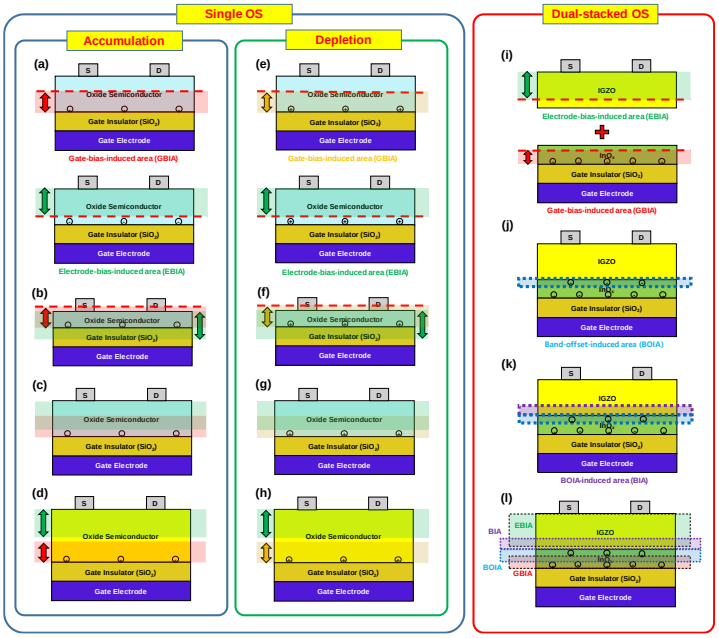

Figure 2. 9 Conduction mechanism in a single OS-based TFT (accumualtion and depletion mode) and dual-stacked OS-based TFT. (a), (e) Two kinds of areas (GBIA and EBIA) induced by gate bias and source-drain bias. Relationship between GBIA and EBIA when (b), (f) only GBIA including OS, (c), (g) GBIA and EBIA including OS, and (d), (h) GBIA and EBIA not including OS. (i) GBIA induced in the bottom OS layer (InO_x) and EBIA induced in the upper OS layer (IGZO). (j) BOIA induced from confined electrons by band-offset. (k) BIA induced by BOIA. (l) Final connection between GBIA, BOIA, BIA, and EBIA. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.6 Conduction mechanism in a daul-stacked OS-based TFTs

Figure 2. 9i-9l show the conduction mechanism of dual-stacked OS layers in the accumulation mode of TFT based on the conduction mechanism in single OS layer of TFT mentioned above. Since GBIA is formed at the bottom of the OS layer adjacent to the gate insulator, it affects the bottom OS layer in dual-stacked OS. Similarly, since EBIA is formed at the top of OS layer adjacent to the source-drain electrodes, it affects the upper OS layer in dual-stacked OS. In this study, InO_x with high field-effect mobility was used as the bottom OS layer, and IGZO with good off-state performance such as threshold voltage and current on-off ratio was used as the upper OS layer.

As shown in Figure 2. 8c above, in the dual-stacked structure, the electrons are confined by band-offset at the boundary between IGZO and InO_x and this effect cannot be explained by single OS structure. As a result, as shown in Figure 2. 9j, the area induced by confined electrons is formed at the top of InO_x layer and named as band-offset-induced area (BOIA). It is consistent with Figure 2. 8c, representing the energy band diagram. BOIA induces another area in the bottom of IGZO layer, named as BOIA-induced area (BIA), as shown in Figure 2. 9k. In summary, BOIA and BIA are formed at each of the boundary of the connected semiconductors when upper OS layer and bottom OS layer are junctioned. When

gate bias and source-drain bias are applied, GBIA and EBIA are formed and they are connected to BOIA and BIA as shown in Figure 2. 9l. After all, GBIA with accumulated electrons is connected to EBIA sequentially, which can lead to high current flow. However, if the thickness of IGZO which means the upper layer in dual-stacked OS increases, EBIA and BIA is not connected. It means that the accumulated electrons in GBIA cannot be involved in current flow from source to drain, resulting in the bulk characteristics of EBIA.

Meanwhile, in the case of depletion mode of dual-stacked OS-based TFT, the depleted electrons in GBIA can be considered as a key factor instead of the accumulated electrons. GBIA and EBIA are formed by gate bias and source-drain bias respectively, and they are connected to BOIA and BIA as accumulation mode. Then, there is little current flow from source to drain by the influence of depleted electrons in GBIA. In addition, if the thickness of IGZO increases, it represents the characteristics of the bulk characteristics of EBIA as accumulation mode.

It is important to design the optimal thickness of OSs due to the characteristics of dual-stacked structure. Especially, in the case of IGZO used as the buffer layer at the top in dual-stacked OS-based TFTs, the field-effect mobility convergences into maximum value as the thickness of IGZO increases within the overlapping

range of EBIA and BIA, as shown in Figure 2. 10 and Table 2. 4. On the other hand, in the case of InO_x used as the channel layer at the bottom, the minimum optimized thickness should be maintained to reduce leakage current. Therefore, only the thickness of IGZO were adjusted to verify the conduction mechanism. This precise design of the thickness of OS layers will provide the realistic design rules for actual applications in the display industry.

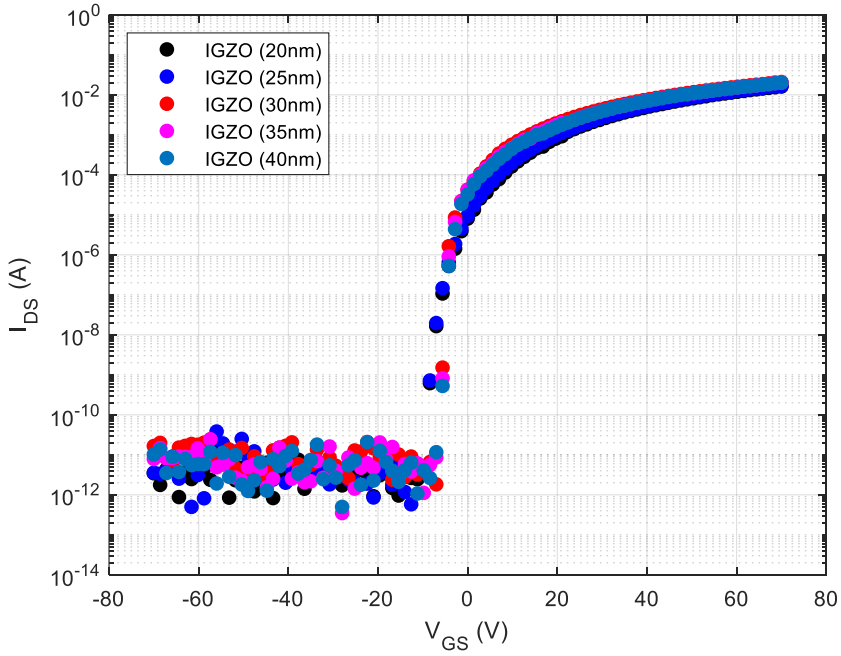

Figure 2. 10 Transfer curves of the dual-stacked OS-based TFTs according to the thickness of IGZO (20, 25, 30, 35, and 40 nm) with InO_x thickness fixed (10 nm). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Parameters \ Thickness	20 nm	25 nm	30 nm	35 nm	40 nm
Field-Effect Mobility ($cm^2/V \cdot s$)	61.27	65.41	73.32	73.35	73.28
I_{on}/I_{off}	$>10^8$	$>10^9$	$>10^9$	$>10^9$	$>10^9$
Subthreshold Swing ($V \cdot dec^{-1}$)	0.52	0.46	0.43	0.44	0.42
Threshold Voltage (V)	4.27	4.17	4.34	4.58	4.12

Table 2. 4 The values of the electrical parameters in dual-stacked OS-based TFTs according to the thickness of IGZO (20, 25, 30, 35, and 40 nm) with InO_x thickness fixed (10 nm). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.7 Transmission line method (TLM) for the resistances

Most analyses about conduction mechanisms are performed without external bias because it is very difficult to explain them in the actual operating state. They are insufficient to explain the conduction mechanism, so new analysis is required under actual operating conditions. For this purpose, transmission line method (TLM) was introduced. It is widely used to extract the resistance values such as contact resistance, bulk resistance, and sheet resistance in operating condition depending on the channel length [53-57]. Figure 2. 11a shows the top view and side view of the actual model for using TLM with channel width of 500 μm and different channel length of 30 μm (L_1), 50 μm (L_2), 80 μm (L_3), 120 μm (L_4), and 200 μm (L_5). Figure 2. 11b is an example for calculation using TLM. The y-values (R_T) of each black dot are extracted from the reciprocal of the slope of I-V curve which are measured along different channel length. The trend line is drawn to obtain the y-intercept which means double of the contact resistance, and x-intercept which means double of the transfer length. Transfer length is generally used to calculate the specific contact resistance (ρ_C) [58-60]. However, in this study, it was not used because the total resistance was calculated by contact resistance and bulk resistance.

Figure 2. 11c-11e show the actual total resistance (R_T) on V_{GS} of 20 V in single

InO_x (10 nm), single IGZO (30nm), and dual-stacked OS (InO_x 10 nm + IGZO 30 nm) depending on the channel length. Bulk resistance was calculated by subtracting two contact resistance values from the total resistance value. The exact values of R_C, R_B, and R_T for each material are listed in Table 2. 5. (Bulk resistance in dual-stacked OS is the value where dual-stacked OS layer is considered one effective OS layer.) In all materials, bulk resistance was much greater than contact resistance. The ratio of contact resistance to bulk resistance (R_C/R_B) was measured in single InO_x, single IGZO, and dual-stacked OS with very low values of 2.0 %, 0.46 %, and 2.3 %, respectively.

The total resistance (or bulk resistance) of InO_x was over 10 times lower than that of IGZO, which corresponds to the higher field-effect mobility in single InO_x TFT than in single IGZO TFT. On the other hand, the total resistance in dual-stacked OS-based TFT was almost same as that of single InO_x TFT which corresponds to the high field-effect mobility in dual-stacked OS-based TFT similar to that in single InO_x TFT, as shown in Figure 2. 5b. Figure 2. 12 also represents TLM curves on V_{GS} of 10 V and 40 V measured in single InOx, single IGZO, and dual-stacked OS. The exact values of R_C, R_B, and R_T for each material are listed in Table 2. 6 and Table 2. 7. The trends of each resistance in V_{GS} of 10 V and 40 V were similar to that of V_{GS} of 20 V.

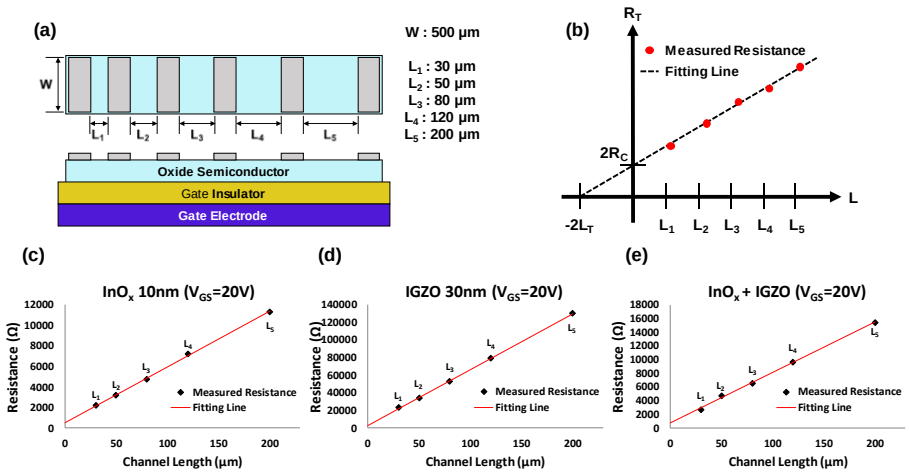

Figure 2. 11 Resistance analysis using transmission line method (TLM). (a) Top view and side view of the model for measurement using TLM. (b) Method to obtain contact resistance (y-intercept) using TLM. Plotting of total resistance according to channel length at constant V_{GS} (20 V) in (c) InO_x (10 nm) and (d) IGZO (30 nm), and (e) InO_x + IGZO (10 nm + 30 nm). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

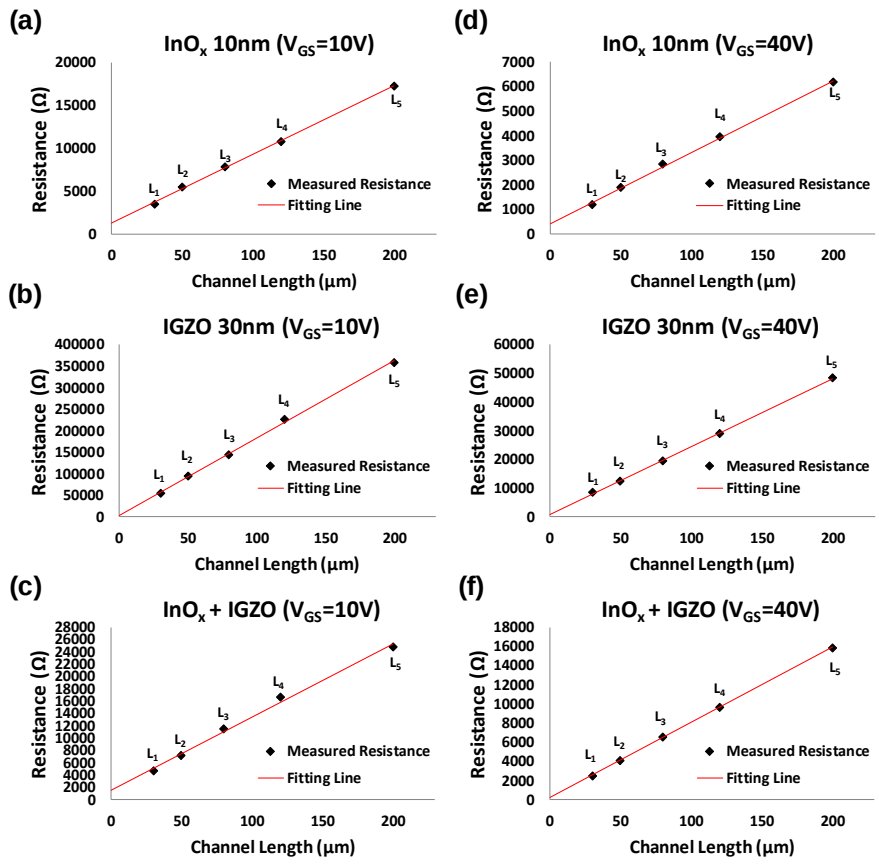

Figure 2. 12 Plot of total resistance according to channel length at V_{GS} of 10 V (a)-(c), and V_{GS} of 40 V (d)-(f). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Resistances / Materials	R_C (Ω)	R_B (Ω)	R_T (Ω)	R_C/R_B (%)
InO_x (10 nm)	250	12500	13000	2.0
IGZO (30 nm)	650	140000	141300	0.46
InO_x + IGZO (10 nm + 30 nm)	350	15000	15700	2.3

Table 2. 5 The resistances and the ratio of contact resistance to bulk resistance in single InOx TFT, single IGZO TFT, and dual-stacked OS-based TFT (V_{GS} = 20 V at 200 μm of channel length). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Resistances / Materials	R_C (Ω)	R_B (Ω)	R_T (Ω)	R_C/R_B (%)
InO_x (10 nm)	600	19500	20700	3.1
IGZO (30 nm)	1800	415000	418600	0.43
InO_x + IGZO (10 nm + 30 nm)	700	27000	28400	2.5

Table 2. 6 The resistances and the ratio of contact resistance to bulk resistance in single InOx TFT, single IGZO TFT, and dual-stacked OS-based TFT (V_{GS} = 10 V at 200 μm of channel length). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Resistances / Materials	R_C (Ω)	R_B (Ω)	R_T (Ω)	R_C/R_B (%)
InO_x (10 nm)	180	6500	6860	2.8
IGZO (30 nm)	500	49000	50000	1.0
InO_x + IGZO (10 nm + 30 nm)	190	7500	7880	2.5

Table 2. 7 The resistances and the ratio of contact resistance to bulk resistance in single InOx TFT, single IGZO TFT, and dual-stacked OS-based TFT (V_{GS} = 40 V at 200 μm of channel length). Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.8 Equivalent circuit modeling: single and dual-stacked OS

Equivalent circuit model allows the use of resistance values measured under actual operating conditions, enabling more accurate verification of the conduction mechanism [61,62]. By using contact resistance and bulk resistance of single OS-based TFT, electronic circuits can be built and it is shown in Figure 2. 13a. This circuit consists of two contact resistances and one bulk resistance (The resistance between probe tip and electrodes is negligible because it is a metal-to-metal contact. The resistance between OS and electrodes may vary slightly depending on the direction of the current, but it was considered the same value because it is smaller than bulk resistance). Since the resistances are affected by accumulated electrons formed at the boundary between OS and gate insulator, they are absolutely dependent on the gate voltage which induces these electrons. Figure 2. 13b shows the circuitous approach in dual-stacked OS-based TFT. This circuit consists of four contact resistances (two R_{C12} and two R_{C2}) and two bulk resistances (R_{B1} and R_{B2}). As in single OS-based TFT, bulk resistance of the bottom OS layer (R_{B1}) also depends on the gate voltage, so the calculated value in single OS can be applied. However, bulk resistance of the upper OS layer (R_{B2}) does not contact directly with the gate insulator, so it should be estimated from other resistive components because it is rarely affected by the accumulated

electrons.

Figure 2. 13c is an equivalent circuit in single OS-based TFT based on Figure 2. 13a. This is a simple series circuit, where each resistance can be obtained by electrical measurement. Total resistance can be calculated by followed equation:

$$R_T = 2R_C + R_B, \quad (2.\ 3)$$

where R_T is total resistance, R_C is contact resistance, and R_B is bulk resistance. Resistance values in Table 2. 5 were calculated by this Equation 2. 3.

Figure 2. 13d is an equivalent circuit in dual-stacked OS-based TFT based on Figure 2. 13b. This is a circuit mixed in series and parallel, and all measured resistance values in single OS-based TFT (Figure 2. 13c) are available in this circuit except for R_{C12} and R_{B2}. Total resistance can be calculated by followed Equation:

$$R_T = 2R_{C2} + \frac{1}{\frac{1}{R_{B2}} + \frac{1}{2R_{C12}+R_{B1}}}, \quad (2.\ 4)$$

where R_T is total resistance, R_{C2} is contact resistance between electrode and OS 2, R_{C12} is contact resistance between OS 1 and OS 2, R_{B1} is bulk resistance in OS 1, and R_{B2} is bulk resistance in OS 2. In addition, R_{C12} was calculated separately through different series model with four contact resistance (two R_{C2} and two R_{C12}) and one bulk resistance as shown in Figure 2. 14.

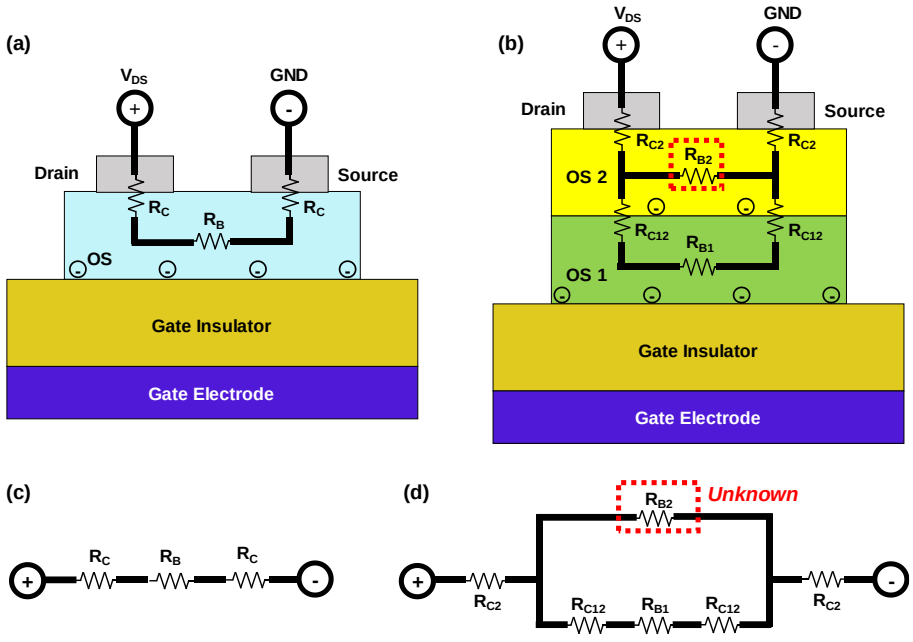

Figure 2. 13 Circuitous approach using contact resistance and bulk resistance in (a) single OS-based TFT, and (b) dual-stacked OS-based TFT. Equivalent circuit modeling in (c) single OS-based TFT, and (d) dual-stacked OS-based TFT. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

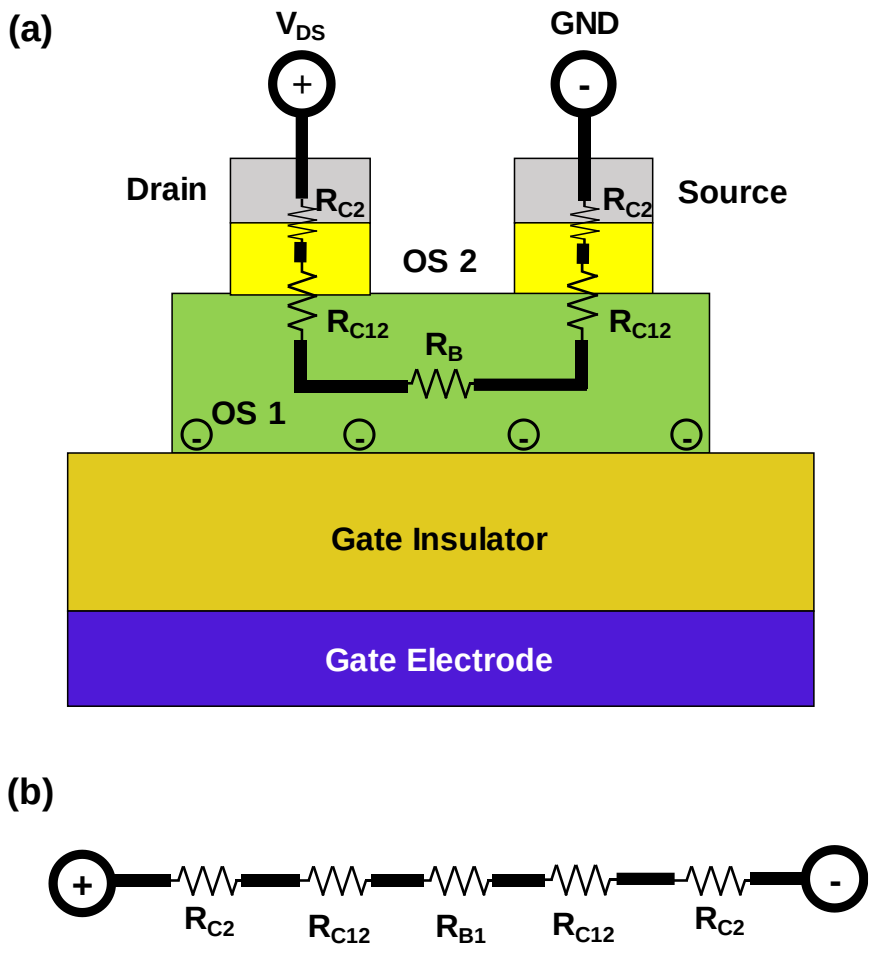

Figure 2. 14 (a) Circuitous approach with a bulk OS (OS 1) and a patterned OS (OS 2) to obtain contact resistance between OS 1 and OS 2 (R_{C12}). (b) Equivalent circuit modeling. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.9 Estimation of bulk resistance of upper OS layer in dual-stacked OS

Total current values (I_{DS}) in single InO_x, single IGZO, and dual-stacked OS are all linearly dependent on the values of V_{GS} where V_{DS} was fixed at 1 V for the convenience of calculation as shown in Figure 2. 15a-15c. In particular, I_{DS} in single IGZO (Figure 2. 15b) only flows when a certain V_{GS} more than 6.5 V is applied, meaning IGZO exhibits the property similar to insulator when there are no electrons accumulated by V_{GS}. Other electronic sources that act like electrons accumulated in single OS are required for current conduction in IGZO, which is the upper OS layer of dual-stacked OS-based TFT. That is the confined electrons mentioned above when presenting the mechanism of current conduction using the induced areas in the dual-stacked OS-based TFT.

To confirm this, I_{B2} passing through R_{B2} in dual-stacked OS-based TFT was calculated using the Equation 2. 4 with V_{DS} fixed at 1 V, where R_{C2} corresponds to R_C in single IGZO and R_{B1} corresponds to R_B in single InO_x. I_{B2} in dual-stacked OS (green dot) on V_{GS} of 20 V was plotted above the trend line to compare it with I_B in single OS as shown in Figure 2. 15d. I_{B2} in dual-stacked OS-based TFT had the same effect as I_B when applying V_{GS} of 11.2 V in single IGZO. It means electronic sources, which are confined electrons, exist at the bottom of the upper

layer in dual-stacked OS, less than the ones in single OS. The ratio of A to B was 34.8%, with A corresponding to the calculated value of I_{B2} in dual-stacked OS and B corresponding to the measured value of I_B in single IGZO.

I_{B2} on V_{GS} of 10 V and 40 V in dual-stacked OS-based TFT were estimated with this ratio, and they were also plotted above the trend line to be compared with I_B in OS, as shown in Figure 2. 15e. In addition, I_{B2} on V_{GS} of 10 V and 40 V were also calculated by the same method as I_{B2} on V_{GS} of 20 V, which were listed in Table 2. 8. In this case, I_{B1} in the bottom OS layer of dual-stacked OS-based TFT and I_B in single InO_x TFT were fixed by the same value to confirm the change in the upper OS layer of dual-stacked OS-based TFT. The calculated I_{B2} and estimated I_{B2} were almost same, meaning that I_{B2} was absolutely affected by the electronic sources, which were confined electrons. Based on the analysis from measurements, calculations, and estimation, it was confirmed that current conduction in the upper OS layer of dual-stacked OS-based TFT was affected by the confined electrons formed between the upper OS layer and bottom OS layer, which was consistent with conduction mechanism above presented. This means that there were electrons confined at the interface of dual-stacked OS, which could be another conduction path just like electrons accumulated at the bottom channel layer (InO_x layer).

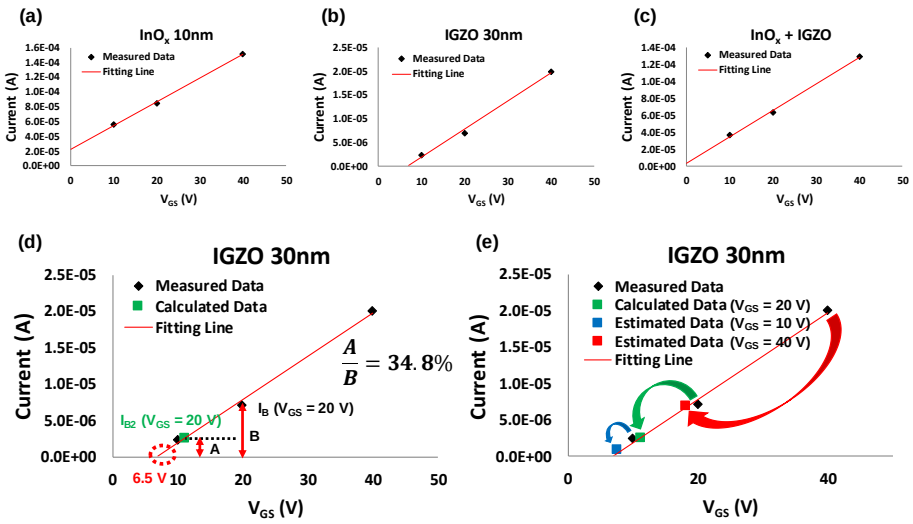

Figure 2. 15 Total current values (I_{DS}) in (a) single InO_x, (b) single IGZO, and (c) dual-stacked OS according to V_{GS} (V_{DS} = 1 V). (d) Calculated I_{B2} from measured I_B on V_{GS} of 20 V. (e) Estimated I_{B2} on V_{GS} of 10 V and 40 V based on calculated I_{B2} on V_{GS} of 20 V. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Parameters / V_{GS} (V)	V_{B2} (V)	I_{B2} (A)
10 (Estimated)	7.7	8.3×10^{-7}
20 (Calculated)	11.2	2.5×10^{-6}
40 (Estimated)	18.2	6.8×10^{-6}

Table 2. 8 Calculated and estimated values according to V_{GS} in dual-stacked OS-based TFT using equivalent circuit. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.10 Stabilities of OS-based TFTs in PBS and NBS

Another important criterion for evaluating the performance of OS-based TFTs is stability, which should be considered importantly as a switching device in the display. To evaluate the stability of dual-stacked OS-based TFTs, positive bias stress (PBS) measurements were carried out compared to a single IGZO TFT over 3600 s at V_{GS} of 20 V and V_{DS} of 10 V, as shown in Figure 2. 16a. Also, the result of PBS measurements with threshold voltage change are listed in Table 2. 9. Dual-stacked OS-based TFT represents a small shift of 2.62 V after 3600 s, similar to single IGZO TFT representing 2.65 V. Subsequently, negative bias stress (NBS) measurements were carried out over 3600 s at V_{GS} of -20 V, V_{DS} of 10 V as shown in Figure 2. 16b. The result of NBS measurements with threshold voltage change are listed in Table 2. 10. Dual-stacked OS-based TFT also represents a small shift of 1.72 V after 3600 s, similar to single IGZO TFT representing 1.67 V. As a result, it was confirmed that dual-stacked OS-based TFT represented good stability similar to single IGZO TFT in both PBS and NBS. This can be attributed to the influence of IGZO layer, which are used as the top layer in dual-stacked OS of TFT structure. Although the oxygen vacancies inside the channel layer supply the conductive carriers, the vacancies also behave as carrier traps. They act as electron trap sites in PBS and NBS enhancement [46,47].

As shown in Figure 2. 5d, InO_x contains about 40 % oxygen vacancies. This is significant compared to single IGZO and dual-stacked OS with less than 20 % oxygen vacancies. As expected, the results of PBS and NBS measurements of single InO_x TFT are not good, as shown in Figure 2. 17 and Table 2. 11. Negative bias illumination stress (NBIS) test was also carried out over 3600 s at V_{GS} of -20 V and V_{DS} of 10 V under irradiation of 0.4 mW/cm^2 of blue (450 nm) light-emitting-diode (LED) light sources, as shown in Figure 2. 18. Dual-stacked OS-based TFT represents a small shift of 5.87 V after 3600 s, similar to single IGZO TFT representing 6.12 V (Table 2. 12). InO_x TFT data was not added due to severe performance degradation after NBIS.

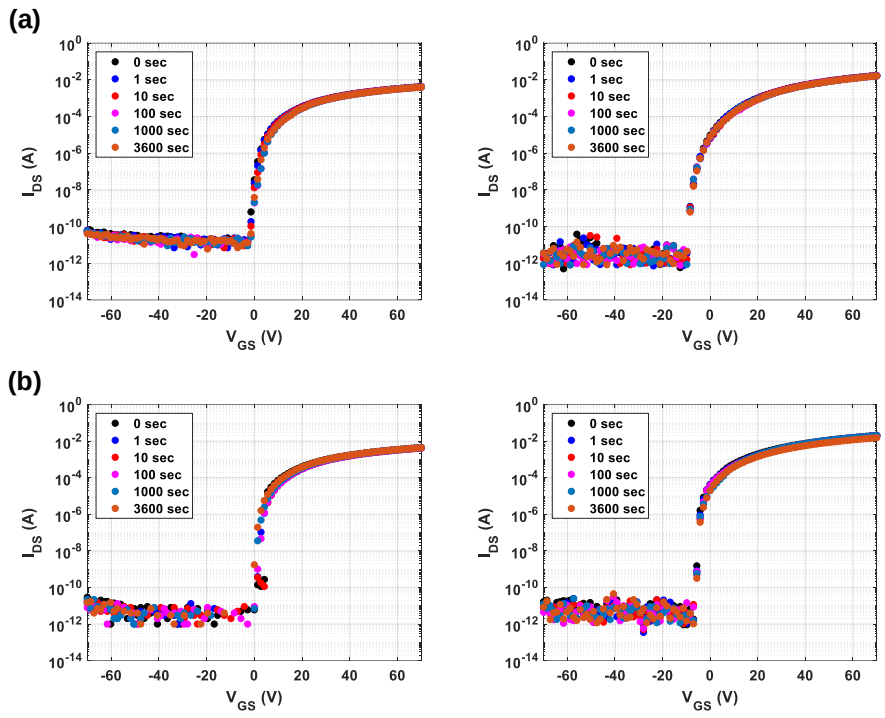

Figure 2. 16 (a) Positive bias stress (PBS) results for a single IGZO TFT and dual-stacked OS-based TFT at V_{GS} = 20V and V_{DS} = 10V, respectively. (b) Negative bias stress (NBS) results for a single IGZO TFT and dual-stacked OS-based TFT at V_{GS} = -20V and V_{DS} = 10V. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

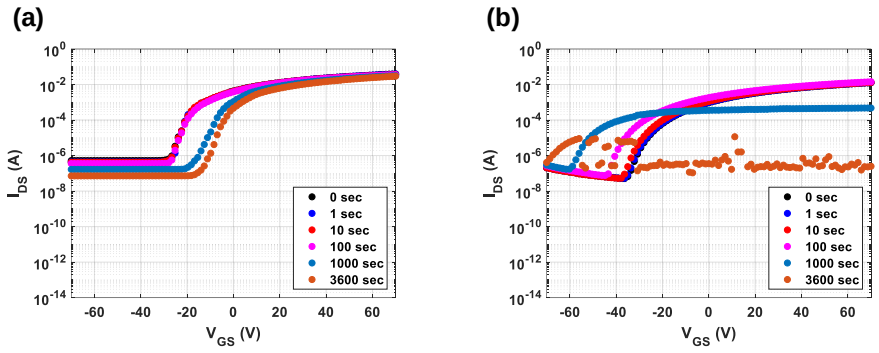

Figure 2. 17 The results of positive bias stress (PBS) and negative bias stress (NBS). (a) PBS results for single InO_x TFTs at V_{GS} = 20V and V_{DS} = 10V. (b) NBS results for single InOx TFTs at V_{GS} = -20V and V_{DS} = 10V. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

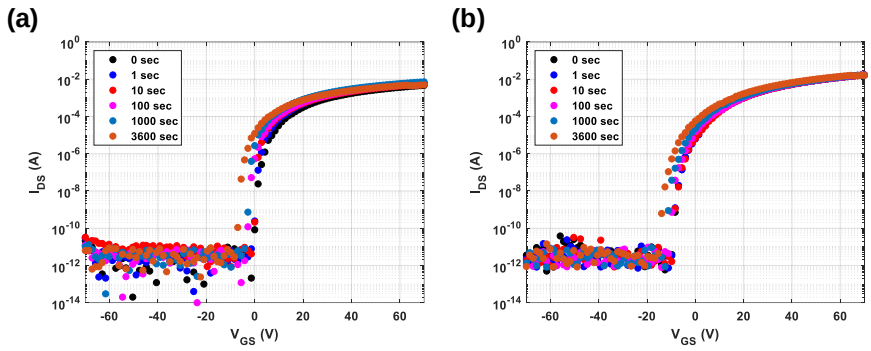

Figure 2. 18 The results of negative bias illumination stress (NBIS) for (a) IGZO TFTs and (b) dual-stacked OS-based TFT at V_{GS} = -20V and V_{DS} = 10V under irradiation of 0.4 mW/cm^2 of blue (450 nm) light-emitting-diode (LED) light sources. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Bias Test	ΔV_{TH}					
	0 sec	**1 sec**	**10 sec**	**100 sec**	**1000 sec**	**3600 sec**
IGZO	-	0.01	0.03	2.14	2.58	2.65
InO_x + IGZO	-	0.02	0.03	2.22	2.59	2.62

Table 2. 9 Threshold voltage shifts (ΔV_{TH}) in single IGZO TFT and dual-stacked OS-based TFT after PBS test. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Bias Test	ΔV_{TH}					
	0 sec	**1 sec**	**10 sec**	**100 sec**	**1000 sec**	**3600 sec**
IGZO	-	0.00	0.02	1.21	1.54	1.67
InO_x + IGZO	-	0.00	0.01	1.23	1.61	1.72

Table 2. 10 Threshold voltage shifts (ΔV_{TH}) in single IGZO TFT and dual-stacked OS-based TFT after NBS test. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

V_{th} (V)	0 sec	1 sec	10 sec	100 sec	1000 sec	3600 sec
InOx (PBS)	-	1.63	3.29	3.53	12.24	15.30
InOx (NBS)	-	0.25	2.18	10.68	23.23	-

Table 2. 11 Threshold voltage shifts (ΔV_{TH}) in single InO_x TFTs after PBS and NBS test. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

Bias Test	ΔV_{TH}					
	0 sec	**1 sec**	**10 sec**	**100 sec**	**1000 sec**	**3600 sec**
IGZO	-	0.22	0.61	2.63	3.88	6.12
InO_x + IGZO	-	0.16	0.54	2.11	3.26	5.87

Table 2. 12 Threshold voltage shifts (ΔV_{TH}) in single IGZO TFT and dual-stacked OS-based TFT after NBIS test. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.11 Conclusion

In summary, I have prevailed the working mechanism and the role of dual-stacked OSs with the concept of induced area, consisting of the channel layer at the bottom and the buffer layer at the top, resulting in outstanding electrical performance TFTs. In the case of the bottom OS layer in dual-stacked OS, InO_x was deposited on SiO_2, acting as gate insulator, to improve the field-effect mobility. In the case of the upper layer in dual-stacked OS, IGZO was subsequently deposited to reduce the leakage current. As a result, electrical performances of dual-stacked OS-based TFTs were remarkably improved for very high field-effect mobility of ~80 $cm^2/V \cdot s$, ideal threshold voltage near 0 V, and very high on-off current ratio of $>10^9$, which could not be realized by a single OS-based TFT alone. Field-effect mobility and threshold voltage, which have been considered for trade-off so far, have been improved at the same time, resulting from the investigation of the interface phenomena in dual-stacked OS TFTs. In addition, these dual-stacked OS-based TFTs represent little threshold voltage shifts of 2.62 V and 1.72 V at PBS and NBS respectively. Meanwhile, accumulated or depleted electrons in gate-bias-induced area (GBIA) are a key factors in conduction mechanism of dual-stacked OS-based TFTs. GBIA is connected to electrode-bias-induced area (EBIA) by band-offset-induced area

(BOIA) and BOIA-induced area (BIA) induced by the band-offset, resulting in contribution of current conduction. Transmission line method (TLM) was applied to obtain contact resistance and bulk resistance under actual operating condition. The equivalent circuits were also introduced to verify the current path. All resistant components measured in a single OS-based TFT were used to calculate bulk resistance (R_{B2}) of the upper OS layer in dual-stacked OS-based TFT (V_{DS} = 1 V). I_{B2} in the upper OS layer of dual-stacked OS-based TFT was smaller than I_B in a single IGZO TFT although I_{B1} in the bottom OS layer of dual-stacked OS-based TFT is same as I_B in single InO_x. It means that there are other electronic sources in the upper OS layer of dual-stacked OS similar to the electrons accumulated between OS layer and gate insulator. R_{B2} on V_{GS} of 10 V and 40 V in dual-stacked OS were estimated by calculated R_{B2} on V_{GS} of 20 V. These estimated values were similar to those calculated on V_{GS} of 10 V and 40 V, which precisely validated the role of the electrons confined between the bottom OS layer and the upper OS layer. Based on the comprehensive verification of phenomena at the interface of dual-stacked structure, I developed new design rules for the high performance OS-based TFTs. Such proposed design rules are expected to be implemented widely for applications that require fast response, ultra-high resolution, and low power consumption.

2.12 Experimental section

Fabrication of the TFTs: To fabricate the single OS-based and dual-stacked OS-based TFTs, the heavily B-doped p-type Si wafers (P^{++}-Si) with thermally grown 200 nm SiO_2 layer was used as a role of the gate electrode and the gate insulator, respectively. These wafers were subsequently cleaned by detergent for 15 min, de-ionized (DI) water rinsing for 20 min, acetone for 15 min, and isopropyl alcohol (IPA) for 15 min. All cleanings except DI water rinsing were conducted in ultrasonic bath. InO_x or IGZO layer was deposited on a SiO_2 / Si substrate by using RF sputter (DAEKI HI-TECH co., Ltd, Co-Sputtering System) with a planer round target consisting of InO_x or IGZO (In:Ga:Zn:O = 1:1:1:4 at%) under 10^{-4} mTorr at room temperature. The RF sputtering power for InO_x or IGZO layer was fixed at 40 W in mixed Ar / O_2 (50 sccm / 5 sccm) gases and at 90 W in Ar (25 sccm) gas, respectively. Then, sputtered InO_x or IGZO layers were annealed in the air at 250 ℃ for 90 s by RTA method. After sputtering OS layer(s), as the electrodes of source and drain, Al was deposited with a thickness of 100 nm by thermal evaporation using fine metal masks (FMMs). Channel width and length of FMMs are 1000 μm and 50 μm, respectively. Optical microscopy (OM) image was added in Figure 2. 19 to show the real channel length (51.2 μm). And all TFTs were patterned using photolithography and wet etching process to

prevent leakage current.

Measurement and analysis: The current-voltage characteristics for all TFTs were measured using an Agilent 4155B semiconductor parameter analyzer with compliance current of 10^{-2} A at room temperature in the dark conditions. The absorption and bandgap of a single OS layer were measured from 300 to 800 nm by UV-vis (Lambda 35, PerkinElmer). And work function and energy gap from VBM to Fermi energy were measured by UPS (AXIS SUPRA, Kratos). XPS (AXIS SUPRA, Kratos) equipped with a monochromic Al αK X-ray source was used to analyze the chemical properties of OS layers. The samples for HR-TEM observation were prepared by ion-beam processing techniques through Quanta 3D FEG. A platinum-plated layer with a thickness of 15 nm was deposited via sputter before TEM sample preparation to make its surface more conductive. The HR-TEM images were all obtained by a JEM-2100F field emission electron microscope from JEOL Ltd.

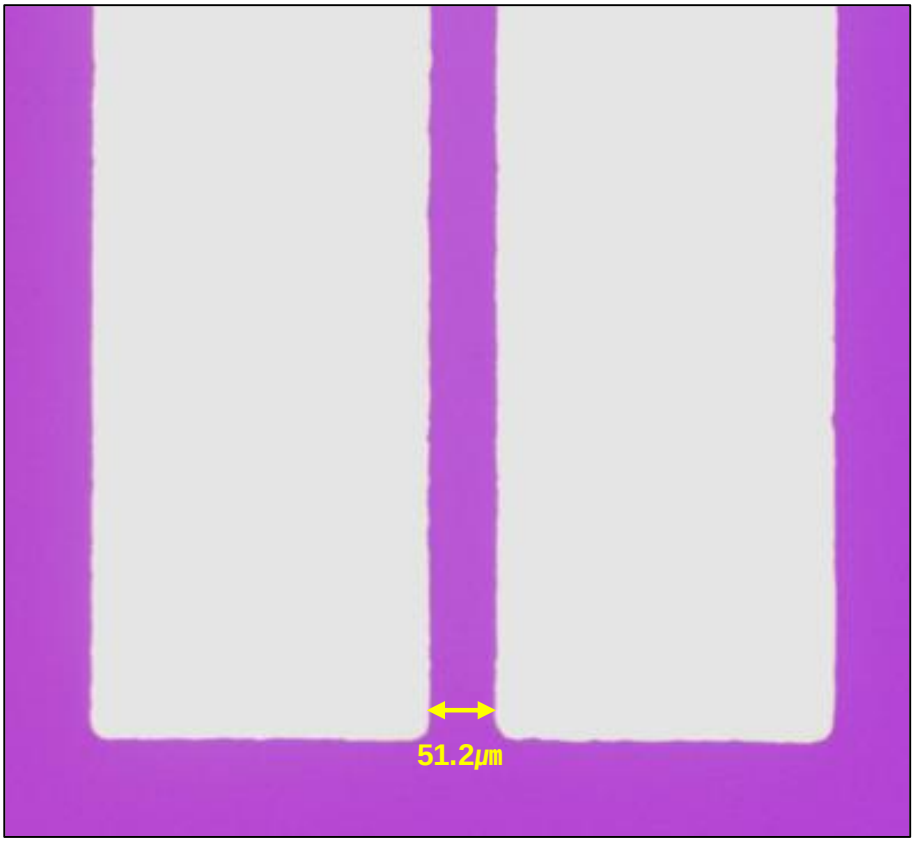

Figure 2. 19 Optical microscopy (OM) image of source-drain electrodes in TFTs. Reproduced with permission of Ref. 40. Copyright 2021 American Chemical Society.

2.13 References

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Chapter 3

Derivation of Excitatory Postsynaptic Current Model with Time-Varying Term for Synaptic Thin-Film Transistors

3.1 Introduction

Synaptic devices that mimic a biological synapse in the brain are emerging as an alternative to overcome the so-called von Neumann bottleneck problem [1,2]. A synapse is an interface that transmits the electrical signal from one neuron to another. The synaptic weight determines the intensity of transmitted signals across a synapse by the connection strength between neurons and post neurons [3]. For example, a synapse can have a heavy synaptic weight when steady transmissions pass through the synapses. Otherwise, they are weakened. This characteristic, synaptic plasticity, is a biological process in which synaptic activity causes changes in synaptic weight and is considered the main principle of learning and memory [3-6]. It is generally divided into short-term plasticity (STP) to support computations and long-term plasticity (LTP) to provide a physiological basis for learning and memory [4,7,8]. They are represented by excitatory postsynaptic current (EPSC) generated when the stimulus arrives at the presynaptic membrane [3,8].

In the synaptic devices, three-terminal synaptic thin-film transistors (TFTs) have been proposed to obtain the advantage of simultaneous signal processing and information storage by emulating synaptic weight modulation with both drain and gate voltage (V_{DS} and V_{GS}) change. The general purpose of developing the

synaptic TFTs is to improve the linearity of EPSC accumulated in the sequential voltage pulses and to maintain the LTP as long as possible [9-14]. Many studies have been on synaptic performance improvement, mechanism identification, or new applications [15-30].

However, a systematic approach of EPSC has been absent as there is a lack of an analytical model for the synaptic TFTs. Several studies have adopted a simple serial RC-delay circuit model to calculate the paired-pulse facilitation (PPF) index [30-32]. Although the RC-delay circuit model is simple to represent the shape of EPSC, it is not possible to directly bridge the EPSC with the operating condition of synaptic TFTs (*e.g.*, V_{GS}, V_{DS}, and synaptic information). Thus, a comprehensive model emulating the EPSC of synaptic TFT is necessary, which can represent characteristics of EPSC when a single V_{GS} pulse is applied.

Here, we proposed an analytical model that emulates the EPSC of synaptic TFTs, which can be referred to as a single-pulse-driven synaptic EPSC (SPSE) model [33]. The SPSE model includes the capacitive effect (explained with the serial RC model) and the synaptic window information (offsetting the peak drain current in the EPSC). In the model, the electrical condition applied to the synaptic TFTs (*e.g.*, V_{GS} and V_{DS}) can affect the capacitive effect and the size of the synaptic window, leading to specific characteristics of EPSC. I have fabricated

synaptic TFTs with various gate insulators [34,35] (*e.g.*, SiO_2 and ion-gel) and confirmed that the measured EPSC of those devices could be clearly and systematically analyzed with the SPSE model. For example, ion-gel-based TFTs' superior LTP and STP properties can be captured by analyzing the measured EPSC with the SPSE model. Moreover, based on the model, I have defined the energy consumption of the synaptic TFT, which can potentially provide a standard to compare energy costs. SPSE model enables a comprehensive understanding of EPSCs generated by a single V_{GS} pulse and based on this, it is expected to implement synaptic devices with superior linearity by predicting EPSCs accumulated by multiple V_{GS} pulses.

3.2 Derivation of SPSE model for synaptic TFTs

In synaptic TFTs, the drain current changes over time when the gate electrode admits the pulse of electrical potential (*i.e.*, EPSC). Figure 3. 1a shows the synaptic TFT structure with capacitive effect driven gate insulator (GI). I can obtain the drain current as a function of the time by solving the following equation:

$$I_{DS}(t) = \frac{W}{L}\int_{V_S}^{V_D}\int_{\varphi_0}^{\varphi_{ch}} \frac{\sigma(\varphi,t)}{-E_z(\varphi,t)} d\varphi d\varphi_{ch}, \qquad (3.\ 1)$$

where *t* is the time, *W* is the channel width, *L* is the channel length, V_D (or V_S) is the voltage at the drain (or source) electrode, φ_0 is the electrostatic potential at the surface point between channel and gate insulator, φ_{ch} is the electrostatic potential at the surface point between channel and electrodes, σ is the channel conductivity, E_z is the electric field inside the channel, and φ is the electrostatic potential along the direction perpendicular to the channel/gate insulator interfaces (*i.e.*, the z-direction).

When the pulse of electrical voltage is applied to the gate electrode, the capacitive structure of the gate electrode/gate insulator/channel starts to accumulate (or dissipate) charge carriers at the gate insulator/channel interface [34,36], causing the gate to respond to the electric field. To formulate such time-varying capacitive effect in Equation 3. 1 efficiently, I assumed the followings:

(1) the temporal shape of voltage pulse at the gate is a square with the width of t_w and the amplitude of V_0 shown in Figure 3. 1b (*i.e.*, $t \leq 0$ *or* $t \geq t_w$: $V_{GS} = 0, 0 \leq t \leq t_w : V_{GS} = V_0$); (2) the capacitive effect delays the electrical quantities (*i.e.*, E_z) with the time-delaying constant of $\tau(x)$ to reach their steady-state values at the voltage given to the gate (*i.e.*, $E_z(t = \infty)$ at $V_{GS} = V_0$); (3) the position-dependent effect of $\tau(x)$ is lumped to $\langle\tau\rangle$, which is a nominal parameter reflecting the capacitive effect of the device. With these assumptions, I can employ an empirical model to quantify the electric field inside the channel in Equation 3. 1 as:

$$E_z(\varphi, t) = \begin{cases} \left(1 - \gamma_{rp} e^{-\frac{t}{\langle\tau\rangle_{rp}}}\right) E_z^{on}(\varphi), & 0 \leq t \leq t_w : V_{GS} = V_0 \\ \left(1 + \gamma_{rx} e^{-\frac{t - t_w}{\langle\tau\rangle_{rx}}}\right) E_z^{off}(\varphi), & t \geq t_w : V_{GS} = 0 \text{ V} \\ E_z^{off}(\varphi), & t \leq 0 : V_{GS} = 0 \text{ V} \end{cases} \quad (3.2)$$

where $E_z^{on}(\varphi)$ (or $E_z^{off}(\varphi)$) is the steady-state electric field inside channel when the gate voltage is 'on' : $V_{GS} = V_0$ (or 'off' : $V_{GS} = 0$ V). $\langle\tau\rangle_{rp}$ (or $\langle\tau\rangle_{rx}$) depicts the lumped time-delaying constant when the square pulse of gate voltage is 'on' (or 'off'), which can be referred to the responsive time-delaying constant (or the relaxed time-delaying constant), and γ_{rp} (or γ_{rx}) is the responsive (or relaxed) ratio constant and positively defined to represent the non-zero electric field at $V_{GS} = 0$ V before EPSC (or after an EPSC). As seen in Equation 3. 2, E_z decouples t and φ variables into two independent functions, which greatly

relaxes mathematical complexity to solve the drain current model in Equation 3. 1. I noted that the validity of lumped parameter $\langle\tau\rangle$ and the empirical model of the electric field in Equation 3. 2 have been confirmed, which will be discussed next section.

By substituting Equation 3. 2 into Equation 3. 1, I can mathematically perform the integration (see next section for details) and obtain the analytical equation of SPSE model to describe EPSC in synaptic transistor as

$$I_{DS}=\begin{cases}\left(1-\gamma_{rp}e^{-\frac{t}{\langle\tau\rangle_{rp}}}\right)\ I_{DS}^{on}(V_{GS}=V_0,V_{FB}=V_{F0}), & 0\ \le\ t\ \le t_w\\ \left(1+\gamma_{rx}e^{-\frac{t-t_w}{\langle\tau\rangle_{rx}}}\right)\ I_{DS}^{off}(V_{GS}=0\ \text{V},V_{FB}=V_{F1}), & t\ \ge t_w\\ I_{DS}^{off}(V_{GS}=0\ \text{V},V_{FB}=V_{F0})\ , & t\ \le 0\end{cases} \tag{3. 3}$$

where

$$I_{DS}^{on/off}=\frac{W}{L}\sigma_0\frac{V_T}{\beta-1}\left(\frac{2\varepsilon_0\varepsilon_r k_B T_0\sin(T\pi/T_0)}{q^2N_t(T\pi/T_0)}\right)^{\frac{\beta}{2}}\left(\frac{C_i}{\varepsilon_0\varepsilon_r}\right)^{\beta-1}\left(\frac{(T_0/T)^3\pi N_t}{B_c(2\alpha)^3}\right)^{\frac{T_0}{T}}\left[\left(\frac{V_{GS}-V_{FB}-\varphi_S}{\beta V_T}\right)^{\beta-1}\left(\frac{\beta}{\beta-1}\right)-\left(\frac{V_{GS}-V_{FB}-\varphi_D}{\beta V_T}\right)^{\beta-1}\left(\frac{\beta}{\beta-1}\right)\right]. \tag{3. 4}$$

σ_0 is the conductivity prefactor, q is the charge of electron, ε_0 is the vacuum permittivity, ε_r is the relative permittivity, C_i is the areal capacitance of gate insulator, V_{F0} is V_{FB} before a V_{GS} pulse is finished, V_{F1} is V_{FB} after a V_{GS} pulse, $V_T=k_BT/q$ is the thermal voltage, and $\beta=2T_0/T$. φ_S and φ_D are the surface potential at the source and drain electrodes, respectively. They are expressed as

$$\varphi_S = V_{GS} - V_{FB} - \beta V_T W_0 \left[\sqrt{\frac{q^2 N_t (T\pi/T_0)}{2\varepsilon_0 \varepsilon_r k_B T_0 \sin(T\pi/T_0)}} \frac{\varepsilon_0 \varepsilon_r}{C_i} \exp\left(\frac{V_{GS} - V_{FB} - \emptyset_F}{\beta V_T} \right) \right] \quad (3.5)$$

and

$$\varphi_D = V_{GS} - V_{FB} - \beta V_T W_0 \left[\sqrt{\frac{q^2 N_t (T\pi/T_0)}{2\varepsilon_0 \varepsilon_r k_B T_0 \sin(T\pi/T_0)}} \frac{\varepsilon_0 \varepsilon_r}{C_i} \exp\left(\frac{V_{GS} - V_{FB} - \emptyset_F - V_{DS}}{\beta V_T} \right) \right] \quad (3.6)$$

where W_0 represents the principal branch of the Lambert Function [37,38] and $\emptyset_F$ is the Fermi potential. All parameters are listed in Table 3. 1.

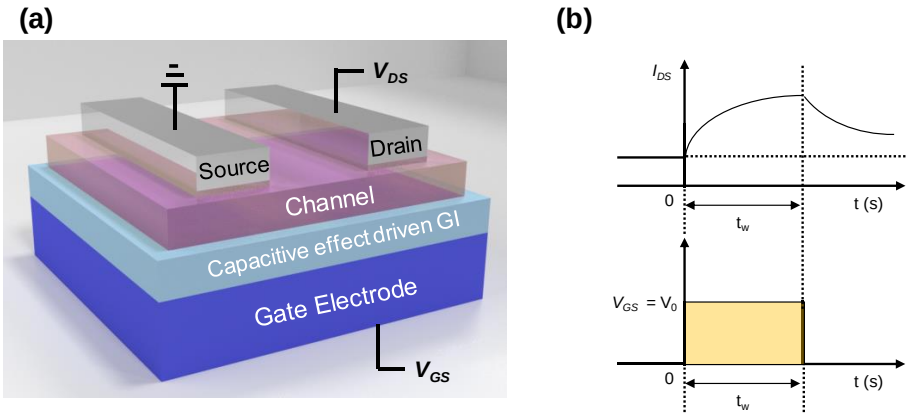

Figure 3. 1 (a) Schematic image of synaptic TFTs. (b) I_{DS} by a single V_{GS} pulse with the width of t_w. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

Variables	Values	Units
ε_r	3.6	-
T	293	K
T_0	381.3	K
N_t	11.95×10^{19}	cm^{-3}
σ_0	5.75×10^{8}	$S\ cm^{-1}$
α	9.56×10^{7}	cm^{-1}
B_c	2.8	-
α	9.56×10^{7}	cm^{-1}
B_c	2.8	-

Table 3. 1 Parameter values of synaptic TFT with the combination of SiO_2 and IGZO for calculation through SPSE model. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

3.3 Detailed derivation of SPSE model

In this section, I explain the process of deriving the newly defined equation and confirm how reasonable each parameter value described in main manuscript. As shown in Equation 3. 2, only the electric field components in the z-axis direction ($E_z(\varphi, t)$) were represented because φ variation along the channel length direction (x-direction) is much smaller than the z-axis direction. It is represented using as

$$\nabla \cdot \nabla\varphi = -\left(\frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} + \frac{\partial^2\varphi}{\partial z^2}\right) \approx -\frac{\partial^2\varphi}{\partial z^2} = -\frac{\partial E_z}{\partial z}. \quad (3.\ 7)$$

It can be also combined with Poisson equation to obtain the following equation:

$$\frac{\partial E_z}{\partial z} = -\frac{qn_t}{\varepsilon_0\varepsilon_r}, \quad (3.\ 8)$$

n_t is the total number of trapped electrons in localized states given by references 37-39:

$$n_t \approx \frac{\pi N_t}{(T_0/T)\sin(T\pi/T_0)} \exp\left(\frac{q\left(\varphi-\varphi_{ch}-\emptyset_F\right)}{k_B T_0}\right). \quad (3.\ 9)$$

When an external bias is applied to OSs, the electrons flow along the percolating-conduction path by a hopping process [39]. It affects σ and can be expressed as [37-39]:

$$\sigma = \sigma_0 \left(\frac{\sin(\pi T/T_0)(T_0/T)^4 n_t}{B_c(2\alpha)^3}\right)^{\frac{T_0}{T}}. \quad (3.\ 10)$$

I can also calculate φ_0 using the definition of the Lambert W_0 function as:

$$\varphi_0 = V_{GS} - V_{FB} - \frac{W_0}{C_i}\left(\frac{2\varepsilon_0\varepsilon_r\pi N_t k_B T}{\sin\left(\frac{\pi T}{T_0}\right)}\right)^{\frac{1}{2}} e^{\frac{q\left(V_{GS}-V_{FB}-\varphi_{c\acute{\imath}}-\emptyset_F\right)}{2k_B T_0}}. \qquad (3.\ 11)$$

E_z can be calculated by integrating Equation 3. 8, where Equation 3. 9 is substituted into Equation 3. 8. Equation 3. 9 can be obtained by substituting Equation 3. 1 with three terms following: calculated E_z, Equation 3. 10, and Equation 3. 11.

3.4 Synaptic performance via SPSE model

The SPSE model in Equation 3. 3 has the time-domain function which can quantify the synaptic performances (e.*g.*, LTP and STP) with the time-delaying constants and the ratio constants. In the meantime, $I_{DS}^{on/off}$ in Equation 3. 3 can reflect the electrical properties being supposed to be held during the transient state in EPSC of the synaptic TFTs. To understand how this model responds to the time-delaying and the ratio constants, I systematically tune γ_{rp}, γ_{rx}, $\langle\tau\rangle_{rp}$, and $\langle\tau\rangle_{rx}$ parameters and study EPSC with Equation 3. 3. Here, I assume that the synaptic TFT is with the channel layer as indium-gallium-zinc-oxide (IGZO) and the gate-insulator as SiO_2. It has a channel width and length of 1000 and 50 μm, respectively. The values of parameters for the devices are taken from the reference 39 and listed in Table 3. 1.

Figure 3. 2a show the calculated drain current using the model with γ_{rp} of 0.2500, 0.4500, 0.6500, and 0.8500, and γ_{rx} of 1.200, 2.200, 3.200, and 4.200 when the square pulse applied to the gate is 1 V. As the magnitude of the ratio constants increases, the difference between the level of the drain current at $t = 0$ and $t = t_w$ gets larger. This indicates that the size of the synaptic window, which corresponds to the capacity of writing memory in the device, can be widened at a higher ratio constant. For a higher-performance synaptic device, it

would be better to let the synaptic window be more significant, as the device can have more memory slots at a given time window (*i.e.*, it is closely related to the performance of STP in synaptic devices). Also, the larger synaptic window can reduce the noise ratio (*i.e.*, higher signal-to-noise ratio). Also, it is noted that lower γ_{rx} can let the peak current level at $t = t_w$ be less reduced after an EPSC, meaning better LTP.

The slope (or the gradient) of EPSC can determine the synaptic performance. The gentler the slope is, the more time it takes to reach the saturation value. This situation is required for the synaptic devices that need to keep the EPSC as long as possible, related to LTP to provide the learning and memory in synaptic devices. In the SPSE model, it can be mainly achieved by $\langle\tau\rangle_{rp}$ and $\langle\tau\rangle_{rx}$. Figure 3. 2b show the calculated EPSC results using the model with $\langle\tau\rangle_{rp}$ and $\langle\tau\rangle_{rx}$ of 4, 6, 8, and 10 ms when the pulse applied to the gate is 1 V. At higher $\langle\tau\rangle_{rp}$ and $\langle\tau\rangle_{rx}$, I can see that the slope angle of the rising or falling drain current becomes lower.

The EPSC value after a V_{GS} pulse can be changed slightly compared to the initial steady-state EPSC value, which is one of the essential characteristics of the synaptic devices (e.*g.*, the nonvolatile memory). In the SPSE model, the flat-band voltage (V_{FB}) can reflect the EPSC change. Figure 3. 2c shows how EPSC

changes according to the change in V_{FB} ($|\Delta V_{FB}|$). It can be seen that a larger $|\Delta V_{FB}|$ increases the offset of drain current after an EPSC. During the relaxed state of EPSC ($t > t_w$), the time-delaying and the ratio constants can determine the decaying-rate of the drain current (see Figures 3. 2a and 2b), but at the limit of $t \to \infty$, $|\Delta V_{FB}|$ can be a sole parameter to make the memorized drain current. For example, the EPSC eventually returns to its initial value with $|\Delta V_{FB}| = 0$ (represented with red line in Figure 3. 2c) regardless of the magnitude of the time-delaying and the ratio constants, which means that the stored information is volatilized.

The SPSE model suggests that both the time-delaying and the ratio constants should be larger to obtain better synaptic properties in the short term. At the same time, $|\Delta V_{FB}|$ should be non-zero for the long-term memory effect. Materials in the synaptic device can be changed to tune the values of these parameters. For example, the gate insulator material with higher capacitance can be selected for larger time-delaying constants. When the capacitance of the gate insulator is large, the response time increases due to the capacitive effect, which acts as a factor in increasing $\langle\tau\rangle_{rp}$ and $\langle\tau\rangle_{rx}$. This case, however, may be suffered by the small pool of limited candidates of materials. Another way to achieve the parameter condition is to tune synaptic devices' operating conditions. For example,

increasing V_{GS} or V_{DS} can let the device have higher time-delaying constants or the ratio constants (see Figure 3. 3).

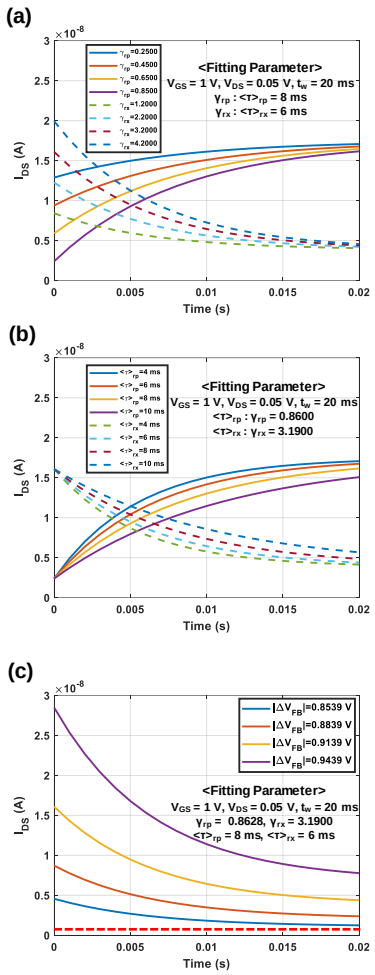

Figure 3. 2 Fitting simulation using SPSE model. I_{DS} according to (a) γ_{rp} (0.2600, 0.4600, 0.6600, and 0.8600) in the responsive region and γ_{rx} (1.2000, 2.2000, 3.2000, and 4.2000) in the relaxed region, (b) $\langle\tau\rangle_{rp}$ (4, 6, 8, and 10 ms) in the responsive region and $\langle\tau\rangle_{rx}$ (4, 6, 8, and 10 ms) in the relaxed region, and (c) $|\Delta V_{FB}|$ of 0.8539, 0.8839, 0.9139, and 0.9439. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

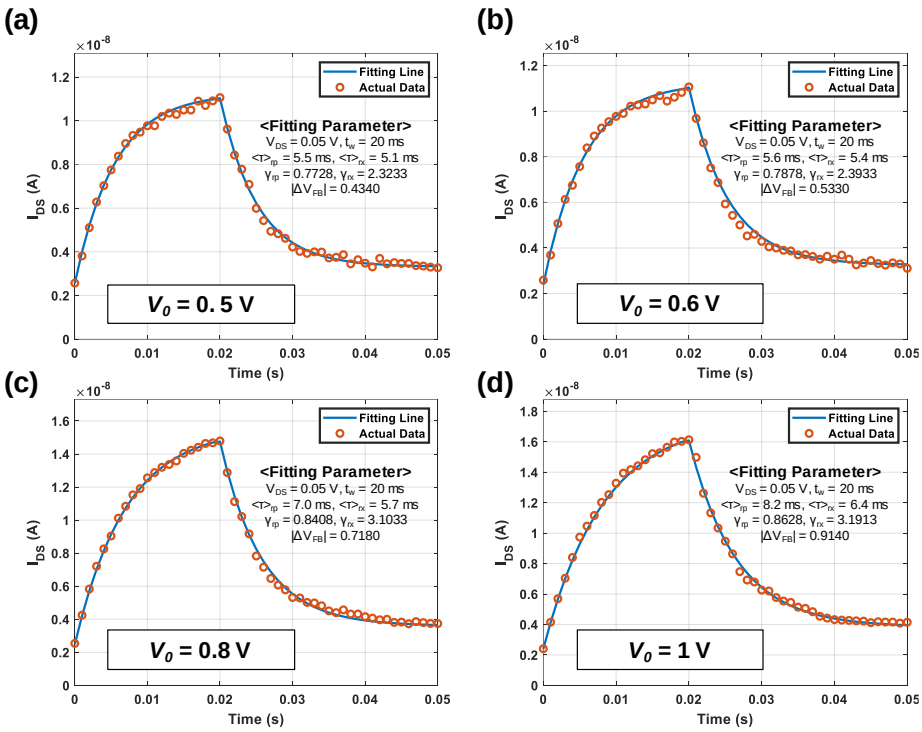

Figure 3. 3 Actual EPSC and fitted EPSC using SPSE model in synaptic TFT with the combination of SiO_2 and IGZO according to V_0 of (a) 0.5, (b) 0.6, (c) 0.8, and (d) 1 V at fixed V_{DS} = 0.05 V. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

3.5 Validation of SPSE model with synaptic TFTs

I aim the validity of the SPSE model in terms of that the model can explain and analyze the EPSC of the synaptic TFTs. To validate the model, I prepared n-type synaptic transistors with an IGZO thin-film (30-nm-thick) as a channel layer and SiO_2 (200-nm-thick) as a gate insulator layer. Then, water-in-bisalt (WiBS)/polymer electrolyte (*i.e.*, ion-gel electrolyte) was also used as a gate insulator in synaptic TFTs to confirm the expandability of SPSE model. In the case of SiO_2-TFTs, Al was deposited for source and drain electrodes with channel length (L) of 50 μm and channel width (W) of 1000 μm by thermal evaporation using fine metal masks (FMMs). Since it is assumed that the electrical properties in $I_{DS}^{on/off}$ in Equation 3. 3 are supposed to be kept in the transient process of EPSC, I primarily could fit those parameters in the model with the transfer curves of the IGZO TFTs (in this study, I would like to refer this step as 'pre-fitting process'). The fitted parameters for the electrical properties in the pre-fitting process are shown in Table 3. 1, referring to the values obtained in our previous study using the same IGZO TFTs [39].

After the pre-fitting process, I measured the EPSC of synaptic transistors under the gate pulse of various V_0 conditions (0.5, 0.6, 0.8, and 1 V), t_w = 20 ms, and V_{DS} = 0.05 V (see Figure 3. 3). The measured EPSC shows the typical-temporal

evolution of the drain current where it linearly increases first and then saturated under the pulse of V_{GS}. With the SPSE model, I could fit this observed trend with $\langle\tau\rangle_{rp}$ and γ_{rp} for the temporal region $t < t_w$. The drain current with fitted $\langle\tau\rangle_{rp}$ and γ_{rp} show monotonic increment at higher V_0 (see Figure 3. 3). For γ_{rp}, it is reasonable to extract higher γ_{rp} at higher V_0, since the n-type TFTs show an increment of the drain current at the higher applied voltage at the gate electrode. This means the synaptic window can be improved when I apply the higher level of the gate pulse. In the meantime, the fitted $\langle\tau\rangle_{rp}$ shows the range of 5.5 ~ 8.2 ms, which leads to the nominal capacitance value of 2.43 × 10^{-6} ~ 5.29 × 10^{-6} F/cm^2 with the trans-conductance of 2.21 × 10^{-7} ~ 3.23 × 10^{-7} /ohm (at V_0 = 0.5 ~ 1 V and V_{DS} = 0.05 V). The increment of fitted $\langle\tau\rangle_{rp}$ indicates that the nominal capacitance rises and that the trans-conductance of the channel is reduced. It is noted that the extracted nominal capacitance is slightly higher than that of the 200-nm-thick SiO_2 insulator (~ 1.59 × 10^{-8} F/cm^2).

In the relaxed region ($t > t_w$), the drain current lowers the level rapidly and then approaches a value that can be slightly higher than the current level before applying the gate pulse. The decrement characteristics of the drain current can be analyzed with $\langle\tau\rangle_{rx}$ and γ_{rx}. For the fitted γ_{rp} and $\langle\tau\rangle_{rp}$, I observe that the trends are similar to those in the responsive region ($t < t_w$) (see Figures 3. 4a

and 4c), where higher V_0 leads to higher γ_{rx} and $\langle\tau\rangle_{rx}$. These characteristics well corresponds to the theoretical study in Section B. It is noted that the way to fit γ_{rx} is different from that of γ_{rp}. For example, γ_{rx} = 3 means that the drain current at $t = t_w$ is 300% higher than that the current at the end of EPSC process. The fitted values of $\langle\tau\rangle_{rx}$ are similar to those of $\langle\tau\rangle_{rp}$ at V_0 = 0.5 and 0.6 V. On the other hand, there are obvious differences between the fitted values of $\langle\tau\rangle_{rx}$ and $\langle\tau\rangle_{rp}$ at V_0 = 0.8 and 1 V (see Figures 3. 4b and 4d). This analysis has confirmed that the EPSC of synaptic TFT can be studied with the SPSE model, indicating that the assumption of lumped parameter $\langle\tau\rangle$ and the empirical model can be valid to account for the measured EPSC of the synaptic device.

The time-delaying and the ratio constants can be also influenced by the variation of V_{DS}. I measured the EPSC of synaptic transistors under the gate pulse of various V_{DS} conditions (0.05, 0.06, 0.07, and 0.08 V), t_w = 20 ms, and V_0 = 1 V (see Figure 3. 5). At higher V_{DS}, it is found that the fitted time-delaying constants ($\langle\tau\rangle_{rp}$ and $\langle\tau\rangle_{rx}$) get lower and the fitted ratio constants (γ_{rp} and γ_{rx}) get higher (see next section for details). Such trends indicate the synaptic window become widen, but the EPSC more rapidly increases and then quickly reaches to the saturated value, implying the synaptic performance may be compromised. In the meantime, the extracted nominal capacitances for V_{DS} = 0.05 ~ 0.08 V are

$4.33 \times 10^{-6} \sim 5.29 \times 10^{-6}$ F/cm^2, which are similar to each others. It implies that the nominal capacitance is not much affected by V_{DS} (but it mainly depends on V_0), and the decrement of fitted time-delaying constants at higher V_{DS} can be caused from the increment of trans-conductance of the device.

As mentioned in previous section, ΔV_{FB} indicates the quantified capability of synaptic LTP. It has been known that none-trivial ΔV_{FB} is caused by the electrons trapped at the channel/gate insulator interfaces [40,41]. I have found that the fitted ΔV_{FB} value strongly depends on the magnitude of V_0, but it is not sensitive to the change in V_{DS} (see Figure 3. 4e). This observation well corresponds to the report that higher gate voltage improves the synaptic properties after the EPSC [10,42,43]. For the temporal length (t_w) of EPSC, I noted that the fitting parameters are not sensitive to t_w (see Figure 3. 6 for EPSC at various t_w).

When the materials used in synaptic devices are changed, EPSC shapes under the same electrical conditions are also different. In our previous study, I have improved LTP with a TFT using WiBS/polymer electrolyte as a gate insulator, where an IGZO works as the channel layer [35]. The measured EPSC data by a single different V_{GS} pulse (0.5, 1, 2, and 3 V) were fitted with the SPSE model (V_{DS} = 1 V and t_w = 20 ms) as shown in Figure 3. 7. All fitting parameter values

were listed in Table 3. 2. With an electrolyte as the gate insulator, it is difficult to specify the capacitance of the insulator because ions move inside the electrolyte and are easily affected by external electric fields (*i.e.*, the capacitance can depend on V_{GS} or V_{DS}). In this analysis, I measured the average capacitance in the applied voltage range and substituted it into the SPSE model. The fitted parameters ($\langle\tau\rangle_{rp}$, $\langle\tau\rangle_{rx}$, γ_{rp}, γ_{rx}, and ΔV_{FB}) monotonically increase as V_{GS} increases, which well agree with the trend observed with the synaptic TFTs of SiO_2 and IGZO combinations used in Figures 3. 3 and 3. 4. However, γ_{rx} shows the value which is ten times lower than γ_{rx} with the SiO_2-TFTs, indicating the drain current at the end of EPSC process is slightly lowered than that at $t = t_w$. This analysis can be coherent to the long-term robustness feature of WiBS-TFT, showing that the SPSE model can be applied to various kinds of synaptic TFTs.

The analysis in previous sections suggests that increasing V_{GS} results in improved synaptic properties. However, it may increase the energy consumption in the synaptic devices. Therefore, it is necessary to consider the energy consumption and to quantify it. The qualify factor of energy consumption (E_c) can be obtained in the responsive region ($t < t_w$) as the following:

$$E_c = V_{DS}\left(t_w + \langle\tau\rangle_{rp}\ \gamma_{rp}\left(e^{-\frac{t_w}{\langle\tau\rangle_{rp}}} - 1\right)\right)\ I_{DS}^{on}(V_{GS} = V_0, V_{FB} = V_{F0}) - V_{DS} I_{DS}^{off} t_w. \quad (3.\ 12)$$

When I_{DS} is a constant and I_{DS} $(t = 0)$ = 0 A, Equation 3. 12 can be reduced

into $V_{DS} \times I_{DS} \times t_w$, which is for an ideal case and has been used in references 44-47. Equation 3. 12 excepts the initial energy (blue area in Figure 3.8a) consumed in the absence of V_{GS} pulse and only considers the energy (green area in Figure 3. 8a) when V_{GS} pulse is applied. Shortly, Equation 3. 12 can be fair to compare the energy consumption between various synaptic devices.

Figure 3.8b shows the calculated E_c at a single V_{GS} pulse of V_0 = 0.5, 0.6, 0.8, and 1 V (V_{DS} of 0.05 V and t_w of 20 ms). The E_c is 10 ~ 30 pJ and monotonically increases with V_0, which are mainly attributed from the increment of $\langle\tau\rangle_{rp}$ or decrement of γ_{rp}. Equation 3. 12, at the same time, indicates that shortening t_w can lead to reduce E_c. Therefore, obtaining the optimized synaptic conditions can be necessary, and SPSE model may provide a guideline to efficiently adjust parameter conditions according to the purpose of use.

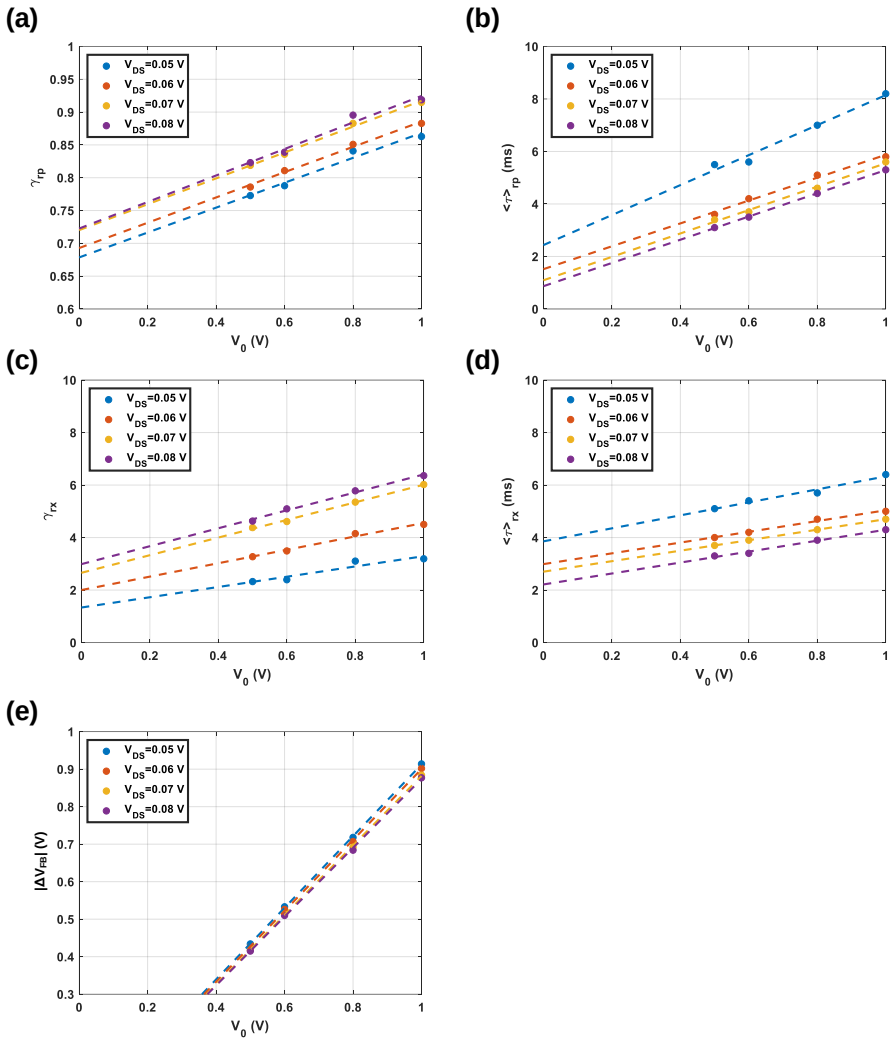

Figure 3. 4 The trends of Synaptic parameters such as (a) γ_{rp}, (b) $\langle\tau\rangle_{rp}$, (c) γ_{rx}, (d) $\langle\tau\rangle_{rx}$, and (e) $|\Delta V_{FB}|$ at V_{DS} of 0.05, 0.06, 0.07, and 0.08 V under the variation of V_0. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

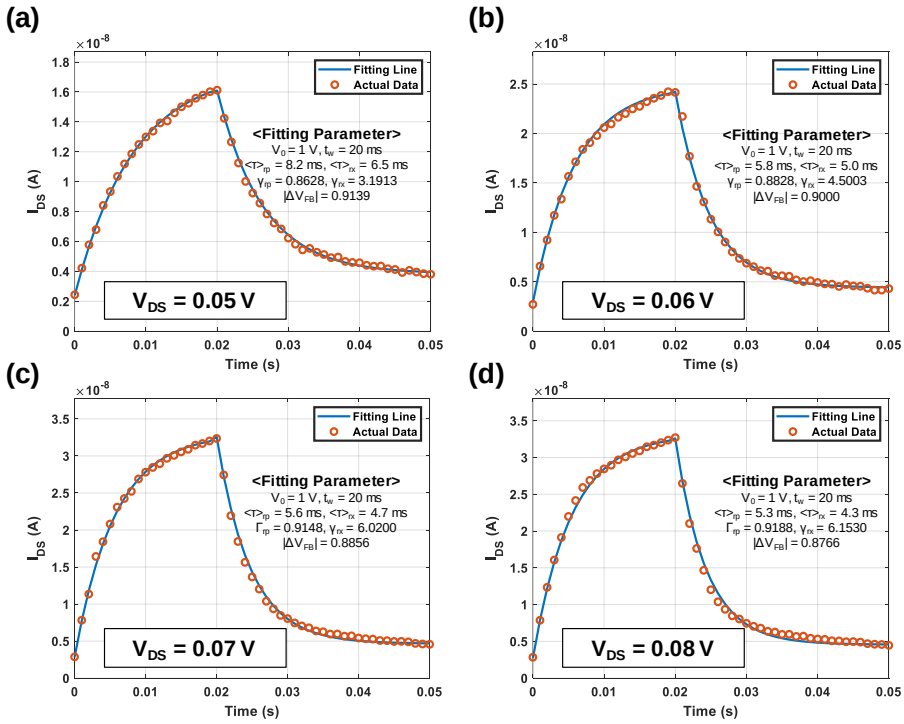

Figure 3. 5 Actual EPSC and fitted EPSC using SPSE model in ynaptic TFT with the combination of SiO_2 and IGZO according to V_{DS} of (a) 0.05, (b) 0.06, (c) 0.07, and (d) 0.08 V at fixed V_0 = 1 V. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

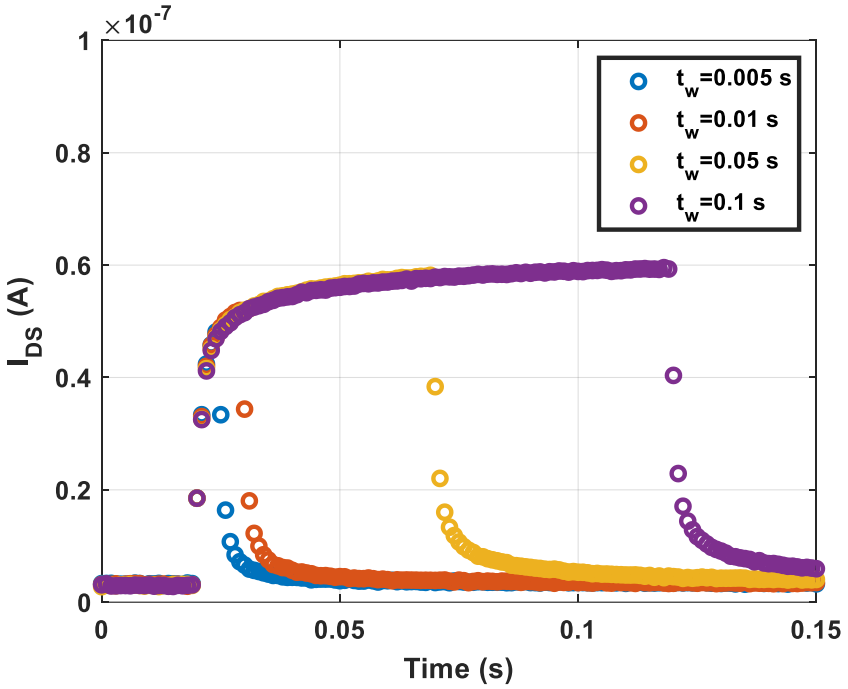

Figure 3. 6 The measured EPSC over time in the synaptic TFTs with the combination of SiO_2 and IGZO at t_w of 0.005, 0.01, 0.05, and 0.1 V. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

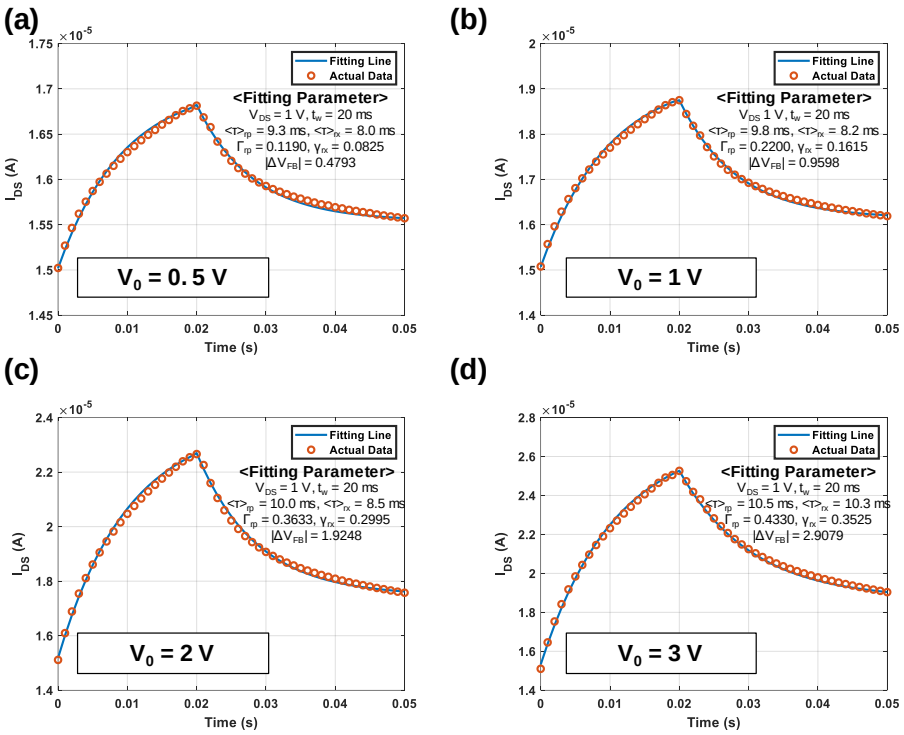

Figure 3. 7 Actual EPSC and fitted EPSC using SPSE model in synaptic TFT with the combination of WiBS/polymer electrolyte and IGZO according to V_0 of (a) 0.5, (b) 1, (c) 2, and (d) 3 V. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

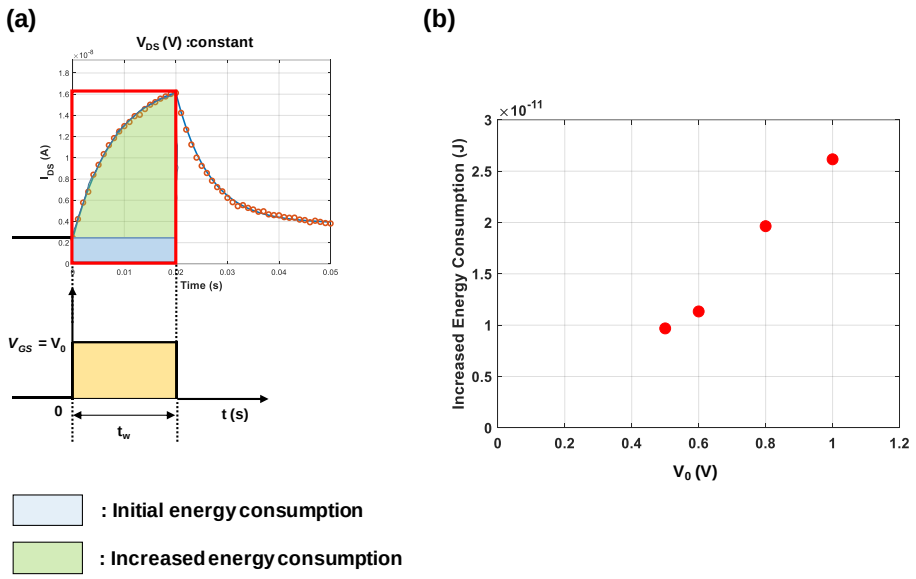

Figure 3. 8 EPSC shape and energy consumption of the synaptic TFT. (a) Initial and increased energy consumption calculated from EPSC shape and (b) the change in increased energy consumption according to V_0. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

Parameters	**Values** (V_{GS} **= 0.5/0.6/0.8/1 V)**	**Units** (V_{GS} **= 0.5/0.6/0.8/1 V)**
$<\tau>_{rp}$	9.3/9.8/10.0/10.5	ms
γ_{rp}	0.1190/0.2200/0.3633/0.4330	-
$<\tau>_{rx}$	8.0/8.2/8.5/10.3	ms
γ_{rx}	0.0825/0.1615/0.2995/0.3525	-
$\lvert\Delta V_{FB}\rvert$	-0.4793/-0.9598/-1.9248/-2.9079	V

Table 3. 2 All parameter values of synaptic ion-gel-based WiBS-TFT for SPSE model according to V_{GS} in Figure 3. 5. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

3.6 Mathematical approach about meaning of the parameters

Both γ_{rp} and γ_{rx} contain the information about the current ratio of the initial current to the saturated current. Figure 3. 9a shows calculated EPSC (blue line) using SPSE model and ideal steady-state drain current (red line) in the responsive region (blue area) when a single V_{GS} pulse is applied. If time-varying term is not included, it appears as an ideal current in a steady-state where the drain current is a red line and increases directly to the blue dot. However, actual EPSC requires a response time, so time-varying term should be included. γ_{rp} can be obtained from the boundary condition of Equation 3. 3 at $t = 0$ using the following equation:

$$I_{DS}^{off}(0\ \text{V}, V_{F0}) = \left(1 - \gamma_{rp}\right)\ \ I_{DS}^{on}(V_0, V_{F0}) \tag{3. 13}$$

$$\gamma_{rp} = 1 - I_{DS}^{off}(0\ \text{V}, V_{F0})/I_{DS}^{on}(V_0, V_{F0}) \tag{3. 14}$$

where $I_{DS}^{off}(0\ \text{V}, V_{F0})$ (or $I_{DS}^{on}(V_0, V_{F0})$) is the steady-state drain current at $V_{FB} = V_{F0}$ and $V_{GS} = 0\ \text{V}$ (or $V_{GS} = V_0$). In this case, I assume that V_{FB} does not change until a V_{GS} pulse is applied. Even if there is a slight change in the parameters, they are all dumped into the ratio constant values. As can be seen in the fitting section of the main manuscript, this assumption is valid. In Equation 3. 13, the left side is the third equation in Equation 3. 3 and the right side is the first equation in Equation 3. 3 at $t = 0$ (the exponential term disappears on the right side). Since EPSC is continuous over all time ranges, the left and right sides must

be always the same. By rearranging the terms, Equation 3. 14 for γ_{rp} can be expressed. As V_0 increases, $I_{DS}^{on}(V_0, V_{F0})$ also increases. Thus, γ_{rp} increases by Equation 3. 14. As V_{DS} increases, $I_{DS}^{off}(0\ \text{V}, V_{F0})$ and $I_{DS}^{on}(V_0, V_{F0})$ move to purple and blue dotted line, respectively, and the difference between $I_{DS}^{off}(0\ \text{V}, V_{F0})$ and $I_{DS}^{on}(V_0, V_{F0})$ increases (see Figure 3. 9b). Consequently, γ_{rp} also increases. As a result, the increase in V_0 and V_{DS} results in increase in γ_{rp}.

Figure 3. 9c shows actual EPSC and ideal steady-state current in the relaxed region (green area) after V_{GS} pulse. γ_{rx} can be obtained from the boundary condition of this EPSC at $t = t_w$ using the following equation:

$$\left(1 - \gamma_{rp} e^{-\frac{t_w}{\langle\tau\rangle_{rp}}}\right)\ I_{DS}^{on}(V_0, V_{F0}) = (1 + \gamma_{rx})\ I_{DS}^{off}(0\ \text{V}, V_{F1}) \tag{3. 15}$$

$$\gamma_{rx} = \left(1 - \gamma_{rp} e^{-\frac{t_w}{\langle\tau\rangle_{rp}}}\right)\ I_{DS}^{on}(V_0, V_{F0}) /\ I_{DS}^{off}(0\ \text{V}, V_{F1}) - 1 \tag{3. 16}$$

where $I_{DS}^{off}(0\ \text{V}, V_{F1})$ (or $I_{DS}^{on}(V_0, V_{F0})$) is the steady-state drain current at $V_{FB} = V_{F1}$ (or $V_{FB} = V_{F0}$) and $V_{GS} = 0$ V (or $V_{GS} = V_0$). In Equation 3. 15, the left side is the first equation in Equation 3. 3 and the right side is the second equation in Equation 3. 3 at $t = t_w$. At this time, the exponential term on the left side does not disappear, otherwise exponential term on the right side disappear. By rearranging the terms, Equation 3. 16 for γ_{rx} can be expressed. As V_0

increases, $I_{DS}^{on}(V_0, V_{F0})$ also increases. Thus, γ_{rx} increases by Equation 3. 16. As V_{DS} increases, $I_{DS}^{off}(0\ \text{V}, V_{F1})$ and $I_{DS}^{on}(V_0, V_{F0})$ move to green and red dotted line, respectively, and the difference between $I_{DS}^{off}(0\ \text{V}, V_{F1})$ and $I_{DS}^{on}(V_0, V_{F0})$ increases (see Figure 3. 9d). Consequently, γ_{rx} also increases. As a result, the increase in V_0 and V_{DS} results in increase in γ_{rx}, which is similar to γ_{rp}. These tendencies of γ_{rp} and γ_{rx} appear the same in all synaptic transistors using n-type OS because EPSC always increases as V_{GS} and V_{DS} increase. However, the differences in value appear entirely depending on the intrinsic material properties and applied variable values.

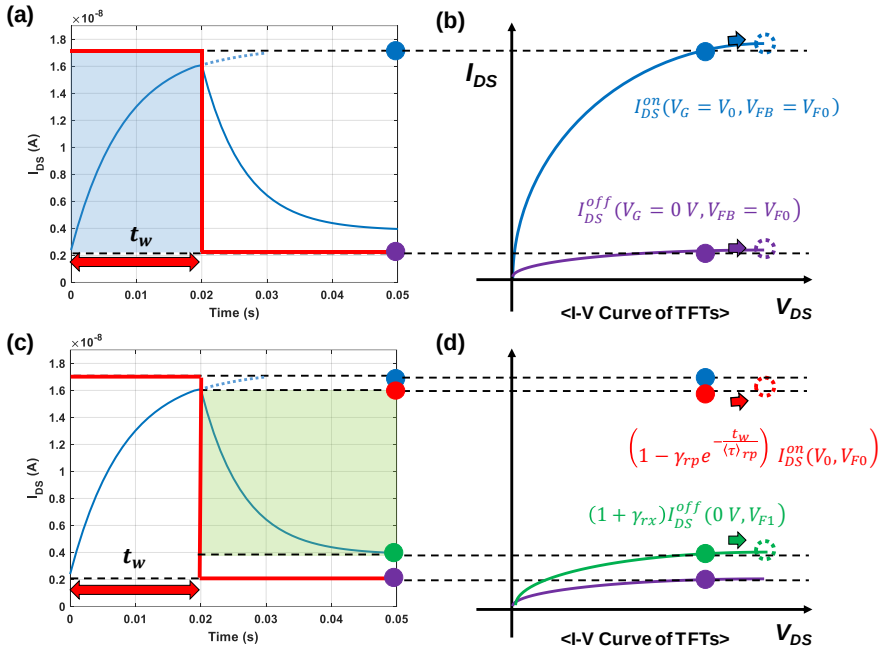

Figure 3. 9 Calculated EPSCs (blue line) using SPSE model and ideal steady-state drain currents (red line) in (a) responsive region and (c) relaxed region. The output curves of the saturated I_{DS} value (blue and green dot) and initial I_{DS} value (purple and red dot) in (b) responsive region and (d) relaxed region according to V_{DS}. Reproduced with permission of Ref. 40. Published under an exclusive license by AIP Publishing.

3.7 Sequential fitting process for SPSE model

The measurement data is fitted through the following process. At first, I_{DS}^{on} (or I_{DS}^{off}) in Equation 3. 3 can be obtained from the steady-state drain current equation taken from the reference 39. At this time, V_{FB} value was obtained from the measured transfer curve and then substituted it into that equation.

Then, the total EPSC equation with time-varying term can be obtained through the sequential process below. Once V_{GS} value is set to V_0, the steady-state EPSC value is determined (red line in Figure 3. 9a). This is the maximum value (blue dot in Figure 3. 9a) that EPSC can reach when t_w is long enough, but in typical synaptic devices, EPSC cannot reach this value because t_w is very short. Then, the initial EPSC value (purple dot in Figure 3. 9a) is set by adjusting γ_{rp} value. Subsequently, increasing EPSC shape in the responsive region is set by adjusting $\langle\tau\rangle_{rp}$ value.

After a single V_{GS} pulse, the gate electrode is reset to 0 V, decreasing EPSC. I assumed that V_{FB} does not change until a V_{GS} pulse is applied. At this time, the saturated EPSC value (green dot in Figure 3. 9c) larger than the initial EPSC value (purple dot in Figure 3. 9a) is set by adjusting V_{FB} ($V_{GS} = 0\ V$). The larger this difference is, the stronger the synaptic performance is. Subsequently, the point (red dot in Figure 3. 9c) at which EPSC start to decrease is set by adjusting

γ_{rx} value. Finally, the decreasing EPSC shape in the relaxed region is set by adjusting $\langle\tau\rangle_{rx}$ value. As I showed in the main manuscript, the fitting through these processes fit very well.

3.8 Conclusion

In summary, I newly proposed SPSE model that can systematically analyze the EPSC of the synaptic TFTs, where it employs the time-delaying constants ($\langle\tau\rangle_{rp}$ and $\langle\tau\rangle_{rx}$) and the ratio constants (γ_{rp} and γ_{rx}). Time-delaying constants, which include the information of nominal capacitance, can determine the increasing rate (or decreasing rate) of EPSC. The ratio constants control the synaptic window, which is the offset of the drain current after the EPSC process. Increasing $\langle\tau\rangle_{rp}$, $\langle\tau\rangle_{rx}$, γ_{rp}, and γ_{rx} can make wider synaptic window and lead to more memory slots in the process of EPSC, which can be enabled with the increment of V_0. For the long-term non-volatile memory effect after the EPSC period, ΔV_{FB} is essential where it mainly depends on the material in the devices. However, in the case of higher V_{DS} at fixed V_0, the time-delaying constants show the opposite tendencies, resulting in the degradation of the synaptic properties. At V_0 = 0.5 ~ 1 V and V_{DS} = 0.05 ~ 0.08 V conditions, the EPSCs of synaptic SiO_2-TFTs and the ion-gel-TFTs (*i.e.*, WiBS-TFTs) are clearly explained using the SPSE model with fitting parameters of $\langle\tau\rangle_{rp}$, $\langle\tau\rangle_{rx}$, γ_{rp}, and γ_{rx}. In particular, the model can capture the improved short-term and long-term synaptic properties of the WiBS-TFTs with higher ΔV_{FB} and lower γ_{rx}. The $V_0 - E_c$ characteristics show that the energy consumption of EPSC

process can be monotonically increased with V_0, and the condition with higher V_0 can lead to better the synaptic performances, but it consume more energy. With the SPSE model, an in-depth understanding of EPSCs by a single V_{GS} pulse will be a guideline to systematically study the performance (e.*g.*, linearity) of the synaptic devices.

3.9 Experimental section

Fabrication of the synaptic TFTs: To fabricate the oxide semiconductor (OS)-based TFTs, the heavily B-doped p-type Si wafers (P^{++}-Si) with thermally grown 200 nm SiO_2 layer (gate insulator) was used as the gate electrode. The wafers were subsequently cleaned by detergent for 15 min, de-ionized (DI) water rinsing for 20 min, acetone for 15 min, and isopropyl alcohol (IPA) for 15 min. All cleanings except DI water rinsing were conducted in ultrasonic bath. IGZO layer was deposited on a SiO_2/Si substrate by radio frequency (RF) sputter (DAEKI HI-TECH co., Ltd, Co-Sputtering System) with a planer round target consisting of IGZO (In:Ga:Zn:O = 1:1:1:4 at%) under 10^{-4} mTorr at room temperature. The RF sputtering power was fixed at 90 W in Ar (25 sccm) gas. Then, sputtered IGZO layer was annealed at the atmospheric pressure condition at 250 ℃ for 90 s by rapid temperature annealing (RTA) method. Thereafter, aluminum electrodes (source and drain) were deposited with a thickness of 100 nm by thermal evaporation using FMMs. Channel width and length of FMMs are 1000 and 50 μm, respectively. And all synaptic TFTs were patterned using photolithography and wet etching process to prevent leakage current.

Synthesis of WiBs/polymer electrolyte layer: To synthesize WiBS/polymer

electrolyte film, 21 M lithium bis (trifluoromethanesulfonyl) imide (LiTFSI) [TCI Co., Ltd, >98%] was dissolved in DI water. Then, additional 7 M lithium trifluoromethanesulfonate (LiOTf) [Sigma-Aldrich, 99.995%] in the previously mixed solution. Finally, polyethylene glycol dimethacrylate (PEGDMA) [Sigma-Aldrich, M_n = 550] and 2-hydroxy-2-methylpropiophenone (HOMPP) [Sigma-Aldrich, 97%] were mixed in a weight ratio of 100:100:2. Arbitrary mixer (AR 100, Thinky mixer) was used to homogeneously blend all materials.

Measurement and analysis: The current-voltage characteristics for the synaptic TFTs were measured using Keysight B2902A and Agilent 4155B semiconductor parameter analyzer with compliance current of 10^{-2} A at room temperature in the dark conditions.

3.10 References

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Chapter 4

Conclusion

In this thesis, I proposed two engineering strategies for conduction mechanisms and principles based on physical approache. Chapter 2 introduced the implementation of high-performance dual-stacked TFTs and working mechanism via equivalent circuit modeling. InO_x with high carrier concentration was used as a channel layer at the bottom of OSs, and IGZO with superior off-state characteristics was used as a buffer layer at the top of OSs. First of all, the electrical properties in TFTs with single InO_x and single IGZO were verified according to the thickness, respectively. Based on the optimized conditions of dual-stacked OSs, dual-stacked TFTs comprising an optimized thickness of 10 nm InO_x and 30 nm IGZO realized the superior field-effect mobility of of ~80 $cm^2/V \cdot s$, ideal threshold voltage near 0 V, and very high on-off current ratio of $>10^9$. In addition, I presented the conduction mechanism step by step using the concept of the induced areas. When the seperate materials are junctioned, band-offset occurs, causing the energy band to bend. This was confirmed by XPS, UV-vis, and UPS analysis. This phenomena acts as another charge source for the current flow as well as the electrons accumulated by the gate bias. Furthermore, in-situ analysis was conducted through changes in bulk resistance according to external bias in dual-stacked TFTs to support this mechanism. For this purpose, TLM, a powerful method of extracting various resistive elements, was introduced.

The existence of confined electrons was confirmed between two OSs, which affects current flow to improve field-effect mobility. Based on the comprehensive verification of phenomena at the interface of dual-stacked structure, I developed new design rules for the high performance OS-based TFTs. Such proposed design rules are expected to be implemented widely for applications that require fast response, ultra-high resolution, and low power consumption.

In Chapter 3, I analytically proposed an SPSE model of synaptic TFTs. SPSE model can simulate EPSC of synaptic device at given TFT-operating conditions. EPSC with the SPSE model can be characterized with quantified parameters for the capacitive effects and the synaptic windows, which also depend on the electrical condition applied to TFT. In addition, flat-band voltage shift was applied to represent the nonvolatile memory characteristics. I simulated how the synaptic characteristics change when only each variable is changed while other parameter values are fixed. It was confirmed that the larger all variables, the more synaptic characteristics appeared. There are two ways to control the variables in synaptic TFTs: selction of appropriate materials and adjustment of electrical conditions. In the case of material selection, it is difficult to increase all variables at the same time because the materials have their own characteristics. Therefore, I decided to control the variables by adjusting the electrical conditions. As a result

of fitting through the SPSE model, It was confirmed that V_{GS} is more critical factor than V_{DS}. Synaptic TFTs with different gate insulators (*e.g.*, SiO_2 and ion-gel) are used to confirm the performance of SPSE model. Ion-gel-typed TFTs represented excellent synaptic properties, which were realized as quantified values of variables. In addition, SPSE model enables the estimation of energy consumption, which can potentially be leveraged to compare the energy cost of EPSC fairly. With the SPSE model, an in-depth understanding of EPSCs by a single V_{GS} pulse will be a guideline to systematically study the performance (e.*g.*, linearity) of the synaptic devices.

■ Advantages

-. The highest field-effect mobility (~80 $cm^2/V \cdot s$) among those known so far was obtained among the studies using sputtering in the low temperature process (250 ℃).

-. For the first time, I used the in-situ method to confirm the presence of confined electrons and to confirm that they actually contribute to the flow of current in dual-stacked TFTs.

-. For the first time, I proposed transient drain current model with time response

in synaptic TFTs and systematically analyzed the meaning of each variable in this model.

-. I defined exact energy consumption that occurs when square voltage pulse was applied to synaptic TFTs.

■ Disadvantages

-. Due to the leaky characteristics of InO_x, there is a slight deviation in dual-stacked TFTs between the devices.

-. Since the sputtering process is required twice for dual-stacked structure, the process cost may increase.

-. For mathematical convenience, ΔV_{FB} was used as a step function, or the time-delaying constants and the capacitance value were used at the same time in SPSE model. It is more of an empirical model than a physical model. Further reinforcement of these values was needed to have a more physical meaning.

■ Future research direction

-. It is necessary to find materials with better properties as a channel of dual-stacked TFT and structural changes are also necessary.

-. It is necessary to check whether in-situ analysis through TLM is possible even

in a wider range of external bias.

-. For the SPSE model to have more physical meaning, more variables such as ΔV_{FB} and time-delaying constants should be defined as a function of time.

List of publications

1. ACS Applied Materials & Interfaces, 13 (43), 51266-51278 (2021). **Changik Im**, Jiyeon Kim, Nam-Kwang Cho, Jintaek Park, Eun Goo Lee, Sung-Eun Lee, Hyun-Jae Na, Yong Jun Gong, Youn Sang Kim, “Analysis of Interface Phenomena for High-Performance Dual-Stacked Oxide Thin-Film Transistors via Equivalent Circuit Modeling”.

2. Journal of Applied Physics, Accepted (2022). **Changik Im**, Jiyeon Kim, Jae Hak Lee, Minho Jin, Haeyeon Lee, Jiho Lee, Jong Chan Shin, Chan Lee, Youn Sang Kim, Eungkyu Lee, “Excitatory postsynaptic current model for synaptic thin-film transistors”.

3. ACS Applied Materials & Interfaces, 11 (4), 4103-4110 (2019). Junhee Lee, Jinwon Lee, Jintaek Park, Sung-Eun Lee, Eun Goo Lee, **Changik Im**, Keon-Hee Lim, Youn Sang Kim, “Solution-Grown Homojunction Oxide Thin-Film Transistors”.

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요 약 (국문초록)

산화물 박막 트랜지스터의 이중 적층 구조에서의 계면 현상 분석과 시냅틱 전류 모델링

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디스플레이 분야에서의 박막 트랜지스터(TFT)는 스위칭 소자로 사용되어 왔다. 기존 사용하던 평면 디스플레이 기기가 투명하고 유연하게 변화하고 있고, 이에 따라 이러한 특성들을 모두 갖춘 산화물 반도체(OS)가 TFT의 채널층으로 각광받고 있으며, 지속적인 연구 또한 진행되고 있다. 인듐-갈륨-아연 산화물(IGZO) 반도체는 안정적인 오프전류 특성과 0 V에 가까운 이상적인 임계전압으로 인해 TFT의 채널 층으로 활발히 사용되고 있다. 그러나 뛰어난 오프 특성에도 불구하고 IGZO TFT는 낮은 전계효과 이동도(약 10 $cm^2/V \cdot s$)로 인해 제약이 크며, 이는 디스플레이

해상도와 전력 소비량에 심각한 영향을 미친다. 이 문제를 해결하기 위해 이중 OS를 사용하는 이중 적층 TFT가 도입되었다. 그러나 전계효과 이동도(30-60 $cm^2/V \cdot s$)가 크게 개선됐음에도 불구하고 오프 전류 특성은 여전히 문제가 된다.

본 연구에서는 우수한 오프 특성을 유지하면서도 매우 높은 전계효과 이동도(~80 $cm^2/V \cdot s$)를 갖는 이중 적층 TFT가 구현됐다. 전도 메커니즘을 시각적으로 나타내기 위해서 네 가지의 유도 영역을 새롭게 제안했으며, 보다 정확한 확인을 위해 등가회로 모델링과 전송선 방식도 도입했다. 이것은 이중 적층 TFT의 전도 메커니즘을 체계적으로 이해하는 데 도움을 줄 것이며, 추후 고성능 OS 기반 TFT를 설계하는데 새로운 기준이 될 것이다.

인간의 뇌를 모방하는 시냅스 장치는 뇌에서 영감을 받은 신경 동형 시스템으로 많은 관심을 끌었다. 특히 시냅스 TFT는 동시 신호 처리와 정보 저장의 장점을 갖고 있다. 다만 흥분성 시냅스 후 전류(EPSC)는 전기적 조건에 따라서 다르게 나타나고 시간이 지남에 따라 변화하기 때문에 다루는데 지금까지 어려움이 있었다. 이러한 복잡성 때문에 지금까지 반복적인 실험 측정만으로 조건이 확인되었다.

이를 분석하기 위해, 단일 펄스 구동 시냅스 EPSC(Single-Pulse Driven Synaptic EPSC) 모델이 제안되었다. 이 모델은 시간이 지남에 따

라 변화하는 EPSC를 나타낼 수 있는 최초의 모델로 주어진 TFT 작동 조건에서 시냅스 장치의 EPSC를 시뮬레이션할 수 있다. SPSE 모델은 TFT에 적용되는 전기적 조건에 따라 용량 효과와 시냅스 창을 의미하는 정량화된 매개변수를 특성화할 수 있다. 다양한 게이트 절연체를 사용하여 SPSE 모델의 타당성 또한 검증했다. 이 모델은 EPSC의 에너지 비용을 비교하는 데 잠재적으로 활용될 수 있는 에너지 소비량 추정을 가능하게 한다. SPSE 모델은 시냅스 장치의 EPSC에 대한 포괄적인 이해를 바탕으로 더 나은 시냅스 성능을 위한 적절한 작동 조건을 설계하기 위한 지침을 제공할 것이다.

주요어: 박막 트랜지스터, 전계효과 이동도, 전도 메커니즘, 등가회로, 시냅스 장치, 흥분성 시냅스 후 전류, 드레인 전류 모델, 에너지 소모

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