공학석사학위논문

은-산화구리 코어-쉘 나노 와이어 네트워크에 기반한 유연·신축성 멤리스터 소자의 제작

Fabrication of Flexible and Stretchable Memristors based on Ag@Cu_2O Core-Shell Nanowire Networks

2023 년 2 월

서울대학교 대학원

기계공학부

김 문 주

은-산화구리 코어-쉘 나노 와이어 네트워크에 기반한 유연·신축성 멤리스터 소자의 제작

Fabrication of Flexible and Stretchable Memristors based on Ag@Cu_2O Core-Shell Nanowire Networks

지도교수 고 승 환

이 논문을 공학석사 학위논문으로 제출함

2022 년 10 월

서울대학교 대학원

기계공학부

김 문 주

김 문 주의 공학석사 학위논문을 인준함

2022 년 12 월

위 원 장 : 도형록 (인)

부위원장 : 고승환 (인)

위 원 : 송한호 (인)

Abstract

Stretchable memristors are promising electrical components that can improve the mechanical robustness of neuromorphic devices. By the enhancement of mechanical robustness, they can be applied to wearable devices and soft robotics. Herein, a flexible and stretchable memristor based on nanowire networks is reported. The memristor mainly consists of Ag@Cu_2O core-shell nanowires that are synthesized through a modified polyol process. The relative shell thickness was controlled in the synthesis process to achieve high stability and low energy consumption. The fabricated memristor shows memristive switching ratio over 10^4, with HRS resistance of ~100MΩ and LRS resistance of ~7kΩ. It operated stably with retention time of 25000s and went through more than 200 switching cycles without significant resistance change. Furthermore, it well operated in harsh mechanical environments up to 9% strain and 30℃ heating. The experimental results and the theoretical modelling of the core-shell NWs network based memristor was verified through simulation results, based on an implicit computational model.

Keyword : Stretchable memristors, Ag@Cu_2O core-shell nanowires, Nanowire networks, Neuromorphic engineering

Student Number : 2020-24015

Table of Contents

List of Figures

Figure 11. The LRS resistance of the memristor versus the relative shell thickness.

Figure 12. (a) Retention test and (b) set/reset cycling test of the memristor.

Figure 13. IV-curves in various (a) strain conditions and (b) temperature conditions.

Figure 14. (a) Single junction conductivity modeling and (b) simulation result.

Figure 15. (a) Network conductivity modeling and (b) simulation result.

Figure 16. Formation of conductive filaments on nanowire junctions as voltage is incrementally applied between the electrodes.

Chapter 1. Introduction

1.1. Backgrounds and previous studies

Neuromorphic engineering attempts to mimic the neuro-biological structure of the nervous system. The mimicked nervous system increases the operation speed of a hardware and decreases memory usage. In addition, it can solve the bottleneck effect which is a critical problem in conventional Von Neumann architecture. To successfully mimic the nervous system of human, the system requires an electrical component called a “memristor”, which works both as a calculator and a memory. Therefore, recent studies have been dedicated to manufacture memristors with higher similarity with the human nervous system(1-4).

Flexibility and stretchability need to be achieved for memristors to be applied in wearable devices and soft robotics. However, less attempt has been made to manufacture stretchable memristors. This is because it is difficult to achieve flexibility and stretchability since memristors are usually made of rigid materials such as metal and metal-oxide(5).

As one of the methods to manufacture stretchable memristors, structural designs to endure mechanical damages were introduced. Discrete structure designs that distributed separated small subunits of memristors on stretchable spaces made the memristor unit to overcome mechanical deformations. Particularly, in the study by Yang et al(6), Au/AgNPs/Au memristors on polydimethylsiloxane (PDMS) substrate which operated well in 60% strain were introduced. Wang et al(7) demonstrated Ag/HfO_2/Au memristors on Styrene-ethylene-butylene-styrene

(SEBS) substrate that can endure 40% strain.

Previous studies mainly focused on structural approaches, not material approaches. These approaches may obtain stretchability on blank spaces of the substrate, but the region where memristor units lay still remain brittle. For complete stretchability and flexibility, the materials that compose the memristor should also endure mechanical stress.

1.2. Purpose of Research

Herein, stretchable memristors based on Ag@Cu_2O core-shell nanowire networks are introduced. Because of the distinguishable electric properties of metallic Ag and semi-conductive Cu_2O, the total resistance of the NWs network transits from high resistance state (HRS) to low resistance state (LRS) or the opposite. Thus, the NWs network operates as a nonvolatile memristor. In this study, we optimized the synthesis process of Ag@Cu_2O core-shell NWs to fabricate a memristor that assures high stability and low energy consumption while going through multiple switching cycles.

The flexibility and stretchability of the memristor is obtained by modifying both its composing material's property and its structure. First, to modify the material property of the main composing material, we synthesized the metal/semiconductor composite as nanowires. This is because 2-dimensional nanowires show higher flexibility and stretchability compared to 3-dimensional bulk metal or semiconductor. Second, we deposited the nanowires to a flexible polymer substrate in a random network form. The random network structure of the

nanowires shows high flexibility and stretchability compared to orderly distributed nanowires. With these material and structural enhancements, memristors based on Ag@Cu_2O core-shell nanowire networks can operate in harsh strain conditions.

Chapter 2. Materials and Method

2.1. Materials

AgNWs of average 30nm thickness and 30μm length were used for both the electrode and core of the core-shell NWs. They were synthesized via a modified polyol method. Copper(II) chloride dihydrate ($CuCl_2$) (≥99.95%), sodium dodecyl sulfate (SDS) (≥98.5%), sodium hydroxide (NaOH) (≥98%, pellets), and hydroxylamine hydrochloride ($NH_2OH \cdot HCl$) (99%) were purchased from Sigma Aldrich. These materials were used when synthesizing Ag@Cu_2O core-shell NWs.

2.2. Fabrication of AgNWs electrode

Firstly, PDMS were coated on 1mm glass, in order to be used as the substrate for electrodes. Spin coating method (300rpm, 30s) was used for this process. The thickness of the substrate was carefully controlled. If the substrate is too thick, less stretchability is achieved and can be torn when stretching. On the other hand, if the substrate is too thin, it is hard to control. The optimized spin coated PDMS substrate had a thickness of 0.15~0.2mm. Afterwards, 1mL of AgNWs were transferred to the PDMS substrate by vacuum filtration method. The transferred AgNWs showed resistance under 20Ω. Ag NWs were patterned into rectangular-shaped electrode structures with ~60μm electrode spacing, through 355nm wavelength laser ablation.

2.3. Synthesis of Ag@Cu_2O Core-Shell NWs

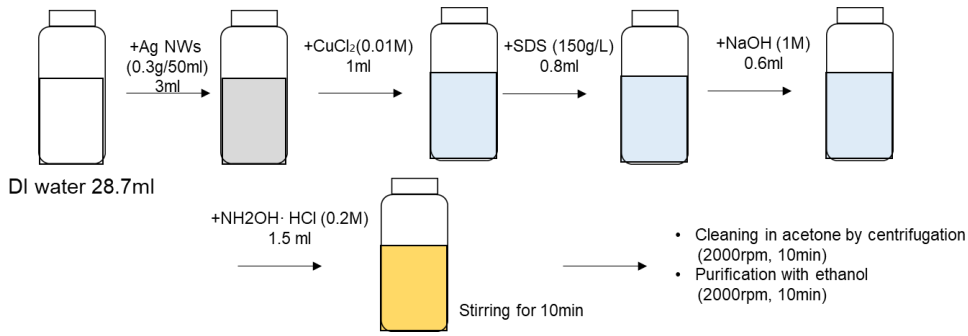

Figure 1. The schematic diagram of the fabrication process of core-shell NWs.

Ag@Cu_2O core-shell NWs were synthesized via a modified Au@ Cu_2O core-shell NPs synthesis process reported by Zhu et al(8) and Yuan et al(9). 2.7mL of AgNWs, 1mL of 0.01M $CuCl_2$ solution, 0.8mL of SDS aqueous solution(150g/L), and 0.6mL of 1M NaOH solution were put into 28.7mL of DI water in succession. After 3 min of stirring at 100rpm, 1.5mL of 0.2M $NH_2OH·HCl$ solution was put in and 10 minutes of additional stirring was progressed. The core-shell NWs were cleaned with acetone using centrifugation (2000rpm, 10mins). Then, they were redispersed in ethanol and cleaned again by the same method of centrifugation.

AgNWs and $CuCl_2$ solution are the main ingredient that composes the Au@Cu_2O NWs. SDS solution is added to work as a dispersant and NaOH solution are added to control the pH of the whole solution during the synthesis process. Finally, $NH_2OH·HCl$ solution works as a reducing agent to reduce the Cu^{2+} of the $CuCl_2$ solution to Cu^{+} of Cu_2O. The Cu^{2+} ions are first randomly dispersed in the solution and then attaches around the AgNWs as the $NH_2OH·HCl$ solution is added. In this study, we successfully modified the study by Zhu et al, by changing the main matieral form AgNPs to AgNWs. Compared to the previous study by Zhu et

al, the synthesis time (excluding the cleaning process) was remarkably reduced from more than 1 hour to 15 minutes. The optic images of the AgNWs aqueous solution and Au@Cu_2O NWs dispersed in ethanol are shown in **Figure 2a**.

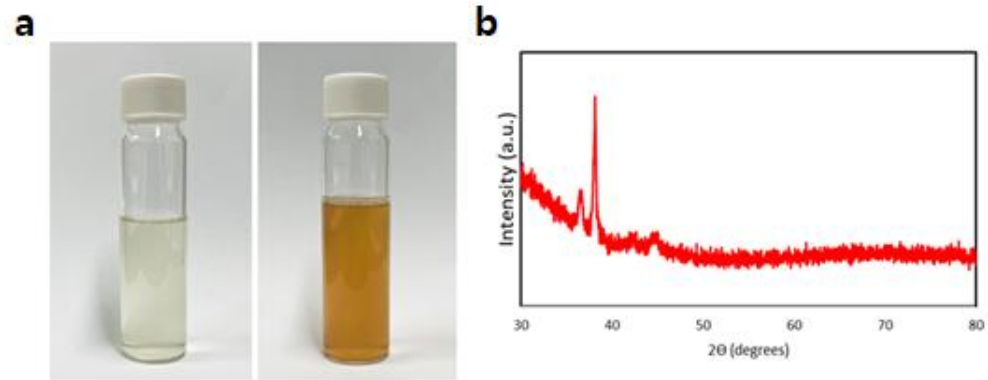

Figure 2. (a) Optic images of AgNWs aqueous solution and Au@Cu_2O NWs dispersed in ethanol and (b) X-ray diffraction of the synthesized core-shell NWs.

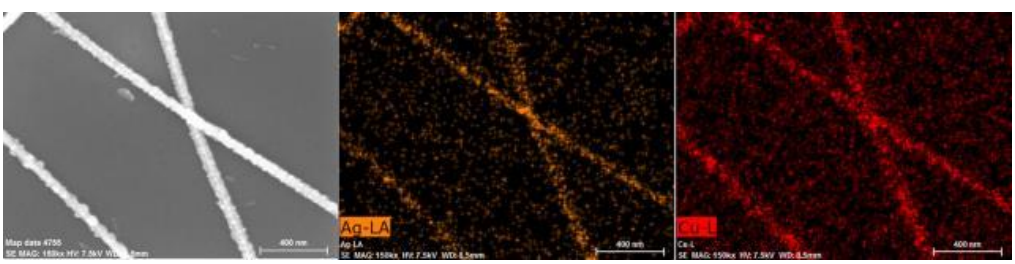

Figure 3. EDS elemental maps of the synthesized core-shell NWs.

Ag cores and Cu_2O shells of the NWs were identified by XRD pattern analysis (**Figure 2**) and EDS elemental maps (**Figure 3**). Ag peak and Cu_2O peak appeared in the XRD pattern. The known main peak of Ag (JCPDS: 04-0783) is 38 degrees, and the main peak of Cu_2O (JCPDS: 05-0667) is 36 degrees according to JCPDS. Likewise, Ag cores and Cu shells were observed in EDS elemental maps.

Therefore, we could conclude that the Ag@Cu_2O core-shell NWs were successfully synthesized.

2.4. Fabrication of the Memristor

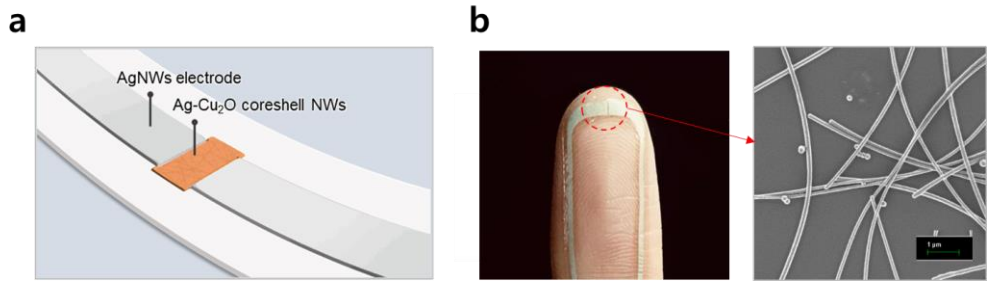

Figure 4. (a) Schematic of the fabricated memristor and (b) an optic image of the memristor on a finger.

Synthesized core-shell NWs were deposited onto the AgNWs electrode by vacuum filtration method. 6.5mL of Ag@Cu_2O core-shell NWs solution were used per sample. In order to enhance the stretchability of the memristor, we used a pre-strain method. Before transferring the core-shell NWs, the PDMS substrate was stretched 20%. Then, the NWs were transferred to the stretched PDMS, and the pre-strain was carefully released afterwards. This method significantly enhanced the stretchability of the memristor

Eventually, a random percolation network of core-shell NWs was formed in the 60μm spacing between two AgNWs electrodes. **Figure 4b** shows the optic image of the memristor on a finger. As shown, they are flexible and small enough to be applied to wearable devices.

Chapter 3. Memristor Characterization

3.1. Operation Mechanism

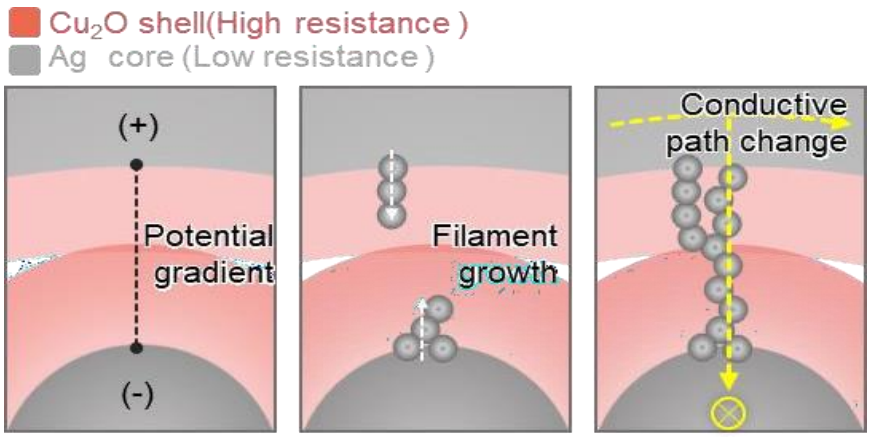

Figure 5. The schematic diagram of the set process.

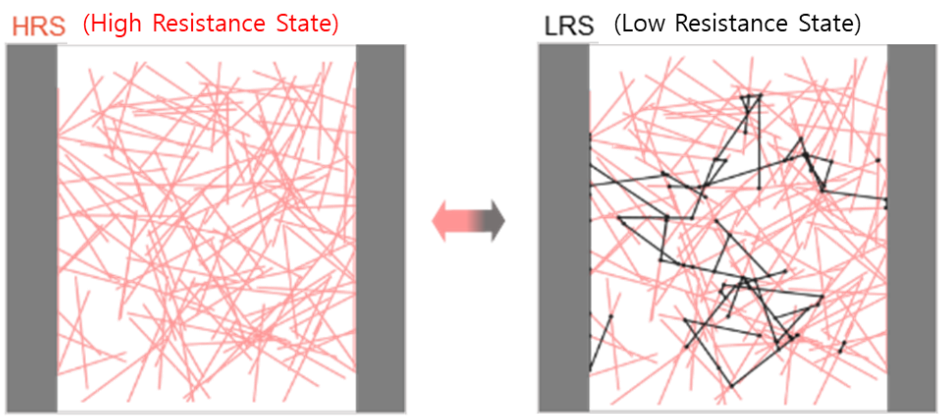

Figure 6. The schematic diagram of the switching process between the HRS and the LRS.

The fabricated Ag@Cu_2O core-shell NWs network memristor reversibly transits from the HRS (high resistance state) and LRS (low resistance state) or the

opposite way, reflecting the electrical material characteristics of Ag and Cu_2O. As a conductive material, Ag shows relatively low resistance. On the other hand, Cu_2O is a semiconductor material which shows relatively high resistance. The resistance of the memristor is controlled by the formation and destruction of a conductive filament that passes through the Cu_2O shells (**Figure 5**).

Originally, conductive paths form through the Cu_2O shells of the NWs network (**Figure 6**). Therefore, the high resistance of Cu_2O dominantly affects the resultant resistance between the electrodes. This is the HRS for which the resistance is ~100MΩ.

When voltage is applied with appropriate compliance current (the compliance current was chosen as 0.1mA in this study), each nanowire obtains different electrical potential. Therefore, electrical potential gradient is formed between adjacent nanowires. Due to the potential gradient, oxygen vacancies migrate in specific direction and align through the Cu_2O shell. This "filament" consisting of oxygen vacancies is conductive, connecting some of the conductive Ag cores of the NWs network. As the low resistance of Ag cores affect the resultant resistance between electrodes (**Figure 6**), the memristor switches to the LRS with resistance of ~7kΩ. When voltage is applied between the electrodes, current will mostly flow through the nanowires that are connected through the conductive filament and Ag cores. This is because the resistances of the conductive filament and Ag cores are significantly lower than the Cu_2O shell. Therefore, the LRS resistance will rely on the length of the "conductive path" formed by the conductive filament and Ag cores.

The memristor can switch again to the HRS by destroying the conductive filaments. This can be done by applying voltage without setting any compliance

current. As high current flows through the conductive filaments, rupture forms because of the heat generated by Joule heating(10, 11). Using an IR camera, we observed instantaneous sparks in some of the junctions during the switching process from LRS to HRS. This means that the temperature of some junctions in the NWs networks rises instantaneously, which implies that the conductive filament is destroyed due to Joule heating.

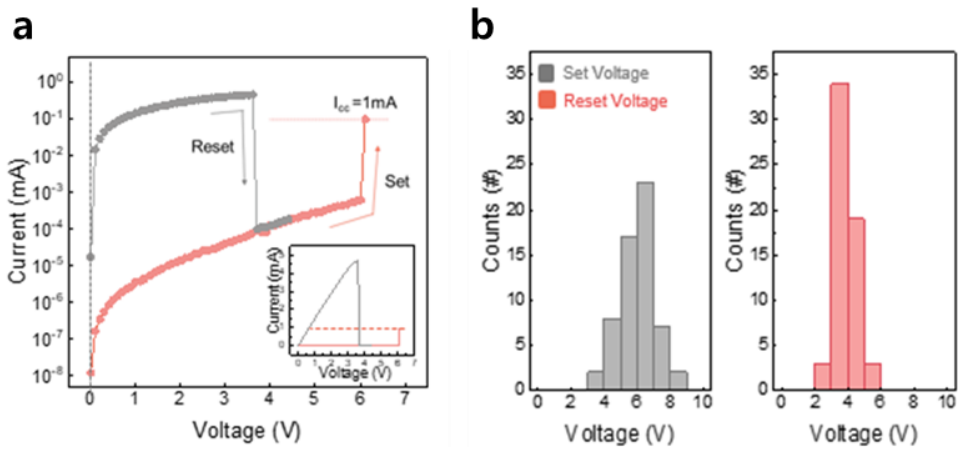

Figure 7. (a) The I-V curve of the memristor and (b) the set/reset voltage of 59 memristor samples.

Figure 7a displays the I-V curve of the memristor. The y-axis is in log scale, and the inset shows the y-axis in linear scale. The “set process” is when the conductive filament forms and the resistance switches from HRS to LRS. We set the compliance current of 0.1mA during the set process, to prevent the rupture of the conductive filament. The switching occurs when ~6V is applied, and this voltage is called the “set voltage”. Oppositely, the “reset process” is when the conductive filament is ruptured and the resistance switches from LRS to HRS. In this case, we did not set the compliance current so that the filament could be

destroyed by Joule heating. This switching occurs when ~4V is applied, and this voltage is called the “reset voltage”.

Because the electric properties of HRS and LRS relies on the resistance of the random network of NWs, it needs to be proved that all the fabricated memristors shows similar set voltage and reset voltage.

To confirm the consistency of the memristor fabrication process, we fabricated 59 samples to investigate the set and reset voltage. Both could be fitted into normal distribution curves with average 3.80V and 6.00V, respectively. Therefore, it can be concluded that the fabricated memristors show reasonable consistency.

3.2. Shell Thickness Optimization

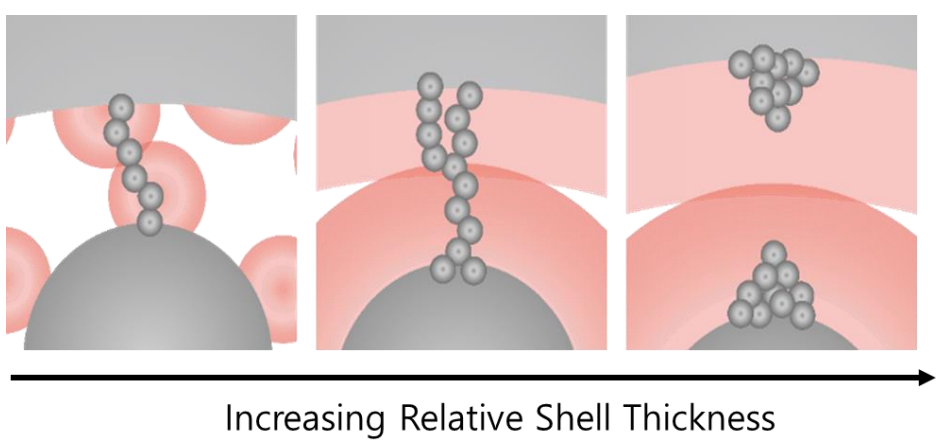

Figure 8. The schematic diagram of the Cu_2O shell as the RST increases.

We discovered that the thickness of the Cu_2O shell is a key factor which determines the performance of the memristor, especially its stability and set/reset voltage. If the shell is too thin, poorly coated defects exist and the Ag core is

exposed. This can result in unstable operation performance of the memristor. On the other hand, if the shell is too thick, it is hard for the oxygen vacancy filament to fully penetrate through the Cu_2O shell. Then, the voltage required for switching between HRS/LRS states gets higher. This implies that the memristor require more energy for operation, which is clearly a disadvantage. Also, because high voltage is applied, the NWs can be damaged even before reaching the targeted voltage. More importantly, if the thickness exceeds a critical point, the memristor does not switch to the LRS, which means that it no longer functions as a memristor. Therefore, finding the appropriate shell thickness that assures high stability and low energy consumption is important.

The thickness of the Cu_2O shell can be controlled in the synthesis step, by adjusting the amount of 0.01M $CuCl_2$ solution. More precisely, the thickness of the Cu_2O shell will depend on the AgNWs to $CuCl_2$ solution volume ratio. For experimental convenience, we fixed the volume of AgNWs and controlled the volume of 0.01M $CuCl_2$ solution for optimization. A total of 6 samples were made for comparison and 0.1mL, 0.3mL, 0.5mL, 1mL, 2mL, and 3mL of $CuCl_2$ solution were used for each sample.

Figure 9 shows SEM images of the Ag@Cu_2O core-shell NWs when the amount of 0.01M $CuCl_2$ solution is 0.1mL, 0.3mL, 0.5mL, 1mL, 2mL, and 3mL. It can be easily observed that the thickness of the NWs increases significantly as the amount of $CuCl_2$ solution increases. The thickness of the $CuCl_2$ can be estimated by subtracting the AgNW core diameter from the total thickness, and dividing the number by 2. The diameter of the AgNW core was approximately 30nm in average.

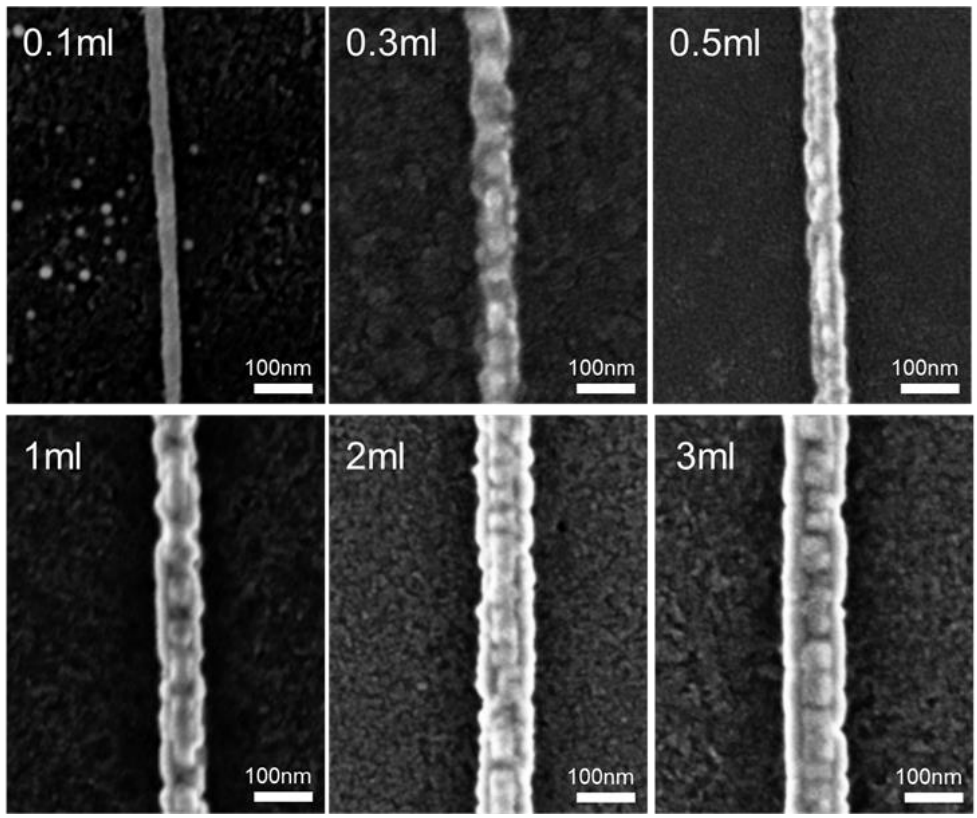

Figure 9. SEM images of the core-shell NWs when the amount of 0.01M $CuCl_2$ solution is 0.1mL, 0.3mL, 0.5mL, 1mL, 2mL, and 3mL. The scale bars are 100nm.

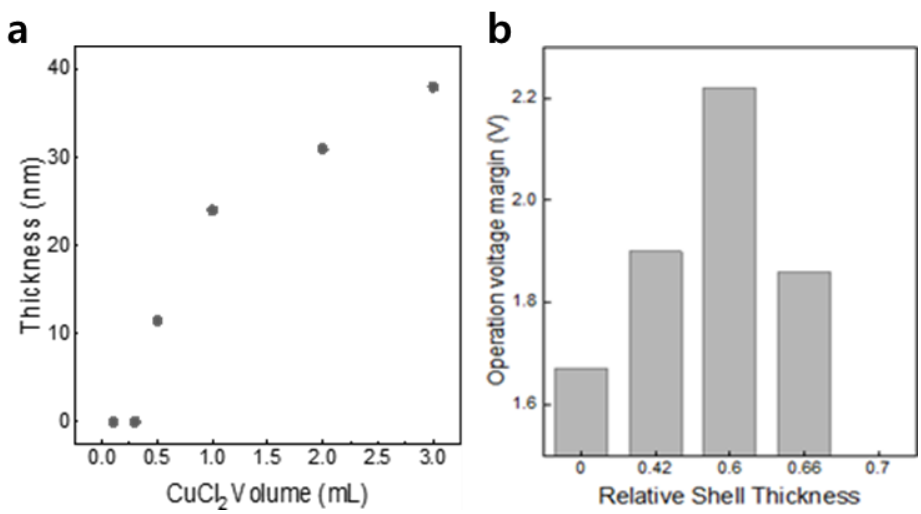

Figure 10. (a) Shell thickness of the NWs versus the volume of $CuCl_2$ and (b) operation voltage margin versus relative shell thickness.

For accurate analysis, the thicknesses of the NWs were measured and showed in **Figure 10 (a)**. For the cases of 0.1mL and 0.3mL of $CuCl_2$ solution, the Cu_2O shells were not uniformly coated onto the Ag cores and clusters were observed. Therefore, their thickness was unable to be measured. For the 0.5mL case, we could determine the average thickness of the shell. Still, poorly coated defects existed. For the cases of 1mL, 2mL, and 3mL, the Cu_2O shells were uniformly coated and no defects were observed. As $CuCl_2$ solution volume increased, the thickness of the shell increased. For the 3mL case, the memristor did not turn to the LRS, not functioning as a memristor. It could be concluded that the cases of 0.5mL, 1mL, and 2mL of $CuCl_2$ solution were suitable for a well-operating memristor.

Operation voltage margin was investigated to examine the manipulability of the memristor. Operation voltage margin is defined as the difference between set and reset voltage. Big operation voltage margin indicates that the set voltage range and reset voltage range is distinctively different, making it easy to switch between LRS and HRS. This is because the voltage range needed for set switching and reset switching can be clearly separated.

Relative shell thickness in **Figure 10** is defined as $RST=(D_w-D_c)/ D_w$, where D_w is the thickness of the entire wire and Dc is the thickness of its core. It is a dimensionless number which stands for the ratio between core-shell NWs' shell and core thicknesses. When the $CuCl_2$ solution volume was 0.1mL, 0.3mL, 0.5mL, 1mL, 2mL, and 3mL, the RST was 0,0, 0.42, 0.6, 0.66, and 0.7, respectively.

The operation voltage margin was biggest at RST of 0.6 (**Figure 10, b**). Accordingly, it was concluded that the optimum volume of $CuCl_2$ solution needed in the synthesis process is 1mL and the optimum RST of the core-shell NWs is 0.6.

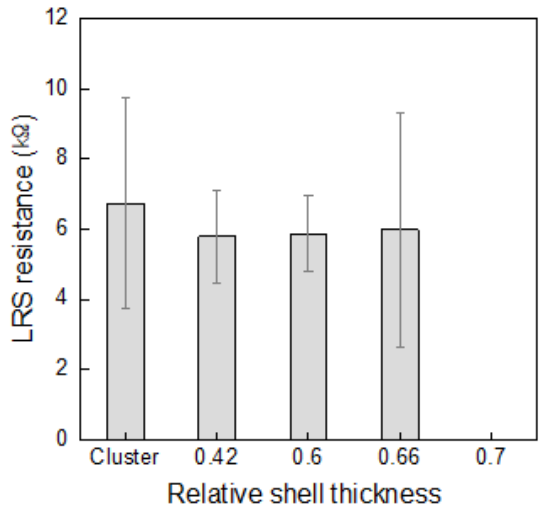

Figure 11. The LRS resistance of the memristor versus the relative shell thickness.

The LRS resistances of the memristors with different RST were investigated. The LRS resistance depends on quantity nanowire junctions that has a fully conductive filament. If there are many junctions with conductive filament, the conductive path crossing through the NWs network with be relatively short, and the LRS resistance will be low. On the other hand, if there are less junctions with conductive filament, the conductive path crossing through the NWs network will be long, resulting in relatively high LRS resistance. In this way, the LRS resistance may depend on the characteristic of the random NWs network. Therefore, it should be assured that the LRS resistance does not fluctuate too much and remains consistent despite the randomness of the network.

The optimal case we chose, which is when the RST is 0.66, shows the highest consistency. The LRS resistance is between approximately 5kΩ and 7kΩ, which may be seen as reasonable consistency.

3.3. Reliability Test

To verify that the fabricated memristor shows high performance with reliable stability, retention test and cycle test were conducted. In addition, since the objective of this study is to make a stretchable memristor, it was proved that the memristor operates in high strain conditions.

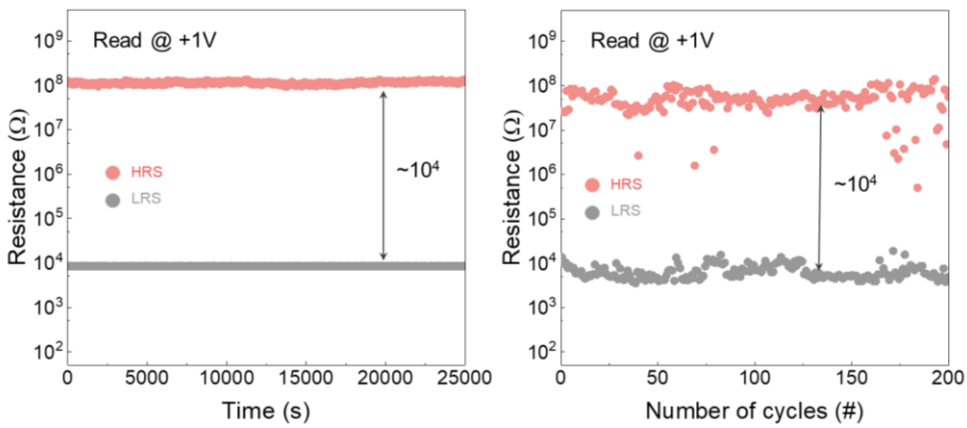

Figure 12. (a) Retention test and (b) set/reset cycling test of the memristor.

One of the important indexes that shows the stability of the memristor is the retention time. The retention time indicates how long the memristor can remain its HRS and LRS resistance without significant change. Generally, the HRS resistance decreases and LRS resistance increases as time passes. Therefore, it is necessary to investigate the time which the difference between the HRS resistance and LRS resistance remains constant. Retention test with a reading bias of V_r = +1.0V was conducted. The resistance has been recorded every 1s for both HRS and LRS. **Figure 12a** shows that HRS resistance of ~100MΩ and LRS resistance of ~7kΩ were maintained for 25000s, which is about 7 hours. The HRS/LRS resistance ratio

remained bigger than 10^4 for the entire experiment time. A previous study by Kim et al(12) demonstrated TiOx-based memristors with 10000s retention time and 10^3 HRS/LRS resistance ratio. Xin et al(13) demonstrated a ITO/PFP/AI memristor with 11000s retention time and 10^2 HRS/LRS resistance ratio. Compared to previous studies, our memristor showed long retention time and big HRS/LRS resistance ratio.

Another index that shows the stability of the memristor is the set/reset cycling test. A set/reset cycling test of the memristor with a reading bias of V_r = +1.0V was conducted over 200 cycles. LRS resistance and HRS resistance was measured in 1.0V reading voltage bias alternatively as the memristor was continuously switched. The reset voltage slightly decreased as the number of cycles increased, while the set voltage showed no significant change. The HRS/LRS resistance ratio also remained bigger than 10^4 over the entire cycles. Wang et al(14) demonstrated an Au/Ti/MoS2/Ti/Au memristor with 160 switching cycles and $10\sim10^4$ HRS/LRS ratio. Qian et al(15) reported an Ag/*h*-BN/Cu memristor with 550 switching cycles and 10^2 HRS/LRS resistance ratio. Compared to previous studies, our memristor endures reasonably many switching cycles.

The retention test and set/ret cycling tests shows that the fabricated memristor is suitable for usage. It operated normally through 25000s retention time and 200 switching cycles, which implies the memristor is stable compared to previously reported memristors.

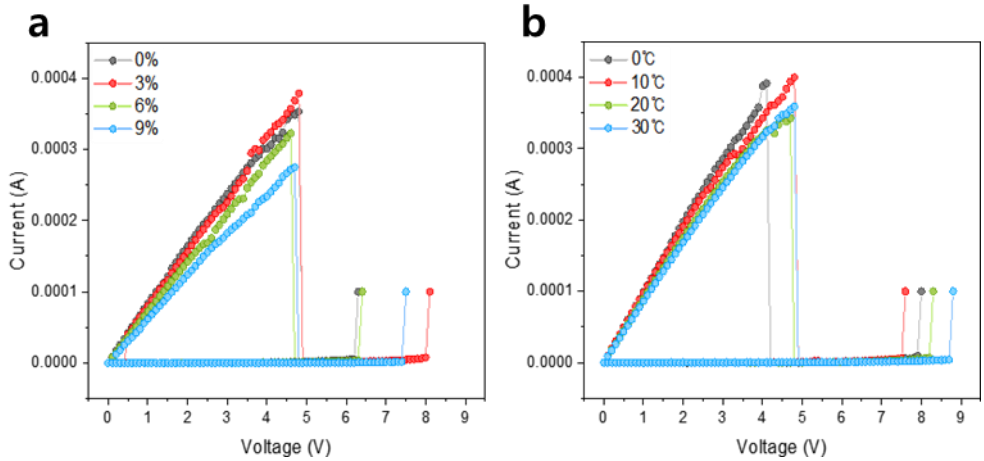

Figure 13. IV-curves in various (a) strain conditions and (b) temperature conditions.

Our memristor normally operated in both harsh strain and temperature conditions. 0%, 3%, 6%, 9% strain were applied in the parallel direction with the electrodes. The LRS resistance increased as strain increased. However, no tendency was observed between the set/reset voltage versus strain. Overall, the I-V curves in all strain conditions were distributed with minor fluctuations (**Figure 13, a**).

0℃, 10℃, 20℃, 30℃ additional heating were applied to the memristor in room temperature (25℃). Heating was applied by a Peltier effect module, and the temperature was controlled by changing the current that flows through the module. For accurate temperature control, temperature was continuously measured through an IR camera. The LRS resistance increased merely as temperature increased. Nevertheless, like the strain variation experiment, no tendency was observed between the set and reset voltage versus temperature. It can be concluded that the I-V curves in all temperature conditions were distributed within similar range (**Figure 13, b**).

The results of these two experiments show that the memristor does not break

down, and maintains proper operation in various strain and temperature conditions. Furthermore, the result of the strain variation test verifies that the memristor is stretchable. LRS resistance tendency, which increases as strain and temperature increase, shows further application possibility of this Ag@Cu_2O core-shell network to be used as strain and temperature sensors.

Chapter 4. Simulation

4.1. Single Junction Conductivity Modelling

Even though a single junction formed by two nanowires shows memristive characteristics, it does not assure that a nanowire "network" operates as a memristor. Therefore, we conducted a simulation to support the theoretical background of our study. This method also attributed to the visualization of the resistance transition process of the core-shell NWs.

The simulation algorithm used in this study is a modified version of the algorithm introduced in Manning et al(16), Hochstetter et al(17) and Panda et al(18). The simulation algorithm in Manning et al modeled nanowire networks that are plain nanowires, not core-shell nanowires. We modified it to be applied for core-shell nanowires.

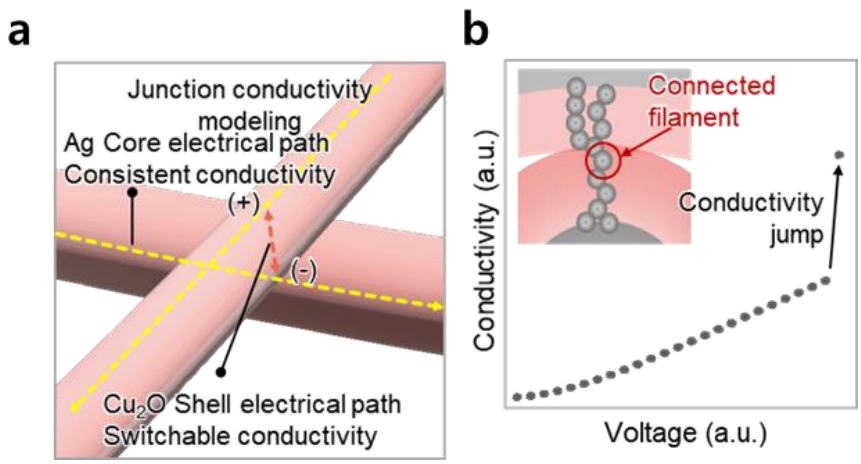

Figure 14. (a) Single junction conductivity modelling and (b) simulation result.

A single junction formed by two different nanowires was modeled (**Figure 14, a**). To differentiate the electrical properties of the Ag core and Cu_2O, we modeled them as a resistance with different electrical properties. The Ag core electrical path was assumed as a resistance with consistent conductivity. On the other hand, the Cu_2O shell electrical path was assumed as a resistance with variable conductivity that switches between a low resistance value and a high resistance value. This is because the resistance of the Cu_2O shell changes as the conductive filament forms and disappears. The conductivity of this variable junction resistance was modelled to follow the equation $d\Gamma/dI=\alpha I\beta$, where Γ is conductivity of each junction, I is the current passing through the junction, and α, β are random variables. We adjusted the random variables α and β to match the experimental results.

However, this exponential form of equation is incomplete, since it cannot explain the "conductivity jump" that occurs at the instance when the filament is fully connected. In reality, the conductivity of the shell does not increase exponentially as the filament grows. Instead, it is clear that there will be a conductivity jump at the instant when the final part of the filament is formed and the Ag cores are fully connected with a conductive filament. Therefore, to complement the weakness of the governing equation, we added an algorithm that embodies the conductivity jump. From previous experiments, we observed that most of the samples go through a conductivity jump when they reach a critical conductivity point. To match with the experimental results, we set the conductivity jump to occur when the conductivity gets 60 times bigger than the initial conductivity. The simulation result of the single junction conductivity, reflecting both the governing equation and conductivity jump algorithm, is shown in **Figure 14b**.

4.2. Network Conductivity Modelling

Then, the simulation was extended to a network model. Nanowires (lines) with random lengths were distributed in the given space. Then, a “adjacent matrix” that displays whether the nanowires are connected or not was defined. If nanowires were connected and formed a junction, variable junction resistances were added. After modelling the NWs network with the governing equation and the conductivity jump algorithm, we implicitly calculated the current flow and conductance at each junction. Then, the resultant conductance of the whole network was calculated. The implicit computational model is based on the Kirchhoff's Current Law (KCL). First, initial conductance of the nanowires and junctions was set. Second, an initial current I_0 was loaded on each side of the electrodes. After setting the conductance and current, new conductance values were calculated by applying the KCL on each junction. The current on the electrodes was incremented and the conductance was repeatedly calculated until the total voltage difference between two electrodes matched the desired output voltage (**Figure 15, a**).

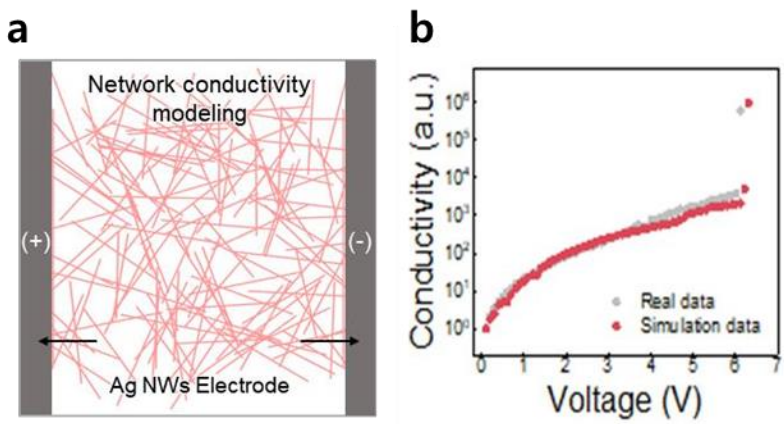

Figure 15. (a) Network conductivity modeling and (b) simulation result.

Figure 15b shows the computational results. After adjusting the random variables α and β, the simulation results closely approached the real data obtained from previous experiments. Therefore, in this part, we proved by a computational method that not only single nanowire junctions, but also random nanowire networks show memristive characteristics.

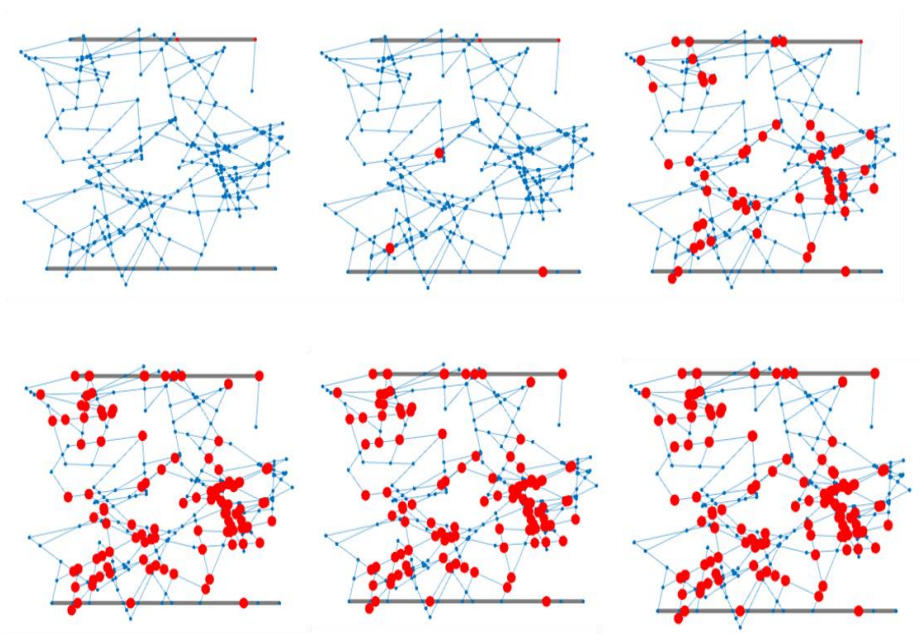

Figure 16. Formation of conductive filaments on nanowire junctions as voltage is incrementally applied between the electrodes.

Additionally, we conducted a simulation to visually show the formation of conductive filaments on nanowire junctions as voltage is incrementally applied between the two electrodes on each side (**Figure 16**). The location of the junctions where conductive filaments formed appeared to be random, as expected. When conductive filaments were plenty enough to form a complete path between the electrodes, the whole network was switched on to the LRS.

Chapter 5. Conclusion

In this paper, Ag@Cu_2O core-shell nanowire networks are transferred on stretchable PDMS substrate to fabricate a nonvolatile memristor that can be used for neuromorphic engineering. Compared to previous studies that modified structural designs to achieve high stretchability, nanowire networks were used to obtain stretchability in material level. To achieve the goal of this study, first, we modified the synthesis process of the core-shell NWs based on previous studies. As a result, we could significantly reduce the synthesis time to approximately 15 minutes. The synthesis result was confirmed through EDS and XRD results. Second, we achieved stable operation of the memristor through optimization of the Cu_2O shell thickness. The optimum RST value was 0.6, which is when 1ml of 0.01M $CuCl_2$ is added in the synthesis process. Third, we verified the reliability of the manufacture memristor. The memristor maintained switching ratio over 10^4 for 25000s time and 200 switching cycles. Moreover, it could endure mechanical damages up to 9% strain and 30℃ additional heating in room temperature condition. This Ag@Cu_2O core-shell nanowire networks based stretchable memristor is expected to dedicate to the development of neuromorphic devices that are highly similar to neurons of human beings, by improving mechanical durability and allowing applications in curved surfaces.

References

1. John R, Yantara N, Ng S, Patdillah MB, Kulkarni M, Jamaludin N. Ankit, SG Mhaisalkar, A. Basu, and N. Mathews. Adv Mater. 2021;33:2007851.

2. Lin P, Li C, Wang Z, Li Y, Jiang H, Song W, et al. Three-dimensional memristor circuits as complex neural networks. Nature Electronics. 2020;3(4):225-32.

3. Pei Y, Yan L, Wu Z, Lu J, Zhao J, Chen J, et al. Artificial visual perception nervous system based on low-dimensional material photoelectric memristors. ACS nano. 2021;15(11):17319-26.

4. Wang S, Song L, Chen W, Wang G, Hao E, Li C, et al. Memristor-Based Intelligent Human-Like Neural Computing. Advanced Electronic Materials. 2022:2200877.

5. Mohammad B, Abi Jaoude M, Kumar V, Al Homouz DM, Nahla HA, Al-Qutayri M, et al. State of the art of metal oxide memristor devices. Nanotechnology Reviews. 2016;5(3):311-29.

6. Yang M, Zhao X, Tang Q, Cui N, Wang Z, Tong Y, et al. Stretchable and conformable synapse memristors for wearable and implantable electronics. Nanoscale. 2018;10(38):18135-44.

7. Wang T, Cui Z, Liu Y, Lu D, Wang M, Wan C, et al. Mechanically durable memristor arrays based on a discrete structure design. Advanced Materials. 2022;34(4):2106212.

8. Zhu S, Deng D, Nguyen MT, Chau Y-tR, Wen C-Y, Yonezawa T. Synthesis of Au@ Cu2O core–shell nanoparticles with tunable shell thickness and their degradation mechanism in aqueous solutions. Langmuir. 2020;36(13):3386-92.

9. Yuan G, Lu M, Fei J, Guo J, Wang Z. Morphologically controllable synthesis of core–shell structured Au@ Cu 2 O with enhanced photocatalytic activity. RSC advances. 2015;5(88):71559-64.

10. Strachan JP, Strukov DB, Borghetti J, Yang JJ, Medeiros-Ribeiro G, Williams RS. The switching location of a bipolar memristor: chemical, thermal and structural mapping. Nanotechnology. 2011;22(25):254015.

11. Kim S, Jung S, Kim MH, Chen YC, Chang YF, Ryoo KC, et al. Scaling effect on silicon nitride memristor with highly doped Si substrate. Small. 2018;14(19):1704062.

12. Kim M, Yoo K, Jeon S-P, Park SK, Kim Y-H. The effect of multi-layer

stacking sequence of TiOx active layers on the resistive-switching characteristics of memristor devices. Micromachines. 2020;11(2):154.

13. Xin Y, Zhao X, Jiang X, Yang Q, Huang J, Wang S, et al. Bistable electrical switching and nonvolatile memory effects by doping different amounts of GO in poly (9, 9-dioctylfluorene-2, 7-diyl). RSC advances. 2018;8(13):6878-86.

14. Wang L, Liao W, Wong SL, Yu ZG, Li S, Lim YF, et al. Artificial synapses based on multiterminal memtransistors for neuromorphic application. Advanced Functional Materials. 2019;29(25):1901106.

15. Qian K, Tay RY, Nguyen VC, Wang J, Cai G, Chen T, et al. Hexagonal boron nitride thin film for flexible resistive memory applications. Advanced Functional Materials. 2016;26(13):2176-84.

16. Manning HG, Niosi F, da Rocha CG, Bellew AT, O'Callaghan C, Biswas S, et al. Emergence of winner-takes-all connectivity paths in random nanowire networks. Nature communications. 2018;9(1):1-9.

17. Hochstetter J, Zhu R, Loeffler A, Diaz-Alvarez A, Nakayama T, Kuncic Z. Avalanches and edge-of-chaos learning in neuromorphic nanowire networks. Nature Communications. 2021;12(1):1-13.

18. Panda D, Sahu PP, Tseng TY. A collective study on modeling and simulation of resistive random access memory. Nanoscale research letters. 2018;13(1):1-48.

국문 초록

은-산화구리 코어-쉘 나노 와이어 네트워크에 기반한 유연·신축성 멤리스터 소자의 제작

김문주
기계공학부
서울대학교 대학원

신축성 멤리스터는 뉴로모픽 공학을 웨어러블 전자기기와 소프트 로보틱스에 접목시킬 수 있도록 하는 유망한 전기 소자이다. 본 연구에서는 나노 와이어 네트워크에 기반한 유연하고 신축성 있는 멤리스터를 개발하였다. 멤리스터의 주요 재료인 은-산화구리 코어-쉘 나노 와이어는 선행 연구의 합성 기법을 변형 및 발전시켜 합성하였다. 멤리스터의 높은 안정성과 낮은 에너지 소비량을 달성하기 위해서는 코어-쉘 나노 와이어의 상대적인 쉘 두께(RST)를 최적화해야 하는데, 이는 합성 과정에서 성공적으로 제어되었다. 최적화 과정을 거쳐 제작된 멤리스터는 10^4 이상의 높은 HRS/LRS 저항 비율을 보이며, HRS 저항은 ~100MΩ, LRS 저항은 ~7kΩ이었다. 25000s의 시간동안 안정적으로 작동하였으며, 큰 저항 변화 없이 200회 이상의 스위칭 사이클을 거쳤다. 또한, 최대 9%의 변형과 30℃의 가열이 가해진 기계적 환경에서도 잘 작동하였다. 이러한 실험 결과와 이론적 모델링은 시뮬레이션 결과를 통해 검증하였다.

주요어 : 신축성 멤리스터, 은-산화구리 코어-쉘 나노 와이어, 나노 와이어 네트워크, 뉴로모픽 공학
학 번 : 2020-24015