Ph.D. DISSERTATION

# Development of 3D vertical structure ReRAM device for various applications

by

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DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING

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# Development of 3D vertical structure ReRAM device for various applications

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# 1.1. Abstract

Due to the Fourth Industrial Revolution, enormous data based on information and communication technology (ICT) is being created. It is expected that 175 zettabytes of data will be generated by 2025. NAND flash memory is mainly responsible for storing enormous amounts of data, and the current mass-produced product is 176-layer three-dimensional vertical NAND (V-NAND). However, the allowable thickness of the packaged chip is 30 μm. Excluding the packaging thickness of 15 μm, V-NAND is expected to be up to 400 layers. According to V-NAND's technology roadmap, 400 layers will be developed in 2026, and there will be difficulties in improving the density. To replace V-NAND, research on next-generation memory is being conducted. In this dissertation, ReRAM, which uses resistance change characteristics, will be described.

The memristor concept was introduced in 1971, and since Hewlett-Packard (HP) started developing it in 2008, many studies have been continuously conducted. In the early days, research on the use of memory devices was mainly conducted. Recently, research has been conducted in various fields such as neuromorphic computing, biocompatible memory devices, and wearable devices. Since the resistance change memory operates in a simple structure of metal/insulating film/metal, it is possible to manufacture a crossbar type $4F^2$ array structure. Here, F represents the feasible minimum line width. DRAM, NAND, and NOR flash memory have unit cell sizes of $6F^2$, $5F^2$, and $10F^2$, respectively, so ReRAM is advantageous in terms of integration. In addition, if the resistance change element is manufactured in a three-dimensional vertical structure (V-ReRAM), it exists compatibility with the V-NAND process. Since it operates at a voltage lower than the V-NAND operating voltage of 20V, the interference effect can be reduced. It has the advantage of being able to manufacture products with a greater number of layers in the vertical direction. The channel hole of the V-NAND must be larger than a certain level to contact the Si substrate region. Since V-ReRAM only needs to have a voltage difference

between a word line and a bit line, the size of the channel hole can be reduced compared to V-NAND, which helps to improve horizontal integration.

The sneak current flowing through the adjacent cell must be suppressed to fabricate the resistive device into an array. It can be suppressed by using a selector or the self-rectifying feature. To use the selector, a middle electrode is required between the resistive layer and the selector, but in V-ReRAM, since the middle electrode is shared by all cells, sneak current suppression using the selector is impossible. Therefore, it is necessary to fabricate a V-ReRAM by utilizing a resistance switching layer having self-rectification characteristics. In this dissertation, 1) selecting a resistive layer with self-rectifying properties to be applied to V-ReRAM, 2) fabrication and application of V-ReRAM cell array, and 3) charge loss effects in V-ReRAM are explained.

A crosspoint device is fabricated to select a resistance switching layer with self-rectification characteristics. A representative self-rectifying thin film is $HfO_2$, which has an electrical switching mechanism by trapping and detrapping electrons into oxygen vacancy. The electrons flowing into the resistance switching layer start to fill the trap site, and when all the trap sites are filled, it changes to the low resistance state (LRS), called the SET process. Under the reverse-biased voltage condition, the trapped electrons are detrapped, but the inflow of electrons is blocked by the high work function of the top electrode, returning to the high resistance state (HRS), which is called the Reset process. Accordingly, it might have a self-rectifying characteristic. However, since the device's set voltage is +8V, and the reset voltage is as high as -8V, oxygen vacancies with a negative charge are moved by the electric field. The oxygen vacancies are rearranged, and the current path is also changed in all operations, causing distribution. To improve the variation, Al is doped into the $HfO_2$ thin film, and the traps formed around Al exhibited a deeper trap depth, and the doped Al also suppresses the movement of oxygen vacancies. The distribution of HRS is improved by 85% by the deeper trap, whose migration was inhibited. In addition, the read voltage margin (Vread margin) of the $HfO_2$-based

resistance change device is 1.5 V level, so a wider margin is needed considering the device variation. The read margin can be improved by adding a $Ta_2O_5$ thin film to relieve the electric field applied to $HfO_2$ and shifting HRS. Therefore, a double layer of Al-doped $HfO_2$ and $Ta_2O_5$ was selected as a thin film to be applied to V-ReRAM.

The fabricated V-ReRAM consists of two layers of the word line and is manufactured in the same hole type as V-NAND. The diameter of the hole is 1 μm, the TiN used for the word line is 40 nm thick, and the operating area is 0.1256 $\mu m^2$. By applying the self-rectifying thin film selected to the V-ReRAM, similar DC I-V characteristics are obtained with crossbar structure. The word line thickness is deposited to 3 nm, and the diameter of the hole is minimized to 500 nm to confirm the minimum operable area in the V-ReRAM. The resistive switching operation is confirmed with an operating area of 0.0047 μm2, which is smaller than the operating area of V-NAND (0.0071 μm2). In the worst-case scenario, where only the selected cell from 32 cells of the 4x4 two-layer array is placed in the HRS, and all the remaining cells (31 cells) are in the LRS, it can read the HRS state of the selected cell without interruption of the sneak current. The array is further expanded to fabricate a 9x9 two-layer device, and every cell shows regular resistive switching operation proved by measuring the DC I-V characteristic. A V-ReRAM array with a 9x9 two-layer is applied to a binary neural network (BNN) application. After training the BNN that classifies 30 images with 3x3 pixels belonging to ‘L’, ‘I’, and ‘X’, we perform off-chip training to transfer it to the V-ReRAM array. The result was an average of 98.23% accuracy, which will be improved with a larger array.

V-ReRAM has a structure in which all cells share the resistive switching layer in the vertical direction, like the charge trap layer of V-NAND. Therefore, the data distortion caused by charge loss, which is similar to V-NAND, also appears in V-ReRAM. A V-ReRAM device with a three-layer structure is fabricated to confirm this phenomenon. With the interference effect, trapped electrons in the LRS move to the neighboring cells in the HRS by diffusion. It

leads to shifting the neighboring cells in the HRS to the LRS direction. As a result, the cell in the HRS changes to an intermediate state between HRS and LRS. In addition, if the first and third layers of the three-layer device are switched into the LRS, the interference effect of the middle layer is further increased. Such interference may deteriorate the retention characteristics of the memory. To improve the interference phenomenon, we are evaluating a structure that increases the electron movement distance by recessing the insulating film between the word line layers, and a structure in which a resistive switching layer is deposited after recessing the TiN electrode and isolating through etching. Also, it is necessary to study the resistive switching layer with excellent characteristics in charge loss.

In this dissertation, we confirm the possibility of using a V-ReRAM device with a 9x9 two-layer array structure as a memory and operating in a smaller operation area than V-NAND.

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**Keywords**: resistive switching memory, vertical structure, memristor, self-rectifying, uniformity, $HfO_2$, $Ta_2O_5$

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# 1.2. Table of Contents

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## 1.3. List of Tables

# 1.4. List of Figures

# 1. List of Abbreviations

| | |
|---|---|
| AES | Auger Electron Spectroscopy |
| AHO | Al:$HfO_2$ |
| AHT | Al:$HfO_2$/$Ta_2O_5$ |
| ALD | Atomic Layer deposition |
| BE | Bottom Electrode |
| BNN | Binary Neural Network |
| BRS | Bipolar Resistive Switching |
| CBA | Cross Bar Array |
| DC | Direct Current |
| DRAM | Dynamic Random Access Memory |
| ECM | Electrochemical metallization |
| FESEM | Field Emission Scanning Electron microscopy |
| HNN | Hardware Neural Network |
| HO | $HfO_2$ |
| HRS | High Resistance State |
| HRTEM | High Resolution Transmission Electron Microscopy |
| $I_{cc}$ | Compliance Current |
| I-V | Current-Voltage |
| LRS | Low Resistance State |

| | |
|---|---|
| MIM | Metal-Insulator-Metal |
| PCRAM | Phase Change Random Access Memory |
| PR | Photoresist |
| ReRAM | Resistive switching Random Access Memory |
| RS | Resistive Switching |
| SEM | Scanning Electron Microscopy |
| TCM | Thermal Change Mechanism |
| TE | Top Electrode |
| TEM | Transmission Electron Microscopy |
| VCM | Valence Change Mechanism |
| V-NAND | Vertical NAND |
| V-ReRAM | Vertical Resistive switching Random Access Memory |

# 1. Introduction

## 1.1. Resistive switching Random Access Memory

Resistive switching random access memory (ReRAM) is one of the most promising next-generation non-volatile memories and has been actively researched for decades. ReRAM operates by changing the resistance into a high resistance state (HRS) and low resistance state (LRS) and has a simple structure of metal-insulator-metal (MIM). Figure 1.1 shows many mechanisms for resistive switching (RS), which are categorized to phase change mechanism (PCM), the thermo-chemical mechanism (TCM), valence change mechanism (VCM), electrochemical metallization (ECM), and electronic mechanism.[1] Among them, recently, there have been many reports of VCM and ECM that form ionic-based filaments in the resistive switching layer.[2] However, filament-based devices require electrical forming to form filaments and selector devices to suppress sneak current for cell array. For electrical forming, a higher bias must be applied to the resistive switching layer, which can cause device reliability problems. An additional area is required to fabricate the selector devices, which is disadvantageous in terms of integration. Electronic switching mechanisms change the resistance by trapping/detraping electrons and thus have forming-free and self-rectifying characteristics.[3] It has the advantages of improving reliability and increasing density.

ReRAM can be fabricated in a stacked structure such as vertical NAND (V-NAND), which is the mainstream of the NAND flash memory market and has significant advantages compared to V-NAND. First, V-NAND uses a polycrystalline-Si (poly-Si) channel with very low electron mobility of ~0.1 $cm^2/Vs$, but V-ReRAM operates faster than V-NAND because it can use metal bit lines. In V-NAND, the cell is complexly composed of the metal gate (or control gate)/block oxide/trap nitride (or floating gate)/tunneling oxide/channel poly-Si, whereas V-ReRAM is composed of metal-insulator-metal. Third, regarding integration, the unit cell of V-ReRAM can be manufactured in $4F^2$, but V-NAND has a unit cell area of $5F^2$, where F represents the minimum feature size.[4] Finally, since V-ReRAM has a lower operating voltage than V-NAND, the interference effect with neighboring cells can be reduced.

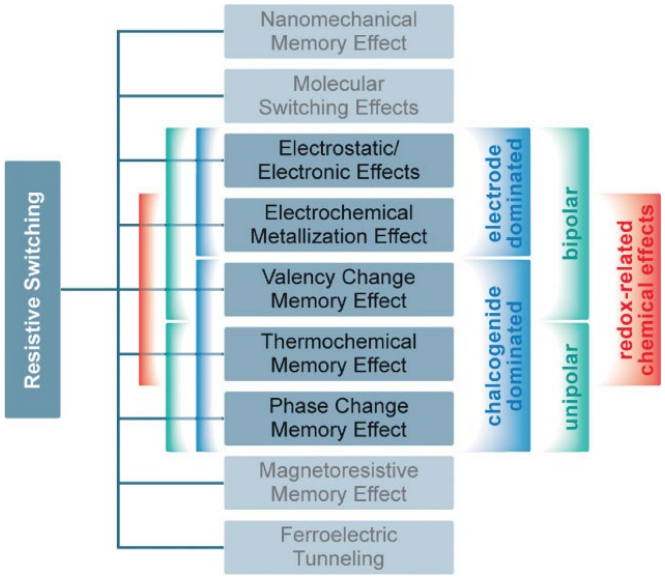


Figure 1.1 Classification of the resistive switching mechanism. Adapted from [1].

## 1.2. Key factors for a vertical ReRAM array

Although ReRAM has been actively studied for the past decade, some critical issues in fabricating a high-density array include line resistance, sneak current, overset, etc. Among them, it is most important to suppress the sneak current to accurately read the written data. As shown in Figure 1.2, when attempting to read (write) a selected cell (cell 1), an unwanted current path through the unselected cells (cell 2/3/4) is formed and interferes with the reading (writing) operation.[5] An additional selector device is required to suppress the sneak current, but the select element cannot be applied to V-ReRAM, which shares a resistive switching layer in the vertical direction.[6] Therefore, V-ReRAM requires the resistive switching layer with self-rectification characteristics actuated by trapping and detrapping of the electron. In addition, the atomic layer deposition (ALD) process is essential to ensure that the resistive switching layer and the bit line metal can be uniformly deposited on the vertical structure.

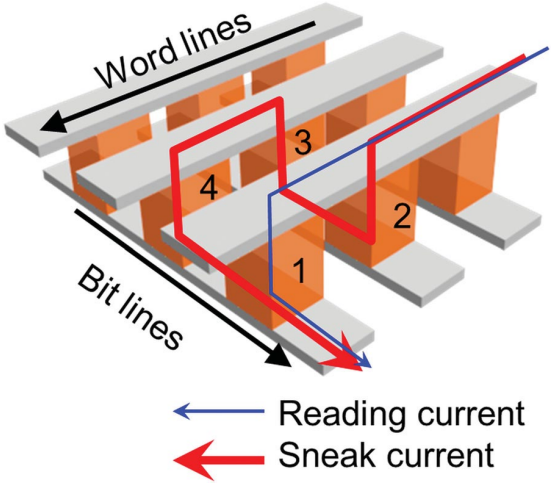


Figure 1.2 Schematic diagram of sneak current problem in CBA structure. Adopted from [5].

## 1.3. Research scope and objective

The most important thing in V-ReRAM array operation is uniform on/off characteristics with self-rectification characteristics and a sufficiently large memory window. After selecting the optimal resistive switching layer, the V-ReRAM array can be applied to various applications. Moreover, since the insulating film between word lines is very thin (< 50 nm), it is necessary to consider the problem of interference with adjacent cells.

In Chapter 2, to select the optimal resistive switching layer, the electrical characteristics of the HfO2-based RS layer in the crosspoint structure are compared. The effect of Al doping on $HfO_2$ is introduced, and the effect is verified through simulation. Furthermore, the electrical properties of the bilayer with $Ta_2O_5$ are explained.

In Chapter 3, the fabrication process of the V-ReRAM array with a 9x9 two-layer is described, and the electrical characteristics are compared with the crosspoint results. Self-rectification characteristics for sneak current suppression in a 4x4 two-layer array are examined in a worst-case scenario. A BNN application using the fabricated V-ReRAM is introduced.

In Chapter 4, the charge loss of V-NAND flash memory is explained, and the interference effect in V-ReRAM having the same structure as V-NAND is introduced. Finally, a structure for reducing the interference effect is suggested.

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# 2. Decision of resistive-switching layer for 3D vertical ReRAM

## 2.1. Introduction

As ultra-high-density 3D vertical-NAND (V-NAND) dominates the market, next-generation memory-based high-density storage memory has been studied with the goal of substituting the V-NAND, and this is also the case with resistive switching memory (ReRAM). ReRAM has strong advantages in scalability, fast switching speed, and nonvolatility. For fabricating a three-dimensional structure with a ReRAM, there are two ways for stacking in general: a horizontal structure, which is a method of stacking word line (WL) and a bit line (BL), and a vertical structure, which is a method of stacking WL and BL with a hole structure.[1] The horizontal structure requires a photo/etch process for every layer, which increases cost and manufacturing steps. An extra area is required for each layer's pad contact between WL and BL. In addition, the horizontal structure requires advanced lithography technology to shrink the WL and BL for high-density integration. On the other hand, the vertical structure can only secure the density by increasing the number of stacks, and the current photo process is a 40 nm-level process.[2] Also, the WL is made in the form of a stair, but BL is shared so that BL contacts do not increase regardless of the number of layers in the vertical structure. Therefore, adopting the vertical hole structure is advantageous and efficient in terms of ease of density increase, simplicity of process, and cost to make ReRAM with a 3D structure called vertical ReRAM (V-ReRAM).

To realize high-density memristor arrays, however, the problem of sneak current for accurate write/read operations must be alleviated. In a horizontal structure array, a method of connecting resistors and rectifiers in series is generally adopted, such as 1-selector-1-resistor (1S1R) and 1-transistor-1-resistor (1T1R), which requires middle electrodes for the bias application.[3] In the V-ReRAM array, when a middle electrode is inserted, each memristor is not isolated but shorted due to a structural limitation. Since the RS layer is connected in the vertical direction, the middle electrode between the selector and the RS layer cannot be separated for each cell. For this reason, self-rectifying characteristics are essential for memristors to be applied to V-ReRAM to avoid sneak current issues. In particular, the most representative advantages of the electronic switching based self-rectifying memory compared to filamentary ReRAM are 1) sneak current can be suppressed without a selector, 2) the fabrication process is simplified so that the device characteristics and uniformity can be improved, 3) low-power (extremely low current) operation is capable. Other than that, electroforming-free switching and the capability of the multilevel resistance states are also considered advantages.[4]

Herein, a hole-etched V-ReRAM array using self-rectifying memory operating based on electronic switching was made, and its electrical properties were evaluated. To optimize the performance of the V-ReRAM, first, the electrical properties of the several switching layers were compared. We made the trap depth deeper by Al doping to $HfO_2$ to improve the switching uniformity and the rectification capability of the self-rectifying memory. Studies have reported improved electrical characteristics of high-k dielectric film for DRAM or the ferroelectric device by introducing Al doping

into $HfO_2$ with the deeper trap.[5, 6] And several studies are reporting the performance enhancement in the valence change mechanism (VCM) or filamentary switching based ReRAM led by the doped Al to $HfO_2$.[7, 8] However, the enhancement of the switching characteristics in trap/detrap-based ReRAM by doped Al-induced deeper trap depth has been hardly reported. A method for improving device reliability based on trap depth engineering in eBRS ReRAM is proposed in this work. In addition, a $Ta_2O_5$ was applied as a blocking layer in anticipation of increasing the on/off ratio and improving the rectification function. For a comparison, Pt/$HfO_2$/TiN, Pt/Al: $HfO_2$/TiN, and Pt/$Ta_2O_5$/Al: $HfO_2$/TiN devices were fabricated. The electrical characteristics and the materialistic properties of the devices were evaluated, and based on the measurement results, Pt/$Ta_2O_5$/Al: $HfO_2$/TiN stack was selected due to its excellent properties.

## 2.2. Experimental

The electrical characteristics were evaluated first on the crosspoint device to select the resistive switching layer and optimize the V-ReRAM's stack. Pt/$HfO_2$/TiN crosspoint device (HO device), Pt/Al: $HfO_2$/TiN crosspoint device (AHO device), and Pt/$Ta_2O_5$/Al: $HfO_2$/TiN crosspoint device (AHT device) were made to evaluate the effects of Al doping and inserted $Ta_2O_5$ layer. TiN 50 nm was sputtered on $SiO_2$/Si substrate through reactive sputtering (ENDURA, ENDURA 5500) as the bottom electrode (BE). The maskless lithography (Nano System Solutions. Inc, DL-1000 HP) was exploited to define the photoresist (PR) patterns used as an etching mask. The TiN film was etched through the ICP etcher (Oxford instruments, PlasmaPro System100 Cobra), and the etch byproduct was removed by PR asher (Plasma finish, V15-G). On top of the TiN BE patterns, the switching layer and blocking layer were deposited appropriately for the HO device, the AHO device, and the AHT device, respectively. A-10-nm-thick $HfO_2$ and a-10-nm-thick-Al: $HfO_2$ were deposited through the thermal atomic layer deposition (ALD, CN1, custom-made ALD cluster system) using tetrakis(dimethylamido)hafnium (TDMAHf, $Hf(N(CH_3)_2)_4$) as a precursor and ozone ($O_3$) as an oxidant. Aluminum was doped in-situ while depositing $HfO_2$ with a precursor trimethylaluminum (TMA, $C_3H_9Al$) for Al: $HfO_2$ deposition, and the Al to Hf ratio was 1:9. A-5-nm-thick $Ta_2O_5$ was deposited using the plasma-enhanced atomic layer deposition (PEALD, CN1, Atomic Premium plus 200) with a precursor tris(diethylamido)(tert-butylimido)tantalum(V) ($(CH_3)_3CNTa(N(C_2H_5)_2)_3$). $H_2O$-activated plasma was used as an oxidant. Top

electrode (TE) patterns were formed through the lift-off process, and Pt 50 nm was deposited using an e-gun evaporator (SORONA, SRN-200i). The fabrication process of the crosspoint device is included in Figure 2.1.

## 2.3. Results and Discussions

The electrical and materialistic characteristics were analyzed to select the RS layer to be applied to optimize the V-ReRAM fabrication. The measurement was conducted on the crosspoint devices first to evaluate the effect of Al doping, excluding the influence originating from the devices' structure. The HO device, AHO device, and AHT device were fabricated as depicted in the experimental section and Figure 2.1. Representative I-V curves measured on the HO device, the AHO device, and the AHT device are shown in Figure 2.2 (a)-(c), respectively. Forward-to-reverse current ratio (F/R ratio, $\frac{I_{LRS,forward}}{I_{LRS,reverse}}$) and the on-to-off current ratio (on/off ratio, $\frac{I_{LRS,forward}}{I_{HRS,forward}}$) depending on the read voltage are presented as insets. It can be found that the uniformity of the HRS current was improved in the AHO device and the AHT device through I-V curves. The switching window was hardly attained over the cycles in the HO device with compliance current ($I_{cc}$) 10 nA. However, a wider and clearer switching window was obtained in the AHO device; it was even improved in the AHT device. The on/off ratio and the F/R ratio were the highest in the AHT device among the candidates, as found in the insets. It is thought to be due to the enhanced rectifying capability led by the insertion of $Ta_2O_5$, a blocking layer, as Yoon et al. reported previously.[9] In addition, a higher voltage is required to apply the same electric field as the HO device and the AHO device to the AHT device since the thickness of the inserted layers (5-nm-thick-$Ta_2O_5$ layer and 10-nm-thick-Al: $HfO_2$) increased. Thus, the maximum on/off ratio and the F/R ratio appeared at a higher read voltage in the AHT device than in the HO and AHO devices, and so did the set voltage. It is more

clearly presented in the current-electric field (I-E) graphs in Figure 2.3(a), and it can be found that the AHT device showed the highest on/off ratio. The current of the negative voltage region ($I_{LRS,\ reverse}$) was higher in the AHO device than in the HO device. The barrier height between Pt and Al: HfO2 is estimated to be lowered due to the Al doping effect. However, the F/R ratio of the AHO device was higher than that of the HO device because the $I_{LRS,\ forward}$ increased as well as the $I_{LRS,\ reverse}$. The $I_{LRS,\ reverse}$ of the AHT device was the lowest, proving the superior rectification capability. This is more apparently shown in the I-E curves in Figure 2.3(b).

Each device's I-V curves depending on the electrode area are presented in Figures 2.1(d)-1(f). Since the switching window of the HO device was hardly attained with $I_{cc}$ 10 nA, the HO device was set with the $I_{cc}$ 100 nA while the AHO device and AHT device were both set with $I_{cc}$ 10 nA. Insets are the mean and standard deviation (STD) current values from five measurement results determined by the device area. The HO device and the AHO device were read at 4.5 V, while the AHT device was read at 5.5 V, considering the thickness difference of the RS layer. Regardless of the stack configuration, the HRS current increased according to the device area in all three devices, while the LRS current did not show any area dependency. This means the LRS current flows along the specific path while the HRS conduction occurs over the whole device's area. This tendency corresponds with our group's previous work that demonstrated the switching mechanism of $Pt/Ta_2O_5/HfO_2/TiN$ self-rectifying ReRAM.[9]

Direct current (DC) voltage sweep cycling measurement was conducted as presented in Figure 2.4(a)-2(c). Considering the thickness difference, LRS and HRS

current were measured at 4.5 V in the HO device and the AHO device, and at 5.5 V in the AHT device to match the initial current levels. In the HO device, the HRS current increased drastically starting from the 60$^{th}$ cycle, and the device turned on completely at the 63rd cycle. On the other hand, the AHO device and the AHT device showed stable resistive switching over 100 cycles, and a clearer switching window could be attained in the AHT device than in the AHO device.

Cumulative probabilities of each device's LRS/HRS current are presented as insets to compare the switching uniformity. Coefficient of variation (CV, $\frac{Mean\ (\mu)}{Standard\ deviation\ (\sigma)}$) of LRS current ($CV_{LRS}$) was 1.26 for the HO device, 0.95 for the AHO device, and 1.29 for the AHT device. CV of HRS current ($CV_{HRS}$) was 1.62, 0.30, and 0.08 in the same order as the LRS current. When comparing up to 62 cycles, the last cycle before the HO device failed the switching, and the $CV_{LRS}$ was 1.35 for the HO device, 1.10 for the AHO device, and 1.41 for the AHT device. $CV_{HRS}$ was 0.86, 0.14, and 0.09 in the same order. As predicted from the cycling results, the HO device showed the poorest uniformity. The HRS current uniformity was improved significantly in the devices that adopted Al: $HfO_2$ as a resistive switching layer compared with the device using $HfO_2$. Not as great enhancement as HRS, the LRS current uniformity was also enhanced in the AHO device and the AHT device.

A cell-to-cell uniformity was also compared in 30 different devices, respectively, as shown in Figures 2.4(d)-2(f). As written in the graph, $CV_{LRS}$ was 1.82 for the HO device, 1.48 for the AHO device, and 1.01 for the AHT device. $CV_{HRS}$ was 0.64 for the HO device, 0.08 for the AHO device, and 0.07 for the AHT device. Uniformity

improvement was more apparent in cell-to-cell measurement results in both LRS and HRS current than in cell-to-cell results. As with the cycle-to-cycle results, LRS uniformity was also improved but was not as noticeable as HRS current. In both cycle-to-cycle and cell-to-cell measurement results, the switching uniformity was improved in the AHO device and the AHT device, and the AHT device showed the best operation with a $CV_{HRS}$ of 0.14 or less.

The data retentions of the off-state (HRS) and on-state (LRS) at different temperatures ranging from 85 to 160℃ were measured to compare the thermal stability led by Al doping as presented in Figures 2.5(a)-(c). Currents were read at 4.5 V in the HO device and the AHO device and, 5.5 V in the AHT device, and the measurement was conducted in a pulse mode. The HO device showed stable HRS retention at 85℃ up to $10^4$ seconds. In the AHO device, the HRS current at 85℃ was stable for more than $2\times10^4$ seconds, and the AHT device did not fail even after $5\times10^4$ seconds. Not only at 85℃ but in all temperature ranges, the HRS data retention was improved in the AHO and the AHT device compared to the HO device, and the AHT device showed the longest data retention among the three devices. To estimate the data retention time at room temperature, the HRS retention time at each temperature was plotted similarly to the Arrhenius-type graph fashion as presented in the insets of Figure 2.5(a)-3(c). When extrapolating the retention time versus the 1/kT, the HRS retention of the HO device at room temperature was estimated to be 21 days, 49 days for the AHO device, and 53 days for the AHT device. When the LRS retention was

measured at 110℃, the current of the HO device dropped to the off-state level in less than 100 seconds, as shown in Figure 2.5(a). In the AHO device, the LRS retention was slightly enhanced, and the current was maintained for ≈200 seconds. However, the AHT device showed a drastic improvement, and the LRS retention was maintained for ≈2000 seconds.

The switching uniformity and thermal stability were improved in the AHO and AHT devices compared with the HO device. The improvement was particularly significant in the HRS current, while the enhancement in the LRS current was not noticeable as much. That is, Al doping to $HfO_2$ mainly influenced the HRS conduction mechanism. In the previously published work from our group, Yoon et al. reported that HRS conduction was governed by the deep traps (≈1.0 eV) while the LRS conduction mainly occurs based on the electron traps in the shallow traps in the Pt/$Ta_2O_5$/$HfO_2$/TiN self-rectifying memory.[10] The shallow and deep traps of $HfO_2$ are the intrinsic defect sites, oxygen vacancy ($V_o$), formed during the deposition of $HfO_2$ in the device fabrication process. The oxygen vacancies in $HfO_2$ can exist in five charge forms of -2, -1, 0, +1, and +2, corresponding to up to four extra electrons in the vicinity of the vacant $O^{2-}$ site, and the charge form determines the energy level.[11-13] $V_o^{2+}$ and $V_o^{+}$ are more stable forms than others, and they act as the deep and shallow traps, respectively, based on energy level differences. [14, 15]

The conduction mechanism was analyzed based on the electrical properties change according to the temperature to figure out the role of doped Al and how it affected the HRS conduction. The I-V curves in the high voltage region in HRS of the HO,

AHO, and AHT devices were attempted to fit with the Poole-Frenkel (P-F), Schottky, and the tunneling mechanisms. The best linear fitting results were achieved from the P-F fitting for all three devices, as shown in Figure 2.6. The plots in the form of $Ln(I/E*T^{3/2})$ vs. 1/T according to the P-F equation, and the results fit well with the P-F mechanism.

The activation energy corresponding to the trap depth could be acquired from the slopes of the best-liner-fitted graphs at each voltage. The trap depth measured in HRS was ≈1.2 eV for the HO device and ≈1.41 eV for the AHO device, as presented in the insets of Figures 2.6(a) and (b). The estimated trap depth of $HfO_2$ and Al: $HfO_2$ were similar to the literature values.[16] Moreover, the activation energy was increased by 0.21 eV, which coincides with the previously reported activation energy increment by 0.26 eV after Al doping.[17] This increase demonstrates the existence of the deeper traps formed by the Al doping. The electrons are more stably trapped in the trap sites with deeper depth, which increases the switching uniformity and the thermal stability of the devices. The increment of the deep trap depth in the AHO device can be explained as the deeper trap ($V_o^{2+}{}_{Al}$) was formed in Al: $HfO_2$ after Al doping.[16] There are previous results that doped Al substitutes the Hf site, and the $V_o$ with higher energy level is formed, and this plays the role of deeper traps beside the innate deep traps formed in $HfO_2$. The formation of the deeper trap in the Al: $HfO_2$ layer is estimated to increase the HRS current uniformity.

The trap depth acquired from the AHT device was ≈1.6 eV, slightly higher than that of the AHO device but still similar value to the precedent studies.[17] The highest

switching uniformity and the thermal stability shown in the AHT device can be explained by the deepest trap depth. This can result from factors other than only Al doping, such as the interfacial traps formed at the $Ta_2O_5$/Al: $HfO_2$ interface. When $Ta_2O_5$ was deposited through PEALD, the $O_2$/Ar plasma was exploited as an oxidant as described in the experimental section. Applied plasma during the deposition deepened the defects that already have a deeper depth than the HO device. Considering the trap depth extracted from the P-F fitting, the HRS retention improvement of the AHT device can be comprehended in that context. The role and effect of the interface trap of the $Ta_2O_5$/Al: $HfO_2$ will not be profoundly discussed here, which will be presented in our further work. The dielectric constant extracted from the fitting results was 7.78 for the HO device, 5.37 for the AHO device, and 8.83 for the AHT device. These coincide considerably well with the square of the refractive index ($n \approx 1.9$-$2.2$) acquired from the spectroscopic ellipsometry measurements and the literature value ($n \approx 1.85$-$2.1$).[17] Doped Al into $HfO_2$ did not affect much dielectric constant as already reported in the precedent studies. [18]

To figure out the reason for relatively poor LRS uniformity, the materialistic analyses were performed through Auger electron spectroscopy (AES), as shown in Figure 2.7. The AES analyses were conducted on the HO device and the AHO device in LRS and HRS to compare the RS layer change before and after switching. The switching area was sputtered with the rate of 31 Å/min from Pt TE surface to the middle of TiN BE. In the HO device, the hafnium (Hf) and the oxygen (O) profile change in LRS and HRS was noticeable not only within the RS layer but also at the interfaces of both electrodes, as presented in Figures 2.7(a) and (b). Hf and O moved

along with the applied bias during the resistive switching. A significant change in Hf and O could be the reason for the LRS uniformity degradation since the LRS conduction is governed by the shallow traps ($V_o^+$).

On the other hand, the Hf and O profile changed less in the AHO device before and after resistive switching, as can be found in Figures 2.7(c) and (d). However, as enough reset voltage to eliminate the electrons from deep traps is about -8 V in both devices (Figure 2.1), Hf and O migration cannot be completely prohibited even in the AHO device. When voltage was applied up to about -8 V without $I_{cc}$, which is high enough to initiate the ionic migration as shown in Figure 2.8, the current started to increase rapidly rather than the rectification. The electroforming occurred at about -9 V, and the devices showed ionic switching as presented in the inset of Figure 2.8(a). In other words, the voltage sweep range for a full reset is similar to the range that initiates the ion migration, meaning that $V_o$ could migrate according to the applied bias polarity. Thus, the reliability in LRS was not improved significantly even after Al doping. Even though both the HO device and the AHO device failed at electroforming in the positive bias range, the current still increased abruptly, as presented in Figure 2.8(b). The shallow traps governing the LRS conduction are more affected by applied field than Al doping, so there was no noticeable LRS reliability improvement in the AHO device.

The enhancement of LRS uniformity and stability in the AHT device could result from the plasma treatment during the $Ta_2O_5$ deposition. This corresponds to the previous study reporting the enhanced LRS data retention by the plasma treatment in Pt/$HfO_2$/TiN memory cells.[19] As stated above, $O_2$/Ar plasma used in the $Ta_2O_5$

deposition process could deepen the trap depth and form extra traps at the interface, which increased the retention time and improved the switching uniformity in LRS and HRS of the AHT device. More detailed explanations of the switching mechanism in the HO device and the AHO device are included in Figures 2.9 and 2.10.

To sum up the measurement results and the analyses so far, the switching reliability and the uniformity of the Al: $HfO_2$ adopted devices were highly improved compared to the HO device. Because of the deeper trap formed by the doped Al, HRS uniformity and the off-state data retention was highly enhanced. Also, the AHO device showed high F/R ratio and on/off ratio than the HO device. However, the uniformity and the thermal stability of LRS were not improved as much as HRS. Meanwhile, in the AHT device, HRS uniformity and the LRS uniformity were drastically enhanced. The data retention of HRS and LRS was significantly increased, and the F/R and on/off ratio were the highest. Overall, the AHT device showed the most superior electrical characteristics among the candidates. Therefore, the stack of the AHT device, Pt/$Ta_2O_5$/Al: $HfO_2$/TiN, was selected for implementing the 9×9×2 vertical ReRAM array.

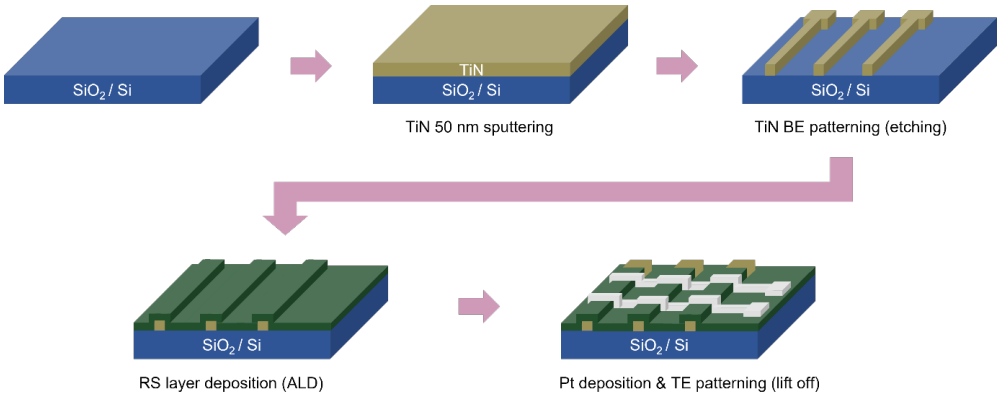


Figure 2.1 Fabrication flow of the crosspoint device.

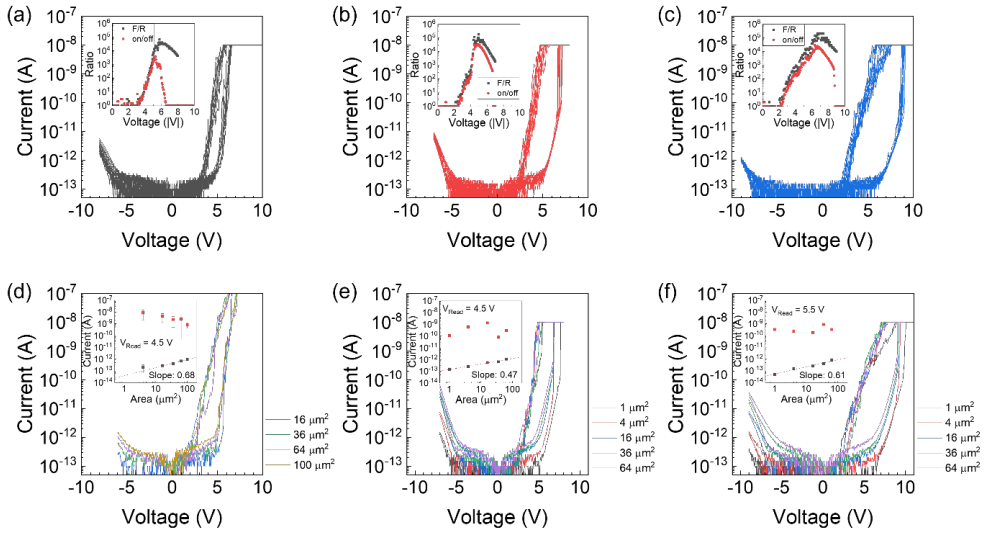


Figure 2.2 Representative I-V curves of the 2 μm x 2 μm (a) HO device, (b) AHO device, and (c) AHT device with $I_{cc}$ 10 nA. Insets are the on/off ratio and F/R ratio of each device. Representative I-V graphs depending on the switching area of the (d) HO device, (e) AHO device, and (f) AHT device. Insets are the LRS and HRS current tendency according to the switching area.

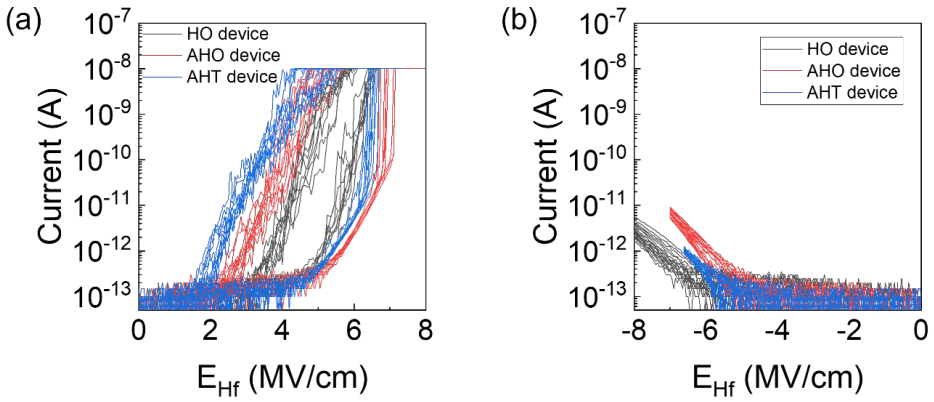


Figure 2.3 I-E plots of the (a) positive voltage region and the (b) negative voltage region measured in the HO device (black lines), the AHO device (red lines), and the AHO device (blue lines).

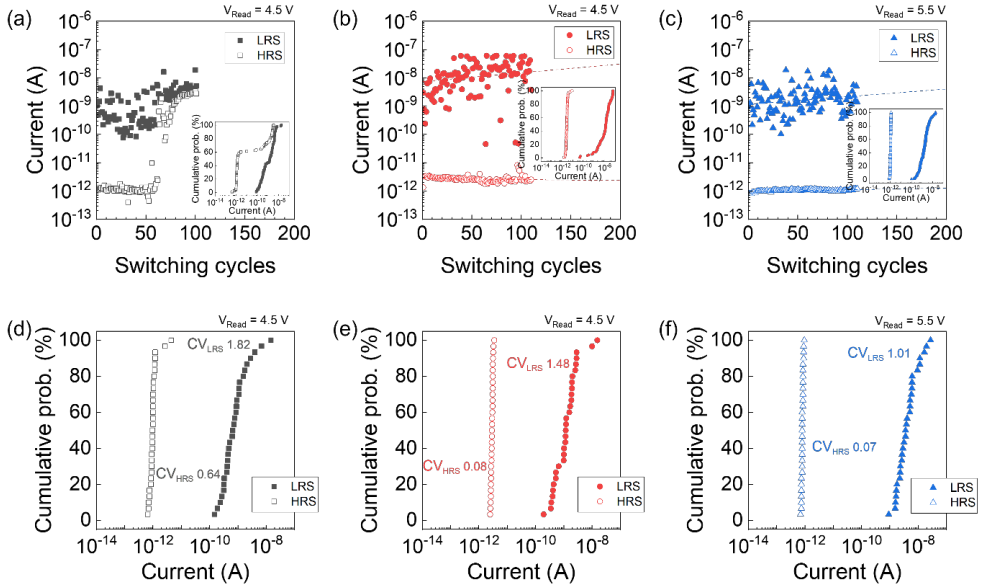


Figure 2.4 DC cycling results of the (a) HO device, (b) AHO device, and (c) AHT device. Insets are the cumulative probabilities of LRS and HRS current. Cell-to-cell cumulative probability of the LRS and HRS current measured in the (d) HO device, (e) AHO device, and (f) AHT device. The switching area is 10×10 μm$^2$.

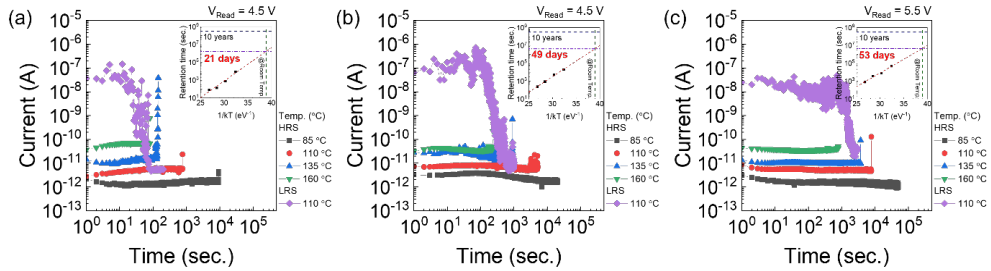


Figure 2.5 LRS and HRS data retention measured at different temperatures of the (a) HO device, (b) AHO device, and the (c) AHT device. Insets are the HRS retention time versus 1/kT graph (time-failure graph).

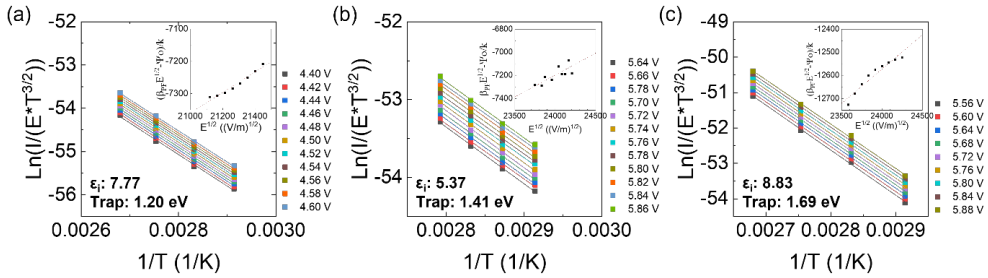


Figure 2.6 P–F fitting and the plots in the form of $Ln(I/(E*T^{3/2}))$ vs. 1/T according to the P–F equation in HRS measured in the (a) HO device, (b) AHO device, and the (c) AHT device. Insets are fitting results of each figure.

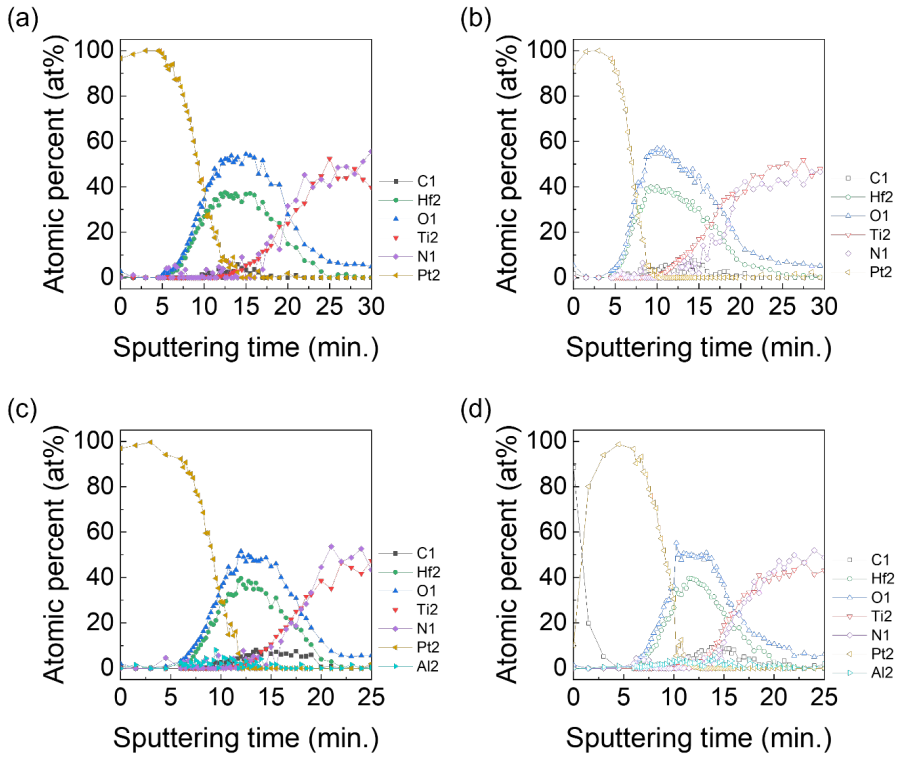


Figure 2.7 AES depth profiles of (a) HO device in HRS, (b) HO device in LRS, (c) AHO device in HRS, and (d) AHO device in LRS.

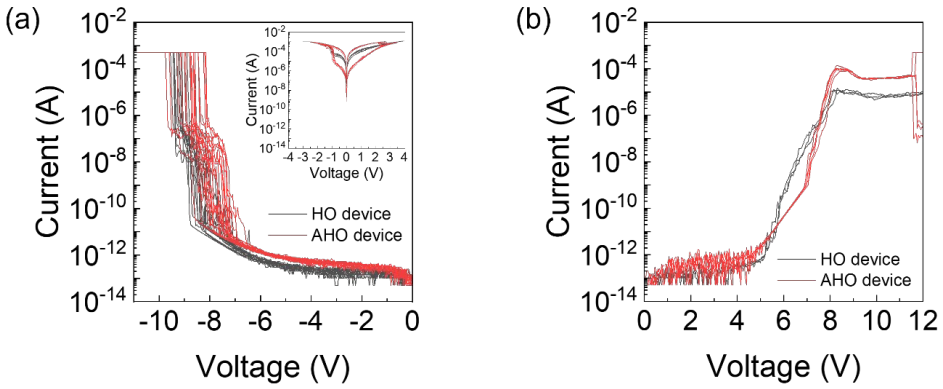


Figure 2.8 (a) Negative forming curves of HO and AHO devices. I-V graphs of the ionic resistive switching of HO device and AHO device after negative forming. (b) I-V curves in the positive voltage region of the HO device and the AHO device.

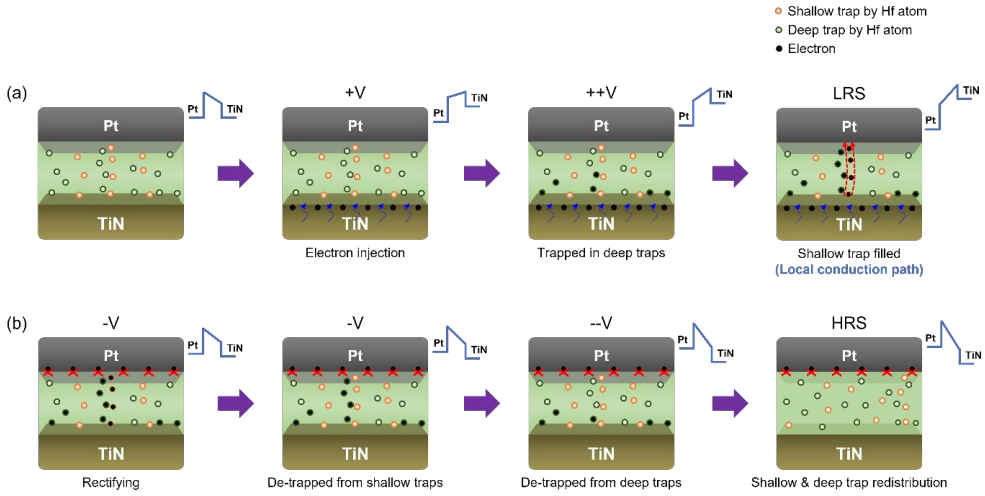


Figure 2.9 Schematic diagrams of the (a) SET and (b) Reset process in HO device

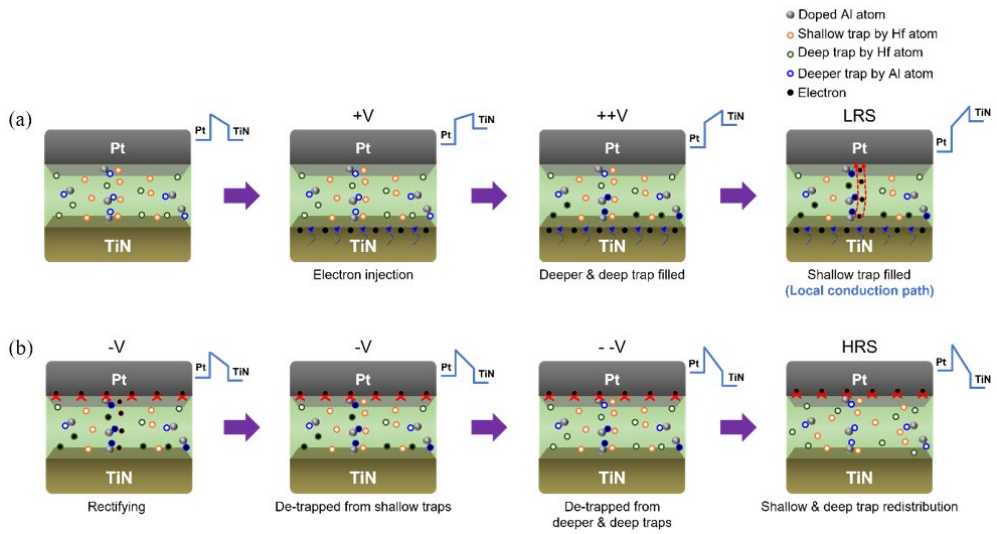


Figure 2.10 Schematic diagrams of the (a) SET and (b) Reset process in AHO device.

## 2.4. Summary

The electrical characteristics of the HO, AHO and AHT crosspoint devices were evaluated to find the proper resistive switching layer to be applied for the vertical ReRAM array. The AHT device showed the highest F/R ratio and on/off ratio, and a wide and clear switching window was obtained through the DC voltage sweep measurement. The HRS uniformity was improved in AHO and AHT devices compared to the HO device, and the AHT device, in particular, showed the lowest $CV_{HRS}$ value. The data retention was tested at high-temperature ranges for thermal stability comparison, and the AHT device showed the longest retention time regardless of the temperature. The expected room temperature HRS retention was acquired by extrapolating the data retention according to the temperature, and 53 days were expected for the AHT device, which was superior to the HO and AHO devices. P-F fitting was conducted to analyze the switching mechanism, and the deepest trap depth was acquired in the AHT device, which is estimated to be the reason for switching uniformity and stability enhancement. The deeper trap formation through Al doping and the insertion of a blocking layer $Ta_2O_5$ induced the high switching uniformity and stability in the AHT device. The HRS and the LRS switching uniformity and thermal stability were also improved in the AHT device compared with others. Based on the measurement results, the $Pt/Ta_2O_5/HfO_2/TiN$ stack was chosen for the V-ReRAM application.

## 2.5. Bibliography


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# 3. Fabrication of 3D vertical ReRAM and Applications

## 3.1. Introduction

Resistance Switching Random Access Memory (ReRAM) is a next-generation memory device that has been studied with great interest over the past few decades. [1-3] V-NAND flash memory is currently the mainstream of the memory device market, but it is also expected to face the limit of memory density improvement in the near future. The V-NAND, in general, has a complicated structure as WL/block oxide (BO)/charge trapping layer (CTL)/tunnel oxide (TO)/Poly-Si while the V-ReRAM is composed of WL/resistive switching layer (RS layer)/BL, and the minimum cell size of the $4F^2$ (F: feature size) can be achieved in the V-ReRAM. The channel material for V-NAND, poly-Si, has a low electron mobility of $0.1cm^2/Vs$, which decreases the operating speed of flash memory. On the other hand, the V-ReRAM device can adopt metal as BL because of the simple MIM structure of the ReRAM, which is advantageous for the speed. Moreover, the vertical ReRAM presented in this dissertation can have a smaller hole critical dimension (CD) than the V-NAND.[4] In the case of the V-NAND, since the channel hole must be connected to the Si substrate, the hole open CD needs to be increased as the number of layers and stacks increases due to the hole etch profile issue. However, the V-ReRAM only needs to have a potential difference between the WL plane and the BL so that the hole open CD can be made smaller, which is more efficient than V-NAND regarding integration in the horizontal direction. In addition, the operating voltage of the V-

NAND is about 20 V which can cause the crosstalk issue led by the capacitive coupling.[5] To prevent the crosstalk issue, a certain thickness of the interlayer insulating film needs to be secured, which can be a critical factor of the high-density integration. In the meantime, the operation voltage of V-ReRAM can be reduced to about 10 V and less, which can avoid the coupling issue so that the thickness of the interlayer insulating film can be decreased. For these reasons mentioned above, V-ReRAM can be a great candidate to substitute V-NAND, particularly in terms of vertical stackability.

A hole etched 9×9×2 V-ReRAM array was made with the selected RS layer in section 2, and improved switching uniformity and reliability were acquired. In addition, this device's low operating current and vertical stacking characteristics are suitable for applications that require low power consumption and large storage space, such as hardware neural network (HNN). Therefore, by exploiting the high-density integration and two resistance states-low resistance state (LRS) and high resistance state (HRS), a binary neural network (BNN) simulation was conducted for image classification. The hardware implementation of neural networks is achieved through the V-ReRAM array in this study.

## 3.2. Experimental

A TiN 40 nm was sputtered through radio frequency (RF) sputtering (Sorona, SRN 120) using the Ti target with the $N_2$ flow on the $SiO_2$/Si substrate for the first-layer BE. On the TiN thin film, $SiO_2$ 50 nm was deposited through plasma-enhanced chemical vapor deposition (PECVD, Oxford instruments, PlasmoPro System100) as the first-layer insulator between two vertically stacked BE layers. The second-layer BE TiN 40 nm and the second-layer insulator $SiO_2$ 30 nm were deposited in the same condition as the first layer. The PR patterns were defined using maskless lithography (Nano System Solutions. Inc, DL-1000 HP). It was dry-etched from the second-layer insulator $SiO_2$ to the first-layer BE TiN altogether in-situ to form BE patterns (GIGALANE, NeoS-MAXIS 200L). The line width for the BE was 160 μm to avoid the influence of line resistance. The byproducts produced during the etch process were removed using an asher (plasma finish, V15-G). The sidewall of the first and the second layer TiN was exposed after etching, which can be the parasitic resistive switching area. The sidewall-passivation $SiO_2$ 60 nm was deposited through PECVD to avoid unwanted parasitic switching and limit conduction to occur only in the memory cell. After that, photolithography was performed to make vertical holes, and the etching process was performed under the same conditions as BE etching. $HfO_2$ 10 nm was deposited for the HO V-ReRAM, and Al: $HfO_2$ 10 nm was deposited for the AHO V-ReRAM and the AHT V-ReRAM, respectively, with thermal ALD (CN1, custom-made ALD cluster system) in the same condition that was described in the crosspoint device fabrication methods. Al layer and $HfO_2$ layer were deposited in-situ

using the same thermal ALD with the ratio of 1:9 for Al: $HfO_2$ deposition. $Ta_2O_5$ 5 nm was deposited for the AHT device through PEALD (CN1, Atomic Premium plus 200) in the same condition as depicted in section 2.1.1. The TE pattern was made through the lift-off process after depositing a 50-nm-thick Pt with an e-gun evaporator (SORONA, SRN-200i).

To expose the BE of the first and second layer memory for being contactable during the electrical properties measurements, the RS layer of the front part (orange-circled) was first etched until the second-layer insulator $SiO_2$ was exposed, as shown in Figure 3.1. (Oxford instruments, PlasmaPro System100 Cobra) The exposed $SiO_2$ was wet etched using buffered oxide etchant (BOE) so that the second-layer BE TIN could be open. Then the second-layer BE of the front part (orange-circled) was etched in the $BCl_3/Cl_2$ atmosphere, and the byproducts were removed through ashing. The first-layer insulator of the front part (orange-circled) and the second-layer insulator of the back part (green-circled) were wet-etched together with the BOE to open the first (orange-circled) and the second (green-circled) layer BE TiN at the same time.

The cross-section of the completed device was observed with the field emission scanning electron microscope (FESEM; HITACH, S4800). A-200k kV high-resolution transmission electron microscope (HRTEM; JEOL, JEM F200) was used to verify each layer was well defined in the V-ReRAM. To analyze the materialistic properties of the resistive switching layers, analyses through scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDS) were conducted. The depth profile of the HO device and the AHO device was analyzed through Auger electron spectroscopy (AES; ULVAC-PHI, PHI710) with a sputtering

rate of 31 Å/min. The thickness and the refractive index of $HfO_2$ and Al: $HfO_2$ were measured through spectroscopic ellipsometry (SE; Wollam, ESM-300). Electrical properties were measured using a semiconductor parameter analyzer. (SPA; Hewlett Packard, 4145B) The TE was biased, and the BE was grounded during the measurement.

For the simulation of the electrical properties of the V-ReRAM, a model was created using curve-fitting for the LRS and HRS curves in the $V > 0$ region among the current-voltage (I-V) characteristics of the device. In order to confirm the applicability of the binarized neural network of the V-ReRAM array, the learning method was simulated through off-chip learning (ex-situ) using two types of neural networks. The first neural network was a 9×3 network with 9(=3×3) pixel input and 3 category outputs, and the weight was assumed to have a binary state of -1 or 1. The backpropagation and stochastic gradient update (SGD) were used for gradient-based training. The straight-through estimator function was applied to represent the internal real number weights binary, intended to preserve the gradient information during backpropagation. This first neural network was trained for 500 epochs with 30 images. The second neural network had the same number of inputs and outputs as the first network and included information about the previous I-V model. This neural network was only used for testing by copying the weights trained from the first neural network. A voltage input corresponding to the previous 30 images was applied, and the highest current among the output currents was simulated to correspond to the classification result. This shows an off-chip learning simulation of the V-ReRAM array. Both networks were implemented using the python language and the PyTorch framework.

It was assumed that the write-and-verify method is used when writing to the cell. The network was trained to classify the Modified National Institute of Standards and Technology (MNIST) dataset, which was rescaled by half-size from the original 28-by-28-sized greyscale images. The simulation was implemented using the Python language and Pytorch framework.

## 3.3. Results and Discussions

A 9×9×2 V-ReRAM array is fabricated, and the fabrication process is explained in detail in Figure 3.1. The layout of the photomask used for the V-ReRAM array fabrication is presented in Figure 3.2(a), and the top view optical image of the completed 9×9×2 vertical array is included in Figure 3.2(b). The cross-section image of the completed single cell of the V-ReRAM array is shown in Figure 3.3(a), and it was verified that each layer was well defined. The HRTEM and STEM-High angle annular dark-field imaging (STEM-HAADF) images are shown in Figures 3.3(b) and (c). EDS mapping results coincide with Figure 3.3(c) are presented in Figure 3.3(d)-(h), indicating Pt, Si, O, Ti, and Hf, respectively, and it can be seen that all layers were well defined. The amount of the Ta and Al was not detected since 5-nm-thick $Ta_2O_5$, and doped Al in the scanning area was too little to be detected. These results are not included in the manuscript.

The electrical properties of two-layer AHT V-ReRAM were measured, and Figure 3.4(a) is the DC cycling results of 100 cycles. The HRS current was extremely uniform in both positive and negative voltage regions, as shown in Figure 3.4(a). Inset is the F/R ratio and the on/off ratio depending on the voltage. The HRS current in the negative voltage range is maintained as low as the HRS current in a positive voltage range, and thus the F/R ratio and the on/off ratio are similar up to ~ 8 V. This proves the excellent rectification capability of the AHT V-ReRAM. The cumulative probabilities of the LRS and HRS current measured at 5.5 V acquired from DC cycling results are shown in Figure 3.4(b). The $CV_{LRS}$ and $CV_{HRS}$ extracted from the

measurement results are presented in the graph 0.77 and 0.029, respectively. Considering the fact that $CV_{LRS}$ and $CV_{HRS}$ of the AHT crosspoint device (Figure 2.4 (c) in section 2) were 1.29 and 0.08, the uniformity of the LRS and HRS current was greatly improved in the AHT V-ReRAM, which can be originated from the switching area reduction. The switching area was drastically reduced from the crosspoint device (100 $\mu m^2$) to the vertical structure (0.126 $\mu m^2$). The $CV_{HRS}$ of 0.029 is an impressively low value, which means supreme cycle-to-cycle uniformity. Not as greatly enhanced as HRS current, LRS current still showed a uniformity improvement in the vertical structure device. Cycling results of the HO V-ReRAM are included in Figure 3.5(a), and its cumulative probabilities of LRS and HRS current are presented as inset. Both LRS current and HRS current gradually increased, and the take-off voltage shifted to the left. Poor switching uniformity can be found, and the switching window was hardly attained.

The cell-to-cell electrical characteristics were also measured on the 9×9×2 array. The cumulative probabilities of the on and off current measured on 81 cells per layer are presented in Figure 3.4(c). Red circles indicate the currents measured on the first layer cells, and blue squares represent those of the second layer cells. The closed symbols for LRS current and the open symbols for HRS current and unselected cells were floated during the measurement. The $CV_{LRS}$ was 0.64 and 0.74 each, which is similar results to the cycle-to-cycle results measured on the single cell. The $CV_{HRS}$ was 0.23 for both the first and the second layer, which is a slightly increased value compared with Figure 3.4(b). Since the cell-to-cell measurement was conducted on the array, the interference from the neighboring cells was not completely prevented

even with the great rectification capability of the self-rectifying AHT V-ReRAM. The I-V graphs measured on 81 different cells of the second layer of the HO V-ReRAM and the AHT V-ReRAM are presented in Figures 3.5(b) and (c). Despite the lower operating current, the AHT V-ReRAM showed a higher on/off ratio than the HO V-ReRAM. The HRS current in both positive and negative voltage regions was highly uniform in the AHT V-ReRAM, while the current noticeably increased over the cycle in the HO V-ReRAM. Great rectification functionality and highly enhanced switching uniformity of the AHT V-ReRAM are more apparently presented in the I-V graphs.

Figure 3.4(d) shows the excellent self-rectification of the AHT V-ReRAM. The selected cell is located in the first layer at the #6 position, as indicated in the inset. The selected cell was programmed to HRS, whereas all the other cells were programmed to LRS. This corresponds to the worst-case scenario in a crossbar array (CBA) in reading the selected HRS cell.[6] As can be found in Figure 3.4(d), the HRS of cell #6 in the first layer can be well determined, suggesting a sufficient suppression of the sneak current through the neighboring LRS cells due to the high self-rectifying capability of the AHT V-ReRAM. The measurement was conducted in a 4×4×2 array due to the time efficiency. However, the same high functionality is estimated when expanding the array size to 9×9×2. To show that this 4×4×2 array operates well, the cell-to-cell I-V graphs acquired from this array are shown in Figure 3.5(d). The curves from the first layer are green and the second layer is blue.

The low operating current and the vertical stackability of the AHT V-ReRAM make it suitable for applications that require low power consumption and high storage capacity, such as HNN. Since the AHT V-ReRAM has two states, LRS and HRS, it is

proper to be exploited in a BNN. A BNN has been shown to work well as a neural network with only binarized inputs and weights, and its simplicity has attracted attention in the design and implementation of HNN. BNN operates with only -1 or 1, not consecutive real numbers as inputs and weights, and such a simple neural network is specialized to implement HNN. As BNN only operates with -1 or 1, there is a limitation that the number of input and output neurons must be much larger than that of conventional NNs to achieve similar performance. The AHT V-ReRAM presented in this study is suitable for BNN learning because it can easily secure a large storage capacity by utilizing high-density integration and a simplified manufacturing process. In addition, the vertically stacked structure as above can reduce the characteristic change according to spatial variation. In planar CBA, the minimum distance between devices is the same as the feature size, while in the vertically stacked structure, if two devices between one WL and two BLs with different heights are selected, the minimum distance between devices is equal to the thickness of the isolation between the BLs. As the thickness of the isolation is independent of the lithography patterning resolution, spatial variation originating from the line patterning process can be reduced in the AHT V-ReRAM. As the characteristic deviation between devices due to spatial change is lowered, a higher learning accuracy can be obtained.

A simulation was conducted based on a model mimicking the electrical characteristics of the AHT V-ReRAM to demonstrate its feasibility as an HNN. A model simulating LRS and HRS I-V curves in the $V > 0$ range of the device was prepared for the simulations, as shown in Figure 3.6(a). The noise generated by the trap/detrap mechanism of the device was reflected in the form of the read variation.

The read variation significantly impacts the operating performance, which will be discussed later. A BNN training classifies 30 3×3 images (Figure 3.6(b)) belonging to ‘L’, ‘I’, and ‘X’ was conducted for the simulation. Considering the characteristics of the device, training was carried out with pure BNN, and off-chip training was conceived by transferring the trained weights to the simulated self-rectifying ReRAM array, as presented in Figures 3.6(c) and (d). Figure 3.7(a) contains 30 images of 3×3 used for training. Figure 3.7(b) shows the structure of a pure BNN on which weights are trained. A 3×3 image was vectorized and fed to 9 inputs, and 3 outputs were computed. Hyperparameter tuning was performed to classify all 30 images accurately. After confirming that all 30 images were correctly classified, the trained weights were transferred to Figure 3.7(c) and tested. One weight was transferred to two ReRAMs composed one word line (WL) and two bit lines (BLs) with different heights. A weight of 1 was transferred to the first layer LRS and second layer HRS, and a weight ‘-1’ was transferred to the opposite form, which is vice versa. One input was given as a pattern to two BLs with different heights. Input ‘1’ was promised as the application of -8 V on the first layer and 0 V on the second layer, and the input ‘-1’ was the opposite. By applying current through this, multiplication of ‘1’ and ‘-1’ could be performed in hardware. Currents derived by all possible input and weight combinations are shown in Table 1. The input for the 3×3 image recognition test was fed through 9 BLs, and classification was determined through the relative magnitude of the current collected by the 3 WLs. Applying a voltage for vertically stacked two cells is advantageous in terms of integration when applied to a horizontal device as less area can be occupied.

Figure 3.8(a) shows the number of correctly classified images when the test of exposing 30 images to HNN having the weights transferred weights of Figure 3.7(c) was repeated 100 times. A black line represents the results when the test was completed after being read once. Out of 100 tests, there were cases in which all 30 tests were correctly classified, but most of them could not be correctly classified, which was caused by the read variation mentioned above. To verify the influence of the read variation, the final outputs of each WL were statically processed and analyzed during 100 tests. Figure 3.8(b) shows the distribution of final output levels from each WL when Figure 3.7(a) image was tested 100 times. The results for each image in Figure 3.8(a) are presented in the graph at the corresponding coordinates in Figure 3.8(b). The three box plots of each graph correspond to 'L', 'I', and 'X' from the left. The red line, blue box, black range, and red marker in each box plot mean the median, 25-75% cumulative distribution interval, minimum/maximum values, and statistical outliers, respectively. The red and blue lines of Figure 3.8(a) are the test results based on voting among three and five different models of WL outputs, respectively. The most frequent WL output was selected, which corresponds to averaging several model outputs, which is the core of ensemble averaging. The test accuracy was 73.33% for the naive results and 86.67% and 90% each when voted after reading 3 and 5 times, respectively. In the same order, the average test accuracy is 89.73%, 96.13%, and 98.23%.

The box plot in Figure 3.8(b) shows that the classification was well-implemented for each image through the order of the median values of the WL output value. However, it can also be figured out that the order of the actual output can be reversed

by the fact that one median overlaps the min/max range of the other output. Therefore, multiple reads are required to obtain the expected WL output order. This can be supported by the ensemble averaging operating principle in the neural networks field.[7] In the case of a trained model with the same input and variance, it has been proven that averaging models with multiple non-idealities can improve training quality by minimizing variance without compromising training performance (without the influence of bias). In the case of a trained model with the same input and variance, it has been proven that averaging models with multiple non-ideality can improve training quality by minimizing variance without compromising training performance (without the influence of bias). This work also includes a model with the same input and non-ideality with reading variation, and the principle of ensemble averaging can be applied. The V-ReRAM structure has the advantage of high density, and the self-rectifying ReRAM offers a low current and high memory window so that it is possible to create a highly portable neural network with minimal non-ideality.[8, 9] With some more factors considered, the original BNN structure can be extended to larger neural networks, and this can further increase the test accuracy of the simulation.

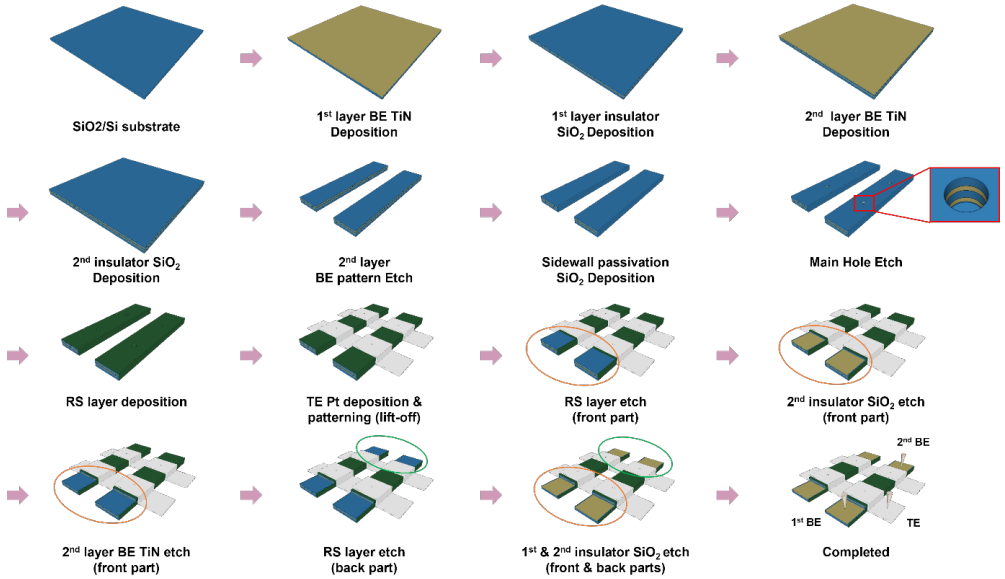


Figure 3.1 Schematic diagrams of the vertical ReRAM array fabrication.

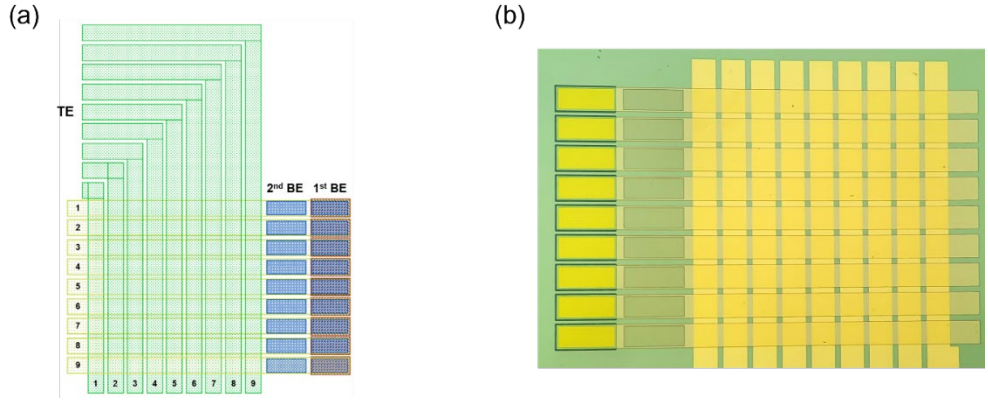


Figure 3.2 (a) Photomask layout of the 9x9x2 vertical ReRAM array, (b) Optical image of the completed 9x9x2 vertical ReRAM array.

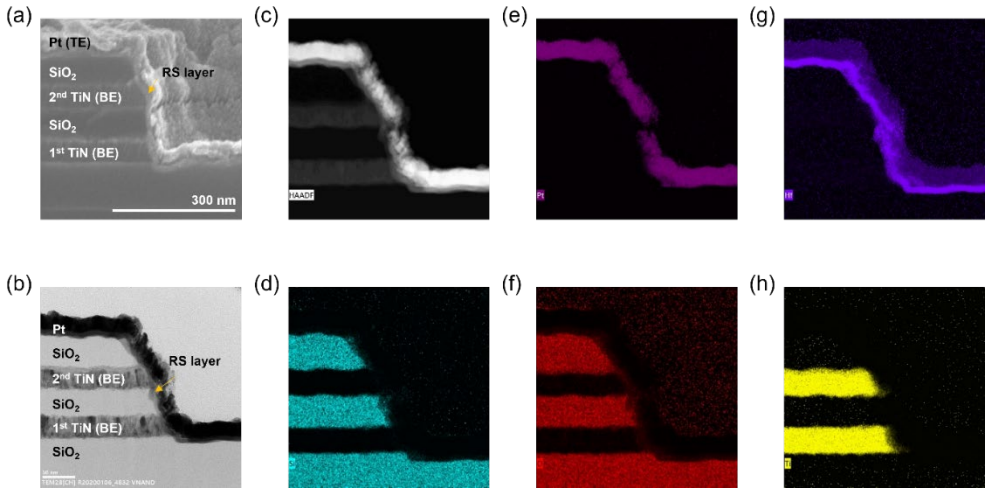


Figure 3.3 Cross-sectional images of the completed AHT V-ReRAM observed through (a) FESEM, (b) HRTEM, (c) STEM HAADF image of the completed AHT V-ReRAM, and the matching EDS mapping results of (d) Si, (e) Pt, (f) O, (g) Hf, (h) Ti.

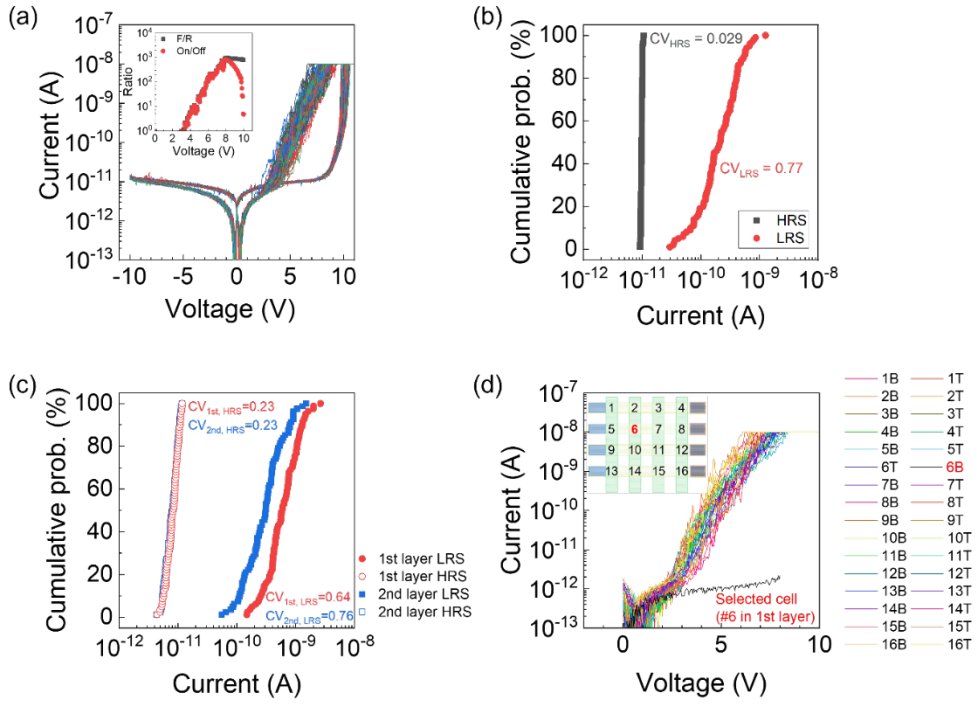


Figure 3.4 (a) DC cycling results of the AHT V-ReRAM (100 cycles), (b) Cumulative probabilities of the HRS and LRS current read at 5.5 V of (a), (c) Cell-to-cell cumulative probabilities of the LRS & HRS current measured in the first and the second layer of the 9×9×2 AHT V-ReRAM array, (d) The reading operation conducted on the 4×4×2 array in the worst case-selected cell is HRS, and unselected cells are LRS. Inset is the layout and numberings of the devices constituting the 4×4×2 array.

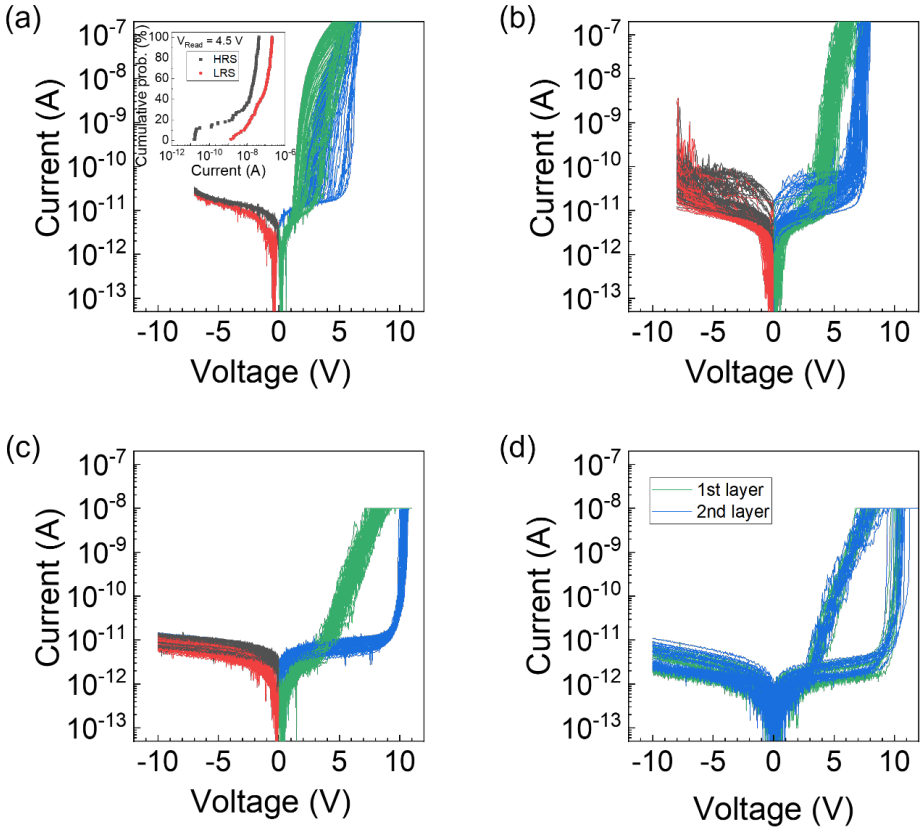


Figure 3.5 (a) DC cycling results of HO devices (inset: cumulative probabilities of LRS and HRS currents); Device-to-device I-V curves measured on 81 cells of the second layer of (b) HO V-ReRAM array and (c) AHT V-ReRAM array; (d) Device-to-device I-V graphs measured on the 4x4x2 AHT V-ReRAM array used in Figure 7d. (Green line: first layer, Blue line: second layer)

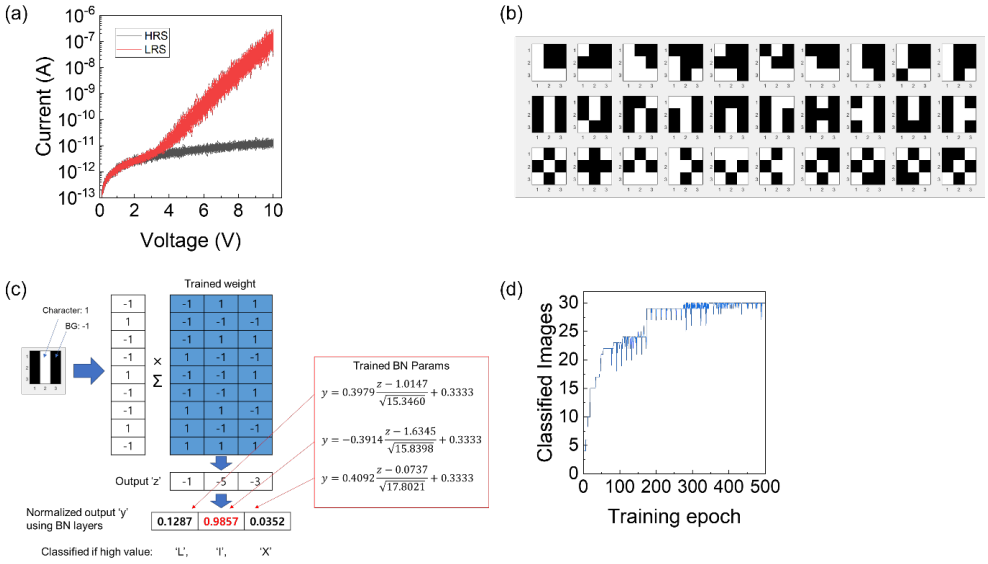


Figure 3.6 (a) Simulated I-V graphs of the AHT V-ReRAM, (b) Input images for training a pure BNN, (c) Schematic diagrams of a pure BNN simulation (software training), (d) Test results acquired through (c).

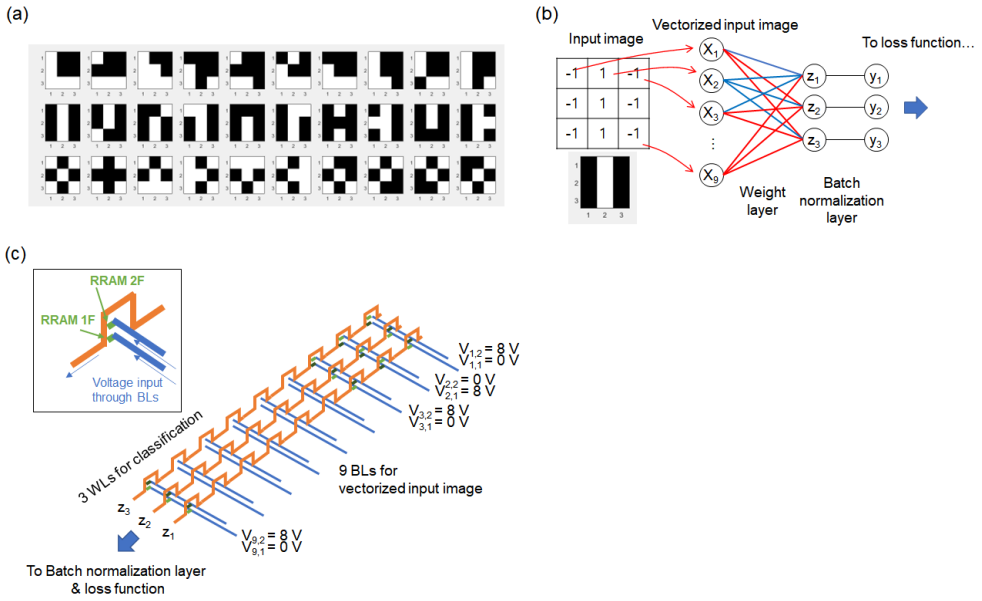


Figure 3.7 (a) 30 input images used for train and test. Schematics of (b) pure BNN training. Blue line indicates a weight of '-1,' and the red line is a weight of '1.' (c) Schematics of HNN with transferred weight from the (b). (Dark green: HRS, Light green: LRS)

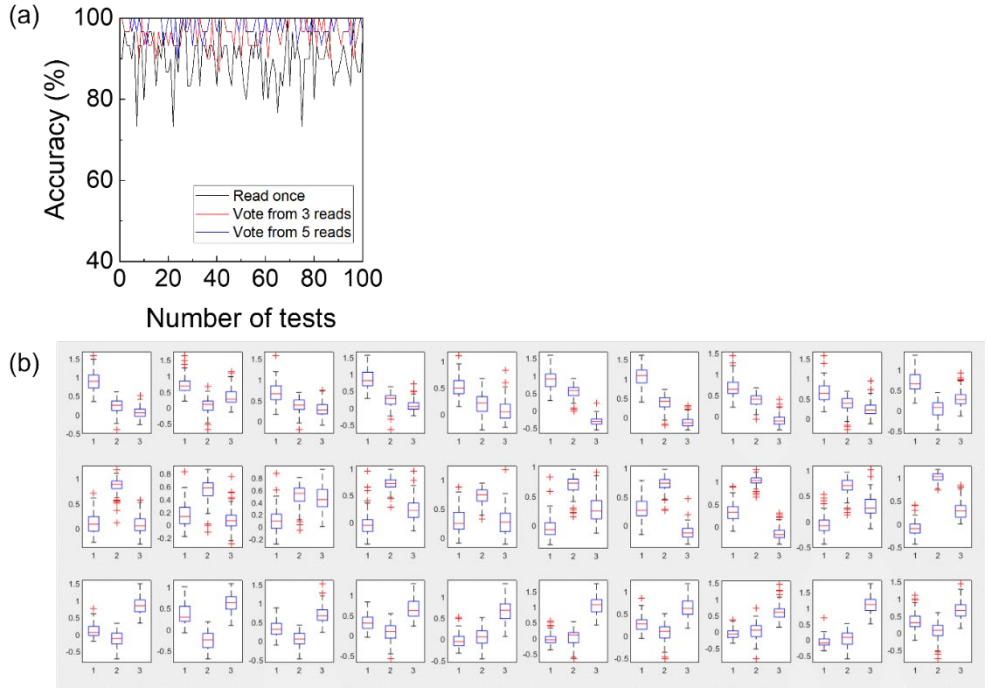


Figure 3.8 (a) The test accuracy of 100 repetitions of exposing 30 images to the weighted HNN in Figure 3.7(c), (b) Statics of final output from each WL.

| BNN input value | Corresponding voltage pair input (1F, 2F) | BNN weight value | Corresponding conductance (1F, 2F) | Output (=input × weight) | Corresponding current output |
|---|---|---|---|---|---|
| 1 | (-8 V, 0 V) | 1 | (LRS, HRS) | 1 | High |
| 1 | (-8 V, 0 V) | -1 | (HRS, LRS) | -1 | Low |
| -1 | (0 V, -8 V) | 1 | (LRS, HRS) | -1 | Low |
| -1 | (0 V, -8 V) | -1 | (HRS, LRS) | 1 | High |

**Table 3.1**. Table showing the summarization of the relation between the software and hardware BNN.

## 3.4. Summary

A 9×9×2 AHT V-ReRAM array was fabricated. The maximum on/off ratio of $10^3$ was obtained with the operating current of 10 nA, which is extremely low power consumption. The $CV_{HRS}$ from cycle-to-cycle and cell-to-cell was 0.029 and 0.23, respectively, which proves the high switching uniformity of the AHT V-ReRAM. The worst-case off-current readout demonstrated the rectifying capability of the AHT V-ReRAM in a 4×4×2 array along with its excellent F/R ratio. The applicability of the AHT V-ReRAM as an HNN was demonstrated owing to its low power consumption and the structural merits of high-density integration. The high storage capacity of the AHT V-ReRAM makes it proper for BNN training particularly, which requires larger inputs and outputs than other neural networks. Image classification of 30 input images was conducted with the aid of the ensemble method, and an average accuracy of 98.23% could be achieved. The higher accuracy is expected to be achieved by increasing the array size and improving the LRS uniformity. As the movement of the shallow traps causes the LRS current distribution, this can be mitigated by introducing applied field concentration on the inserted nanostructure, which will be dealt with in our further study. This study is the first report on the fabrication of a vertically stacked self-rectifying ReRAM array with decent switching performance, and its potential as a high-density storage device was demonstrated through hardware implementation of neural networks.

## 3.5. Bibliography


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# 4. Challenges for charge loss in 3D vertical ReRAM

## 4.1. Introduction

Although V-NAND flash memory is the main storage, it has many problems to solve, such as deep hole etching and uniform oxide/nitride/oxide (ONO) thin film deposition in the process.[1] The high aspect ratio contact (HARC) etching technique is essential to achieve uniform hole diameters between at top and bottom.[2] Different hole diameters change properties, resulting in dispersion between devices. Recently, atomic layer etching (ALE) technology for HARC etching has been studied to improve the variation. In V-NAND with an aspect ratio of 50 or more, a high-level ALD process is required to deposit the uniform ONO thin film because the quality of ONO film affects reliability and endurance as well as variation between devices.

In addition, the slow operation speed caused by using poly-crystal Si as the channel material is an inherent problem of V-NAND. Research on next-generation channel materials is actively conducted, and single-crystal Si and amorphous oxide semiconductor (AOS) are promising candidates.[3] The stress generated while forming the multiple stacked $SiO_2/Si_3N_4$ layers causes the wafer warpage. This warpage can cause misalignment and defocus problems in subsequent photo processing. In addition, there is a problem caused by reducing the insulating film between the word lines to improve the density.

In NAND flash, the loss of the trapped electrons over time is a widely reported issue called the inter-cell interference phenomenon.[4-6] As the trapped charges

diffuse to the adjacent cells through the vertically shared charge trap layer, the switching reliability of the memory cell is degraded.[7] In order to secure the non-volatile characteristics of the charge trap flash memory, minimizing the loss of the trapped electrons is necessary.[8-10] Since the trap/detrap based ReRAM shares a similar switching mechanism, the interference phenomenon cannot be prohibited without implementing structural/materialistic modification. To integrate the high-density V-ReRAM array with superior switching performance in the charge-based memory, the factors influencing the charge loss need to be figured out to understand the inter-cell interference phenomenon. Thus, in this work, these factors inducing the inter-cell interference phenomenon in the hole-etched V-ReRAM were explored. The charge loss was confirmed in the $HfO_2$-based V-ReRAM operating based on the trap/detrap mechanism. The device in the LRS showed LRS retention degradation due to the diffusion of the trapped electrons, and the HRS current increase and set voltage shift were confirmed by the electrons that diffused and flowed into the adjacent cells. As there has been hardly any report on lateral charge loss in 3D V-ReRAM, this work will provide the community with a thorough understanding of the inter-cell interference phenomenon.

## 4.2. Experimental

A TiN 25 nm was sputtered through radio frequency (RF) sputtering (Sorona, SRN 120) using the Ti target with the $N_2$ flow on the $SiO_2$/Si substrate for the first-layer bottom electrode (BE). On the TiN thin film, $SiO_2$ 50 nm was deposited through plasma-enhanced chemical vapor deposition (PECVD, Oxford instruments, PlasmaPro System100) as the first-layer insulator between two vertically stacked BE layers. The second-and third-layer BE TiN 25 nm and the second-and third-layer insulator $SiO_2$ 50 nm and 30 nm, respectively, were deposited in the same condition as the first layer. The PR patterns were defined using maskless lithography (Nano System Solutions. Inc, DL-1000 HP). It was dry-etched from the third-layer insulator $SiO_2$ to the first-layer BE TiN altogether in-situ to form BE patterns (GIGALANE, NeoS-MAXIS 200L). The line width for the BE was 160 μm to avoid the influence of line resistance. The byproducts produced during the etch process were removed using an asher (plasma finish, V15-G). The sidewall of BE TiN was exposed after etching, which can be the parasitic resistive switching area. To avoid unwanted parasitic switching and limit conduction to occur only in the memory cell, the sidewall-passivation $SiO_2$ 60 nm was deposited through PECVD to encapsulate the TiN electrodes. After that, photolithography was performed to make vertical holes, and the etching process was performed under the same conditions as BE etching. $HfO_2$ 10 nm was deposited with thermal ALD (CN1, custom-made ALD cluster system) in the same condition described in the crosspoint device fabrication methods. $O_3$ was used as an oxidant. Top electrode (TE) patterns were formed through the lift-

off process, and Pt 50 nm was deposited using an e-gun evaporator (SORONA, SRN-200i). The top electrode (TE) pattern was made through the lift-off process after depositing a 50-nm-thick Pt with an e-gun evaporator (SORONA, SRN-200i).

To expose the BE of the first- and second-layer memory for being contactable during the electrical properties measurements, the RS layer of the front part (orange-circled) was first etched until the third-layer insulator $SiO_2$ was exposed, as shown in Figure 4.1. (Oxford instruments, PlasmaPro System100 Cobra) The exposed $SiO_2$ was wet etched using buffered oxide etchant (BOE) so that the third-layer BE TIN could be open. Then the third-layer BE of the front part (orange-circled) was etched in the $BCl_3/Cl_2$ atmosphere. The same wet and dry processes were performed until the first insulator appeared, and the byproducts were removed through ashing. The TiN of the first-layer memory and RS layer of the third-layer memory were removed by dry etching. Finally, the remaining $SiO_2$ on the first- and third-layer memory was etched using BOE. Three-layered single V-ReRAM was fabricated to figure out the middle device's state depending on the upper and lower device to distinguish the charge diffusion effect.

The cross-section of the completed V-ReRAM was observed with the field emission scanning electron microscope (FESEM; HITACH, S4800). A-200k kV high-resolution transmission electron microscope (HRTEM; JEOL, JEM F200) was used to verify each layer was well defined. To analyze the materialistic properties of the resistive switching layers, analyses through scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDS) were conducted. The thickness of $HfO_2$ was measured through spectroscopic ellipsometry

(SE; Wollam, ESM-300). Electrical properties were measured using a semiconductor parameter analyzer. (SPA; Hewlett Packard, 4145B) The TE was biased, and the BE was grounded during the measurement.

## 4.3. Results and Discussion

The cross-section image of the completed three-layer V-ReRAM device acquired through HRTEM is shown in Figure 4.2(a). The switching layer $HfO_2$ is more clearly presented in the enlarged image as an inset. A three-layer stack of TiN and $SiO_2$ was hole-etched thoroughly, and a hole was etched down to the first layer of TiN. It can be seen that Pt TE was deposited along with the hole etched structure (dark black region), and $HfO_2$, the resistive switching layer, was deposited beneath the Pt layer. (light gray region) The STEM image of the cross-section is presented in Figure 4.2(b), and the matching EDS results are shown in Figure 4.2(c)-(h). It can be found that each layer was well defined, and the three-layer structure was well fabricated.

Figure 4.3 presents a schematic diagram of the charge migration shown in the 3D VNAND for better comprehension. There is a vertical loss in the WL and BL directions through the tunneling oxide and barrier oxide, and a lateral loss through a shallow trap in the $Si_3N_4$ charge trap layer. To increase the number of stacks for high-density integration, it is essential to reduce the thickness of the interlayer insulating layer between WLs. However, the thickness reduction of the insulating layer causes a decrease in an adjacent cell's threshold voltage (Vth) due to charge migration in the lateral direction, and the degradation in the data retention and the switching reliability issue can occur. The factors inducing such lateral charge loss can be 1) an electric field led by a voltage applied to the adjacent WL and 2) diffusion induced by the concentration gradient of the trapped electrons. Figure 4.4 is the schematic diagram indicating the charge loss direction in the V-ReRAM. As the vertical Pt/HfO2/TiN

memory operation is based on the charge trap/detrap mechanism, the trapped charge can diffuse caused of the concentration gradient.

Before analyzing the charge loss in the lateral direction due to diffusion in 3D V-ReRAM, the effect of one cell to which voltage is applied on the other adjacent cells was analyzed. Figure 4.5(a) is the current-voltage (I-V) curves of the middle device according to the bottom device's state. The black line indicates the middle devices' set when neither the top nor bottom cell was not turned on, which is for comparison. The red line was the set curve when the bottom device was turned on to LRS, and the take-off voltage shifted to the left by Δ1.8 V. The blue line is the switching curve when the bottom was turned back to HRS, and the take-off voltage was about 5 V. The shift still occurred, but the take-off voltage increased comparing the red line. Figure 4.5(b) shows the I-V graphs of the middle device depending on the top device's state. The middle device's take-off voltage shifted with the same tendency as Figure 4.5(a). That is, the inter-cell interference phenomenon can be caused by any adjacent cells depending on their resistance state, and the charge loss can occur in any direction-both top to bottom, and bottom to top, as it is based on the concentration gradient-based diffusion.

Figure 4.5(c) shows the effect of the number of adjacent cells to which voltage is applied in a three-layer device with an insulating film thickness of 50 nm. The solid black line was the HRS and LRS curve when the voltage was applied to the second layer cell. The solid red line is the HRS curve confirmed by applying a voltage to the third layer device to make the LRS state and then applying a voltage to the second

layer device 5 minutes later. Moreover, the solid blue line is the HRS curve confirmed by applying a voltage to the first and third layer devices to make the LRS state and then applying a voltage to the second layer device 5 minutes later. The HRS take-off voltages in the three cases were 7.0 V, 4.2 V, and 3.0 V, respectively, and it can be found that as the number of cells to which the voltage is applied increases, the HRS take-off voltage is pulled in the lower voltage direction. In other words, the effect of field and charge loss by two adjacent cells is greater than that of one adjacent cell.

Figure 4.5(d) is the simulation results showing the number of electrons diffused to the second layer when only the third layer is in the LRS state (solid black line) and when both the first and third layers are in the LRS state (solid red line) as in Figure 4.5(c). As in Figure 4.5(c), it was demonstrated that the number of diffused electrons tends to be larger when there are two adjacent cells than when there is one. In the case of the simulation of Figure 4.5(d), unlike the experimental results where the voltage was applied, the number of electrons is simulated to indicate a relative trend and not an absolute value. In addition, as a result of reflecting only charge diffusion, the charge transfer induced by the field applied by the simulation is not considered here.

To analyze the effect of lateral charge diffusion only among the influences of adjacent cells, the electrical properties were measured in the three-layered single V-ReRAM memory, and the take-off voltage shift over time was compared. In Figure 4.6(a), the second memory cell was set to LRS as a reference. (Solid black line) After 5, 10, 20, and 30 minutes, respectively, a positive voltage bias was applied again and the LRS curve was compared with the reference. The results were marked as purple,

red, blue, and solid green lines, respectively. When the voltage reached the current level 100 pA was compared, the LRS curve shift was Δ0.20 V after 5 minutes, Δ0.25 V after 10 minutes, Δ0.60 V after 20 minutes, and Δ0.65 V after 30 minutes. The shift of the LRS curve in the direction of high voltage means the resistance state gradually increases over time as the electrons diffuse out from the trapped region. In Figure 4.6(b), the second layer device was turned on 5, 10, 20, and 30 minutes after setting the third layer cell, respectively, to compare the shift of the take-off voltage during the set procedure. The solid black line is set the I-V curve of the second-layer cell when both the first and the third-layer cells were in HRS, which is a reference for comparison. Purple, red, blue, and green lines are in that order for 5, 10, 20, and 30 minutes, respectively. After 5 minutes, the take-off voltage of the HRS Curve was 4.7 V, 10 minutes was 4.0 V, 20 minutes was 3.7 V, and 30 minutes was 3.3 V. This reflects the phenomenon in which electrons of the third layer cell in LRS are diffused in the lateral direction, and the take-off voltages of the second-layer device became lower when the set voltage was applied.

Figure 4.7(a) is the LRS data retention measured for 30 minutes in the second-layer cell depending on the resistance states of the first-layer and the third-layer devices. The read voltage was 5 V, and the measurement was conducted in pulse mode. The black squares indicate second-layer data retention when the first-layer and the third-layer devices were in HRS. The LRS current abruptly drops after about 600 seconds. This coincides with the trend of the LRS curves shift over time, presented in Figure 4.6(a), where the shift was Δ0.25 V after 10 minutes and Δ0.60 V after 20 minutes.

The red circles were the LRS retention of the second layer device when the first and the third layer devices were turned on LRS. In this case, the electrons in the first and third layers are trapped and the memories are in LRS, so the diffusion of electrons in the second layer in the lateral direction towards the first and third layers is suppressed. This is the case where the lateral change loss is suppressed, and only a vertical charge loss occurs between the two-layer TiN electrode and the upper electrode Pt. It can be seen that the current level in the retention graph of the black squares is significantly lower than the current level of the retention graph of the red circles. The black squares are the sum of the vertical charge loss and the lateral charge loss, and the red circles are because it can be thought that only vertical charge loss exists. The difference between these two can be considered as a lateral charge loss. In the case of the black squares, the current level in the last minute is about 0.5% compared to the current level in the first minute, and in the case of the red circles, the current level in the last minute is 35.3% compared to the current level in the first minute. It can be seen that the charge loss is quite large. Figure 4.7(b) is the HRS data retention measured in the second layer device depending on the first and the third layer devices' resistance states. Black squares indicate the case when the first and the third layer memories are in HRS for comparison, and the red circles represent the HRS data retention of the second layer cell when the first and the third are turned on. The HRS data retention of the red circles is half an order of magnitude higher than the black squares. That is, the electrons trapped in the first and the third layer memories are diffused to the second layer, which raises the HRS current level higher.

Figure 4.7(c) is a COMSOL simulation result to support the experimental results of Figures 4.6 and 4.7(a)-(b) above. As a result of checking the diffusion degree of electrons over time after the voltage was initially applied and filled with electrons in the third layer, the electron concentration is -3 to +1 ($1x10^{-3}$ to $1x10^{1}$) on the scale on the right of the electron diffusion degree with time after the voltage is initially applied and the electrons are filled in the third layer. After 30 minutes, the electron concentration in the third layer decreased by more than 10 times, and the electron concentration in the second layer increased by about 10 times compared to the initial level, and it can be confirmed that this trend is consistent with the actual experimental results. As mentioned in Figure 4.5(d), the actual results and exact figures may be different because the simulation was conducted only from the point of view of charge diffusion. Figure 4.7(d) is the simulation results of the number of electrons in the second layer memory when the top device was turned on. Depending on the location of the possible conduction path formed at the third layer device, each graph was marked near, normal, and far, indicating -10 nm, 0 nm, and 10 nm, respectively. The inter-cell interference can be influenced by the location of the conduction path formed, which can be another factor degrading the resistance uniformity.

To understand the causes affecting the interference phenomenon, the electrical properties measurement was carried out while changing various factors. In Figure 4.8, the take-off voltage during the set process was compared by adjusting the compliance current ($I_{cc}$) of the memories constituting the three-layer V-ReRAM device to verify the effect of the adjacent cell according to the number of stored electrons. Figure

4.8(a)-(c) is an I-V curve showing HRS and LRS curves in each case of $I_{cc}$ 2 nA, 20 nA, and 200 nA. The set curves of the second layer were compared 5 minutes after applying the voltage to the third layer under each compliance current condition. It can be seen that the higher the $I_{cc}$, the greater the number of stored electrons, so the LRS curves moved to the lower voltage region, and the memory window between the LRS curve and the HRS curve increased. The HRS take-off voltage gradually decreased to 5.7 V when the $I_{cc}$ was 2 nA, 5.0 V with the $I_{cc}$ 20 nA condition, and 4.2 V with the $I_{cc}$ 200 nA. This is more clearly shown in Figure 4.8(d), which compares only HRS curves.

Figure 4.8(e) is the simulation result while adjusting the compliance current to support the previous result. As shown in the experimental results, it shows the amount of diffusion when there is a 10-fold difference in the amount of electrons in the adjacent device that is in the LRS. As in the experiment, when the amount of diffused electrons was checked on a 5-minute basis, the greater the initial electron quantity, the greater the number of diffused electrons. Although this tends to be consistent with the experimental results, it has been mentioned earlier that specific values cannot be identified.

In Figure 4.9, I-V curves were compared by adjusting the stage temperature during device measurement to verify the effect of adjacent cells according to temperature. Figure 4.9(a)-(c) are I-V curves of the HRS and LRS curves during the set process in each case of temperature conditions 25℃, 55℃, and 85℃. The HRS current before take-off and the LRS current increased with increasing temperature. This is because

the electrons move more easily as the energy of the electrons increases during operation according to voltage application, and the current level increases. Figure 4.9(d) shows the HRS curve of the second layer device 5 minutes after voltage application of the third layer cell under each temperature condition. The HRS take-off voltage was lower at 55℃ and 85℃ compared to 25℃, with the voltage shift of 4.1 V at 25℃, 3.0 V at 55℃, and 3.0 V at 85℃.

From 55℃ to 85℃, the take-off voltage of the interference HRS curve did not decrease. However, looking at Figure 4.9(d), which compares only the interference HRS curves under each temperature condition, it can be seen that the current level of the interference HRS curve under the 85℃ condition rapidly increases from about 4.3 V, indicating that electron movement is much more active. Through this, it can be seen that as the temperature increases, the electron movement becomes more active, and the lateral diffusion of electrons pulled from the adjacent cell to which the voltage is applied also becomes more active. Figure 4.9(e) shows the amount of electrons diffusing from adjacent devices that have become LRS according to the temperature as shown in the experimental results as a result of simulation while controlling the diffusion of electrons according to temperature to support the above results. As in the experiment, when the amount of electrons that have been diffused over 5 minutes was verified, the number of electrons diffused at the same time increases. Although this tends to be consistent with the experimental results, it has been mentioned earlier that specific values cannot be identified.

In Figure 4.10, the interference phenomenon was observed depending on the

thickness of the insulating film between adjacent cells. When the interlayer insulating film thickness was 30 nm, 50 nm, and 100 nm, a three-layer device was fabricated, and the I-V curve was verified. The solid black line in the graph is the HRS and LRS curves that appear when voltage is applied to the second layer device, and the solid red line is the HRS curve confirmed by applying a voltage to the second layer device in 5 minutes after applying a voltage to the third layer device to make the LRS state. In Figure 4.10(a) which is in the case of the device with an insulating film thickness of 30 nm, the HRS curve of the solid red line increases at about 3.0 V, whereas the device with an insulating film thickness of 50 nm (Figure 4.10(b)) has an interference HRS take-off at about 4.2 V voltage. It can be seen that the interference HRS curve in the 30 nm insulating film device is pulled in the lower voltage direction because the distance between the cell and the cell becomes closer due to the decrease in the insulating film thickness, which is greatly affected by the applied voltage and the lateral direction charge transfer is easier. In a V-ReRAM second-layer device with an insulating film thickness of 100 nm, the HRS and LRS curve (solid black line) of the first layer and the interference HRS curve (solid red line) of the first layer was observed, which is presented in Figure 4.10(c). The take-off voltage of the interference HRS curve does not change from that of the conventional HRS, unlike the previously shown three-layer V-ReRAM device with an insulating film of 50 nm. When the thickness of the interlayer insulating film is increased from 50 nm to 100 nm, the electron movement distance in the lateral direction is increased, and the effect of the field is reduced. Therefore, it is conceivable to increase the thickness of the interlayer insulating film, which is the simplest method, as an improvement measure

for suppressing the influence of adjacent cells to which voltage is applied in the V-ReRAM. However, after 30 minutes, the HRS curve shifts, which means that although the thickness of the insulating film increases, the movement of electrons cannot be suppressed. (Figure 4.10(d)) In addition, increasing the thickness of the insulating film is disadvantageous in terms of density. Therefore, to suppress the electron movement in the lateral direction in the V-ReRAM, it is necessary to additionally consider the structure and the materials.

To suppress the lateral charge loss, the recess structure shown in Figure 4.11 is suggested. This is a method to lengthen the lateral charge diffusion path by recessing the insulating interlayer oxide to increase the physical distance through which electrons diffuse. In this method, the electron transfer distance can be increased without increasing the thickness of the interlayer insulating film, thereby increasing the time affected by the adjacent cells. In addition, if the recess structure pushed inward is filled with oxide deposited by ALD, it is possible to suppress the phenomenon that electrons filled in adjacent cells are affected by the field. By applying this structure, it is expected that the influence of adjacent cell interference due to lateral charge diffusion of V-ReRAM can be suppressed.

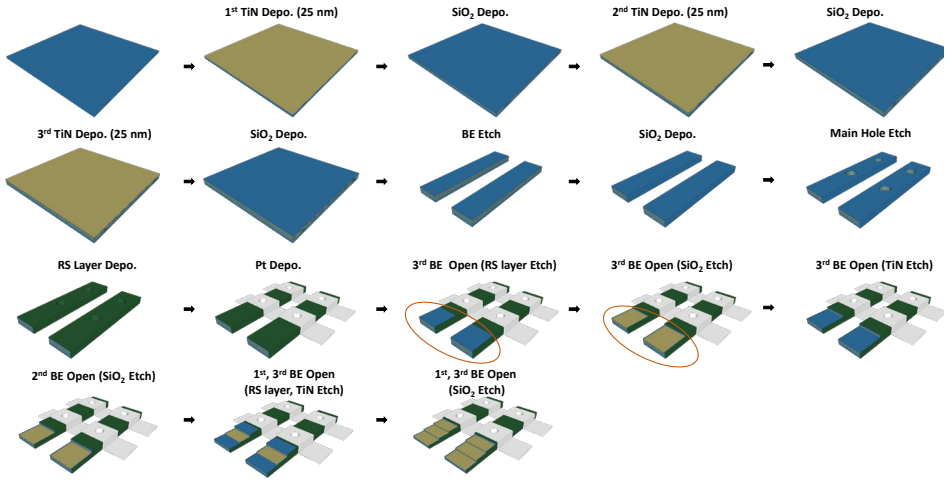


Figure 4.1 Schematic diagrams of the vertical ReRAM with 3-layers.

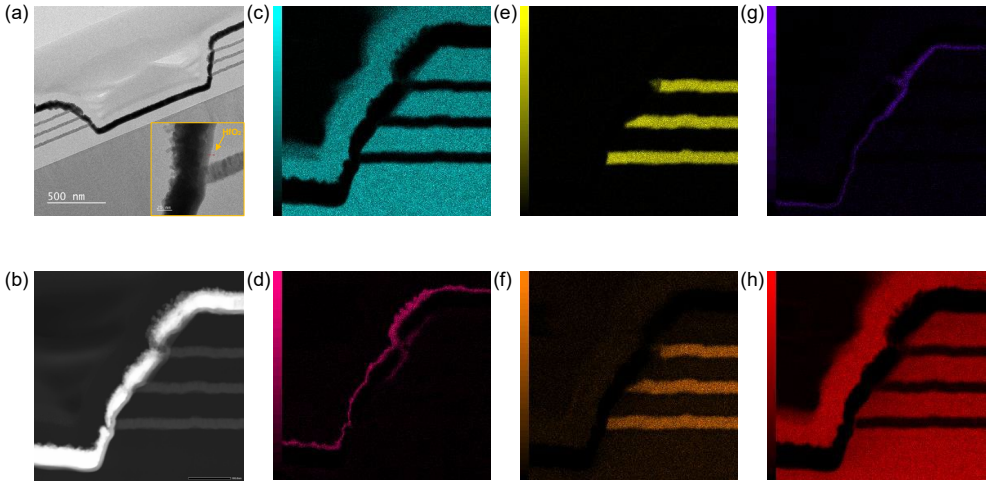


Figure 4.2 Cross-sectional images of the V-ReRAM with 3-layers observed through (a) HRTEM, (b) STEM HAADF image of the V-ReRAM, and the matching EDS mapping results of (c) Si, (d) Pt, (e) Ti, (f) N, (g) Hf, (h) O.

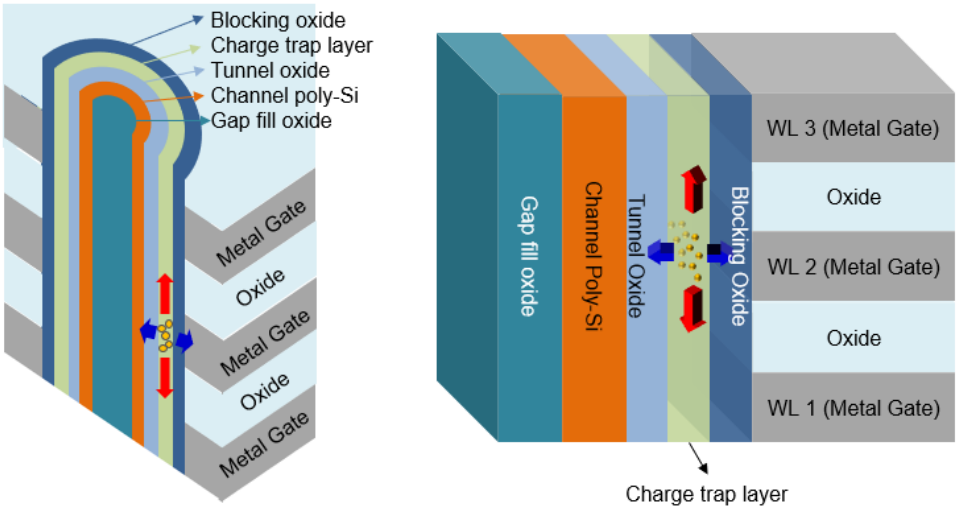


Figure 4.3 Schematic diagrams of the charge migration in V-NAND.

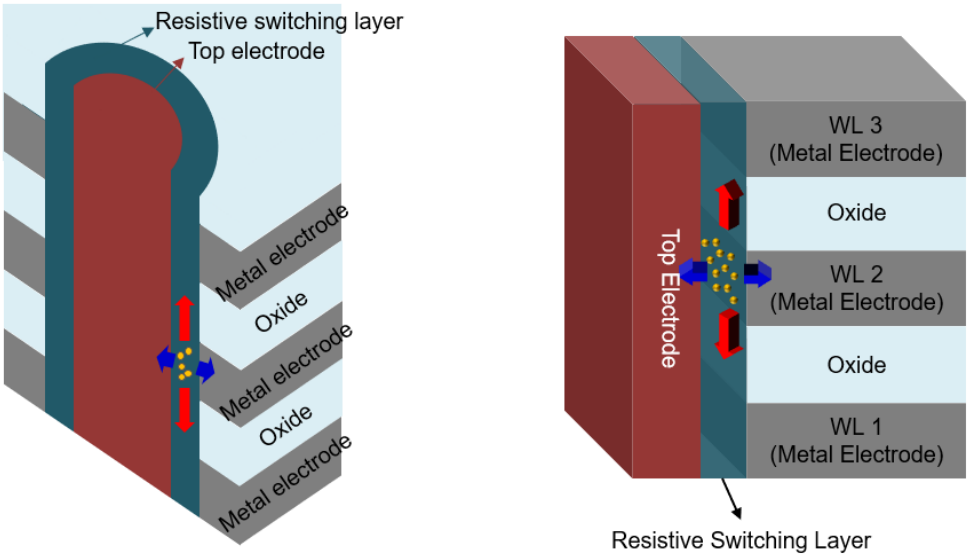


Figure 4.4 Schematic diagrams of the charge migration in V-ReRAM.

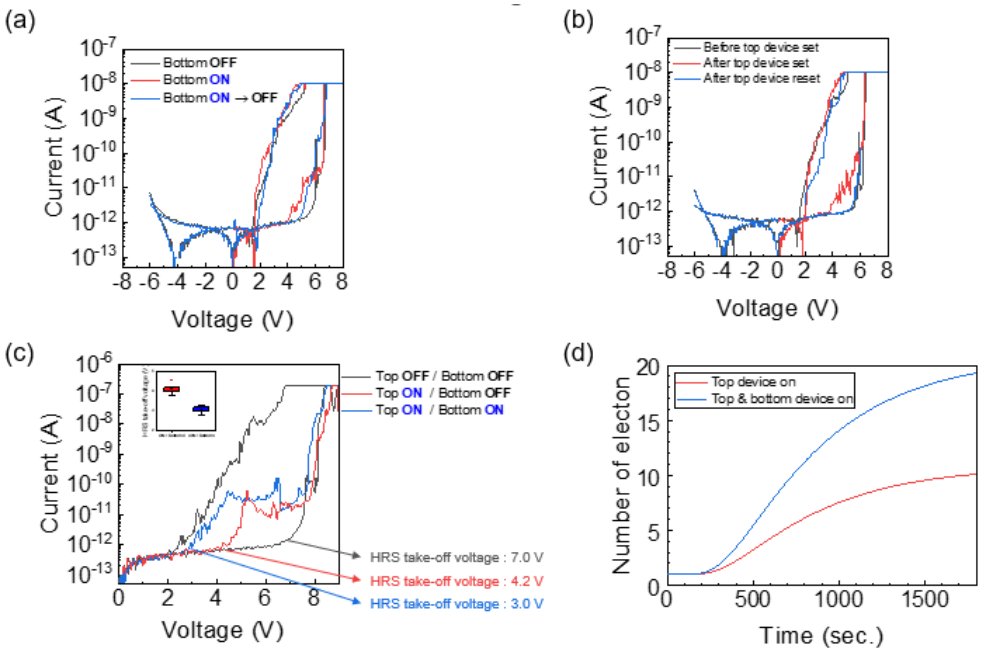


Figure 4.5 (a) I-V curves of the middle device according to the bottom device's state, (b) I-V graphs of the middle device depending on the top device's state, (c) DC IV curve comparison between only top device set and both top/bottom device set, Inset: statically processed HRS take-off voltage measured on the different devices, (d) Simulation results of the electron concentration in the middle device depending on the top & bottom devices' state.

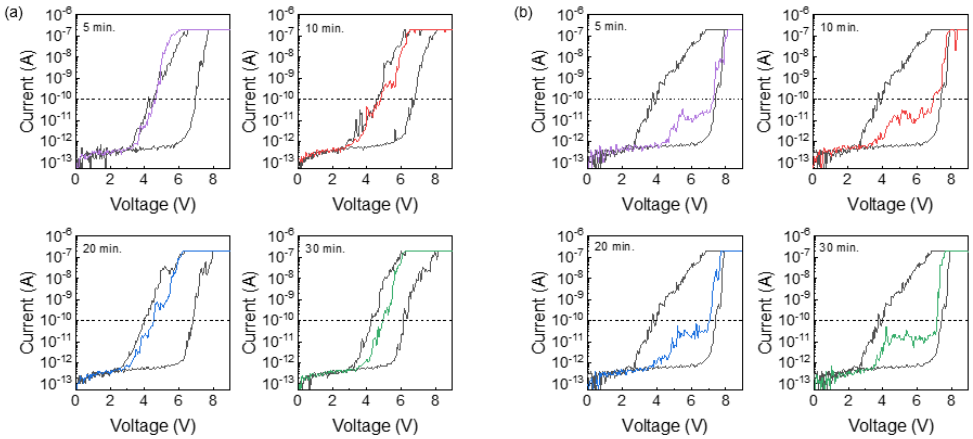


Figure 4.6 DC IV curve shift and retention of middle device in 3 stairs V-ReRAM : (a) LRS curve shift by time variation, (b) HRS curve shift after top device set by time variation.

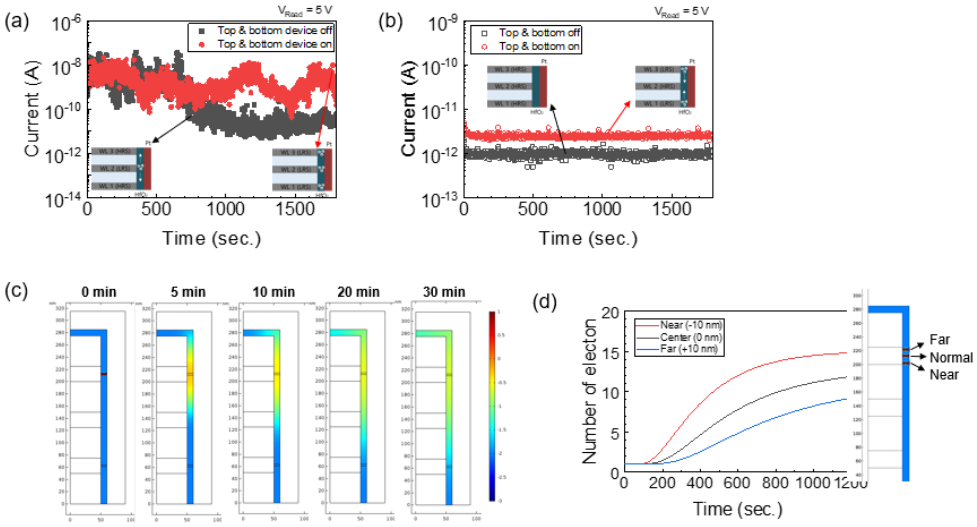


Figure 4.7 (a) LRS retention depending on the top & bottom devices' state, (b) HRS retention depending on the top & bottom devices' states, (c) simulation results of the electron concentration according to the time variation after top device set, (c) Simulation results of electron concentration by time variation after top device, (d) Simulation result: Middle device electron concentration comparison between 3 cases of conducting path formed at top device.

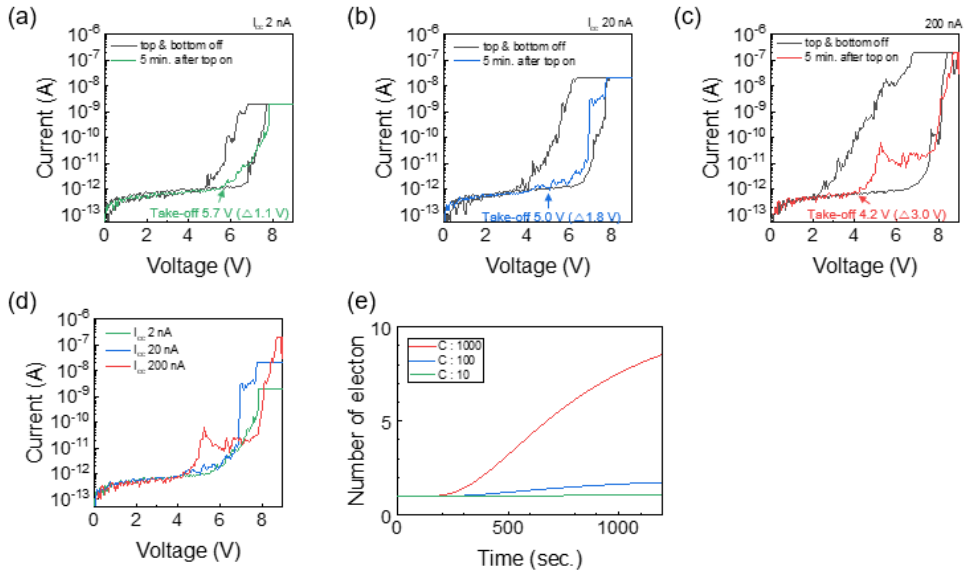


Figure 4.8 Interference phenomenon depending on the compliance current: (a) DC IV curves of the middle device with top & bottom devices off (black lined) and the HRS curves of the mi with (a) $I_{cc}$ 2 nA, (b) 20 nA, and (c) 200 nA, (d) Shifted HRS curves after 5 minutes for various compliance current, (e) Simulation result: Middle device electron concentration comparison between various compliance current.

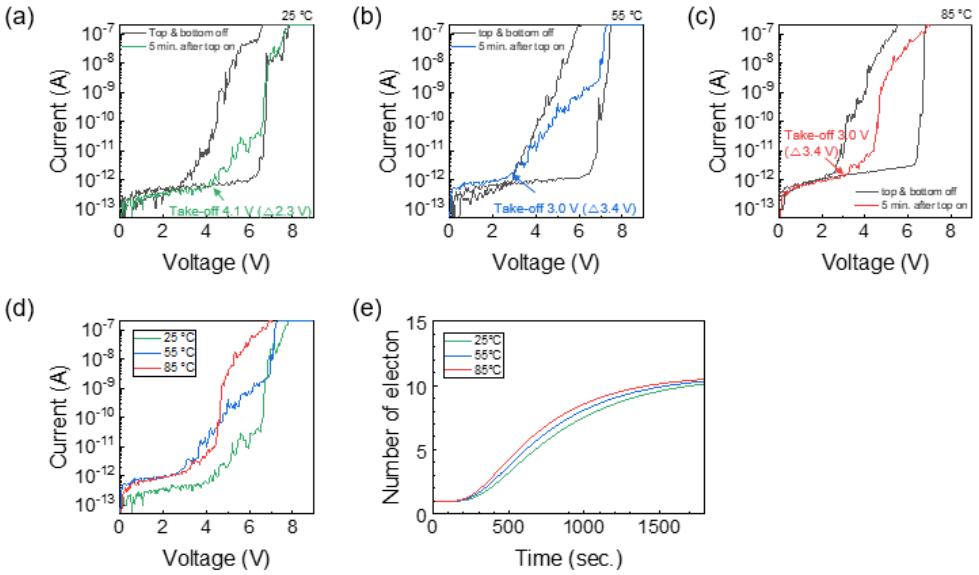


Figure 4.9 Interference phenomenon depending on the temperature: DC I-V curves of the middle device with top & bottom devices off (black lined) and the HRS curves of the mi with (a) 25℃, (b) 55℃, and (c) 85℃ (d) Shifted HRS curves after 5 minutes for various temperature, (e) Simulation result: Middle device electron concentration comparison between various temperature.

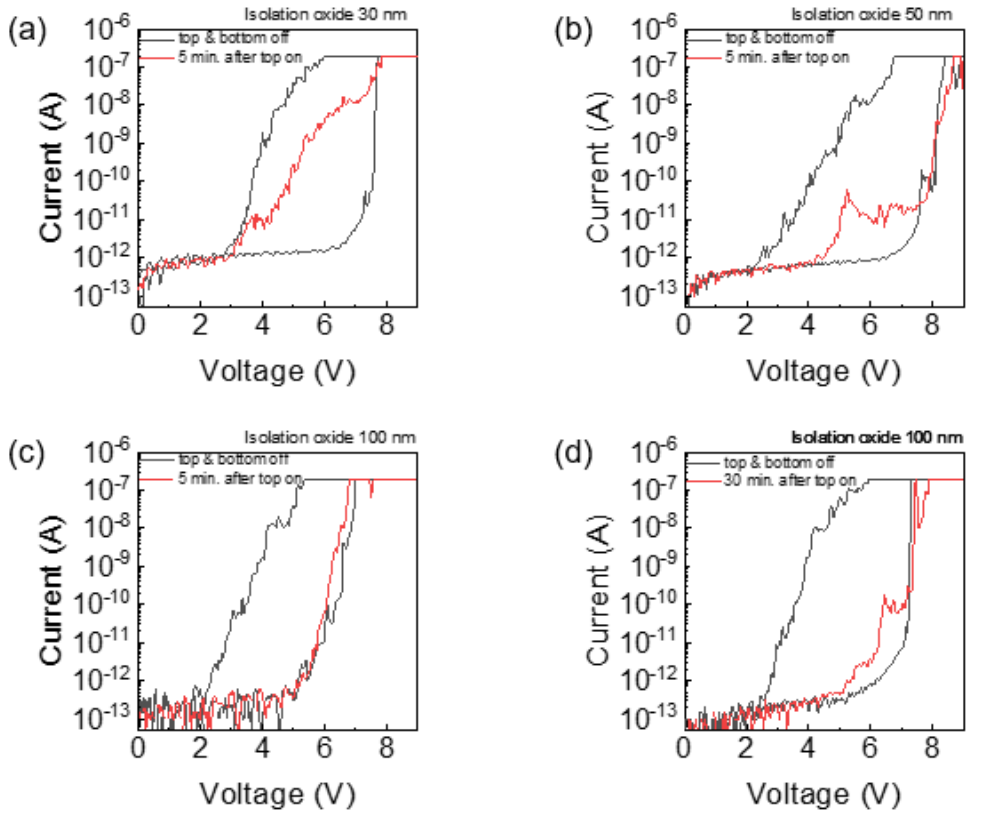


Figure 4.10 DC I-V curves with isolation oxide thickness of (a) 30 nm, (b) 50 nm, (c) 100 nm after 5 minutes, and (d) 100 nm after 30 minutes. (Black lines: middle device with top/bottom in HRS, Red lines: middle device with top device in LRS).

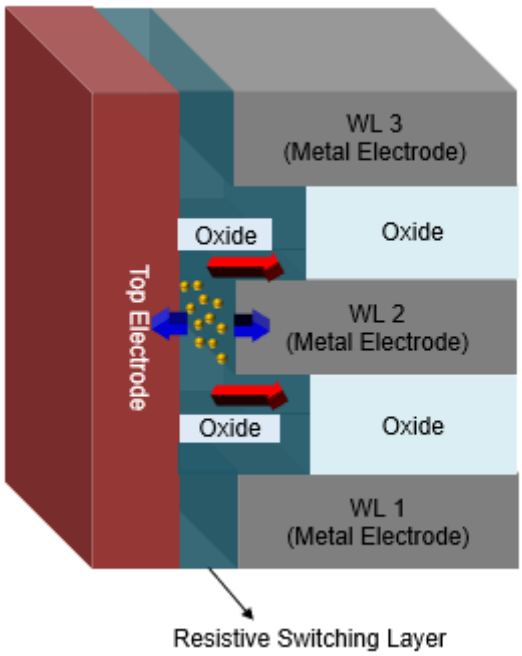


Figure 4.11 Suggesting model for the interference suppression: isolation oxide recess structure.

## 4.4. Summary

In the charge trap/detrap method V-ReRAM, vertically stacked memories share the layer in which the data is stored, that is, the resistance change layer. Thus, the inter-cell interference phenomenon, similar to the lateral charge loss of VNAND, can also be observed in V-ReRAM. The electrical characteristics are affected by the resistance states of the adjacent cells, which degrades the switching uniformity. Also, the memory window may be lowered. Therefore, it is important to understand the lateral charge loss phenomenon and identify its factors. The lateral charge loss according to the resistance state, time, temperature, $I_{cc}$, and insulating film thickness of adjacent cells was observed through electrical characteristics measurement in this work. Furthermore, the diffusion of electrons, which can explain these characteristics, was demonstrated through simulation. Moreover, a V-ReRAM structure that can alleviate such interference was proposed. The diffusion of charges will be lowered, and the interference phenomenon will be suppressed by adopting this structure. The improved lateral charge loss and the suppressed inter-cell interference phenomenon will be reported in our next publication, which is under work. As this is the first time such a phenomenon has been observed and analyzed, this paper will help the community to improve the understanding of the inter-cell interference phenomenon led by the lateral charge diffusion in the charge-based V-ReRAM.

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Technol., 2016.

[10] F. Wang, J. Wu, Y. Li, R. Cao, J. Chen, Appl. Phys. Express 2020, 13, 044001.

# 5. Conclusion

This dissertation examined resistive switching based on the electronic mechanism, and vertical 3D Re-RAM with 9x9 2 layer was fabricated. An RS layer with self-rectification characteristics for V-ReRAM was selected and the electrical characteristics such as DV-IC, retention, and endurance were evaluated. For the V-ReRAM array, Al doping improved HRS variation, and BNN application was performed. However, since it has the same structure as V-NAND, the interference effect reported in V-NAND was also shown in V-ReRAM.

In Chapter 2, The electrical properties of HO, AHO, and AHT crosspoint devices were evaluated to find an appropriate switching layer to apply to the V-ReRAM array. AHT device showed the highest F/R ratio and on/off ratio, and a wide and clear switching window was obtained through DC voltage sweep measurement. P-F fitting was performed to analyze the switching mechanism, and since the deepest trap depth was obtained in the AHT device, it is presumed to be the cause of the improvement of switching uniformity and stability. Deeper trap formation through Al doping and intercalation of the blocking layer $Ta_2O_5$ led to high switching uniformity and stability in the AHT device. Based on the measurement results, a Pt/$Ta_2O_5$/$HfO_2$/TiN stack was selected for the V-ReRAM application.

In Chapter 3, A 9×9×2 AHT V-ReRAM array was fabricated. At an operating current of 10 nA, a maximum on/off ratio of 103 was achieved, which is very low power consumption. The rectification capability of the AHT V-ReRAM has proven to be the worst-case off-current reading in a 4×4×2 array with an excellent F/R ratio.

The high storage capacity of AHT V-ReRAM makes it particularly suitable for training BNNs that require more inputs and outputs than other neural networks. Image classification for 30 input images was performed using the ensemble method, and an average accuracy of 98.23% could be achieved. It is expected that higher accuracy can be achieved by increasing the array size and improving LRS uniformity.

In Chapter 4, Cell-to-cell interference similar to the lateral charge loss of VNAND was observed in V-ReRAM. Electrical characteristics were affected by the resistance state of adjacent cells, which reduces the switching uniformity. It was confirmed that the lateral charge loss occurred according to the resistance state, time, temperature, Icc, and the thickness of the insulating film of the adjacent cell through electrical characteristic measurement. A V-ReRAM structure capable of mitigating such interference has been proposed, and it is expected that the diffusion of charges will be lowered, and the interference will be suppressed.

Considering the packaging thickness, the maximum allowable layer of V-NAND is 400 layers, which is expected to reach by 2026. Therefore, for further stacking, it is necessary to reduce the thickness of the interlayer insulating layer and use a word line material with low resistance. In addition, intensive research on next-generation memory to replace V-NAND is required. Although the LRS variation should be improved, the 9x9 two-layer array of this study shows the possibility of V-ReRAM as a memory. Research on V-ReRAM with a larger array and multi-level operation is needed to achieve higher density. Finally, structural improvement and research on RS layer materials to reduce the interference effect should be conducted.

# 6. Curriculum Vitae

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## I. Education

| | |
|---|---|
| 1998.3 – 2005.2 | B.S.<br>Department of Chemical Engineering<br>Dankook University, Seoul, Korea |
| 2005.3 – 2007.2 | M.S.<br>Department of Chemical and Biological Engineering<br>Seoul National University, Seoul, Korea |

## II. Work Experience

| | |
|---|---|
| 2007.2 – Present | Process architecture engineer<br>Device Solutions, Samsung Electronics,<br>Gyeonggi-do, Republic of Korea |

- Process development for DRAM capacitor and transistor

→ Design rule D46 ~ D18 development (capacitor and transistor)

## III. Research Areas

### 1. Vertical ReRAM device fabrication

- ALD Thin film deposition for vertical ReRAM devices
- Fabrication process set-up

### 2. Analysis of mechanism studies of Resistive switching

- Electrical analysis through DC sweep and pulse measurements
- Chemical analysis through spectroscopies

## IV. Experimental Skills

### 1. Deposition methods

- Atomic layer deposition for resistive switching materials ($HfO_2$, $Ta_2O_5$)
- DC & RF magnetron sputtering (Pt, TiN)
- E-beam evaporation (Pt, Ti)
- Handling and maintenance of high vacuum equipment

### 2. Annealing methods

- Rapid thermal process

- Furnace

**3. Analysis methods**

- X-ray Diffractometer (PANalytical, X'Pert PRO MPD) for measurement of X-ray diffraction, X-ray reflection
- Spectroscopic Ellipsometer (SE, J.A. Woollam, M-2000) for analysis of optical properties and thicknesses of thin films
- Four point probe for resistivity measurement of metals and conducting materials
- Pulse/pattern generator (Agilent, 81110A/ Tectronix, AFG3101C) and digital oscilloscope for pulse switching measurement
- HP4145B and HP4155B for I-V measurement
- Characterizing thin films by XPS, AES, SEM, TEM

# 7. List of publications

## 1. Refereed Journal Articles (SCI)

### 1.1 Domestic

### 1.2. International

1. **Seung Soo Kim**, Soo Kyeom Yong, Whayoung Kim, Sukin Kang, Hyeon Woo Park, Kyung Jean Yoon, Dong Sun Sheen, Seho Lee, and Cheol Seong Hwang, Review of Semiconductor Flash Memory Devices for Material and Process Issues, Advanced Materials, 2200659 (2022)

2. Yumin Kim, Jihun Kim, **Seung Soo Kim**, Young Jae Kwon, Gil Seop Kim, Jeong Woo Jeon, Dae Eun Kwon, Jung Ho Yoon, and Cheol Seong Hwang, Kernel Application of the Stacked Crossbar Array Composed of Self-Rectifying Resistive Switching Memory for Convolutional Neural Networks, Advanced Intelligent Systems, 1, 7, 1900116 (2019)

3. Bo Wen Wang, **Seung Soo Kim**, Haewon Song, Haengha Seo, Xiangyuan Li, Jin Myung Choi, Jinwoo Choi, Jonghoon Shin, and Cheol Seong Hwang, Improving the water-resistance of MgO-based metal-insulator-metal capacitors by inserting a BeO thin film grown via atomic layer deposition, J. Mater. Chem. C, 2022, Advance Article (2022)

4. Bo Wen Wang, Jinwoo Choi, Hyoung Gyun Kim, Seung Dam Hyun, Chanyoung Yoo, **Seung Soo Kim**, Hoin Lee, and Cheol Seong Hwang, Influences of oxygen source and substrate temperature on the unusual growth mechanism of atomic layer deposited magnesium oxide using bis(cyclopentadienyl)magnesium precursor, Journal of Materials Chemistry C, 2021, 9, 15359-15374

## 2. CONFERENCES

### 1.1 Domestic

1. Yumin Kim, Jihun Kim, **Seung Soo Kim,** Young Jae Kwon, Gil Seop Kim, Jeong Woo Jeon, Dae Eun Kwon, Jung Ho Yoon, and Cheol Seong Hwang "Kernel Application of the Stacked Crossbar Array Composed of Self-Rectifying Resistive Switching Memory for Convolutional Neural Network", 제27회 한국반도체학술대회, 강원도하이원리조트, 2020년 2월 12일-14일, Poster

### 2.2 International

# 8. Abstract (in Korean)

## 다양한 어플리케이션을 위한 삼차원 구조의 수직 저항변화 메모리 소자

4차 산업 혁명의 시작과 함께 정보통신기술 (ICT)을 기반으로 하는 수많은 데이터가 만들어지고 있다. 2025년에는 175 제타바이트 수준의 데이터가 창출될 것으로 예상된다. 이러한 데이터의 저장은 NAND flash memory가 주로 담당하고 있으며, 현재 양산되는 제품은 176단 3D V-NAND이다. 그러나 패키지된 칩의 허용 두께가 30 μm 수준이며, 이는 패키징 두께 15 μm를 제외하면 V-NAND는 최대 400 단 정도로 예상된다. V-NAND의 기술 로드맵에 따르면 400단은 2026년에 개발될 것이며, 집적도 향상에 어려움이 존재할 것이다. V-NAND를 대체하기 위한 차세대 메모리의 연구가 이루어지고 있으며, 본 논문에서는 저항변화 특성을 활용한 ReRAM에 대하여 설명할 것이다.

1971년 멤리스터의 개념이 소개되었고, 2008년 휴렛팩커드(HP) 사에서 개발을 시작한 이후, 많은 연구가 지속적으로 진행되고 있다. 초기에는 메모리 소자의 활용을 연구가 주를 이루었으나, 최근에는 뉴로모픽 컴퓨팅, 생체호환성 메모리 소자와 웨어러블 기기 등과 같은 다양한 분야에서 연구가 진행되고 있다. 저항변화 메모리는 금속/절연막/금속의 간단한 구조에서 동작되기 때문에 크로스바 형태의 $4F^2$ 어레이 구조로 제

작이 가능하다. 여기서 F는 구현 가능한 최소 선폭을 나타낸다. DRAM, NAND, NOR 플래시메모리는 각각 $6F^2$, $5F^2$, $10F^2$의 단위 셀 크기에 비하면 집적도 측면에서 유리하다. 또한 저항변화 소자를 삼차원 수직 구조(V-ReRAM)로 제작한다면 V-NAND 공정과 호환성이 우수하며, V-NAND 동작 전압20V 보다 낮은 전압에서 동작하므로 간섭 효과를 줄일 수 있다. 이는 수직 방향으로 더 높은 단수 제품을 제작할 수 있는 효과가 있다. 또한 V-NAND의 채널홀은 Si 기판 영역과 접촉을 위하여 그 크기가 일정 수준 이상이 되어야 하지만, V-ReRAM은 word line과 bit line간 전압차만 존재하면 되기때문에 채널홀의 크기를 V-NAND보다 줄일 수 있으며, 이는 수평 방향 집적도 향상에 도움이 된다.

그러나 저항변화 소자를 어레이로 제작하기 위해서는 인접 셀을 통해 흐르는 sneak 전류가 억제되어야 한다. 이는 셀렉터를 활용하거나 자가 정류 특성을 이용하여 억제할 수 있다. 셀렉터를 활용하기 위해서는 저항변화층과 셀렉터 사이에 중간 전극이 필요하지만, V-ReRAM은 중간 전극을 모든 셀들이 공유하기 때문에 셀렉터를 활용한 sneak 전류 억제가 불가능하다. 따라서 자가 정류 특성을 갖는 저항변화층을 활용하여 V-ReRAM을 제작하여야 한다. 본 논문에서는 1) V-ReRAM에 적용할 자가 정류 특성을 갖는 저항변화층의 선정, 2) V-ReRAM 소자의 제작 및 어플리케이션 적용, 3) V-ReRAM의 전하 손실에 의한 영향에 대하여 설명할 것이다.

자가 정류 특성을 갖는 저항변화층을 선정하기 위하여 크로스포인트 소자를 만들었다. 대표적인 자가 정류 박막은 $HfO_2$이며, 이는 전자의 산소 공공 (oxygen vacancy)으로의 trap과 detrap에 의한 전기적 스위칭 매카니즘을 갖는다. 저항변화층에 유입된 전자는 trap site를 채우기 시작하고, 모든 trap site가 채워지면 저항이 낮은 LRS 상태 (SET)로 변하게 된다. 반대의 전압 조건에서는 trap된 전자들은 detrap 되지만, 상부전극의 높은 일함수 (work function)에 의하여 전자의 유입은 차단되어 저항이 높은 HRS 상태 (Reset)로 돌아가게 된다. 따라서 자가 정류 특성을 가질 수 있다. 그러나 소자의 set 동작 전압이 +8V, reset 동작 전압이 -8v 수준으로 높기 때문에 양의 전하를 갖는 산소 공공은 전계에 의하여 이동하게 된다. 이로 인하여 산소 공공의 재배열이 이루어지고, 전류의 통로 (current path) 또한 모든 동작과장에서 변하게 되며 산포를 유발한다. 이를 개선하고자 $HfO_2$ 박막에 Al을 도핑하였으며, Al 주위에 생긴 공공은 더 깊은 trap depth를 나타냈으며, 도핑된 Al에 의해 산소 공공의 움직임도 억제되었다. 이동이 억제된 deeper trap에 의해 HRS 산포는 85% 개선되었다. 또한 $HfO_2$ 기반의 저항변화 소자의 읽기 전압 마진 ($V_{read}$ margin)은 1.5V 수준으로 소자의 산포를 고려하면 더 넓은 마진이 필요하며, 이는 $Ta_2O_5$ 박막을 추가하여 $HfO_2$에 걸리는 전계를 완화하여 HRS를 shift 시킴으로써 개선할 수 있다. 이를 기반으로 V-ReRAM에 적용할 박막으로 Al 도핑된 $HfO_2$와 $Ta_2O_5$의 이중막을 선정하

였다.

수직 구조의 V-ReRAM은 2층으로 이루어졌으며, V-NAND와 동일하게 hole 타입으로 제작되었다. Hole의 지름은 1 μm이고, word line으로 사용하는 TiN은 40 nm의 두께이며, 동작 면적은 0.1256 $\mu m^2$이다. 앞에서 선정한 자가 정류 박막을 V-ReRAM에 적용하여 크로스바와 동일한 DC IV 특성을 얻었다. 수직 구조의 ReRAM에서 동작 가능한 최소 면적을 확인하기 위하여 word line의 두께를 3 nm로 증착하였으며, hole의 지름은 500 nm로 최소화하여, 현재 양산중인 V-NAND 제품의 동작면적 (0.0071 $\mu m^2$)보다 작은 면적 (0.0047 $\mu m^2$)에서 정상 동작을 확인하였다. 또한 4x4 2층 어레이 32개 셀에서 선택한 셀만 고저항 상태 (HRS)로 두고 나머지 셀 (31개 셀)은 모두 저저항 상태 (LRS)인 최악의 시나리오 (worst scenario) 조건에서 sneak 전류의 방해 없이 선택된 셀의 HRS 상태를 읽을 수 있었다. 이는 제작된 소자의 자가 정류 특성이 우수함을 입증하는 것이다. 어레이를 더 확장하여 9x9 2층 구조의 소자를 제작하였으며, 각 셀의 DC IV를 측정하여 정상 작동하는 것을 확인하였다. V-ReRAM 9x9 2층 어레이를 Binary neural network(BNN) 어플리캐이션에 적용하였다. 'L', 'I', 그리고 'X'에 속하는 3x3 30장의 이미지를 분류하는 BNN을 training 후, V-ReRAM array에 옮겨넣는 off-chip training을 구상하였다. 그 결과 평균 98.23%의 정확도를 얻을 수 있었으며, 더 큰 어레이로 확장하면 결과는 더 올라갈 것으로 예상한다.

V-ReRAM은 V-NAND의 charge trap layer와 동일하게 저항 변화층을 수직 방향으로 모든 셀들이 공유하는 구조를 갖고 있다. 따라서 V-NAND의 고질적인 문제인 전하 손실 (charge loss)에 의한 데이터 왜곡 현상이 V-ReRAM에서도 동일하게 나타나며, 이를 확인하기 위하여 3층 구조의 V-ReRAM 소자를 제작하였다. 간섭효과라 불리는 이 현상은, LRS 상태의 trap된 전자가 확산에 의하여 HRS 상태인 인접 셀로 이동하여 HRS 상태의 인접 셀을 LRS 방향으로 shift 시킨다. 결국 HRS 상태의 셀은 HRS와 LRS의 중간 상태로 변하게 된다. 또한 3층 소자 중, 1층과 3층을 LRS 상태로 만들면, 2층의 간섭 효과를 더욱 커지게 된다. 이는 LRS 상태의 두 인접 셀 사이에 존재하는 HRS의 경우, 저장된 정보의 왜곡이 심해지는 것을 의미한다. 이러한 간섭 현상은 메모리의 retention 특성을 열화 시킬 수 있다. 이를 개선하기 위하여 층간 절연막의 물리적 거리를 증가시켰으나, 이는 집적도를 감소시키는 방향이다. 따라서 동일한 층간 절연막 두께에서 층간 절연막을 wet etch를 통하여 recess 시켜 전자의 이동 거리를 증가시키는 구조와, TiN 전극을 recess 시킨 후 저항 변화층을 증착한 후 recess된 영역에 증착된 저항 변화층을 제외하고 etch하여 격리시키는 구조를 평가 중에 있다. 또한 전자의 확산을 억제할 수 있는 charge loss에 우수한 특성을 갖는 저항 변화층 연구가 필요하다.

본 논문은 9x9 2층 어레이 구조를 갖는 V-ReRAM 소자를 제작하여 메모리로 사용 가능성 확인하였고, V-NAND 보다 작은 면적에서도 동작하는 소자를 제작하여 고집적화에 대한 가능성을 제시하였다.

**핵심어**: 저항변화메모리, 수직 소자, 멤리스터, 자가정류, 산포 개선, $HfO_2$, $Ta_2O_5$

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