Master's Thesis

Design of All-Digital Phase-Locked Loop with Supply Noise-Insensitive Ring Oscillator

전원 잡음에 둔감한 고리 발진기와

디지털 위상 동기 회로 설계

by

Kyungmin Baek

February, 2023

Department of Electrical and Computer Engineering
College of Engineering
Seoul National University

Design of All-Digital Phase-Locked Loop with Supply Noise-Insensitive Ring Oscillator

지도 교수 정 덕 균

이 논문을 공학석사 학위논문으로 제출함
2023 년 2 월

서울대학교 대학원
전기·정보공학부
백 경 민

백경민의 석사 학위논문을 인준함
2023 년 2 월

위 원 장 최 우석 (인)

부위원장 정 덕균 (인)

위 원 이 우근 (인)

Design of All-Digital Phase-Locked Loop with Supply Noise-Insensitive Ring Oscillator

by

Kyungmin Baek

A Thesis Submitted to the Department of
Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for the Degree of
Master of Science
at
SEOUL NATIONAL UNIVERSITY

February, 2023

Committee in Charge:

Professor Woo-seok Choi, Chairman

Professor Deog-Kyoon Jeong, Vice-Chairman

Professor Woogeun Rhee

Abstract

One of the critical blocks integrated into the PAM4-binary bridge, bridging the high-speed DRAM and the low-speed DRAM Tester, is an All-Digital Phase-Locked Loop (ADPLL). Since the transmitter and receiver operate based on the clock signal, whose frequency is doubled compared to the clock signal transmitted from the memory tester by the ADPLL, the ADPLL needs to have a low RMS jitter and high Process-Voltage-Temperature (PVT) tolerance characteristics. However, due to the complex bridge circuit sharing the supply power with the ADPLL, power supply noise (PSN) is the main challenge for the Ring Oscillator (RO) based ADPLL.

This thesis presents a Supply Noise-Insensitive RO-based ADPLL. A supply noise absorbing shunt regulator composed of 31-bit NMOS transistors Array is embedded parallel to the RO. Output codes from the Digital Loop Filter (DLF) not only control the Digitally-Controlled Resistor (DCR) but also the transconductance of the NMOS transistor Array.

The proposed ADPLL is fabricated in the 40-nm CMOS technology. The ADPLL occupies an active area of 0.06 mm^2 and consumes power 13.5 mW, while the proposed scheme only takes 6.6% and 2.8% of it, respectively. At 8 GHz operation, the proposed ADPLL achieves an RMS jitter of 3.255 ps with 1-MHz 40-mVpp sinusoidal noise injected into the supply voltage. With the Supply Noise-Insensitive technique, the RMS jitter lowers to 1.268 ps.

Keywords : All-Digital Phase-Locked Loop (ADPLL), Power Supply Noise (PSN), Ring Oscillator (RO), Supply Noise-Insensitive.

Student Number : 2021-21172

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

Recently, some next-generation dynamic random access memory (DRAM) like Post-DDR5 or LPDDR7 operates at much more higher speed than the past. Moreover, even multi-level signaling such as PAM4 has been discussed for DRAM to overcome the speed limit with the existing binary NRZ data transmitting methods. Although multi-level signaling interface DRAM is under development like this, the testing device for DRAM operation, an automatic test equipment (ATE) still operates at low-speed binary mode lacking a high-speed multi-level communicating. Rather than replacing the old ATE to latest one, other solutions like built-out self test (BOST) [1] or PAM4-binary bridge [2] are invented for cost reduction. One of the solution, the PAM4-binary bridge translates 4 GHz clock and 8 Gb/s NRZ testable data rate to 8 GHz clock and 32 Gb/s PAM4 testable data rate respectively. Figure 1.1 shows the brief

description of the PAM4-binary bridge operation [2].

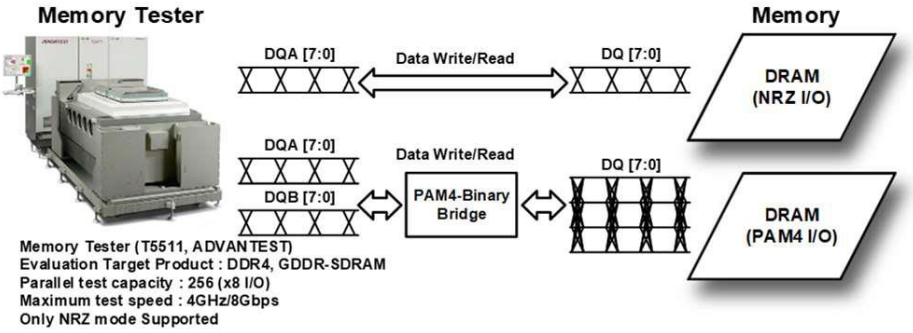


Fig. 1.1 Memory test environment and PAM4-binary bridge operation.

An All-Digital Phase-Locked Loop (ADPLL) is a key circuit embedded in PAM4-binary bridge that doubles the clock frequency received from the ATE and sends it to the next-generation DRAM. As the complex blocks like the transmitter and receiver in PAM4-binary bridge operates based on the output clock signal from the ADPLL, accurate clock generation is the most essential problem. Moreover, multiple phase generation and wide output frequency range are required for Clock and Data Recovery (CDR) in PAM4-binary bridge and ATE operation respectively. To make up with all these conditions, an ADPLL based on a Ring Oscillator is chosen rather than a analog PLL with a LC Oscillator.

Although having advantages of small area, multiple phase generation, and wide output frequency range, a Ring Oscillator has a severe weakness in the power supply noise since it's based on the inverter delay cells. The output frequency of a Ring Oscillator is related to the rising and falling time of the inverter cells decided by the voltage. So the jitter performance is degraded by the supply voltage noise. Furthermore, as the ADPLL shares the supply voltage with the complex circuits in PAM4-binary bridge, the problem becomes more important. In

this paper, an ADPLL with self supply-regulating Ring Oscillator using a NMOS shunt regulator array is proposed. Unlike the other prior works, this method make the Ring Oscillator robust to the power supply noise by the simplist open-loop calibration. The strength and the weakness of a Ring Oscillator is achieved and compensated by this Self Supply-Regulating Ring Oscillator based ADPLL

1.2 Thesis Organization

This paper consists of the following. Chapter 2 briefly describes the background of an ADPLL with a Ring Oscillator in terms of its structure. The strength and weakness of an ADPLL and a Ring Oscillator is described. Then the effect of the oscillator supply noise on the jitter performance in terms of the loop dynamics is analyzed.

Chapter 3 explains the overall architecture of the proposed ADPLL and the design considerations. The analysis of the proposed supply noise absorbing NMOS shunt regulator array implemented digitally controlled oscillator is mainly provided.

Chapter 4 is about the performance measurement and simulation results of the proposed ADPLL manufactured with the 40 nm CMOS technology. The phase noise plot and the jitter performance with and without the supply noise is described. The supply noise cancellation is verified by the real chip measurement.

Chapter 5 concludes this paper and summarizes it.

Chapter 2

Backgrounds

2.1 Overview

In high-speed link circuits, the data signal is transmitted along with the clock signal for more precise data transmission as shown in Figure 2. 1. It means that not only the transmitters and receivers but also the clock generation circuits are essential in high-speed data transmission. Commonly, a Phase-Locked Loop (PLL) has been used for the precise clock generation for this purpose. A PLL generates and aligns the phase and frequency of the output clock to the reference clock by a feedback operation. Mostly, the frequency of the output clock is increased by a dividing factor of a divider.

Figure 2. 2 shows a basic circuit diagram of an analog Charge Pump PLL (CPPLL) and an all-digial PLL (ADPLL), the most common classification of the PLLs [3]. Unlike the earlier technology, CPPLL, the ADPLL replaced a Charge Pump (CP) and a Loop filter (LF) to a Digital Loop Filter (DLF).

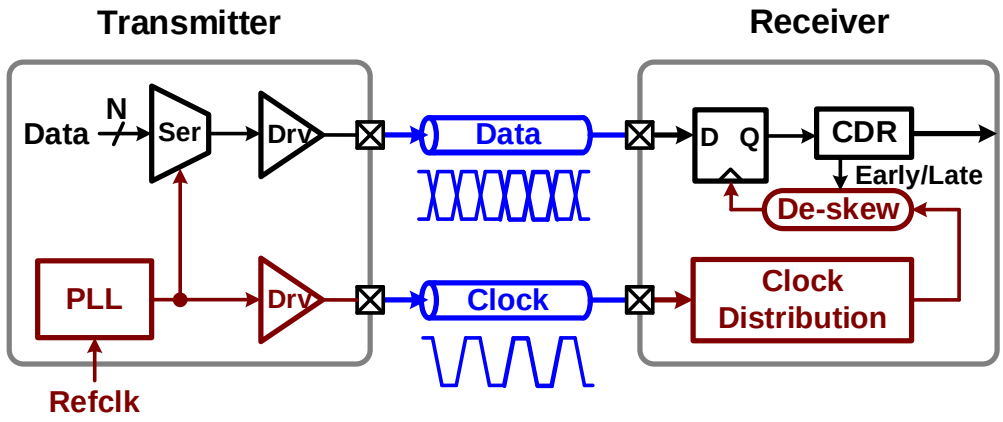
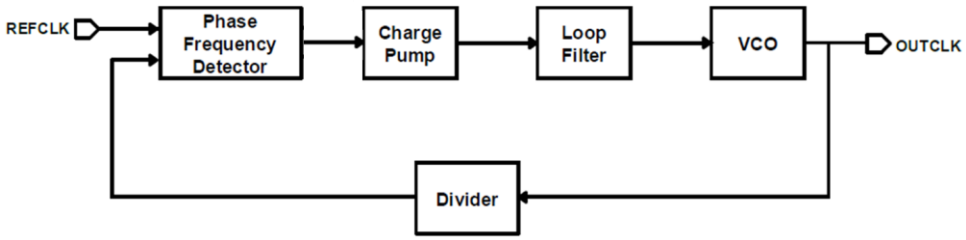
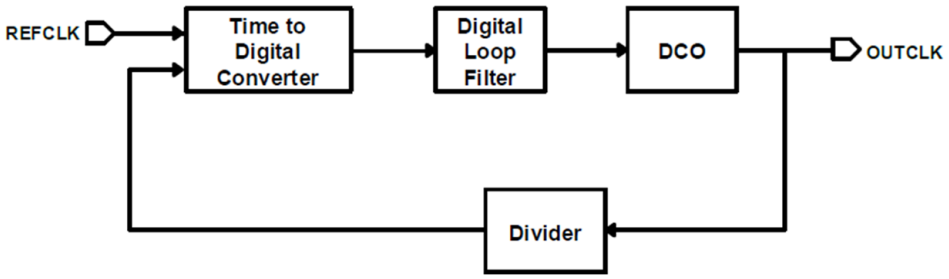


Fig. 2.1 Forwarded-Clock transmitting scheme



(a)



(b)

Fig. 2.2 (a) An analog charge pump PLL (CPPLL) and (b) all-digital PLL (ADPLL)

Compared to the CP and the LF, there are several adventages achieved with the DLF in the ADPLL. Since the DLF is a digital block that communicates with digital signals, it is robust over the Process-Voltage-Temperature (PVT) variation. Moreover, lacking analog tuning voltages enables the ADPLL to adjust to the modern deep-submicron technology with low power supply voltage. Placed and Routed (PNR) with the RTL codes, the DLF is also flexible to the fabrication process technologies and easy to modify the inner algorithms and the variables like the loop gains. On the other hand, the analog CPPLL suffers from leakage current, large area due to the capacitors, device mismatches, and low voltage headroom.

In spite of these valuable characteristics, the ADPLL has flaws like the quantization error that occurs during converting analog signals to digital signals in a Time to Digital Converter (TDC) and the DCO [3]. In addition, these analog-digital mixed circuits suffer from the power supply noise except the DLF. This paper suggest a supply noise-insensitive DCO scheme to solve this problem. Additionally, the most significant part of the ADPLL is a Digitally-Controlled Oscillator (DCO). As the DCO itself generates multi-phase clock signals through the oscillation, the latest technologies have to converge in the single block for the accurate and low-jitter clock signals. All building blocks of the ADPLL is described, but for this reason, the main focus is on the DCO in the following sections.

2.2 Compositions of the ADPLL

In this section, the building blocks of the ADPLL are discussed based on Figure 2.2(b). The TDC as a phase-frequency detector, the DLF that receives the output of the TDC and filters it, and the DCO controls the output frequency by the controlling bits from the DLF are explained in detail.

2.2.1 Time-to-Digital Converter

The Time-to-Digital Converter (TDC), receiving the input reference clock of the ADPLL, translates the phase difference of the reference clock and the divided DCO output clock into digital codewords. The TDC basically delays the reference clock by stages and samples it with the divided output clock using each D-flip flop as shown in Figure 2.3.

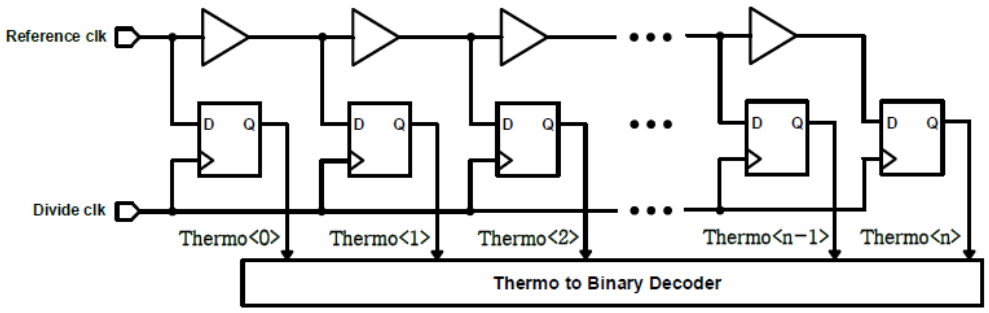


Fig. 2.3 Block diagram of a Basic delay line TDC

As mentioned in the Overview, the crucial problem of the TDC is the quantization error that occurs while translating the analog inputs to digital codewords for the DLF input. In a basic delay line TDC, as shown in Figure 2.3, the delay time of a reference clock delay cell becomes the TDC resolution. By this operation, the TDC transfer curve is stair-shaped as shown in Figure 2.4. Once the phase difference of the reference clock and the divided output clock is less than the TDC resolution, the delay time of a delay cell, it results in the quantization error.

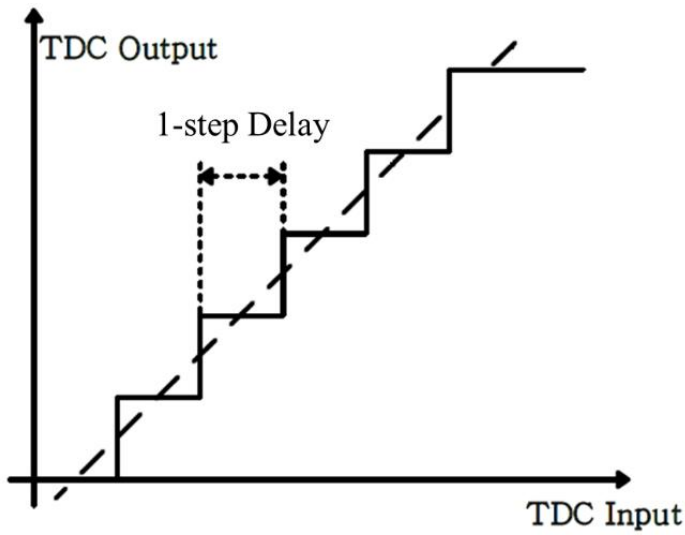


Fig. 2.4 Transfer curve of a TDC

The easiest solution to minimize the quantization error is to lower the delay time of a delay cell. However, the total width of the transfer curve, the TDC input phase difference detection range would be reduced according to Figure 2.4. To overcome this problem and higher the jitter performance of the TDC, several complementary structure have been designed.

For example, a differential delay line TDC and a Vernier delay line TDC have been proposed [4]. Those scheme lowered the TDC resolution by delaying both the reference clock and the divided output clock. Nevertheless, these delay line based TDC lack the capability of tracking the frequency, only behaving as a phase-detector (PD). Dealing with these two problems, a TDC followed by a bang-bang PFD and a phase-frequency detecting TDC are proposed for the latest scheme [5]-[6]. In this ADPLL, a Vernier delay TDC with a bang-bang PFD is implemented. Figure 2.5 shows the block diagram of it.

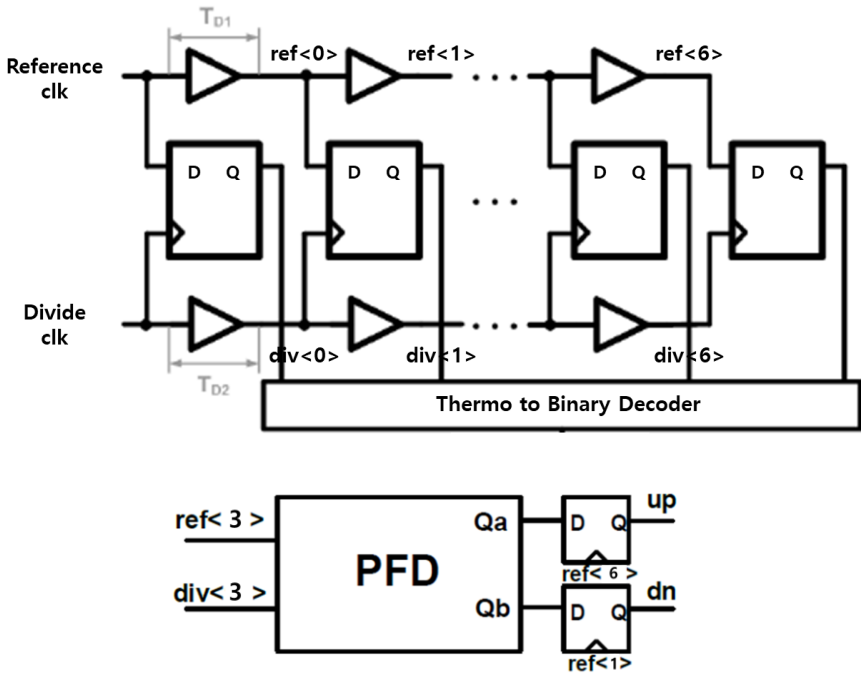


Fig. 2.5 TDC-PFD structure of the designed ADPLL

2.2.2 Digital Loop Filter

Working as a CP and a LF of an analog PLL, a Digital Loop Filter (DLF) is the biggest difference between an analog and a digital PLL. Figure 2.6 shows the 1st order analog LF in the CPPLL and the model transformed to the DLF. In the CPPLL, a resistor and a capacitor decide the loop dynamics of the overall system. As described in the Overview, they cause several problems like large area, difficult to be tuned, and vulnerable to PVT variations. On the other hand, the digital transformed model, DLF is tolerant to PVT variations and easy to modify the loop dynamics by controlling I2C signals.

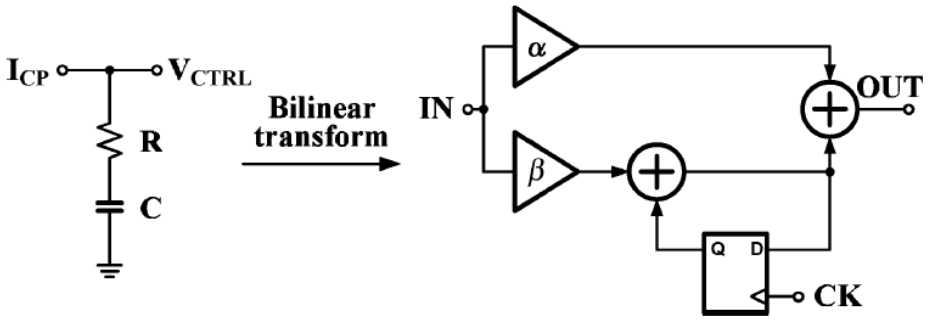


Fig. 2.6 Analog Loop Filter and transformed DLF

In Figure 2.6, the transfer function of the LF is given as Equation (2.1).

$$\mathbf{H_{LF}} = \frac{\boldsymbol{V_{ctrl}(s)}}{\boldsymbol{I_{cp}(s)}} = \boldsymbol{R} + \frac{\mathbf{1}}{\boldsymbol{sC}} \tag{2.1}$$

According to the equation and the qualitative analysis, the capacitor accumulates the charge as an Integral term. The resistor, on the other hand, tracks the transient phase error as a Proportional term after the output frequency is locked.

For the purpose to design the ADPLL based on the CPPLL, the transfer function of the DLF has to be equal to Equation (2.1). Nevertheless, since the LF and DLF operate in continueous time and discrete time domain, respectively, the Equation has to be transformed to the Z-domain model. Using the Bilinear Transform, Equation (2.1) is translated to Equation (2.2),

$$s = \frac{2}{T_s} \cdot \frac{1 - z^{-1}}{1 + z^{-1}}$$

$$\mathbf{H_{DLF}} = \left(R - \frac{T_s}{2 \cdot C}\right) + \left(\frac{T_s}{C} \cdot \frac{1}{1 - z^{-1}}\right) = \alpha + \frac{\beta}{1 - z^{-1}} \tag{2.2}$$

where T_s refers to the sampling period of the DLF, T_{Ref}. The parameter α, and β, a proportional gain and a integral gain of the ADPLL, respectively, are the coefficient that determine the Phase Margin (PM) and the Bandwidth (BW) of the ADPLL. The relationship with the coefficients and the PM and the BW is expressed as Equation (2.3)

$$\alpha = R - \frac{T_s}{2C}, \qquad \beta = \frac{T_s}{C}$$

$$\alpha = \beta \cdot \left(\frac{\tan(PM)}{T_s \cdot \omega_{BW}} - \frac{1}{2}\right), \beta = \frac{T_s}{T_{REF}} \cdot \frac{\Delta TDC \cdot N}{K_{DCO}} \cdot \frac{\omega_{BW}^2}{\sqrt{1 + \tan^2(PM)}} \tag{2.3}$$

ΔTDC, K_{DCO}, and N refers to the resolution of the TDC and the DCO and the dividing factor of the output divider, respectively. As shown in Equation (2.3), the unity gain bandwidth, ω_{BW} and the phase margin $\tan(PM)$ can be modified by the proportional gain and the integral gain.

The top block diagram of the DLF including the input and output signals is shown in Figure 2.7. The input signals from the TDC-PFD are PFD_up/dn and TDC_out[6:0] which are the output signal of the PFD and the TDC, respectively. To replace the CP and the LF, DLF not only filters the output but also controls the DCO. The output signal Row[30:0] and Column[30:0] are the controlling thermometer codes of the DCO for modulating the output clock frequency of the ADPLL.

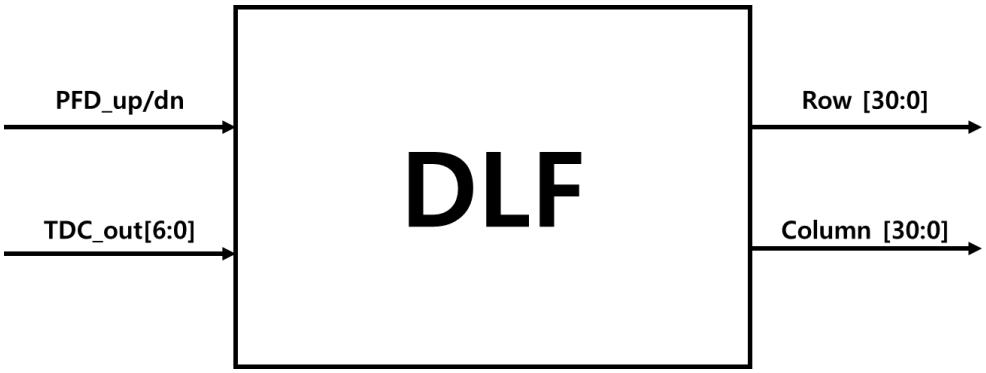


Fig. 2.7 I/O signals of the DLF

Additionally, a Delta Sigma Modulator (DSM) is implemented in the designed DLF. The effect of the DSM is discussed in Chapter 3.

2.2.3 Digitally Controlled Oscillator

Since Digitally Controlled Oscillator (DCO) generates an output clock whose frequency is modulated by the output of the DLF, the oscillator itself is the most important part of the ADPLL that determines the overall performance. The phase noise of the DCO is the main constituent of the total ADPLL output phase noise and the power consumption of the DCO is more than a half of the total ADPLL circuit.

Unlike the DLF which is totally different from the CP and the LF in the CPPLL, the DCO is not a full digital block but contains the similar core oscillator circuit with the VCO in the CPPLL. Therefore, to design the DCO, the first thing to do is to select the type of the VCO to be implemented. Commonly, a Ring Oscillator and an inductance-capacitance (LC) oscillator are the two biggest classification of the VCO.

A circuit diagram of a basic LC oscillator is shown in Figure 2.8(a). The LC oscillator is based on a resonance of a inductor and a capacitor. The resonance frequency f_0 and the quality factor Q of the LC resonator is expressed in Equation (2.4).

$$\boldsymbol{f_0 = \frac{1}{\sqrt{LC}}}, \qquad \boldsymbol{Q = \omega_0 CR} \tag{2.4}$$

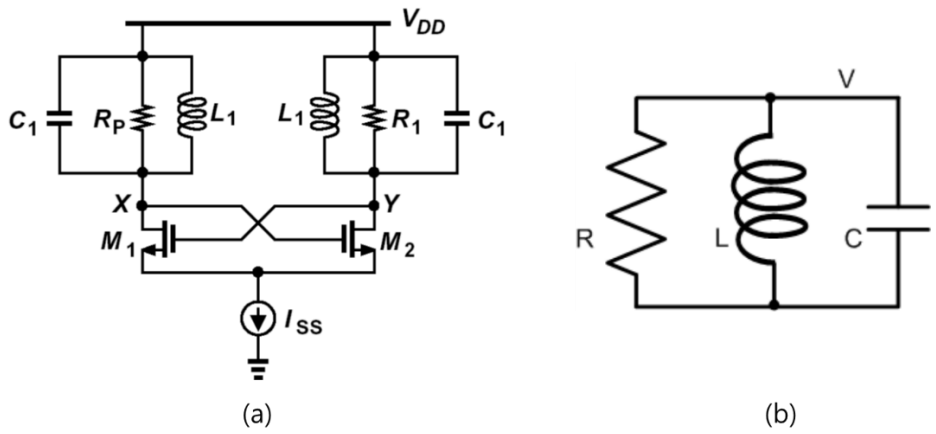


Fig. 2.8 (a) A circuit diagram of a basic LC Oscillator (b) LC resonator

The pros and cons of the LC oscillator come from these characteristics of the inductor and the capacitor and their resonance. First of all, since the resonance frequency is related to the inductance and the capacitance as expressed in Equation (2.4), high-frequency oscillation can be achieved easily. Moreover, as the oscillation frequency is independent to the power supply voltage, the phase noise performance is superior to a Ring Oscillator. However, the LC oscillator occupies larger area and is hard to generate multiple phase and large frequency range clock.

The Ring Oscillator, on the other hand, is shown in Figure 2.9. Basically, the Ring Oscillator is composed of odd number inverters array [7]. By the inverter logic, logical ones and zeros are oscillated at each stage and the states are repeated in two cycle of the loop. For a Ring Oscillator to oscillate, it has to meet Barkhausen Criteria for oscillation as explained in Equation (2.5).

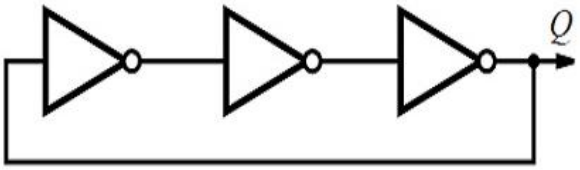


Fig. 2.9 Block diagram of a basic Ring Oscillator

$$\angle \boldsymbol{H_{loop}} = \boldsymbol{N} \cdot \angle \boldsymbol{H_{stage}}(\boldsymbol{f_{osc}}) = -\boldsymbol{\pi}, \quad \left|\boldsymbol{H_{loop}}\right| = \left|\boldsymbol{H_{stage}^{N}}(\boldsymbol{f_{osc}})\right| > \mathbf{1} \tag{2.5}$$

$$\boldsymbol{f_{osc}} = \frac{\mathbf{1}}{\mathbf{2}\boldsymbol{N} \cdot \boldsymbol{\tau_D}} \tag{2.6}$$

H_{loop} and H_{stage} refer to the loop gain and the gain of each stage, respectively and N is the number of the stages. For example, in Figure 2.9, N is equal to 3. The factor deciding the oscillation frequency, $\boldsymbol{\tau_D}$, is the rising and falling delay time of an inverter stage. $\boldsymbol{\tau_D}$ is determined by various parameters like the power supply voltage, the load capacitance of each stage, and the size of the transistors that compose the inverter stage. Therefore, it is easier for the Ring Oscillator to have wider frequency operation range. Furthermore, multiple phase generation is feasible by the multiple stages with narrow space. In this work, the Ring Oscillator is implemented to generate multiple phase clock signal for the PAM4-Binary Bridge.

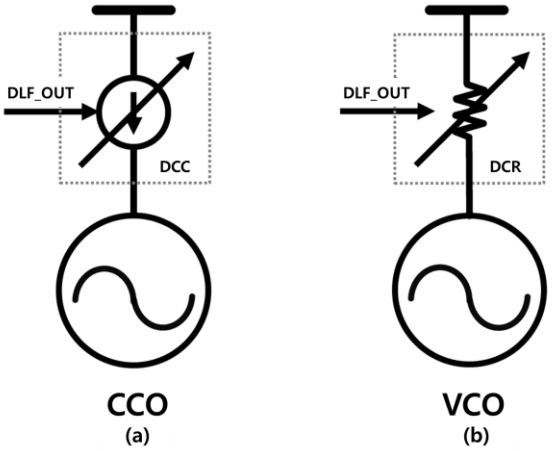


Fig. 2.10 Block diagram of (a) a Current-Controlled DCO and (b) a Voltage-Controlled DCO

There are several methods to control the oscillator digitally after selecting the type of it. For the Ring Oscillator, a common approach is to manipulate the oscillation frequency by the supply voltage. Figure 2.10 shows the two types of DCO working by that mechanism. A Digitally-Controlled Current source (DCC) converts the DLF output control codes to the amount of current, acting as a digital-analog converter (DAC), as shown in Figure 2.10(a). The other method is to convert the codes to the resistance of a variable resistor. A Digitally-Controlled Resistor (DCR) modifies the supply voltage of the Ring Oscillator, also acting as a DAC. In this work, the VCO with the DCR is implemented as the DCO scheme.

Several problems occur with the implemented DCO. One of the problem is a quantization error. Reverse to the TDC operation, as the DCO take the digital codewords from the DLF and generates the analog clock signal, quantization error occurs. Similar to the TDC transfer curve, the transfer curve shown in Figure 2.11 is also stair-shaped. One bit alternation of the control code results in frequency change as much as K_{dco}, a frequency resolution of the DCO. Lowering the resolution can improve the ADPLL jitter performance, but it reduces the frequency operation range. This trade-off is the main consideration of designing the DCO.

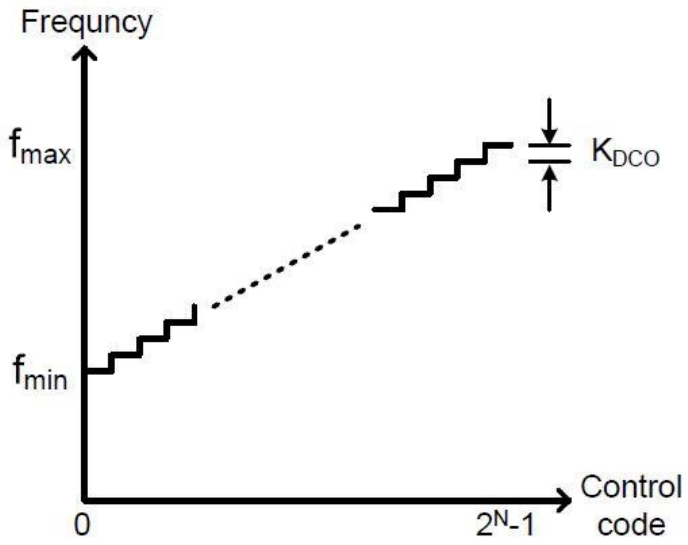


Fig. 2.11 Transfer curve of the DCO

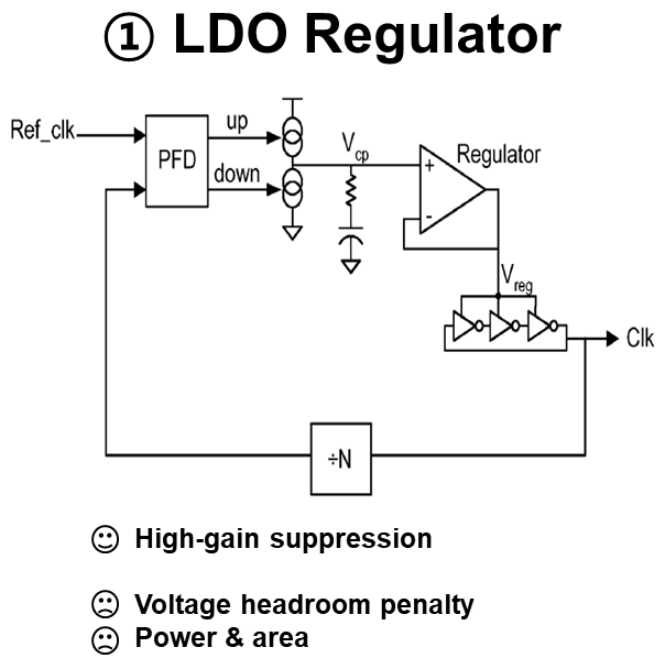
In addition, as the output frequency of the VCO based DCO is determined by the supply voltage of the oscillator, the power supply noise (PSN) is also the critical problem. There are several prior works to solve this problem.

2.2.4 Prior Works of Supply Noise Cancellation

Several techniques have been implemented to mitigate the PSN sensitivity of a Ring Oscillator. To begin with, a Low Dropout Regulator (LDO) is commonly used as a block that regulates the supply voltage [8], [9]. The LDO is preferred since it can suppress the noise powerfully. Nevertheless, the LDO add unwanted parasitic pole to the loop gain, requiring the bandwidth of it to be much more larger than the loop bandwidth of the ADPLL. What is worse, it takes much more area and power than the original ADPLL circuit.

Feed-forward [10], [11] or background calibration [12], [13] are the other technique to remove the PSN. The calibration enables the PSN cancellation in spite of the PVT variation. In addition, as the calibration circuit does not deal with the supply voltage itself, voltage headroom problem disappears. However, the calibration circuit degrades the circuit complexity, and a tremendous settling time is required. Figure 2.12 summarizes the prior works by two classification groups.

The prior solutions all suffer from increasing circuit complexity, and occupying large area and power. It is unreasonable to higher the circuit complexity since it ruins the advantage of implementing a Ring Oscillator. In this work, the simplist solution that minimizes these problems is suggested.



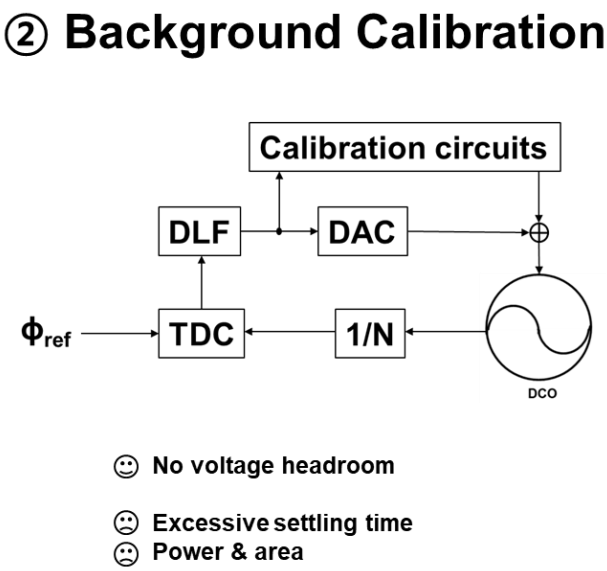


Fig. 2.12 Prior works of supply noise cancellation

2.3 ADPLL Loop Analysis

2.3.1 Loop transfer function

Loop analysis is important for an ADPLL since it is also one kind of feedback loop. In this section, loop transfer function with the loop bandwidth and stablity, and phase noise analysis of all building blocks is discussed. Especially, the focus is on the DCO noise contribution and the supply noise effect.

For the feedback loop, ADPLL, loop transfer function is essential to get the bandwidth and the phase margin for the loop analysis. To analyse the closed loop transfer function of the ADPLL in frequency domain, Bilinear Transform is applied to the z-domain transfer function. Equation (2.7) expresses the frequency domain open loop gain of the basic ADPLL shown in Figure 2.13.

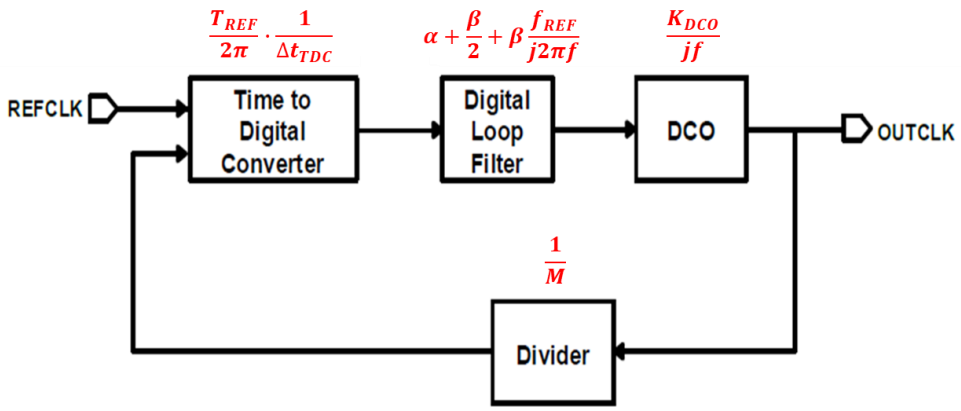


Fig. 2.13 Frequency domain transfer function of the basic ADPLL

$$\begin{aligned} \boldsymbol{A(f)} &= \boldsymbol{K_{TDC}(f)} \cdot \boldsymbol{H_{DLF}(f)} \cdot \boldsymbol{H_{DCO}(f)} \cdot \frac{\mathbf{1}}{\boldsymbol{M}} \\ &= \frac{\boldsymbol{T_{REF}}}{\mathbf{2\pi}} \cdot \frac{\mathbf{1}}{\boldsymbol{\Delta t_{TDC}}} \cdot \left(\boldsymbol{\alpha} + \frac{\boldsymbol{\beta}}{\mathbf{2}} + \boldsymbol{\beta}\frac{\boldsymbol{f_{REF}}}{\boldsymbol{j2\pi f}}\right) \cdot \frac{\boldsymbol{K_{DCO}}}{\boldsymbol{jf}} \cdot \frac{\mathbf{1}}{\boldsymbol{M}} \end{aligned} \tag{2.7}$$

$$\boldsymbol{G(f)} = \frac{\boldsymbol{M} \cdot \boldsymbol{A(f)}}{\mathbf{1} + \boldsymbol{A(f)}} \tag{2.8}$$

K_{TDC}, H_{DLF}, and H_{DCO} refers to the transfer function of the TDC, the DLF, and the DCO, respectively. Equation (2.8) describes the closed loop gain using the open loop gain and the divider factor. Design requirements like a loop bandwidth and a phase margin are satisfied by tuning the loop filter parameter α, β based on the Equation (2.7). In general, loop bandwidth is above the 1/10 of the reference clock frequency and the phase margin has to be a value between 50 to 70 degree. Table 2.1 compares the frequency domain transfer function of CPPLL and ADPLL blocks.

Table 2.1. Comparison of CPPLL and ADPLL block transfer function

	CPPLL	ADPLL
PD / TDC	$K_{PD} = \frac{I_{CP}}{2\pi}$	$K_{TDC} = \frac{T_{ref}}{2\pi \cdot \Delta TDC}$
LF / DLF	$H_{LPF}(f) = R + \frac{1}{j2\pi fC}$	$H_{DLF}(f) = \alpha + \frac{\beta}{2} + \beta\frac{f_{REF}}{j2\pi f}$
VCO / DCO	$H_{VCO}(f) = \frac{K_{VCO}}{jf}$	$H_{DCO}(f) = \frac{K_{DCO}}{jf}$
DIV	$\frac{1}{N}$	$\frac{1}{N}$

2.3.2 Noise modeling

Based on the loop transfer function analysis, transfer function of individual noise sources are derived in this section. Figure 2.14 shows the noise sources of an ADPLL.

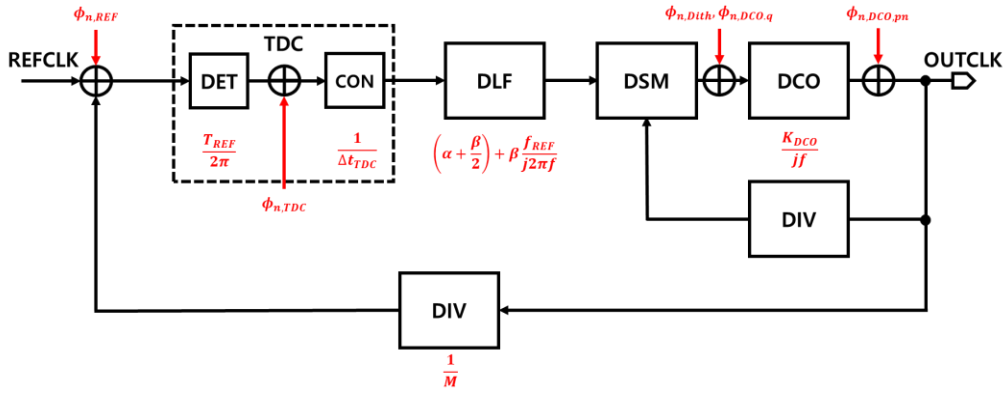
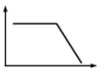
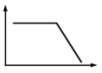


Fig. 2.14 Noise Modeling of an ADPLL

From the left side of Figure 2.14, the noise sources of an ADPLL are Reference Clock Noise, TDC Quantization Noise, Dithering Noise, DCO Quantization Noise, and DCO Phase Noise, respectively. Each Noise Source is also affected by the loop transfer function. Table 2.2 shows the noise sources of an ADPLL and their transfer function to the output signal [14]. The rightmost column shows the transfer characteristics of the noise sources. Low Pass for Reference Clock and TDC Quantiaztion Noise, Band Pass for Dithering and DCO Quantization Noise, and High Pass for DCO Random Phase Noise.

Table 2.2. Noise Sources and Transfer Functions of an ADPLL

Noise	Transfer Function		
Reference Clock Noise	$\phi_{n,REF}$	$N \cdot \frac{H_{open}}{1+H_{open}}$	
TDC Quantization Noise†	$\phi_{n,TDC}$	$\left(\frac{2\pi}{T_R}\right) \cdot N \cdot \frac{H_{open}}{1+H_{open}}$	
Dithering Noise	$\phi_{n,Dith}$	$\frac{1}{jf} \cdot \frac{1}{1+H_{open}}$	
DCO Quantization Noise§	$\phi_{n,DCO,q}$	$\frac{1}{jf} \cdot \frac{1}{1+H_{open}}$	
DCO Random Noise	$\phi_{n,DCO,pn}$	$\frac{1}{1+H_{open}}$	

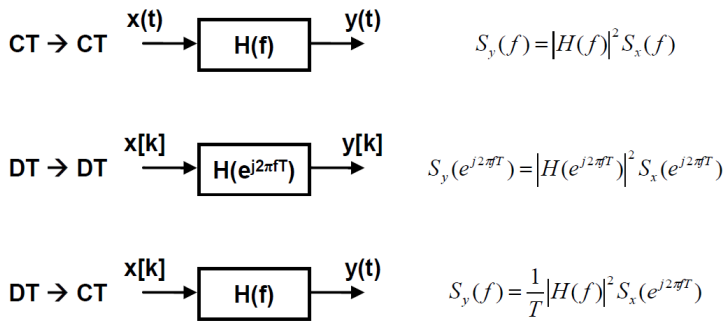


Fig. 2.15 Power Spectral Density Conversion

Figure 2.15 shows Power Spectral Density Conversion of Continueous and Discrete Time signals. By using those conversions, output Phase Noise Power Spectral Density can be driven.

In this paper, the focus is on the power supply noise of the DCO, which is written as DCO Random Phase Noise in the Table 2.2. According to the Table 2.2 and the Figure 2.15, the Power Spectral Density of the output phase noise due to the DCO power supply nosie is expressed as,

$$\boldsymbol{S_{out,DCO}(f) = S_{\phi n,DCO}(f) \cdot \left| \frac{1}{1 + H_{open}(f)} \right|^2} \tag{2.9}$$

where $H_{open}(f)$ is the open loop transfer function of the basic ADPLL A(f) in the Equation (2.8). As it shows a high pass characteristic, the loop bandwidth of an ADPLL has to be wider for lower jitter contribution. Similarly, the power supply noise cancelling schemes like Figure 2.12 have to be low pass filters.

Chapter 3

Design of Supply Noise-Insensitive ADPLL

3.1 Design Consideration

The proposed ADPLL in this paper is designed to be implemented in the PAM4-Binary Bridge. The ADPLL has to transfer the differential 4 GHz reference clock from the ATE to 4-phase, 8 GHz output clock for the GDDR. For the precise operation of the Transmitter and the Receiver in the PAM4-Binary Bridge, the ADPLL design has to focus on accurate phase distribution and improving the overall jitter performance. However, due to the complex circuit in the Bridge, the most crucial design challenge is lowering the supply noise sensitivity of the Ring Oscillator in the DCO.

In this chapter, the overall architecture of the ADPLL and the technique for supply noise-insensitive Ring Oscillator are presented. In PFD-TDC, a Bang-Bang Phase-Frequency Detector (PFD) is implemented with a Vernier delay line TDC to perform phase and frequency detecting. The Digital Block receives the I2C control to alter the parameters of the ADPLL and operates as the DLF function. A 1^{st} / 2^{nd} order Delta Sigma Modulator (DSM) is also constructed in the Digital Block.

The proposed Supply Noise-Insensitive DCO is described in detail. NMOS shunt regulator transistors array, Supply-Sensing Amplifier, and the Supply Noise-Insensitive technique analysis are the contents. Additionally, the scheme of Digitally-Controlled Resistor (DCR) in the DCO is also described for understanding of the supply noise-insensitive technique.

3.2 Overall Architecture

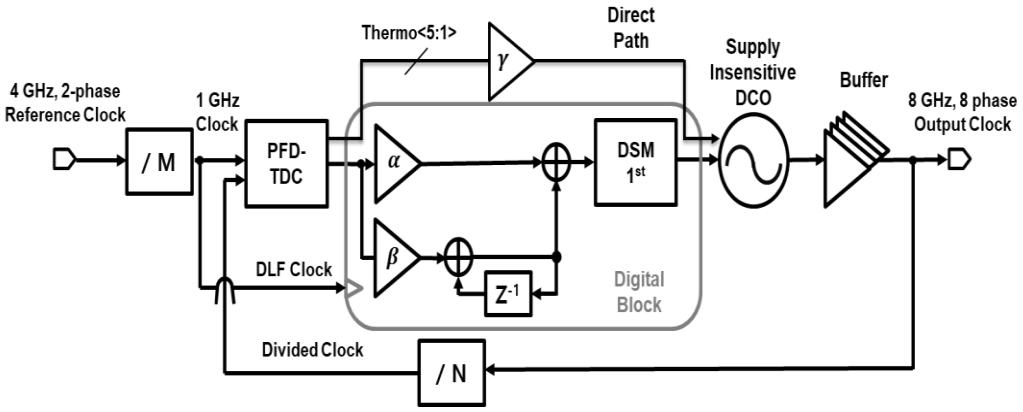


Fig. 3.1 Overall Architecture of the proposed ADPLL

The Overall Atchitecture of the proposed ADPLL is shown in Figure 3.1. The building blocks are Input Divider, PFD-TDC, DLF, DSM, Supply Insensitive Ring DCO, AC-Coupled buffer, and Output Divider, respectively. As the implemented PFD-TDC operation bandwidth is right above 1 GHz, input divider is added to lower the reference clock frequency. To lower the circuit complexity, the DLF also operates based on the divided input clock which can cause a Loop Delay problem. A Direct Path that directly controls the DCO by the PFD-TDC output is also implemented parallel to the DLF to prevent the problem. The middle 5-bit thermometer code of the 7-bit PFD-TDC output is used for the Direct Path operation.

The Digital Block containing the DSM to lower the Phase Noise due to the Dithering Noise, decodes the 10-bit output to the 31-bit row code and the 31-bit column code to manipulate the DCO output frequency.

The output Buffer, the AC-Coupled Resistive Feedback Inverter, alters the common voltage of the output clock signal to the half of the supply voltage, V_{DD}, and make the swing Rail-to-Rail. Figure 3.2 shows the circuit diagram of the implemented AC-Coupled Resistive Feedback Inverter [15]. The proposed DCO scheme is presented in the following sections.

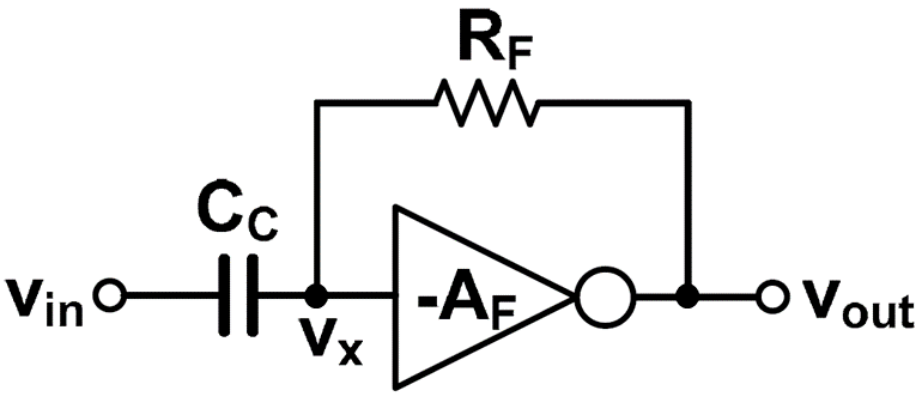


Fig. 3.2 AC-Coupled Resistive Feedback Inverter

3.3 Proposed Circuit Implementation

3.3.1 PFD-TDC and Digital Block

The TDC implemented in the proposed ADPLL is combined with a Bang-Bang PFD to detect frequency difference and make the TDC operation range wider. Figure 3.3 shows the circuit diagram of the PFD-TDC which is based on the Vernier delay line TDC.

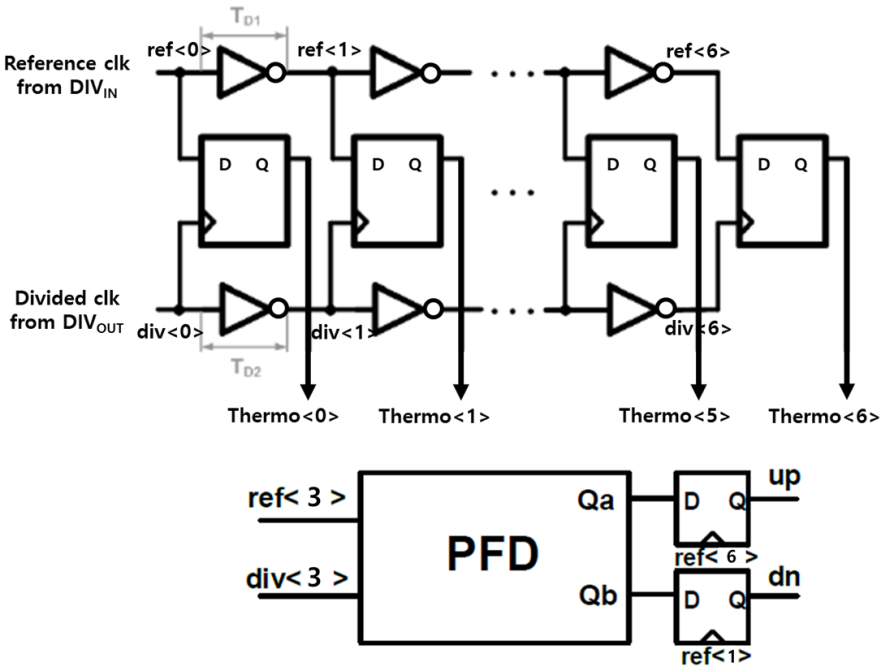


Fig. 3.3 Structure of the PFD-TDC

In the Vernier delay line TDC, 7 inverter pairs working as delay cells and symmetric D-Flip Flop (DFF) samplers are used. The resolution of the TDC is determined by the difference between T_{D1} and T_{D2}, the delay time of each inverter in the pairs. Since the delay has to be minimized to lower the quantization noise of the TDC, each delay cell is composed of a single inverter and the resolution of the TDC is improved to the value of Sub-Gate delay. The single inverter delay method also prevents the sign reversion of the resolution due to the delay variation.

The detection range of the TDC is $7 \cdot (T_{D1} - T_{D2})$, which is also minimized by improving the TDC resolution. The implemented Bang-Bang PFD also compensates the problem. If the phase difference between the reference clock and the divided clock is larger than the TDC detection range, the Bang-Bang PFD corrects the output clock by the UP/DN signal. As described in the Figure 3.3, Refclk<3> and Divclk<3> are used for the PFD input. Refclk<1> and Refclk<6> sample the PFD outputs and hold them until the next positive edge. The Monte Carlo Simulation shows the resolution and the detection range of TDC as 2.5 ps and 17.5 ps at TT corner, respectively. Figure 3.4 shows the logical circuit diagram of the Bang-Bang PFD.

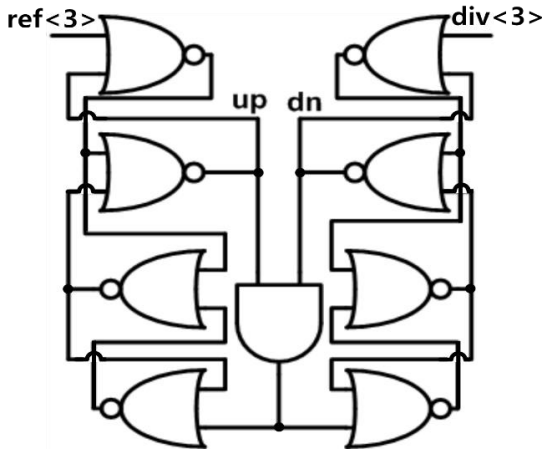


Fig. 3.4 Phase Frequency Detector

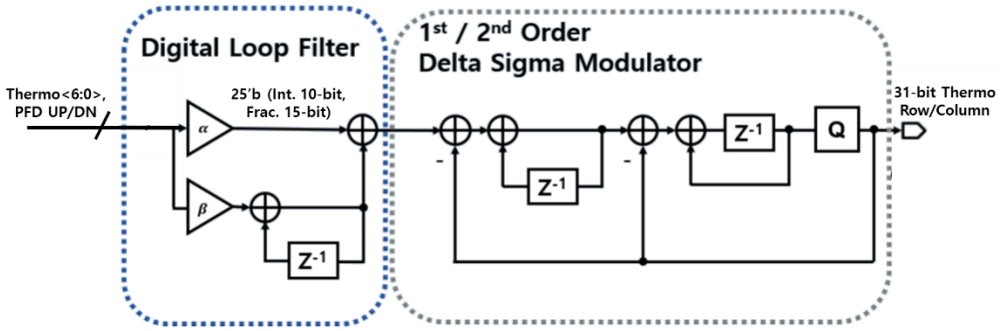


Fig. 3.5 Simplified DLF Architecture

As shown in Figure 3.5, the Digital block in the ADPLL is composed of the DLF and the DSM. It takes the 7-bit TDC thermometer output and PFD up and down signals for the input. Then it yields 31-bit thermometer DCR Row and Column control codes as the output. Proportional Path (α), and Integral path (β) converts the input to 10-bit integer and 15-bit fractional code according to the each gain. These gains are configurable by the I2C control so that the loop bandwidth and phase margin can be optimized. The two outputs from the two paths are summed up for the DSM input.

The DSM is implemented to lower the Dithering Noise and the Quantization Noise [16]. It can also be selected between the first and the second-order mode. The DSM correlates the quantization errors between consecutive outputs and surmise them from the next. The quantization noise shaped 10-bit integer and 15-bit fractional code is the output of the DSM. Finally, the 10-bit Integer of the DSM output is divided to 5-bit from the MSB and the other and decoded to 31-bit thermometer Row and Column code, respectively. The total Digital Scheme is Place and Routed (PNR) using the RTL code.

3.3.2 Proposed DCO with DCR

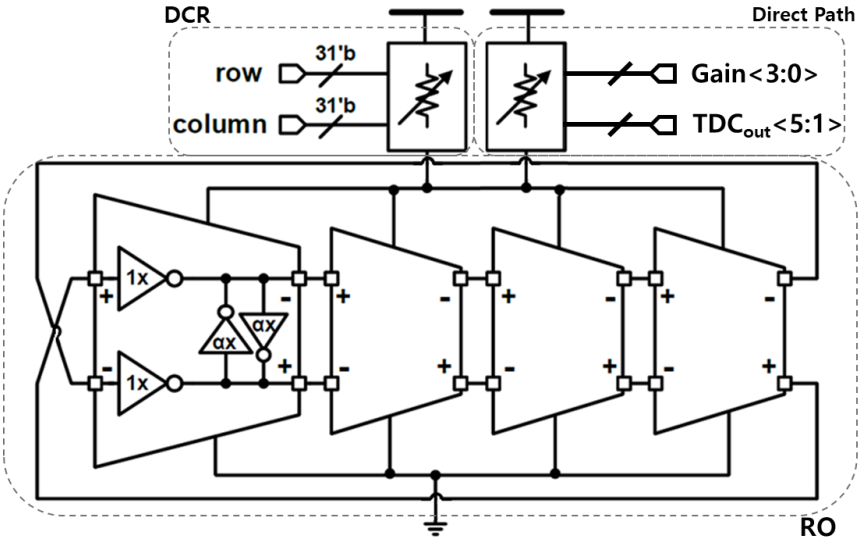


Fig. 3.6 Conventional DCO Architecture

The conventional DCO scheme implemented in the presented ADPLL is shown in Figure 3.6 [17]. The basic operation is adjusting the supply voltage of the Voltage Controlled Ring Oscillator (RO) by the Digitally-Controlled Resistor (DCR). The DCR takes the 31-bit thermometer row and column codes from the Digital Block for the input and manipulates the supply voltage of the RO, working as a Digital to Analog Converter (DAC).

The structure of the DCR is based on [18]. 1024 resistor cells that can be turned on and off are placed on 32×32 square. Each resistor cell is composed of PMOS transistors. When the cell is turned on, the PMOS transistors in the cell are turned on, allowing the current to flow through the cell. Therefore, the voltage drop through the DCR and the net resistance of the DCR is lowered. In other words, a higher control codes from the DLF results in a lower resistance of the DCR.

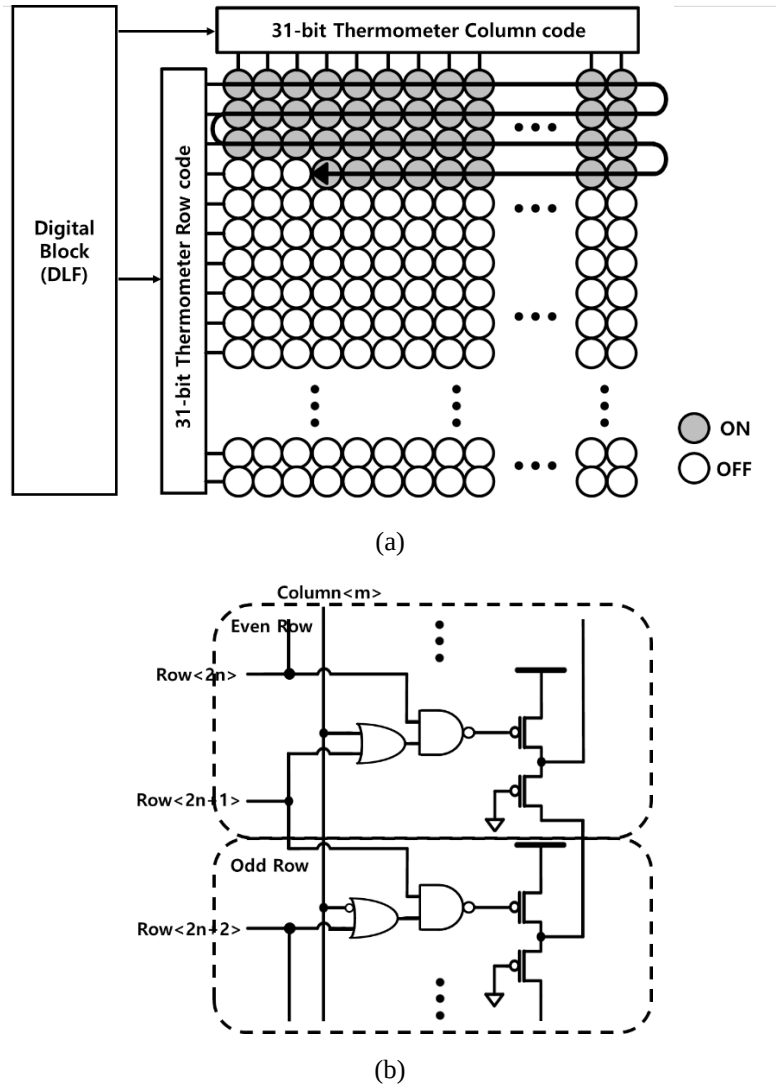


Fig. 3.7 DCR (a) operation mechanism and (b) Even and Odd Cell

The overall structure of the DCR is shown in Figure 3.7. The Row code determines the number of the Row cells that are turned on, and the Column code is the number of the Column cells turned on in the highest activated Row cell line.

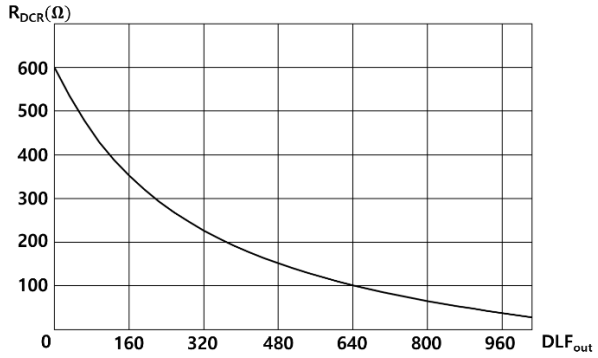


Fig. 3.8 Simulated DCR resistance

To overcome the mismatch of the resistor cells, the cells have to be turned on and off by the way of the Gray Code. As shown in the Figure 3.7(a), the resistor cells continueously operates to maintain the 1-bit difference of the control code with the 1-cell difference of the DCR. Since the Odd Row cells have to turn the cells from the left to the right and the Even Row cells from the right to the left, the structure of the cells have to be dissimilar as shown in the Figure 3.7(b). Therefore, the linearity of the DCR resistance is improved. Figure 3.8 shows the DCR resistance plot by the DLF output code variance. The maximum code is 1024.

Similarly, the Direct Path is composed of PMOS transistors. However, the total resistance of the Direct Path is ignorable compared to the DCR, maintaining the operation range of the DCR.

The 4-stage Pseudo-Differential Ring Oscillator scheme is implemented as a VCO [17]. Unlike the conventional single-ended RO, it does not need to contain odd-number inverter stages. As shown in the Figure 3.6, each delay cell is composed of two reverse-phase main inverters and two latch inverters whose width size is 0.25 times of the main inverters ($\alpha = 0.25$).

The latch inverters guarantee the phase difference between the delay cells, so that the phase error between the 8-phase output clock is minimized. The oscillation frequency of the RO is inversely proportional to the rising and falling time of the inverters in the delay cells and the supply voltage make the inverters speed up. Since the resistance of the DCR is lowered when the DLF output control code is highered, it results in higher supply voltage of the RO. Finally, the oscillation frequency of the DCO is proportional to the DLF output code. Figure 3.9 shows the simulated result of the DCO output frequency range. As the target frequency of the PAM4-Binary Bridge clock is 8 GHz, the DCO is designed to cover 8 GHz among FF, TT, and SS corner.

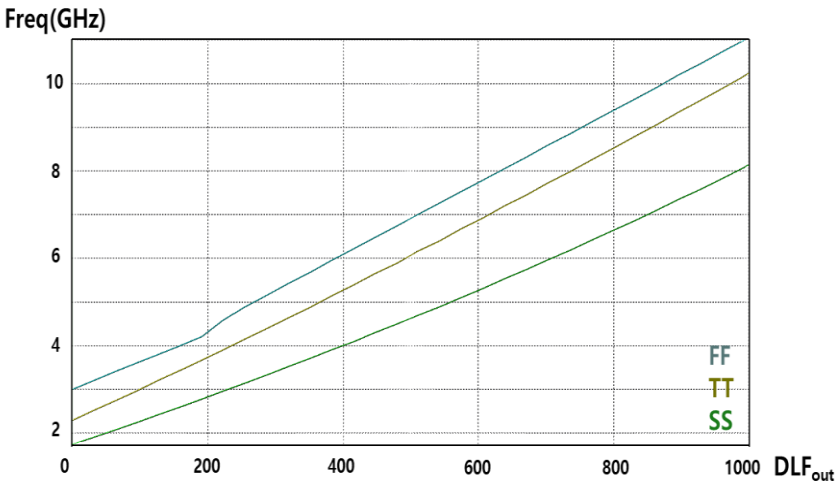


Fig. 3.9 DCO output frequency range

3.3.3 NMOS Shunt Regulator Array

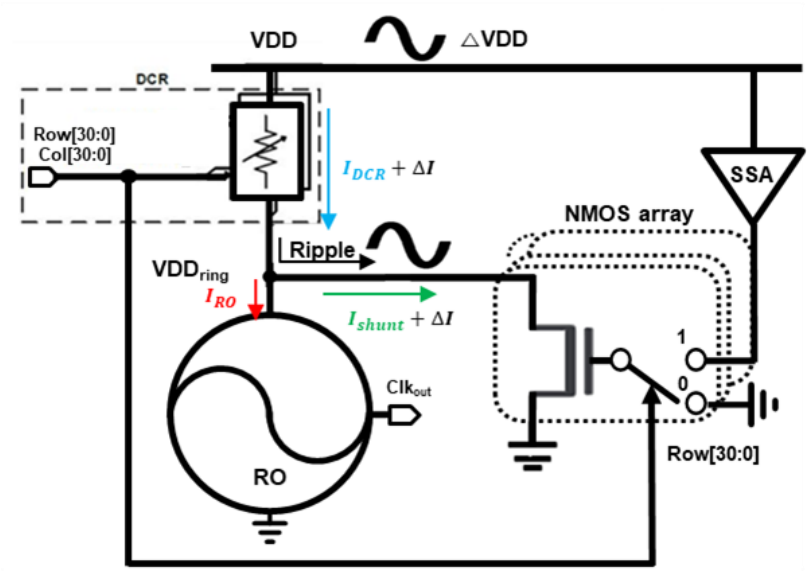
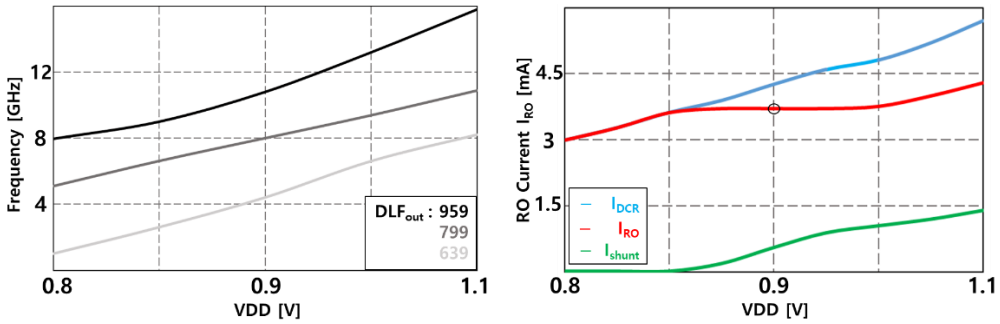


Fig. 3.10 Proposed Supply Noise-Insensitive DCO

In the case when the supply voltage of the DCO changes, the ADPLL is locked again and the DLF alters the control code to maintain the oscillation frequency to 8 GHz. However, instant variation of the supply voltage before the locking time results in instant output frequency alteration as shown in Figure 3.11(a). Therefore, output Phase Noise due to the power supply noise is the most crucial problem in the Voltage-Controlled Ring Oscillator.

To overcome this problem, a 31-bit NMOS transistors array and a Supply-Sensing Amplifier are placed in the proposed Supply Noise-Insensitive DCO as shown in Figure 3.10. The goal of the technique is to make the I_{RO}, the current flowing through the RO when the ADPLL is locked at 8 GHz, irrelevant to the supply voltage as shown in Figure 3.11(b).



(a) (b)

Fig. 3.11 Simulation results of (a) output frequency vs supply voltage and (b) current fluctuation and shunt compensation

As can be seen in Figure 3.10, 31-bit NMOS Shunt Regulator Transistors Array is implemented parallel to the RO. It is designed to absorb the DCR current variation induced by the Power Supply Noise (PSN), ΔI. The gate of the NMOS Array is connected to the DCO supply voltage so that I_{shunt} can track and cancel the amount of the change. As a result, I_{RO} remains stable despite the PSN fluctuation, resulting in better jitter performance.

Each transistors in the NMOS Array is turned on and off by the 31-bit Row control code from the DLF that is used to control the resistance of the DCR as described. The net transconductance of the NMOS Array reversely tracks the net resistance of the DCR by this method. A small resistance leads to a less voltage drop through the DCR, delivering less attenuated supply noise to the power voltage of the RO. As a result, larger transconductance of the NMOS Array is required to make the currnet I_{shunt} larger. The 31-bit Row control code alters both the DCR and the NMOS Array, meeting these requirements to absorb the PSN.

3.3.4 Supply Sensing Amplifier

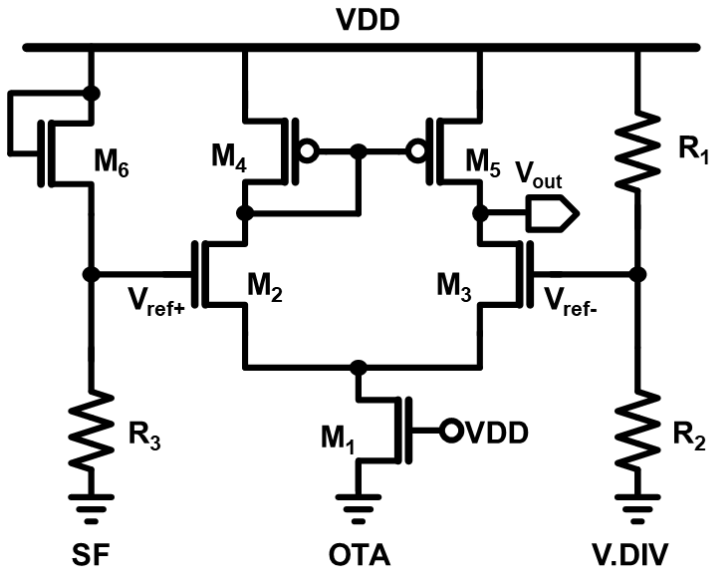


Fig. 3.12 Transistor circuit diagram of the Supply-Sensing Amplifier

The Supply-Sensing Amplifier (SSA) is implemented to offer the supply voltage of the DCO, VDD, to the NMOS Array gates. The common DC level has to be lowered to minimize the static current flowing through the NMOS Array. It allows low static power consumption and voltage headroom of the RO, preserving the frequency range. Moreover, the SSA as an error amplifier has to amplify the PSN to make the NMOS Array more sensitive to the supply nosie while tracking the variance of the supply voltage, VDD.

The transistor circuit diagram of the SSA is shown in Figure 3.12. A Source Follower (SF) level-shifts the common DC level of the supply, VDD, while the small siganl gain of it is almost 1. As a result, V_{ref+} shows the same variance of the supply voltage, while the DC voltage of it is degraded to 0.4 V, right above the threshold voltage of M_2. Meanwhile, the resistors R_1

and R_2 act as a Voltage Divider (V.DIV) to equate the common DC level of V_{ref-} with V_{ref+} for a differential amplifier operation of the Operational Transconductance Amplifier (OTA). Unlike the SF, the V.DIV divides the AC variance of the supply voltage resulting in AC differnece between V_{ref+} and V_{ref-}.

The OTA cell is designed to make a single output, V_{out}, show the same common DC level and doubled AC value compared to V_{ref+}. Figure 3.13 shows the large signal and small signal gain of the SSA. Since the jitter performance is vulnerable to the noise frequency around the loop bandwidth, it is designed to sustain the AC gain over 10 MHz. Figure 3.14 shows the simulation results of the SSA in TT corner. While the common level and peak-to-peak swing of the VDD was 0.9 V and 40 mV, V_{out} showed 0.4V and 80.3 mV, respectively.

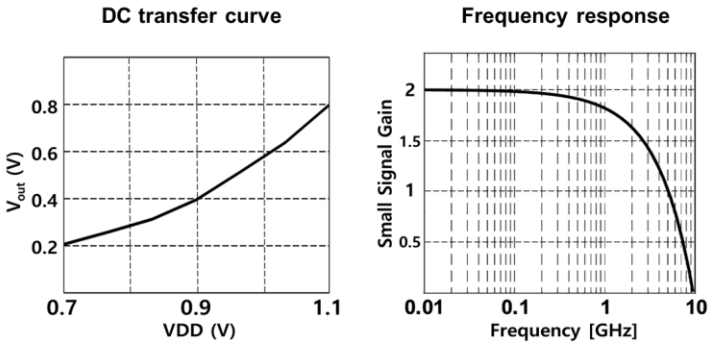


Fig. 3.13 Large signal and small signal gain of the SSA

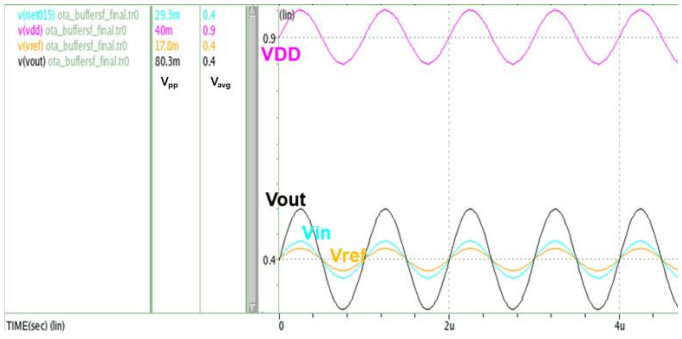


Fig. 3.13 Simulation result of the SSA operation

3.3.5 Supply Noise-Insensitive Technique

When the ADPLL is locked to 8 GHz and the supply voltage is ideal without noise, I_{DCR}, I_{shunt}, I_{RO}, and VDD_{ring} remains stable. VgsN, the gate voltage of the NMOS Array is about 0.4 V as explained in Section 3.3.4. Assume that the instant PSN is injected into the DCO supply voltage as shown in Figure 3.10. The SSA doubles the variance of the supply voltage, changing the gate voltage of the NMOS Array as

$$\boldsymbol{V_{gsN}{}' = V_{gsN} + 2\Delta VDD} \tag{3.1}$$

where ΔVDD is the value of the PSN. Using small-signal drain current model to derive the net current flowing through the NMOS Array, Ishunt, it is expressed as

$$\begin{aligned} \boldsymbol{I_{shunt}{}' = I_{shunt} + \Delta I = g_{mN} \cdot V'_{gsN}} \\ \boldsymbol{= g_{mN} \cdot (V_{gsN} + 2 \cdot \Delta VDD)} \end{aligned} \tag{3.2}$$

where g_{mN} is the total transconductance of the NMOS Array. Since I_{DCR} is the sum of I_{shunt} and I_{RO}, the expressions of VDD_{ring} attenuated by the resistance of the DCR are

$$\boldsymbol{I'_{DCR} = I'_{shunt} + I_{RO} = g_{mN} \cdot \left(V_{gsN} + 2 \cdot \Delta VDD\right) + I_{RO}} \tag{3.3}$$

$$\begin{aligned} \boldsymbol{VDD_{ring} = (VDD + \Delta VDD) - R_{dcr} \cdot I'_{DCR}} \\ \boldsymbol{= (VDD + \Delta VDD) - R_{dcr} \cdot (g_{mN} \cdot \left(V_{gsN} + 2 \cdot \Delta VDD\right) + I_{RO})} \end{aligned} \tag{3.4}$$

For the I_{RO} and VDD_{ring} to be unaffected by the PSN, ΔVDD should be removed from the Equation (3.4). The condition can be fulfilled with the transconductance of the NMOS array, g_{mN}, being

$$\boldsymbol{g_{mN} = \frac{1}{2 \cdot R_{dcr}}}, \quad \boldsymbol{\Delta g_{mN} = \Delta\left(\frac{1}{2 \cdot R_{dcr}}\right)} \tag{3.5}$$

According to the Equation (3.5), g_{mN}, the net transconductance of the NMOS Array has to vary inversely with the net resistance of the DCR, R_{dcr}. To do so, the g_{mN} resolution is designed as the right side Equation (3.5) where the unit of Δg_{mN} is ΔA / (V · Row bit), and the unit of the right-hand side is $\Delta 1$ / (Ω · Row bit). With the method of controlling the NMOS Shunt Regulator Transistors Array with the Row code of the DCR, the condition (3.5) is always maintained automatically, no matter what the output clock frequency is. Like the simulation result in Figure 3.11(b), I_{RO} and VDD_{ring} are irrelevant to the VDD.

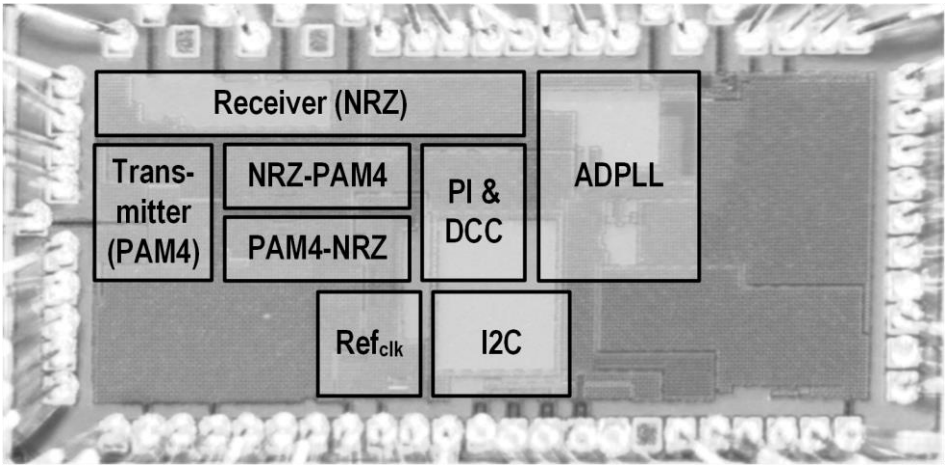
Chapter 4

Measurement Results

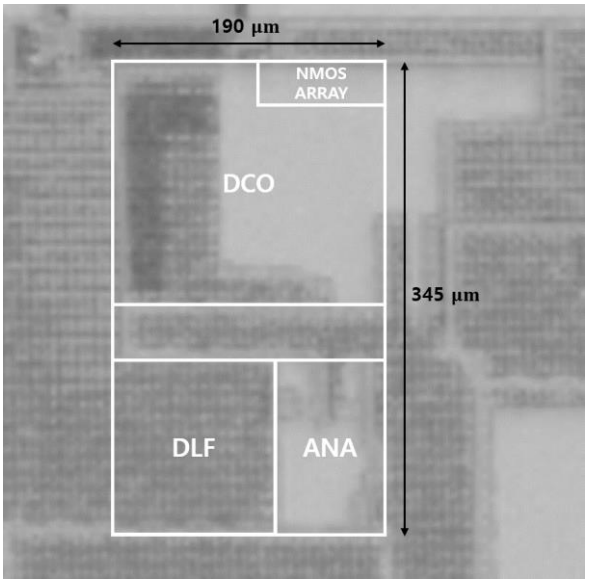
4.1 Chip Photomicrograph

Figure 4.1 shows the die photomicrograph of the PAM4-Binary Bridge and the proposed ADPLL. The proposed ADPLL with the Supply Noise-Insensitive Ring DCO is fabricated in the 40-nm CMOS technology with 0.9 V supply voltage, occupying an active area of 0.06 mm^2. Although the NMOS Shunt Regulator Transistors Array takes 0.0017 mm^2, it does not require additional area, just removing a few decoupling capacitors. The overall power consumption of the ADPLL is 13.5 mW and the Supply Noise-Insensitive scheme only used 0.9 mW.

The other parts of the PAM4-Binary Bridge that are essential for the ADPLL operation are Reference Clock receiver and I2C control block. The I2C block is placed and routed using Verilog RTL codes.



(a)



(b)

Fig. 4.1 Chip Photomicrograph of (a) the PAM4-Binary Bridge and (b) the ADPLL

4.2 Measurement Setup

To measure the performance of the proposed DCO, the supply of the DCO is provided with an AC-coupled signal made from a DC supply (Agilent E3634A) and a function generator (Tektronix AFG 3102C) via an off-chip capacitor [19]. The actual behavior of the on-chip VDD is calculated reversely by the variance of the output clock frequency and the DCO resolution measured with a digital oscilloscope (Tektronix DPO 4054). Figure 4.2 shows the overall measurement setup. The overall measurement control was utilized by the Aardvark I2C. BaLUN translate the single output of the Vector Gen to differential clock signal, and Bias TEE modulates the common level of the reference clock.

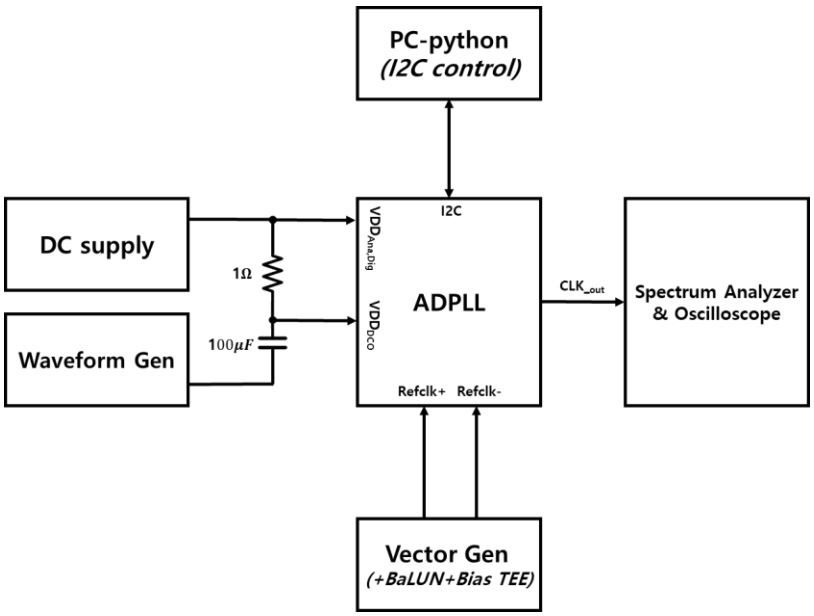


Fig. 4.2 Measurement environment setup diagram

4.3 Measurement Results

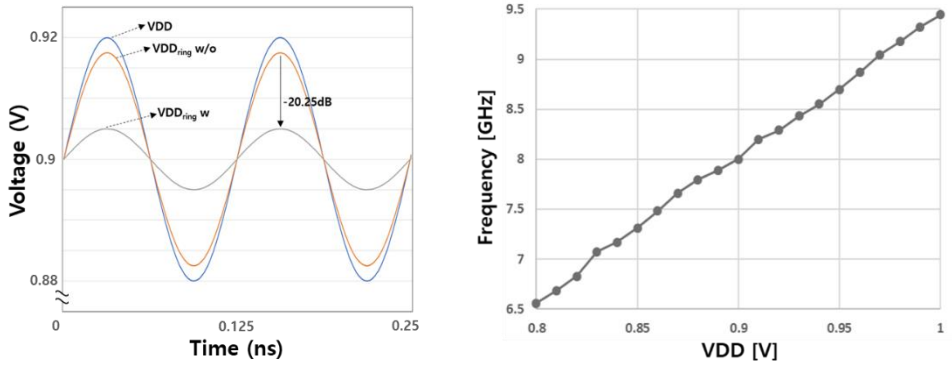
4.3.1 Free-Running DCO

(a) (b)

Fig. 4.3 Measured result of the free-running DCO output clock frequency spectrum (a) with a sinusoidal noise and (b) without the noise

As the method explained in the previous section, a 40-mVpp, 1-MHz sinusoidal supply noise is injected into the on-chip DCO supply voltage, VDD. Figure 4.3 shows the frequency spectrum of the free-running DCO with and without the NMOS Array operation. The center frequency is 5.7GHz. Compared to the spectrum shape without noise, the center frequency changes into a wide frequency band when the supply noise is injected. Nevertheless, when the proposed Supply Noise-Insensitive technique is enabled, the center frequency band is reduced to 0.19 times of the value without the technique. The result is shown in Figure 4.3(a). Although it is meaningless to measure the output Phase Noise of the free-running DCO, the frequency spectrum showed the operation of the proposed technique without loop calibration.

4.3.2 Closed-Loop Performance



(a) (b)

Fig. 4.4 (a) Simulation results of VDD and VDD_{ring} and (b) measured K_{DCO}

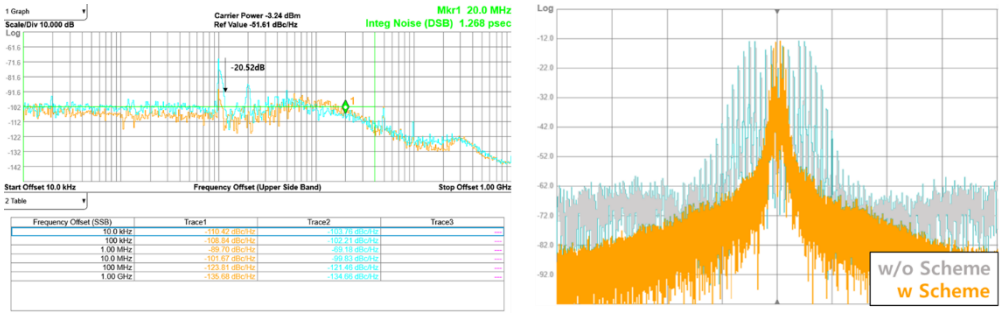
When the ADPLL is locked at the target frequency, 8GHz, the noise alleviating effect of the proposed technique is more evident with the 40-mV_{pp}, 1-MHz sinusoidal supply noise injected to the VDD by the same method in pervious section. As the simulation result shown in Figure 4.4(a), it suppresses the amplitude of VDD_{ring} from 33.3 to 12.1 mV, degraded by -20.24 dB. Without the scheme, VDD_{ring} is merely a result of the VDD divided by the DCR.

Figure 4.4(b) shows measured K_{DCO}, the resolution of the DCO frequency by the supply voltage, in the vicinity of the locked frequency. This measured result of output frequency versus supply voltage was used to derive the on-chip PSN attenuated by decoupling capacitors.

Fig. 4.5 Phase noise plot at 8 GHz without supply noise

Figure 4.5 shows the measured phase noise plot and the calculated RMS jitter without any noise injected. The calculated RMS jitter of the 8GHz output clock integrated from 10 kHz to 40 MHz is 0.58 ps. It is 0.46% of the output clock period.

Figure 4.6(a) plots the phase noise with the same sinusoidal supply noise injected. Without the technique, the total RMS jitter rises to 3.255 ps. However, the NMOS Array scheme lowered the total RMS jitter to 1.268 ps. Moreover, at the 1-MHz offset frequency, the supply-induced spur is measured as -20.52 dB. Figure 4.6(b) also shows the same effect on the frequency spectrum as the free-running DCO.



(a) (b)

Fig. 4.6 (a) Phase noise plot and (b) frequency spectrum with supply noise

4.4 Performance Summary

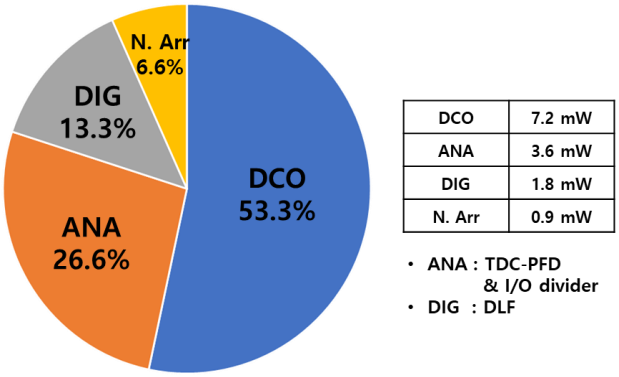


Fig. 4.7 Power breakdown of the proposed ADPLL at 8 GHz operation

Figure 4.7 shows the power consumption ratio of the ADPLL while it operates at 8 GHz. The TDC-PFD and the input/output divider are marked as ANA, and the Digital Block including the DLF is marked as DIG. As a simplified model for the supply noise canceling circuit, the proposed NMOS Array and the SSA occupies only 6.6% of the total power consumption.

Table 4.1 shows the performance summary of the proposed ADPLL and its comparison with previously introduced works. The proposed scheme showed the smallest area and power consumption with the largest noise cancellation. The FoM follows the equation below.

$$FoM = 10log\{\left(\frac{\sigma_{RMS}}{1s}\right)^2 (\frac{Power}{1mW})\} \quad (4.1)$$

Table 4.3 Performance summary and comparison

	JSSC'11 [20]	ISSCC'14 [21]	ISSCC'14 [22]	ISSCC'16 [12]	VLSI'17 [23]	CICC'18 [11]	This work
Technology (nm)	130	20	40	40	65	65	40
Reference (MHz)	625	25	26	200	50	49.15	**4000**
Output (GHz)	2.5	1.6	2.418	3.2	3.2	2.36	8
Supply (V)	1	0.9	1.1	1.1	1	0.94	0.9
Number of output phase	6	8	4	N/A	10	N/A	**8**
Total Power Consumption (mW)	3.1	3.1	6.4	2.92	2.73	5.86	13.5
Power Consumption of calibration circuit (mW)	0.24 (7.7%)	N/A	N/A	N/A	0.45 (16.5%)	N/A	0.9 (**6.6%**)
Calibration	background	self-biased	background	background	background	feed-forward	self-biased
RMS jitter w/o supply noise (ps)	4.6	5.83	N/A	3.54	7.5	0.63	0.58
RMS jitter w supply noise (ps) (w/o calibration)	8	N/A	N/A	N/A	14.1	N/A	3.255
RMS jitter w supply noise (ps) (w calibration) (decrease rate)	4.8 (40%)	5.89	3.29	3.85	7.8 (45%)	N/A	1.268 (**61%**)
Supply noise	20 mVpp white noise	5-MHz 50 mVpp sinusoidal	1-MHz 1 mVpp sinusoidal	0.1-MHz 50 mVpp sinusoidal	0.5-MHz 20 mVpp sinusoidal	0.1-MHz 1 mVpp sinusoidal	1-MHz 20 mVpp sinusoidal
FoM	-221.8	-219.8	-221.6	-224.4	-218.1	-236.3	**-226.9**
area (mm^2) (calibration circuit)	0.08	0.012	0.013	0.022	0.047	0.022	0.06 (**0.0017**)

Chapter 5

Conclusion

In this paper, an ADPLL with the self supply-regulating DCO technique is presented. By implementing simple SSA and the NMOS shunt regulator transistors array parallel to the RO, voltage headroom is lowered and supply noise robustness is improved. The transconductance of the NMOS array is modified by the row control bit of the DCR, which enables the NMOS array to track the supply noise no matter what the output clock frequency is. Moreover, the mechanism allows the technique over PVT variation.

The proposed technique is fabricated with the 40-nm CMOS technology. The quantitative analysis shows the technique reducing center frequency deviation to 0.19 times in free-running mode and the RMS jitter from 3.255 to 1.268 ps in closed loop locked mode. The proposed supply noise insensitive scheme only occupied the area of 0.0017 mm^2 and the power of 0.9 mW, which are 6.6% and 2.8% of the total ADPLL block, respectively.

Bibliography

[1] Jihee Kim. (2022). “Design of High-Speed Transmitter for Built-Out Self-Test of LPDDR5.”, (Masters dissertation). Seoul National University, Korea.

[2] Daeho Yun, Eonhui Lee, Woosong Jung, Kahyun Kim, Kyungmin Baek, and Deog-Kyoon Jeong, “A 32-Gb/s PAM4-Binary Bridge with Sampler Offset Cancellation for Memory Testing.”, *IEEE Transactions on Circuits and Systems II*, Apr. 2022

[3] B. Kim. (2019). “Design of 5/8GHz Dual Mode All-Digital Phase-Locked Loop using Direct Path.”, (Masters dissertation). Seoul National University, Korea.

[4] P. Dudek, et al., “A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line.”, *IEEE Journal of Solid-State Circuits*, vol. 35, no.2, pp. 240-247, Feb. 2000.

[5] Tierno, J.A. “A wide power supply range, wide tuning range, all static CMOS all digital PLL in 65 nm SOI.”, *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 42–51, Jan. 2008.

[6] D.-H. Oh, K.-J. Choo and D.-K. Jeong. “Phase-frequency detecting time-to-digital converter.” *Electronics Letters*, vol. 45, no. 4, Feb. 2009.

[7] B. Razavi, “The Ring Oscillator [a circuit for all seasons].”, *IEEE Solid-State Circuits Magazine*, vol. 11, no. 4, pp. 10-81, Nov. 2019.

[8] A. Arakali, S. Gondi and P. Kumar Hanumolu, “Low-power supply-regulation techniques for ring oscillators in phase-locked loops using a split-tuned architecture.”, *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2169-2181, Aug. 2009.

[9] W. Grollitsch et al., "A 1.4ps RMS-period-jitter TDC-less fractional-N digital PLL with digitally controlled ring oscillator in 65nm CMOS.", *IEEE Int. Solid-State Circuits Conference (ISSCC)*, Dig. Tech. Papers, pp. 478-479, Feb. 2010.

[10] S. Min, T. Copani, S. Kiaei and B. Bakkaloglu, "A 90-nm CMOS 5-GHz Ring-Oscillator PLL With Delay-Discriminator-Based Active Phase-Noise Cancellation.", *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1151-1160. May, 2013.

[11] S. S. Nagam and P. R. Kinget, "A −236.3dB FoM sub-sampling low-jitter supply-robust ring-oscillator PLL for clocking applications with feed-forward noise-cancellation.", *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, Apr. 2017.

[12] C. Yeh, C. Hsieh and S. Liu, "A 3.2GHz digital phase-locked loop with background supply-noise cancellation.", *IEEE Int. Solid-State Circuits Conference (ISSCC)*, Dig. Tech. Papers, pp. 332-333, Feb. 2016.

[13] C. Tien and S. Liu, "A Digital Phase-Locked Loop With Background Supply Voltage Sensitivity Minimization.", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 6, pp. 1830-1839, June 2018.

[14] W. Kim. (2014) “Synthesis of Low Noise All Digital PLL”, (Doctors dissertation). Seoul National University, Korea.

[15] W. Bae. "CMOS Inverter as Analog Circuit: An Overview", *Journal of Low Power Electronics and Applications 9*, no. 3: 26., 2019.

[16] B. Razavi, "The Delta-Sigma Modulator [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 10-15, Jun. 2016.

[17] W. Bae, H. Ju, K. Park, S. -Y. Cho and D. -K. Jeong, "A 7.6 mW, 414 fs RMS-Jitter 10 GHz Phase-Locked Loop for a 40 Gb/s Serial Link Transmitter Based on a Two-Stage Ring Oscillator in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2357-2367, Oct. 2016.

[18] D.-H. Oh, D.-S. Kim, S. Kim, D.-K. Jeong, and W. Kim, "A 2.8Gb/s All-Digital CDR with a 10b Monotonic DCO", *IEEE Int. Solid-State Circuits Conference (ISSCC)*, Dig. Tech. Papers, pp. 222-598, Feb. 2007.

[19] H. Kim, and D. -K. Jeong, "A Low-Jitter 8-GHz RO-Based ADPLL With PVT-Robust Replica-Based Analog Closed Loop for Supply Noise Compensation," *in IEEE Journal of Solid-State Circuits*, vol. 57, no. 6, pp. 1712-1722, Jun. 2022.

[20] A. Elshazly et al., "A 0.4-to-3 GHz digital PLL with PVT insensitive supply noise cancellation using deterministic background calibration," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2759–2771, Dec. 2011.

[21] J. Liu et al., "A 0.012 mm2 3.1 mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walkingone-phase-selection fractional frequency divider," *IEEE Int. Solid-State Circuits Conference (ISSCC)*, Dig. Tech. Papers, Feb. 2014, pp. 268–269.

[22] Y.-C. Huang et al., "17. A 2.4 GHz ADPLL with digital-regulated supply-noise-insensitive and temperature self-compensated ring DCO," *IEEE Int. Solid-State Circuits Conference (ISSCC)*, Dig. Tech. Papers, Feb. 2014, pp. 270–271.

[23] D. Kim and S. Cho, "A supply noise insensitive PLL with a rail-torail swing ring oscillator and a wideband noise suppression loop," *Proc. IEEE Int. Symp. VLSI Circuits*, Dig. Tech. Papers, Jun. 2017, pp. C180–C181.

초 록

고속 DRAM 과 저속 검사 장비를 연결하는 4 단계 펄스 진폭 변조-2 진법 브리지 칩의 주요 구성 회로 중에 디지털 위상 동기 회로가 있다. 이 회로가 검사 장비에서 온 참조 클락의 진동수를 2 배로 빠르게 하여 출력하고, 그 클락을 기준으로 칩의 송수신 회로들이 동작하기 때문에 낮은 RMS 지터와 공정-전압-온도 변화에 둔감한 성능이 요구된다. 하지만, 칩의 복잡한 회로들 때문에 고리 발진기를 기반으로 한 이 회로에게 전원 전압 잡음이 가장 큰 문제점이 된다.

본 논문은 전원 잡음에 둔감한 고리 발진기를 기반으로 한 디지털 위상 동기 회로를 제안한다. 전원 잡음을 흡수하는 단락 레귤레이터 역할의 31-비트 NMOS 트랜지스터 배열이 고리 발진기와 평행하게 구현되었다. 디지털 제어 저항을 조절하는 디지털 루프 필터에서 온 행 조정 비트들이 NMOS 트랜지스터 배열의 트랜스컨덕턴스도 조절하게 디자인하였다.

제안된 디지털 위상 동기 회로는 40-nm CMOS 공정으로 제작되었다. 0.06 mm^2 의 면적을 차지하고 13.5 mW 의 전력을 소모하며, 고안된 전원 잡음 흡수 회로는 각각 0.0017 mm^2 와 0.9mW, 즉, 전체의 6.6%와 2.8%만 차지하였다. 8GHz 동작에서, 제안된 회로는 1-MHz 40-mV_{pp} 사인파 전원 잡음 아래에서 3.255 ps 의 RMS 지터를 보였지만, 고안된 회로의 동작과 함께 1.268 ps 로 줄었다.

주요어 : 디지털 위상 동기 회로, 전원 잡음, 고리 발진기, 전원 잡음 둔감성

학 번 : 2021-21172