Ph.D. DISSERTATION

Implementation of 1-bit Erase in Vertical NAND Flash Memory

적층형 수직 낸드 플래시 메모리에서 1비트 지우기 구현

by

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DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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ABSTRACT

NAND flash memory is non-volatile memory and has the advantage of high density. For higher density, more bits of data are stored in one NAND flash cell or stacked vertical NAND flash technology in which channels are aligned vertically is developed. To store more bits of data in the limited program/erase window, it is necessary to make a narrower memory cell V_{th} distribution. For narrower V_{th} distribution, longer program times and stronger error correction codes are required. A method for overcoming a difference in cell characteristics between an upper word line and a lower word line while increasing the number of WL stacks in a NAND flash memory is required. In addition, NAND flash memory has a matured process, so it has a great advantage as a synaptic device for neuromorphic computing. A synaptic device stores the weights of a neural network, and a NAND flash memory is a non-volatile memory and has a long lifetime, so it is suitable for a synaptic device. However, it is difficult to accurately adjust the bit line current representing the weight of neural network with the existing program/erase method.

In this dissertation, an operation of selectively erasing NAND flash memory cells is proposed and analyzed to overcome the disadvantages while using the advantages of NAND flash memory. In a stacked vertical NAND flash memory array, the erase operation of the selected cell and the erase suppression of the unselected cell are successfully verified by adjusting the voltage at each terminal. As a result of measurement and simulation, it is revealed that the gate induced drain leakage (GIDL) characteristic due to the DSL/SSL gate bias condition has a great influence on the erase operation. The proposed 1-bit erase operation can modify data or reduce the V_{th} distribution by changing the V_{th} of the memory cell in parallel with the traditional program operation without changing the process and structure of the vertical NAND flash memory array. Differences in the characteristics of vertical NAND flash memory cells depending on word line position can be overcome by using a 1-bit erase operation. Also, when using a NAND flash memory cell as a synaptic device, the bit line current dispersion is reduced by 17 times compared to the previous method.

Keywords: Vertical NAND flash memory, erase operation, gate-induced drain leakage (GIDL), 1-bit erase, I_{BL} (or V_{th}) dispersion

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CONTENTS

List of Figures

List of Tables

Chapter 1
Introduction

1.1 NAND Flash Memory Program/Erase Operation

NAND flash memory is the mainstream of non-volatile memory and has the advantages of low cost and high density. A stacked vertical NAND (VNAND) flash memory technology in which the channels are aligned vertically for higher density has been developed. Fig. 1.1 shows the structure of VNAND flash memory. The WLs (Word Lines) are stacked horizontally, and the channels are vertically aligned. BLs (Bit Lines) are at the top of the WL stack, and SL (Source Line) is connected at the bottom. SLs are tied together to minimize resistance. DSL (Drain Select Line) and SSL (Source Select Line) are placed adjacent to BL and SL, respectively, and serve as a select line. A block of NAND flash is a unit of cells bundled with BLs and WLs, and one SSL selects one block.

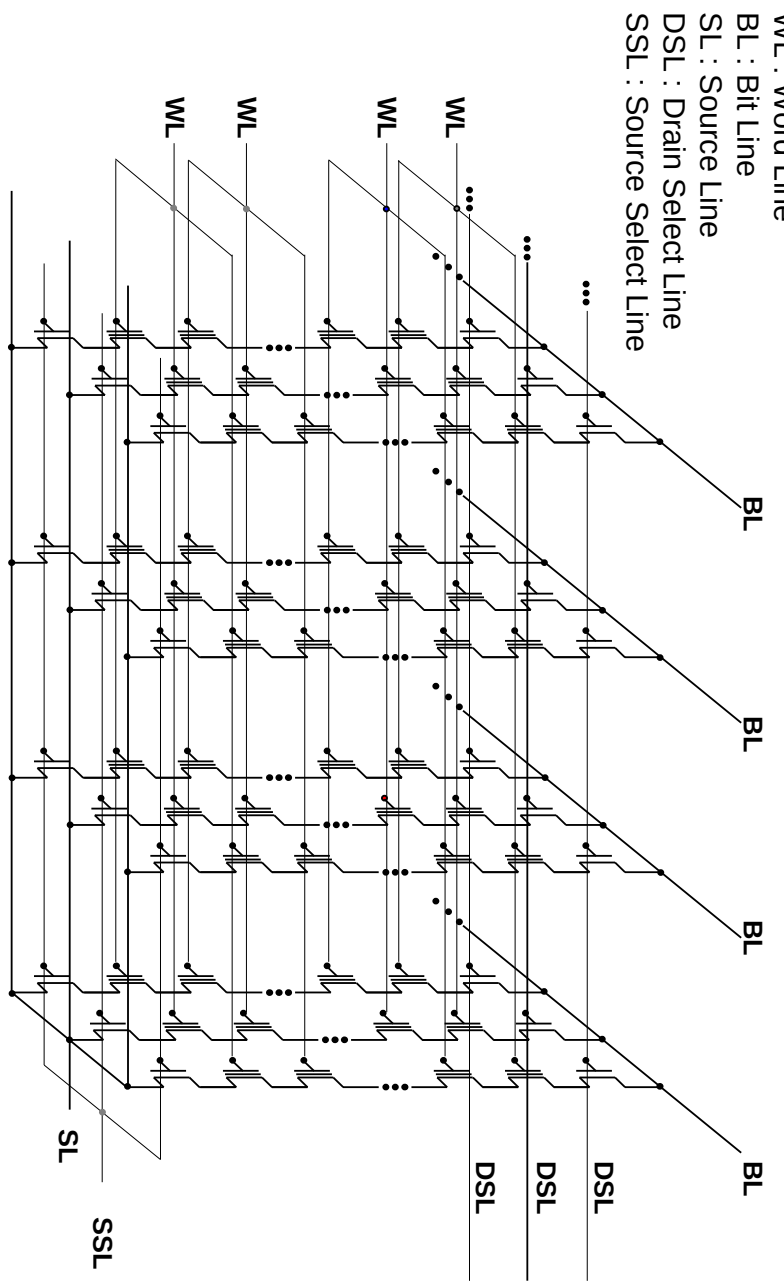

Fig. 1.1. Structure of vertical NAND flash memory

Fig. 1.2 shows the program operation conditions in VNAND flash memory. The program operation is a selective operation that increases only the V_{th} of the selected cell. The high voltage of V_{PGM} is applied to the selected WL connected to the selected cell. 0 V is applied to the selected BL to which the string of the selected cell is connected. To transfer the potential of the selected BL to the channel of the selected cell, a low voltage of V_{Pass} is applied to unselected WLs. V_{CC} is applied to the selected DSL to select a string in which the selected cell is located. To minimize the ΔV_{th} of unselected cells, channel boosting method is used to reduce the potential difference between the selected WL and unselected string. For channel boosting, V_{CC} is applied to unselected BLs and 0 V is applied to unselected DSLs. Apply V_{CC} to the SL which is connected to all strings to prevent the reduction of boosted channel potential and 0 V is applied to the SSL to minimize the influence of the V_{SL}.

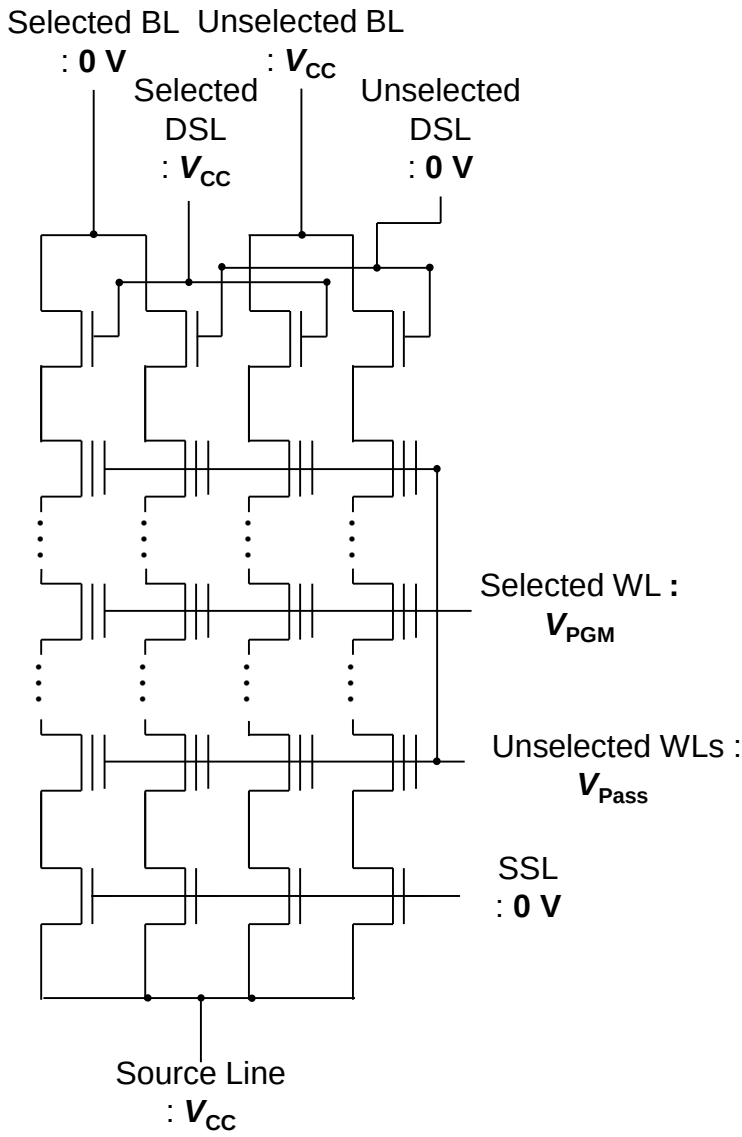

Fig. 1.2. Program operation conditions of VNAND flash memory

Fig. 1.3 shows the erase operation conditions of NAND flash memory. The erase operation of the NAND flash memory does not lower only the V_{th} of a specific cell. Block erase operation that lowers the V_{th} of the cells in a block is performed. In the planar NAND flash memory structure where the channel is located in the p-well, a high voltage of V_{Erase} is applied to the well, and 0 V is applied to the WLs (Fig. 1.3 (a)). The hole carrier for the erase operation is supplied from the p-well and enters the floating gate through FN tunneling to reduce the V_{th} of the cells. BL, SL, DSL, and SSL are floating to prevent breakdown at high potential during erase operation. On the other hand, in VNAND flash memory, the channel stands vertically and there is no p-well. So, hole carriers for erase operation are supplied through GIDL (Gate Induced Drain Leakage). The voltage to BL and SL is V_{Erase}, and V_{DSL} (or V_{SSL}) applied to DSL (or SSL) is lower than V_{Erase} (Fig. 1.3 (b)). GIDL is occurred by the potential difference between BL and DSL and SL and SSL, and hole carriers are generated by GIDL. By applying 0V to the WLs, hole carriers enter the Si_3N_4 layer by FN tunneling.

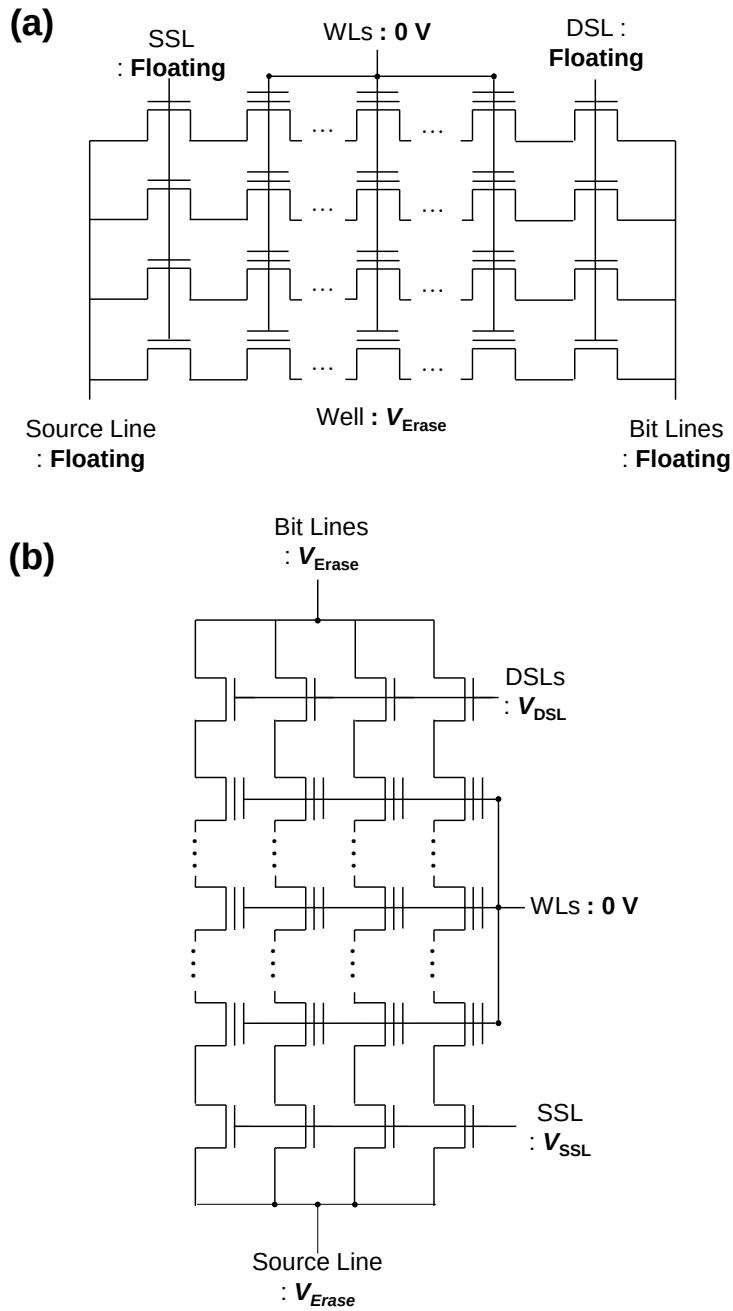

Fig. 1.3. Erase operation conditions of (a) planar NAND flash memory (b) VNAND flash memory

Fig. 1.4 shows the erase pulse diagram of VNAND flash memory. Pulses applied to BL and SL and pulses applied to DSL and SSL are applied at different times to stably generate hole generation by GIDL. In the previous studies, GIDL hole generation had a great effect on the erase characteristics of VNAND [1,2]. In the case of insufficient hole generation, the V_{th}s of the cells after erase operation are not sufficiently lowered, resulting in wide and distorted V_{th} distribution [2]. The wide and distorted V_{th} distribution after the erase operation requires a higher V_{Erase} to make every flash memory cell erased. Higher V_{Erase} to erase a few cells causes poor retention characteristics of VNAND flash memory cells [2,3].

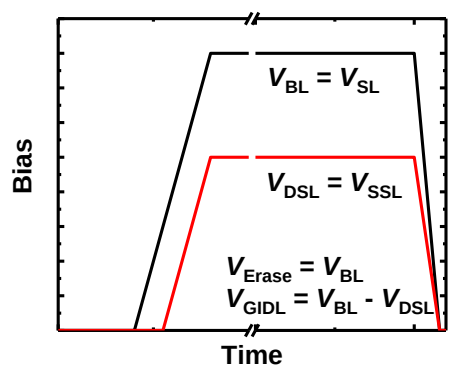

Fig. 1.4. Pulse diagram of VNAND flash memory

1.2 Demand for 1-bit Erase and Previous Works

As mentioned before, commercial NAND flash memory uses a block erase operation that simultaneously erases all cells in a block to lower the V_{th} of the cells. Recently, as the number of WL stacks of VNAND flash memory increases, the block size increases, and the size of data erased by the block erase operation increases. In addition, as the density of memory increases, it becomes important to reduce the V_{th} dispersion of cells. Therefore, a 1-bit erase operation that selectively lowers the V_{th} of a specific cell of a NAND flash memory has been required. In this chapter, we explain the demand for 1-bit erase operation in NAND flash memory.

NAND flash memory has been developed to store more data in one cell. To store more data in one cell, narrower V_{th} distribution must be made in the limited program/erase window. Fig. 1.5 and Table 1 show that the program time increases significantly for more bits/cell. The reason for the longer program time is that it is difficult to make a narrower V_{th} distribution using only ISPP (Incremental Step Pulse Program). However, in previous studies, there is a report that there is a limit to making the V_{th} distribution using only the program operation [4]. Compagnoni et

al. [4] reported the ‘ultimate accuracy’ of NAND flash memory due to electron injection statistics at program operation. Therefore, for a narrower V_{th} distribution, it is necessary to make the ISPP step smaller than the required V_{th} distribution, and the program operation time becomes longer. Even if data is written to the memory using a long program operation time, errors that occur can only be overcome by using ECC (Error Correction Code). The 1-bit erase operation can improve the ‘ultimate accuracy’ of NAND flash memory without the help of ECC by correcting errors that occur at program operation.

In addition, the 1-bit erase operation can be used in an algorithm to improve the retention characteristics of NAND flash memory. Cai et al. [6] proposed the reprogram algorithm to improve the retention characteristics of NAND flash memory by increasing V_{th} of cells after retention V_{th} shift. Data in NAND flash memory is stored as cell V_{th}. As the electrons stored in the floating gate or Si_3N_4 layer escape, the V_{th} of the cells decreases after some time. Data errors due to cell V_{th} shift can be eliminated through reprogram operation. However, the reprogram algorithm has limitations. When the number of cells whose V_{th} increases too much

during program operation increases, a block erase operation must be performed and the stored data must be moved to another new memory cell. The 1-bit erase operation can reduce the V_{th} of cells whose V_{th} increases too much at the reprogram operation, thereby improving the retention characteristics of the memory.

The 1-bit erase operation plays an important role when NAND flash memory is used as a synaptic device in neuromorphic computing. Burr et al. [7] reported the performance of neural networks depending on the characteristics of synaptic devices. NAND flash memory is a uni-directional device that can only be programmed, and neural networks using uni-directional devices show a characteristic that performance improves during learning and then deteriorates when learning continues. On the other hand, the performance of a neural network using bi-directional devices that can be freely programmed and erased improves as training continues. Therefore, when the NAND flash memory becomes a bi-directional device through a 1-bit erase operation, it has good characteristics as a synaptic device of neuromorphic computing. Hsu et al. [8] also proposed a neural network that stores the trained weights in flash memory. The weight transfer using

only program operation showed the result that I_{BL} variation increased as target I_{BL} increased. In neuromorphic computing, which calculates VMM (Vector Matrix Multiplication) through current sum, I_{BL} variations of synaptic devices that store large weight values can affect neural network performance.

To utilize the advantages of NAND flash memory and overcome the aforementioned disadvantages, research on 1-bit erase operation has been conducted. Wang et al. [9,10] proposed 1-bit erase operation in VNAND structure using FeFET (Ferroelectric Field Effect Transistor). In the case of FeFET, the erase operation is performed using only the potential difference of WL and the channel without putting hole carriers in the ferroelectric material layer. Therefore, 0 V is applied to the selected WL and a high voltage is applied to the selected BL for 1-bit erase operation. However, the erase operation was implemented in the fabricated 2D NAND structure without fabricating the VNAND structure. In addition, only the states of the cell are shown after the erase operation without any results on the I_{BL} and V_{th} changes of the cell. Furthermore, it is difficult to significantly change the structure of commercial VNAND flash memory using charge trap devices.

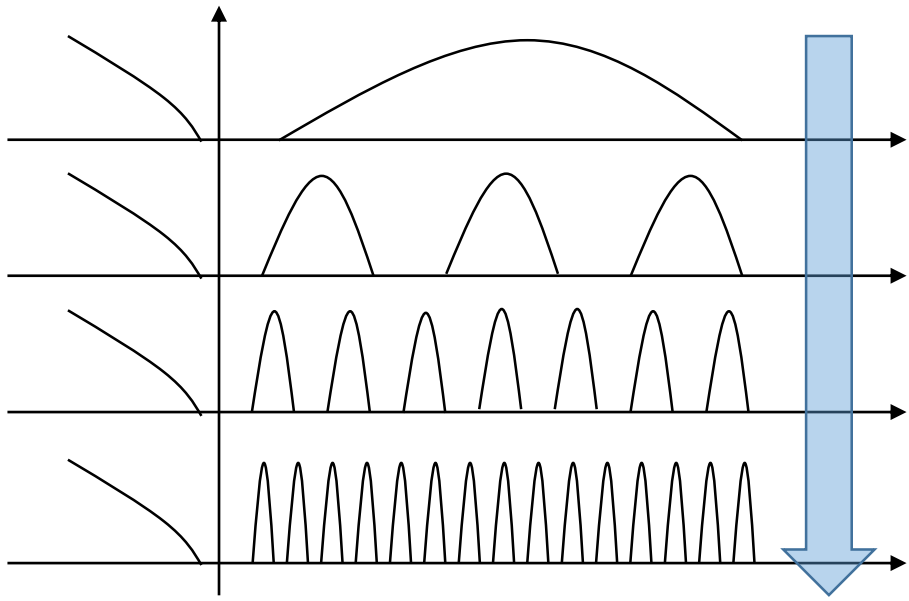

Fig. 1.5. Description of NAND flash memory development from SLC to QLC

Operation Time	Flash cell technology			
	SLC	MLC	TLC	QLC
Density	1 Gb–256 Gb	16 Gb–2 Tb	128 Gb–8 Tb	1 Tb–16 Tb
Page read	20–25 µs	55–110 µs	75–170 µs	120–200 µs
Page program	50–100 µs	0.4–1.5 ms	0.8–2 ms	2–3 ms
Block erase	2–5 ms	5–10 ms	10–15 ms	15–20 ms

Table 1.1. Operation time of NAND flash cell memory technology [5]

1.3 Purpose of Research

As described above, the stacked vertical NAND flash memory has a mature process that can be commercialized and mass-produced. A multi-bit operation that stores a lot of data in one cell is implemented. In addition, it has high scalability through small cell size and vertical channels and has good reliability characteristics such as retention and endurance. However, there is a limitation in that the erase operation reduces the V_{th} of all cells in the block. The reason why there is only Block erase operation is that the erase operation time of NAND flash memory is much longer than the program operation, so writing new data to other WL is faster than erasing and revising data of 1WL. In addition, research on erasing a flash memory cell remotely by applying bias to VNAND terminals far from the memory cell has been lacking. Unlike planar NAND flash memory, which erases using Well, VNAND's erase operation using BL/SL and DSL/SSL terminals can remotely select a specific flash memory cell in 3D.

In this study, we propose and analyze a selective 1-bit erase operation that lowers only the V_{th} of the selected cell in VNAND flash memory. The erase characteristics

of VNAND are measured under various conditions. The measured results are analyzed through simulation and factors affecting the erase of VNAND are analyzed. Based on the measured erase characteristics, 1-bit erase operation is proposed and the characteristics of the 1-bit erase operation are measured. The erase inhibition properties are measured by measuring the V_{th} and I_{BL} of the unselected cells while changing the V_{th} and I_{BL} of the selected cell. The I_{BL} distribution of the cell is measured using the implemented 1-bit erase and compared with the previous method. In addition, the cell characteristics which differ depending on the WL position of VNAND are compared with the case where 1-bit erase is used and the case where it is not.

1.4 Dissertation Outline

This dissertation proceeds in the following order. Chapter 1 describes the program/erase operation of VNAND, the demand for 1-bit erase operation and the results of previous research. Chapter 2 describes the erase characteristics of VNAND. The erase characteristics are measured while adjusting the voltage applied to each terminal of VNAND. The simulation result shows the measured result well, and through this, it shows the analysis result for the erase characteristics of VNAND. Chapter 3 implements 1-bit erase operation based on the results of Chapter 2 and shows the characteristics of 1-bit erase. It shows the inhibition characteristics of 1-bit erase operation and the characteristics of VNAND when 1-bit erase is used. Finally, chapter 4 summarizes the thesis.

Chapter 2
Erase Characteristics of Vertical NAND Flash Memory

2.1 Comparison of Block, 1WL, Negative Bias Erase

Commercial NAND flash memory does not have erase operation that reduces only the V_{th} of a specific cell, block erase operation that erases all cells in block units at once is used to reduce the V_{th} of cells for which program operation has been completed. A block is a unit of erase operation and is a set of cells connected to all WLs and BLs and is classified as SSL in VNAND. Fig. 2.1 (a) shows the block erase condition of VNAND. The pulse diagram of block erase is the same as described in Fig. 1.4. 0 V is applied to all WLs to lower the V_{th} of cells in all WLs. To lower only the V_{th} of a specific cell, first, 1WL erase, which lowers only the V_{th} of the cells of the selected WL, is measured. 1WL erase uses the same pulse diagram as block erase, 0 V is applied to the selected WL, and $V_{Unsel.WL}$ is applied to the rest of the unselected WLs.

Fig. 2.1 (b) shows ΔV_{th}s (=V_{th} after erase operation – V_{th} before erase operation) of the cell after block erase and 1WL erase. The selected cell is programmed with V_{th} 4 V before erase operation. For both block erase and 1WL erase, $|\Delta V_{th}|$ increases as V_{Erase} increases. Comparing $|\Delta V_{th}|$ after block erase and 1WL erase, $|\Delta V_{th}|$ after 1WL erase is smaller than $|\Delta V_{th}|$ after block erase. The reason for smaller $|\Delta V_{th}|$ is that FN tunneling is reduced by smaller potential difference between the channel and the selected WL due to the influence of $V_{Unsel.WL}$ is applied to the adjacent WLs.

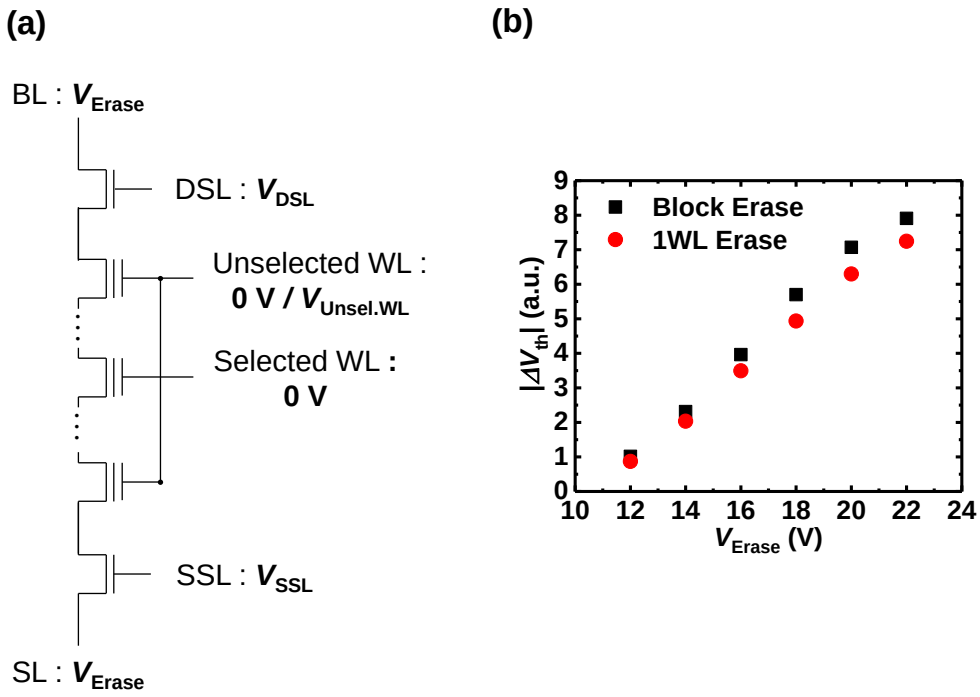

Fig. 2.1. (a) Bias conditions of block, 1WL erase operation (b) comparison of $|\Delta V_{th}|$ after block and 1WL erase operation. ΔV_{th} represents the difference in V_{th} before and after erase operation (ΔV_{th} =V_{th} after erase operation – V_{th} before erase operation)

Fig. 2.2 shows $|\Delta V_{th}|$s of the cell of the unselected WLs depending on $V_{Unsel.WL}$ at 1WL erase. The cells of the unselected WL are divided into cells with low V_{th} (erased cells) and cells with high V_{th} (programmed cells). After 1WL erase, $|\Delta V_{th}|$s of the cells in the unselected WLs is measured. When $V_{Unsel.WL}$ is too low, V_{th} of programmed cells decreases due to high channel potential. On the other hand, When $V_{Unsel.WL}$ is too high, and the WL potential is much higher than the channel potential, so electrons enter the Si_3N_4 layer and the V_{th} of erased cells increases. From the measured results, when the $V_{Unsel.WL}$ is between 6 V and 8 V, the V_{th} of the cells in unselected WL does not change.

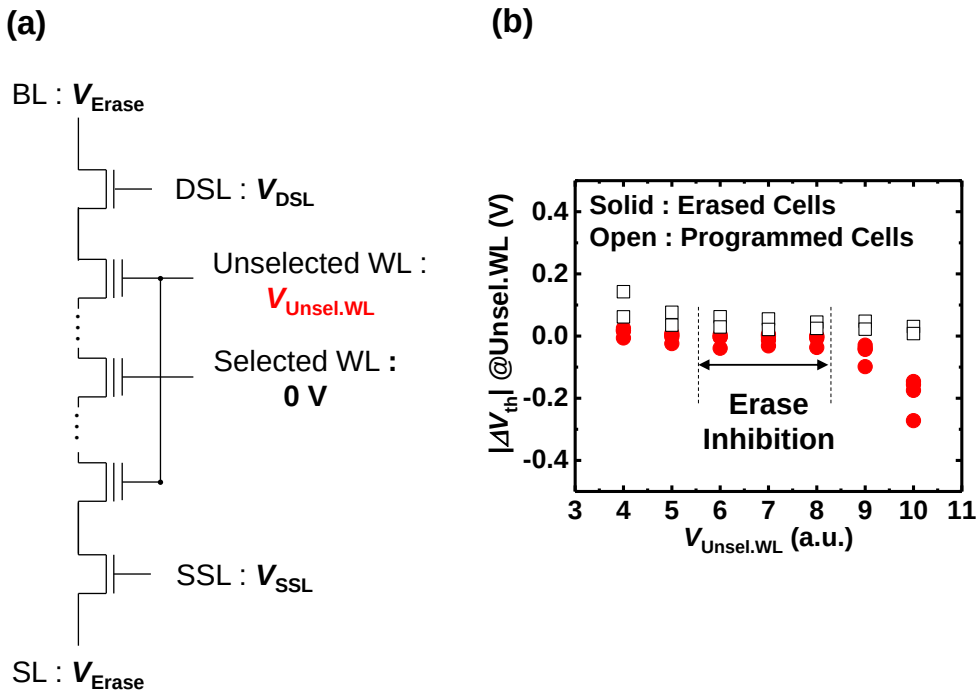

Fig. 2.2. (a) Bias conditions of 1WL erase operation for the effect of $V_{\mathrm{Unsel.WL}}$ (b) $|\Delta V_{\mathrm{th}}|$s of the cells in the unselected WLs depending on $V_{\mathrm{Unsel.WL}}$

Fig. 2.3 (a) shows the bias condition of negative bias erase. When reducing the cell V_{th} of a specific WL, it is easy to perform an erase operation by applying a negative bias to selected WL. To generate GIDL, a complicated pulse diagram is applied to BL, SL, DSL, and SSL. On the other hand, a negative voltage is applied to the selected WL and 0 V is applied to the other terminals for negative bias erase operation. Fig. 2.3 (b) shows $|\Delta V_{th}|$ after 1WL erase using GIDL (GIDL erase) and 1WL erase using negative bias. Both erase operations using GIDL and erase using negative bias occur $|\Delta V_{th}|$ which increases as V_{Erase} increases. However, erase operation using negative bias occurs smaller $|\Delta V_{th}|$ than GIDL erase, and $|\Delta V_{th}|$ does not increase above V_{Erase} of 20 V. From this result, it can be seen that negative bias erase can be performed with a simpler operation, but the efficiency of erase operation is reduced than GIDL erase.

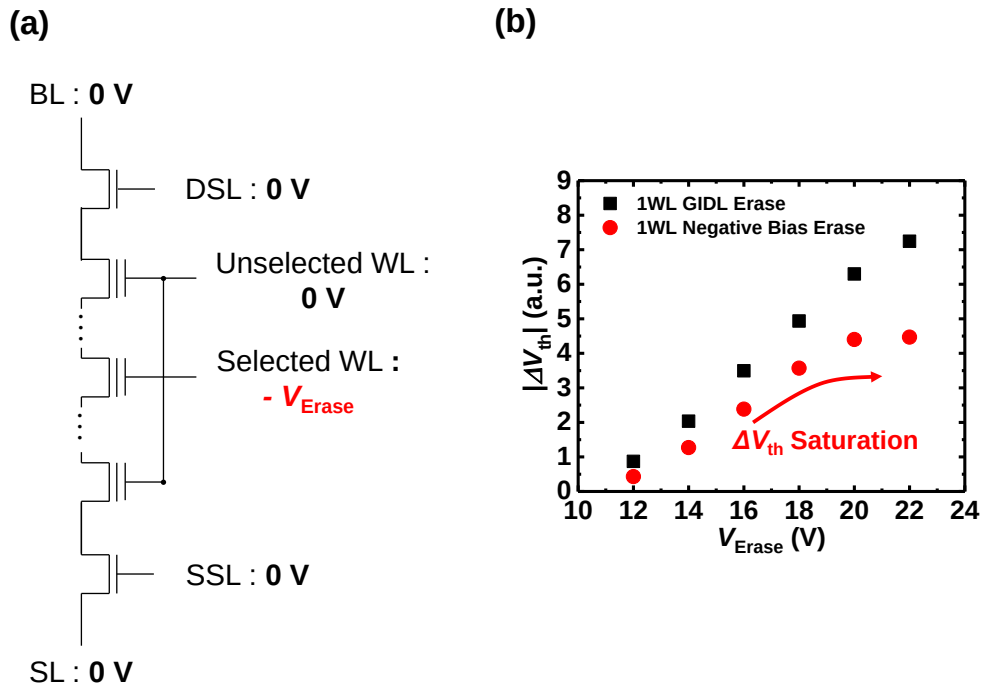

Fig. 2.3. (a) Bias conditions of 1WL negative bias erase operation (b) comparison of $|\Delta V_{th}|$s with 1WL GIDL erase and 1WL negative bias erase

Fig. 2.4 shows V_{WL}-I_{BL} curves during the 1WL negative bias erase operation in Fig. 2.3 (a). Several erase pulses are applied to verify the change of V_{WL}-I_{BL} curves. After the program, in the initial state (Fig. 2.4 (a)), after negative bias erase 1 pulse, the V_{WL}-I_{BL} curves are shown in Fig. 2.4 (b). As V_{Erase} increases, the V_{WL}-I_{BL} curves move to the left, and $|\Delta V_{th}|$ increases. However, V_{WL}-I_{BL} curves after erase operation V_{Erase} of 20 V and V_{Erase} of 22 V are almost the same (results of Fig. 2.3 (b)). However, the slope of V_{WL}-I_{BL} curve after erase operation V_{Erase} of 22 V lies further than V_{WL}-I_{BL} curve after erase V_{Erase} of 20 V. To verify slope of V_{WL}-I_{BL} curves, the same erase pulses are applied up to 10 times and V_{WL}-I_{BL} curves are compared. As shown in Fig. 2.4 (c), the slope of V_{WL}-I_{BL} curve after erase V_{Erase} of 22 V lies further compared to V_{WL}-I_{BL} curve after erase 1 pulse. Also, the slope of V_{WL}-I_{BL} curve after erase V_{Erase} of 20 V lies compared to the V_{WL}-I_{BL} curves of the other V_{Erase}. The decrease in the slope of V_{WL}-I_{BL} curves also affects the cell V_{th}. After erase operation with V_{Erase} of 22 V, cell V_{th} decreases greatly in the first erase pulse, and cell V_{th} tends to increase as the erase pulse is repeated (Fig. 2.4 (d)).

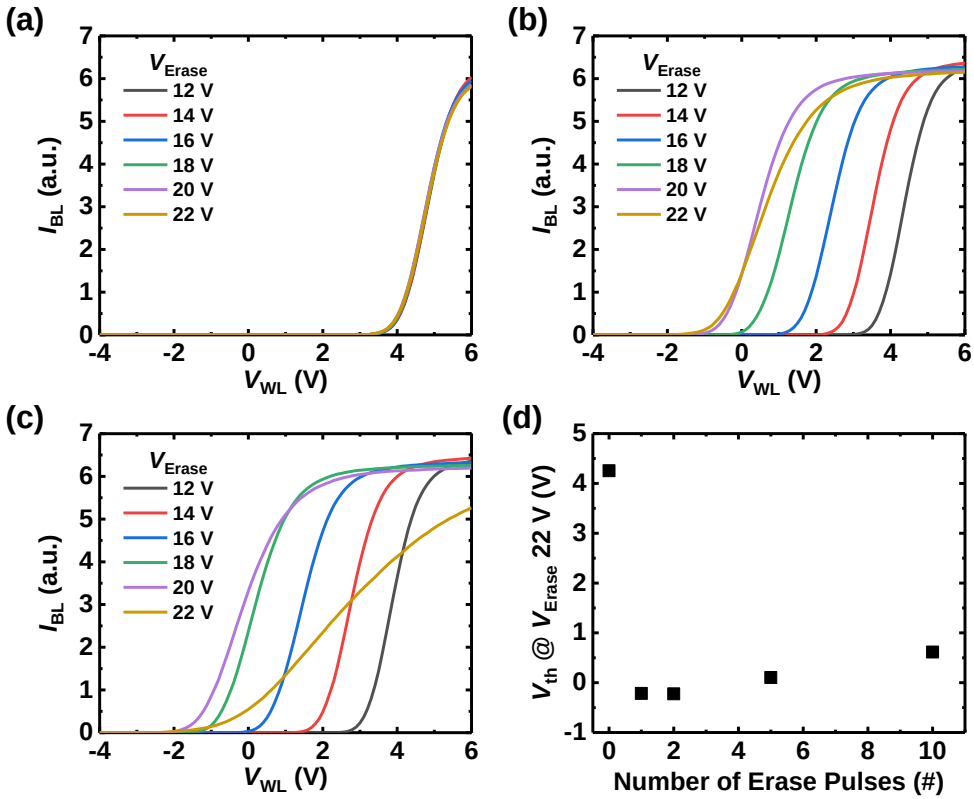

Fig. 2.4. V_{WL}-I_{BL} curves of selected WL cell depending on V_{Erase} (a) before erase operation (b) after 1WL negative erase 1 pulse (c) after 1WL negative erase 10 pulses and (d) V_{th}s after erase operation with V_{Erase} of 22 V

To analyze the characteristics of negative bias erase operation, V_{WL}-I_{BL} curves of cells in the adjacent WLs are measured. Fig. 2.5 (a) shows V_{WL}-I_{BL} curves of N-1th WL cell after programming a cell of the selected Nth WL. Since a cell of Nth WL has high V_{th}, I_{BL} of N-1th WL cell is small. When the cell of Nth WL is erased with a negative bias, I_{BL}s of N-1th WL cell increase and V_{th}s of the cell also decrease (Fig. 2.5 (b)). However, V_{WL}-I_{BL} curve after erase V_{Erase} of 22 V shows a difference from V_{WL}-I_{BL} curves of other V_{Erase}. V_{th} with V_{Erase} of 22 V is higher than V_{th}s of other V_{Erase}, and I_{BL} with V_{Erase} of 22 V is also small. Fig. 2.5 (c) shows V_{th}s of adjacent WLs cells when the cell of Nth WL is negative bias erased with V_{Erase} of 22 V. Similar to V_{th} of Nth WL cell, V_{th} decreases after 1 erase pulse, but as erase pulse is repeated, V_{th} increases. After 10 erase pulses, V_{th} becomes higher than before the Nth WL cell is erased. Even though V_{th} of Nth WL cell is lowered through erase operation, V_{th} of the adjacent cells increases and V_{WL}-I_{BL} curve also moves to the right. This result indicates that electrons enter Si_3N_4 layer of the adjacent WLs while negative bias erase operation with high V_{Erase}. Despite simple operation condition of negative bias erase, negative bias erase operation has side effects of electrons entering Si_3N_4 layer.

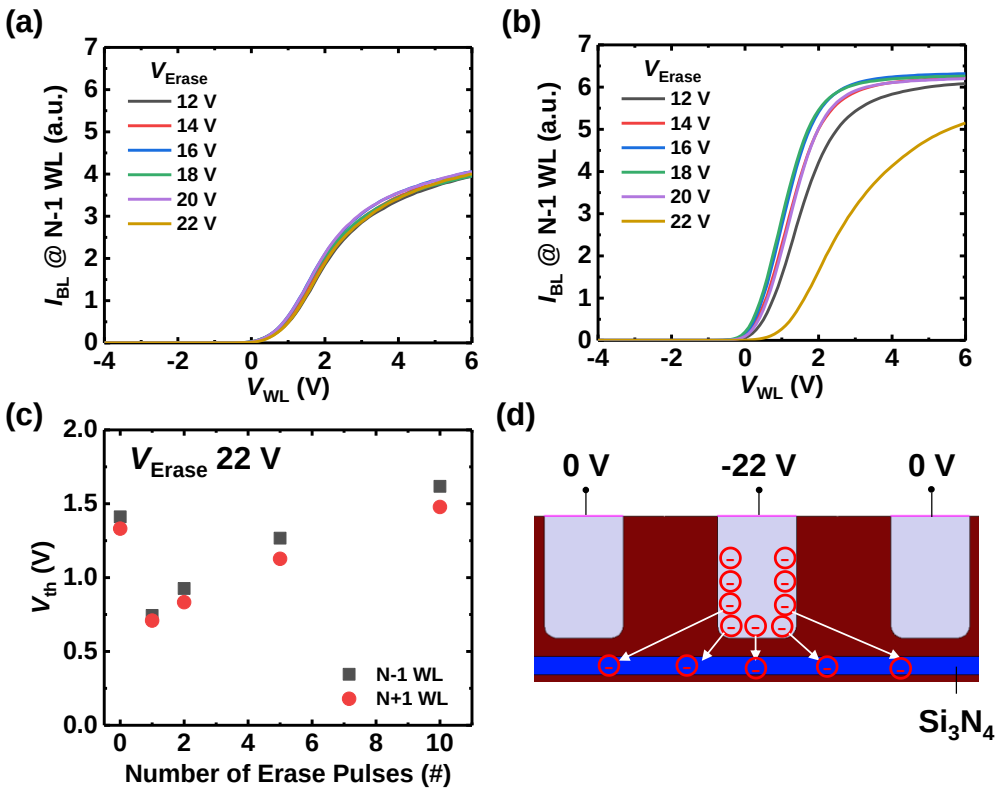

Fig. 2.5. V_{WL}-I_{BL} curves of adjacent WL cell depending on V_{Erase} (a) before erase operation (b) after 1WL negative 10 erase pulses, (c) V_{th}s of adjacent WL cells after erase operation with V_{Erase} of 22 V and (d) schematic of back tunneling due to negative bias erase

2.2 GIDL Hole Generation Conditions

In this chapter, we explain the characteristics of GIDL erase. Erase operation using negative bias is not suitable for erase operation of VNAND since $|\Delta V_{th}|$ after erase operation is smaller than GIDL erase and high V_{Erase} cannot be used. In addition, to reduce only V_{th} of the selected cell, voltage must be applied to BL, SL, DSL, and SSL, and operation complexity is expected to be similar compared to GIDL erase. Therefore, GIDL erase is more suitable for implementing 1-bit erase operation than negative bias erase.

Fig. 2.6 (a) shows the bias condition of 1 WL GIDL erase. V_{Erase} is applied to BL and SL, and V_{DSL} and V_{SSL} are applied to DSL and SSL, respectively. The potential difference between BL and DSL or between SL and SSL is V_{GIDL}. By applying 0 V to the selected WL and 6 V to the unselected WLs, minimize $|\Delta V_{th}|$ of the cells at unselected WL. Fig. 2.6 (b) shows $|\Delta V_{th}|$ after erase operation depending on V_{GIDL}. As V_{Erase} increases, $|\Delta V_{th}|$ increases. There is no difference in $|\Delta V_{th}|$ when V_{GIDL} is 6 V or higher in the same V_{Erase}. When V_{GIDL} is below 6 V, $|\Delta V_{th}|$ decreases as V_{GIDL} decreases. When V_{GIDL} is 1 V, $|\Delta V_{th}|$ is minimal. When V_{GIDL} is 0 V, $|\Delta V_{th}|$

is larger than $|\Delta V_{th}|$ at V_{GIDL} of 1 V. From this result, GIDL hole generation is expected to be very small when V_{GIDL} is under 1 V. Fig. 2.6 (c) shows $|\Delta V_{th}|$s at V_{GIDL} of 1 V, which is the minimum $|\Delta V_{th}|$ condition, and $|\Delta V_{th}|$s at V_{GIDL} of 8 V where GIDL generation occurs sufficiently. $|\Delta V_{th}|$ with V_{GIDL} of 1 V is negligible under V_{Erase} of 14 V.

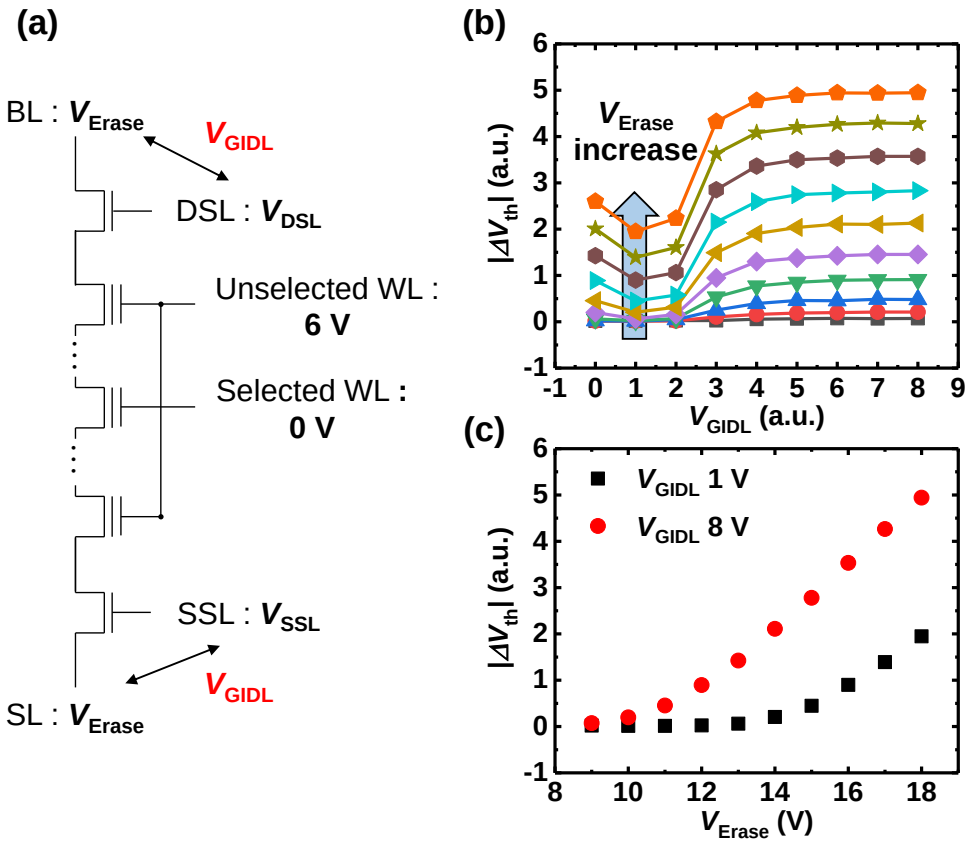

Fig. 2.6. (a) Bias conditions of 1WL GIDL erase operation for the effect of V_{GIDL} (b) $|\Delta V_{th}|$s of the cells depending on V_{GIDL} (c) $|\Delta V_{th}|$s of the cells depending on V_{Erase} at V_{GIDL} of 1 V and 8 V

Fig. 2.7 shows $|\Delta V_{th}|$ after erase operation when V_{GIDL} in the BL direction (V_{DGIDL}) and V_{GIDL} in the SL direction (V_{SGIDL}) are given differently. As we mentioned before, SL is tied in a block to reduce SL resistance. Therefore, GIDL hole generation in the SL direction must not affect the erase operation to implement 1-bit erase operation. Fig. 2.7 (b) shows $|\Delta V_{th}|$s after erase operation depending on V_{DGIDL}. When V_{SGIDL} is 6 V, V_{DGIDL} does not affect $|\Delta V_{th}|$. On the other hand, when V_{SGIDL} is 1 V, $|\Delta V_{th}|$s depend on V_{DGIDL}. It is possible to inhibit erase by applying 1 V to V_{SGIDL} and distinguishing V_{DGIDL}.

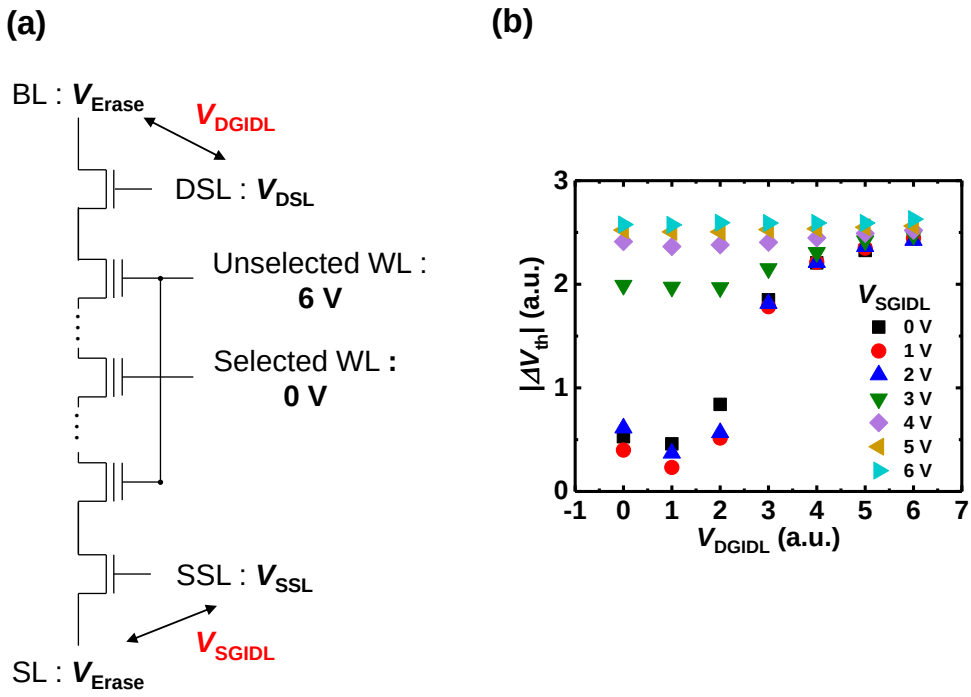

Fig. 2.7. (a) Bias conditions of 1WL GIDL erase operation for the effect of V_{DGIDL} and V_{SGIDL} (b) $|\Delta V_{th}|$s of the cells depending on V_{DGIDL} and V_{SGIDL}

Fig. 2.8 shows the $|\Delta V_{th}|$ when V_{BL} and V_{SL} are given differently. In 1-bit erase operation, V_{BL} and V_{SL} can be applied differently. Therefore, while maintaining V_{DGIDL} and V_{SGIDL} at 6 V, the effect of V_{BL} and V_{SL} is measured. Fig. 2.8 (b) shows $|\Delta V_{th}|$ after erase while maintaining V_{BL} or V_{SL} and changing the opposite side voltage. V_{BL} and V_{SL} have an equal effect on $|\Delta V_{th}|$, and when one of them decreases, $|\Delta V_{th}|$ decreases. For erase efficiency, it is necessary to apply the same voltage to V_{BL} and V_{SL}. In addition, this result indicates that erase inhibition is possible by lowering the voltage of unselected BL ($V_{Unsel.BL}$).

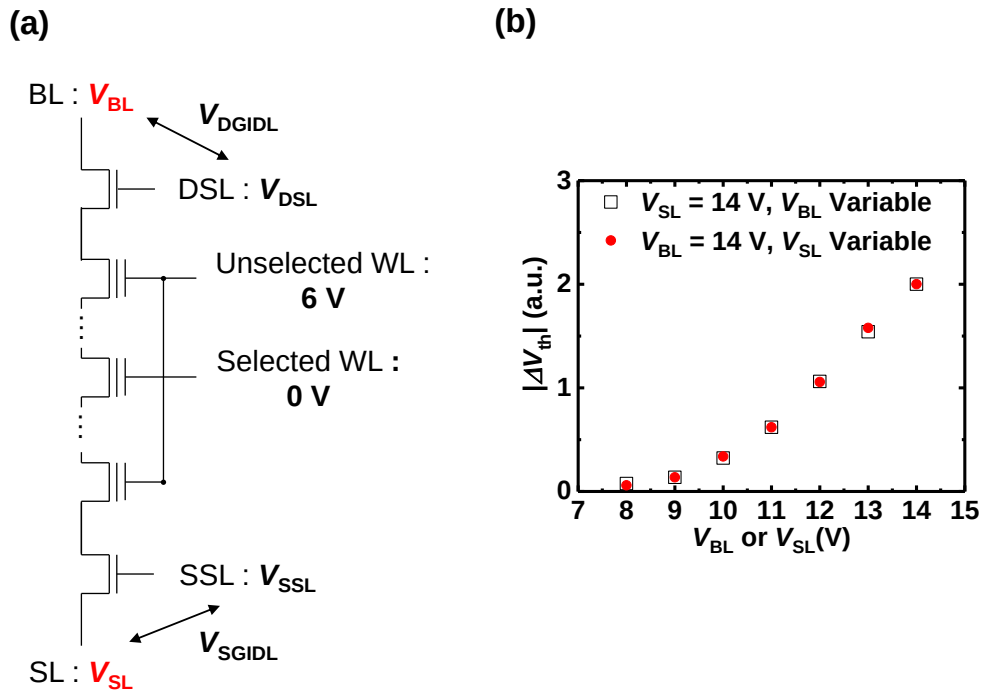

Fig. 2.8. (a) Bias conditions of 1WL GIDL erase operation for the effect of V_{BL} and V_{SL} (b) $|\Delta V_{th}|$s of the cells depending on V_{BL} and V_{SL}

Fig. 2.9 shows the erase characteristics depending on the WL position while applying different V_{BL}, $V_{SL,}$ and erase pulse widths. In the results of Fig. 2.8, when V_{BL} and V_{SL} are applied differently, the potential of VNAND channel can be affected by WL location. Also, it can take time for holes generated by GIDL to spread through the channel, so the erase characteristics may be affected by the WL position. Even though the erase pulse width is reduced to 100 μs by changing the WL position to bottom/center/top, V_{BL} and V_{SL} have the same effect on $|\Delta V_{th}|$, and erase characteristics are not affected by the WL position. This result indicates that the time for the hole generated by GIDL to spread to the channel of VNAND is less than 100 μs, and WL position does not affect channel potential during erase pules.

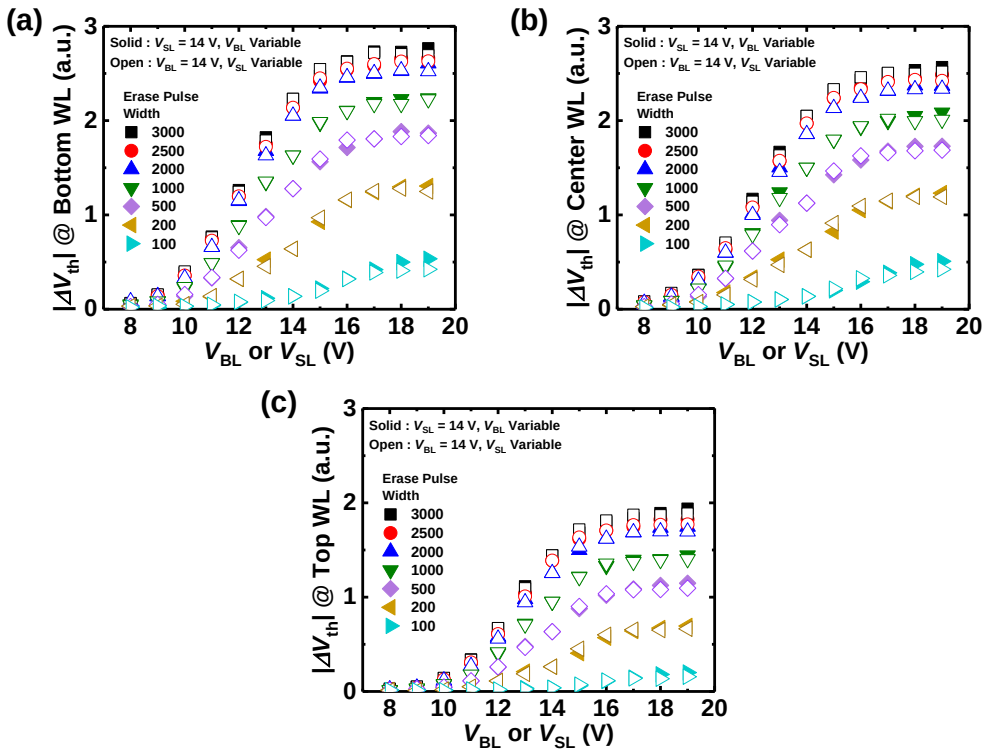

Fig. 2.9. $|\Delta V_{\mathrm{th}}|$ depending V_{BL}, V_{SL}, and erase pulse width at (a) bottom WL (b) center WL (c) top WL

Through the results of Figs. 2.8 and 2.9, erase can be suppressed by lowering the $V_{\text{Unsel.BL}}$ connected to the unselected cell. Also, from the result of Fig. 2.7, only V_{th} of the selected cell can be lowered by giving high V_{DGIDL} only to the DSL where the selected cell is located. Fig. 2.10 shows $|\Delta V_{\text{th}}|$ after erase operation depending on the difference between the $V_{\text{Sel.BL}}$ and $V_{\text{Unsel.BL}}$. When $V_{\text{Unsel.BL}}$ is decreased while maintaining $V_{\text{Sel.BL}}$, $|\Delta V_{\text{th}}|$ of the selected cell is not affected by $V_{\text{Unsel.BL}}$. $|\Delta V_{\text{th}}|$ of the cells connected to the unselected DSL is not affected by $V_{\text{Unsel.BL}}$, and $|\Delta V_{\text{th}}|$s are very small. Only V_{th} of the cell connected to selected DSL and unselected BL is affected by $V_{\text{Sel.BL}}$-$V_{\text{Unsel.BL}}$. As $V_{\text{Unsel.BL}}$ decreases, $V_{\text{Sel.BL}}$-$V_{\text{Unsel.BL}}$ increases, and $|\Delta V_{\text{th}}|$ of unselected BL and selected DSL decreases. When $V_{\text{Sel.BL}}$-$V_{\text{Unsel.BL}}$ is larger than 4 V, $|\Delta V_{\text{th}}|$s of unselected cells are negligible.

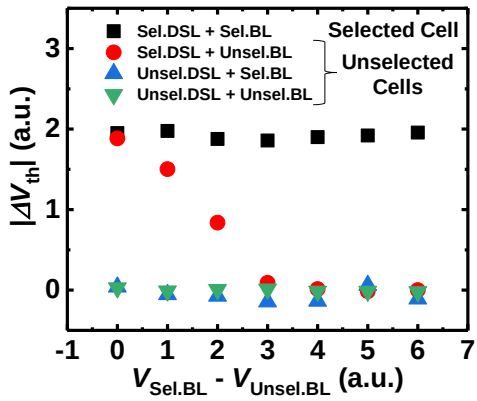

Fig. 2.10. $|\Delta V_{th}|$ depending on the difference between $V_{Sel.BL}$ and $V_{Unsel.BL}$

From the result of Fig. 2.10, erase inhibition is better when $V_{Sel.BL}$-$V_{Unsel.BL}$ increases. However, when a voltage difference between BLs occurs, a breakdown can be occurred. Since BL to BL pitch is a factor that affects the density of memory cell, the BL to BL breakdown voltage is measured. Fig. 2.11 (a) is the result of measuring the flowing current by increasing the voltage of a BL and by applying 0 V to adjacent BLs. As BL voltage increases, the BL to BL current increases. Fig. 2.11 (b) shows BL to BL leakage in log scale. As the BL voltage increases, leakage increases and a large current starts to flow above 6 V, resulting in a breakdown. $V_{Sel.BL}$-$V_{Unsel.BL}$ voltage must be less than 6 V.

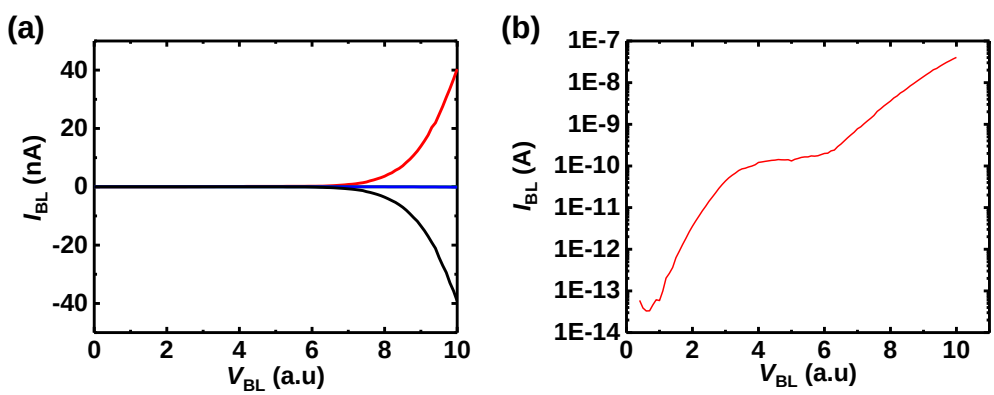

Fig. 2.11. (a) BL to BL leakage current (b) selected BL leakage current in log scale

Fig. 2.12 shows the erase characteristics when both GIDL erase and negative bias are used. As mentioned above, negative bias erase cannot use high V_{Erase}, and there is a side effect that electrons enter the cell from the selected WL or the cell of the adjacent WL through back tunneling. However, with only GIDL erase, the voltage applied to the BL and SL must be increased to lower the V_{th} of the cell, which can be a burden on the circuit. Therefore, we measure whether it is possible to lower V_{Erase} with negative bias erase and GIDL erase (V_{GIDL} of 6 V). Fig. 2.12 (b) shows $|\Delta V_{th}|$ by only GIDL erase and $|\Delta V_{th}|$ by adding negative bias to selected WL and GIDL erase. For erase operation using only GIDL, 0 V is applied to the selected WL, and the $|\Delta V_{th}|$ increases as V_{Erase} increases. For erase operation using GIDL and negative bias, 13 V and 14 V are applied to V_{Erase} to BL and SL, respectively, and negative bias is applied to the selected WL to reduce V_{th} after erase. As the voltage difference between V_{Erase} and the selected WL increases, $|\Delta V_{th}|$ increases. However, the characteristics of the erase operation using the negative bias together are less efficient than the erase operation using only GIDL. As a result, erase operation using negative bias is not suitable for the erase operation of VNAND.

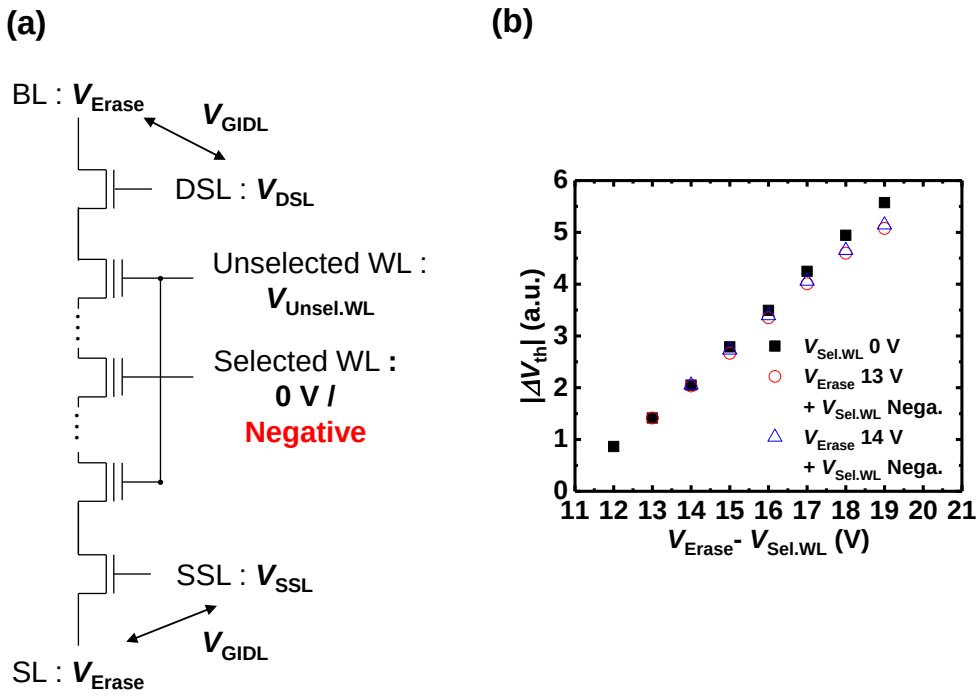

Fig. 2.12. (a) Bias conditions of erase operation using GIDL erase and negative bias erase (b) $|\Delta V_{th}|$s of the cells depending on V_{Erase}-$V_{Sel.WL}$

V_{th} and I_{BL} of NAND flash memory cell change with temperature [11] and GIDL generation are also affected by temperature [12]. GIDL generation has a great influence on the erase characteristics of VNAND, and V_{th} of select gate (DSL, SSL) can affect the erase inhibition condition. Fig. 2.13 shows the results of $|\Delta V_{th}|$ at different temperatures depending on V_{GIDL}. As temperature increases, $|\Delta V_{th}|$ increases. To accurately measure V_{GIDL} for minimum $|\Delta V_{th}|$ (V_{GIDL}@Min.ΔV_{th} in Fig. 2.13 (d)) in the same V_{Erase}, $|\Delta V_{th}|$s are measured more closely when V_{GIDL} is between 0 V and 2 V.

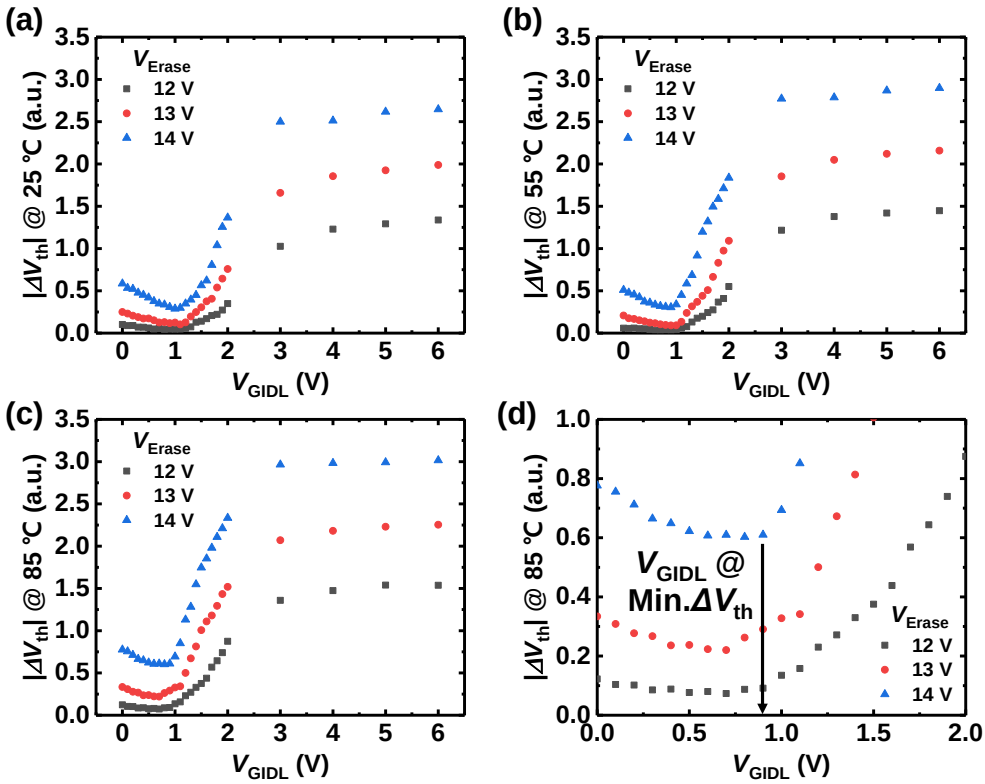

Fig. 2.13. $|\Delta V_{th}|$ depending on V_{GIDL} at (a) 25 ℃ (b) 55 ℃ (c) 85 ℃ (d) an enlarged figure of (c) when V_{GIDL} is 0 V~2 V

Fig. 2.14 (a) shows V_{GIDL}@Min.ΔV_{th} depending on temperature. As the temperature increases, V_{GIDL}@Min.ΔV_{th} decreases and has a slope of -3.4 mV/℃ in case of V_{Erase} of 14 V. To determine the reason for V_{GIDL}@Min.ΔV_{th} change, V_{DSL}-I_{BL} curves are measured. Fig. 2.13 (b) shows V_{DSL}-I_{BL} curves depending on temperature. As temperature increases, I_{BL} increases, and V_{th} of DSL decreases. Fig. 2.13 (c) shows DSL V_{th} depending on temperature. The slope of DSL V_{th} depending on temperature is -3.6 mV/℃, which is almost similar to the change of V_{GIDL}@Min.ΔV_{th}. Temperature affects not only $|\Delta V_{th}|$ but also V_{GIDL} condition for erase inhibition.

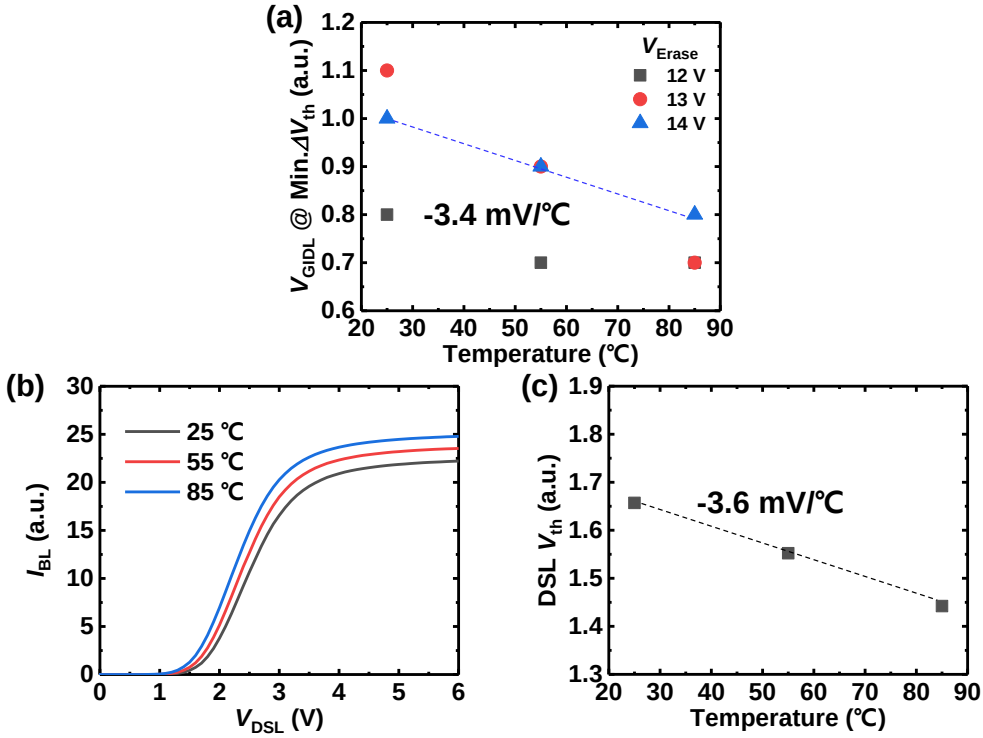

Fig. 2.14. (a) V_{GIDL}@Min.ΔV_{th} depending on temperature (b) DSL V_{DSL}-I_{BL} curves at different temperature (c) DSL V_{th} depending on temperature

2.3 TCAD simulation of VNAND Erase Characteristics

In the previous chapter, the measurement result of erase characteristics was explained. GIDL Erase characteristics in VNAND have been reported [1, 2], but it is not enough to explain the measurement results of the previous chapter. In this chapter, we will explain the measurement results of the previous chapter through TCAD simulation. Fig. 2.15 shows the cross-sectional structure of VNAND, TCAD (Technology Computer Aided Design) model implemented by simulator and its circuit diagram, respectively. VNAND has GAA (Gate All Around) structure in which a cylindrical plug is filled with filler oxide, polysilicon channel, tunnel oxide, Si_3N_4, and block oxide from the center, and WL surrounds the polysilicon channel and ONO structure. Fig. 2.15 (b) shows a model implemented by Sentaurus™-based TCAD simulation with half of the cross-section of VNAND. In the TCAD simulation, the cylindrical coordinate system is applied and proceeded in the same way as the structure of VNAND. The x-axis represents the WL direction with the center of the VNAND plug as the origin, and the y-axis represents the distance from BL to SL with the location connected to BL as the origin. Fig. 2.15 (c) shows the

circuit diagram of the TCAD model. BL is connected to the top of the polysilicon channel, and SL is connected to the bottom. Adjacent to BL and SL, DSL and SSL are placed, respectively. The WL stack has 8 layers, and the 4th WL from the top is the selected WL.

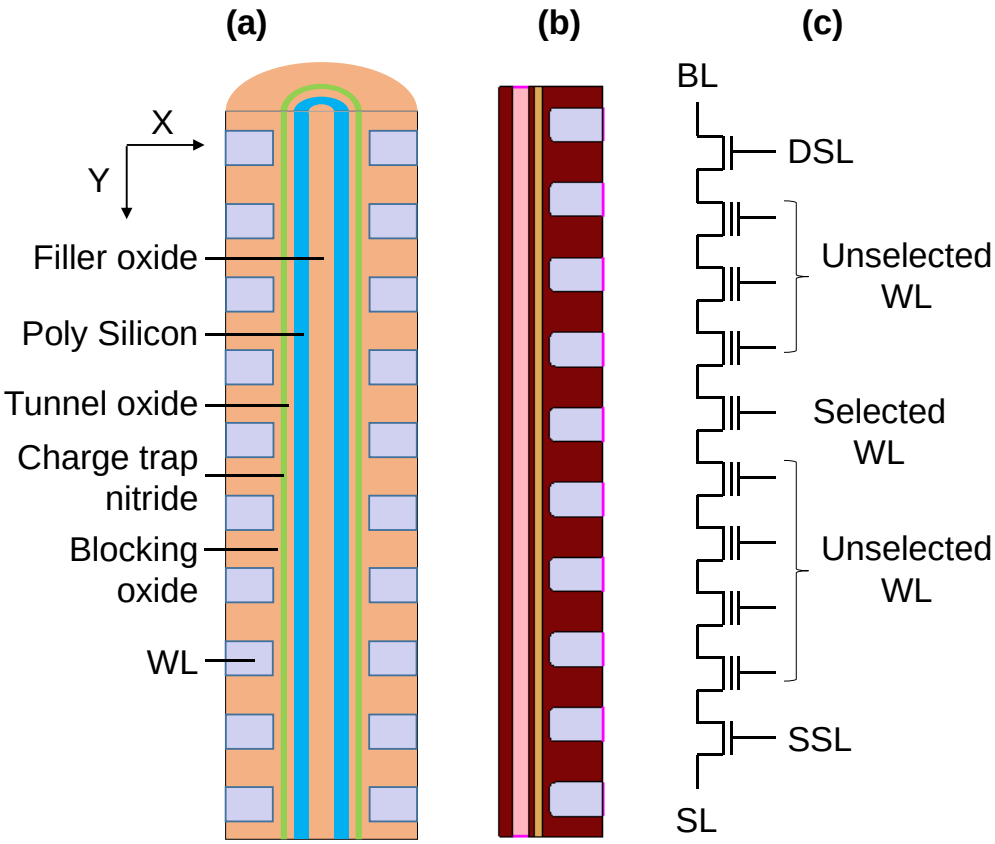

Fig. 2.15. (a) Cross-sectional structure of VNAND (b) model implemented by Sentaurus^{TM}-based TCAD simulation (c) circuit diagram of TCAD model

Fig. 2.16 shows $|\Delta V_{th}|$ after erase operation obtained from the implemented TCAD model and the measured $|\Delta V_{th}|$. V_{th} of the cell before erase operation is 0 V. V_{Erase} is applied 18 V and $|\Delta V_{th}|$ depending on V_{GIDL} is measured. $|\Delta V_{th}|$ obtained from TCAD simulation is similar to the measured result. As V_{GIDL} decreases, $|\Delta V_{th}|$ decreases. When V_{GIDL} is 1 V, $|\Delta V_{th}|$s are minimal. Also, the $|\Delta V_{th}|$ at V_{GIDL} of 0 V is slightly greater than the $|\Delta V_{th}|$ at V_{GIDL} of 1 V. The TCAD model well describes the erase characteristics of VNAND.

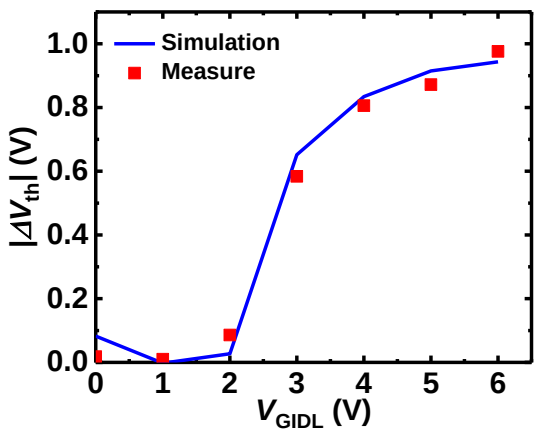

Fig. 2.16. $|\Delta V_{th}|$s comparison by measurement and simulation

In previous research results, it was reported that GIDL hole generation is an important characteristic in VNAND erase operation using GIDL [1, 2]. After GIDL occurs near BL and SL, hole carriers spread to the polysilicon channel, and holes enter the Si_3N_4 layer by FN tunneling due to the potential difference between channel and WL. Therefore, the GIDL generation and channel potential at the moment when V_{BL} and V_{SL} become V_{Erase} (T_1 at Fig. 2.17) are analyzed through TCAD simulation.

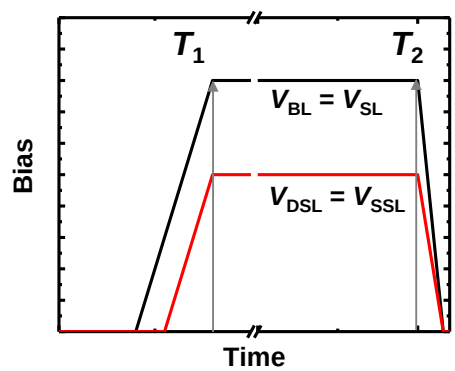

Fig. 2.17. Channel potential and GIDL generation are analyzed at T_1 and T_2 in erase pulse diagram

Fig. 2.18 shows the electric potential and GIDL generation simulated result when V_{Erase} of 18 V and V_{GIDL} of 6 V. In Fig. 2.18 (a), V_{Erase} is applied to BL and SL, and 0 V is applied to the selected WL. Fig. 2.18 (c) shows the channel potential depending on the y-axis value. V_{Erase} applied to BL and SL is reduced while passing through DSL and SSL channels. Channel potential is about 7 V regardless of the location of the WL. Figs. 2.18 (b) and (d) show the GIDL generation result. GIDL generation occurs only in the polysilicon channel and adjacent to BL and SL.

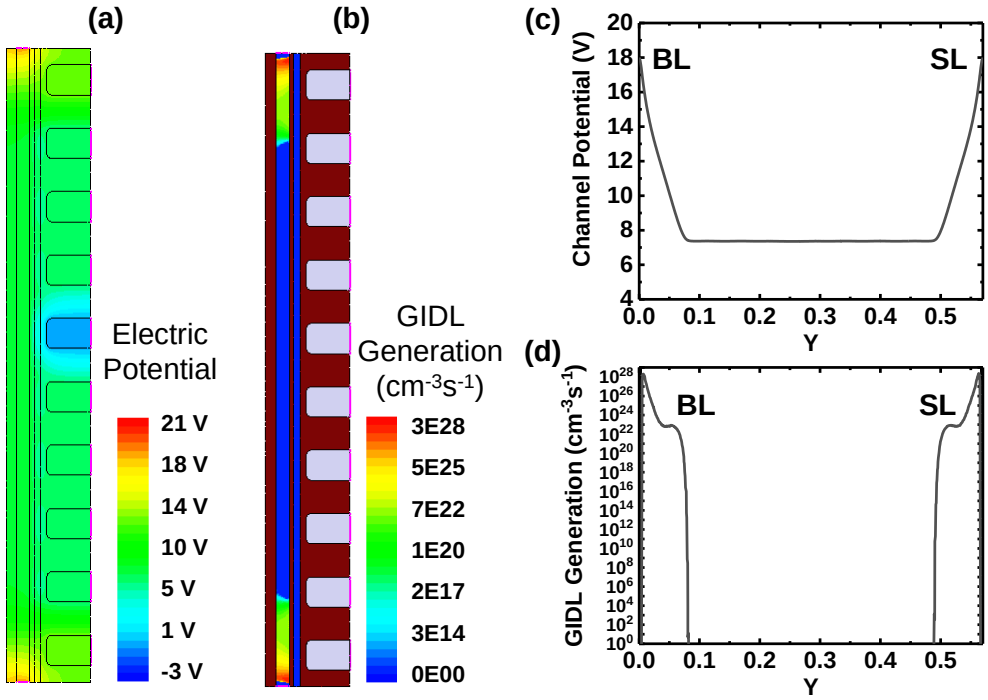

Fig. 2.18. Simulated (a) electric potential and (b) GIDL generation at T_1 (in Fig. 2.17) (c) channel potential and (d) GIDL generation in polysilicon channel

Fig. 2.19 shows simulated channel potential depending on V_{GIDL}. BL and SL potentials are not changed by V_{GIDL}. Since V_{GIDL} represents the potential difference between BL and DSL and SL and SSL, as V_{GIDL} increases, V_{DSL}, and V_{SSL} decrease. Therefore, as V_{GIDL} increases, the channel potential decreases in the DSL and SSL channel areas. Fig. 2.19 (b) shows the channel potential of the selected WL depending on V_{GIDL}. When V_{GIDL} is 0 V, the channel potential is about 13 V, and when V_{GIDL} increases by 1 V, the channel potential decreases by about 1 V.

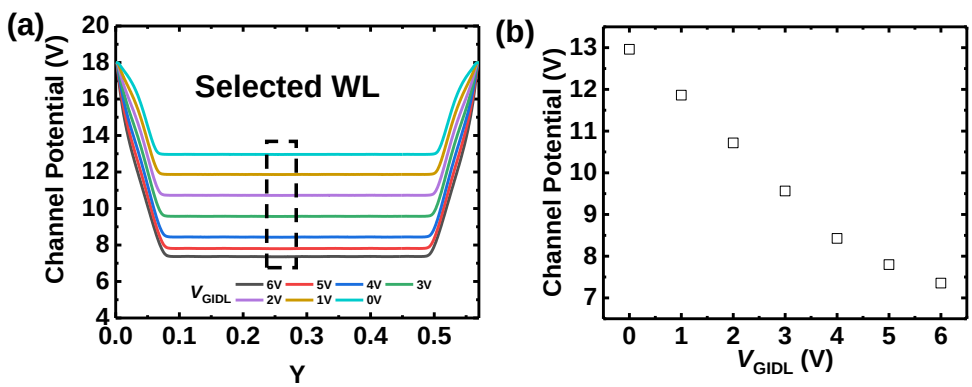

Fig. 2.19. (a) simulated channel potential depending on V_{GIDL} (b) channel potential at selected WL channel depending on V_{GIDL} at T_1

Fig. 2.20 shows simulated GIDL generation results depending on V_{GIDL}. When V_{GIDL} is high, a large GIDL generation value is shown near BL and SL. When V_{GIDL} is low, GIDL generation at BL, SL is small, and larger GIDL generation occurs between DLS, SSL, and unselected WLs than GIDL generation generated near BL, SL. Fig. 2.20 (b) shows the GIDL generation of polysilicon channel depending on V_{GIDL}. Since hole carriers are generated in specific areas of the channel spread over the entire area of the channel, GIDL generation value represents the largest value in the channel. When V_{GIDL} increases by 1 V, GIDL generation increases by about 10 times. When the V_{GIDL} is between 0 V to 2 V, GIDL generation occurs near the WL adjacent to DSL and SSL. Therefore, even when V_{GIDL} decreases, GIDL generation decreases slightly under V_{GIDL} of 2 V.

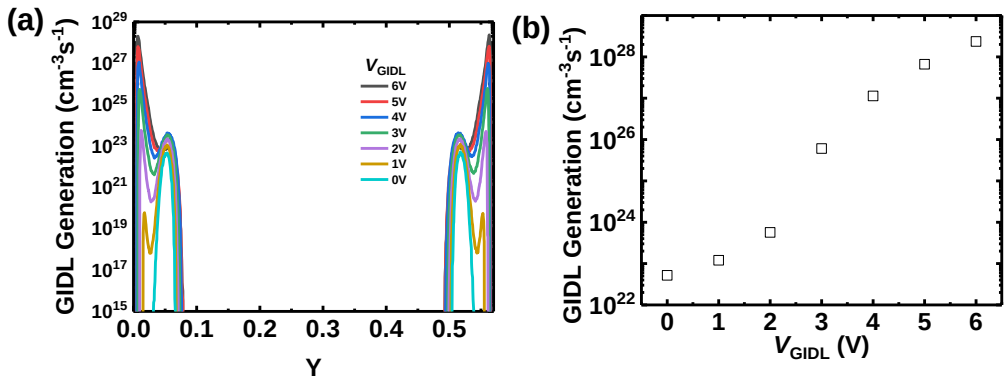

Fig. 2.20. (a) simulated GIDL generation depending on V_{GIDL} (b) largest GIDL generation value depending on V_{GIDL} at T_1

Fig. 2.21 (a) shows $|\Delta V_{th}|$ depending on channel potential. $|\Delta V_{th}|$ decreases as the channel potential increases. As mentioned above, the channel potential causes FN tunneling through the potential difference between WL and channel. The result of Fig. 2.21 (a) indicates that channel potential has little effect on $|\Delta V_{th}|$ when V_{Erase} is not changed but V_{GIDL}. When V_{GIDL} is 0 V and 1 V, as channel potential increases, $|\Delta V_{th}|$ also increases. Fig. 2.21 (b) shows $|\Delta V_{th}|$ depending on GIDL generation. Unlike the result of Fig. 2.21 (a), the larger the GIDL generation, the larger $|\Delta V_{th}|$. When V_{GIDL} is less than 2 V and $|\Delta V_{th}|$ is also almost zero, since GIDL generation is small and is reduced to less than 10^{24} $cm^{-3}s^{-1}$. When V_{GIDL} is 0 V, even when GIDL generation is less than 10^{24} $cm^{-3}s^{-1}$, $|\Delta V_{th}|$ is not 0 and is greater than when V_{GIDL} is 1 V. When V_{GIDL} is 0 V, $|\Delta V_{th}|$ is caused by channel potential rather than GIDL generation.

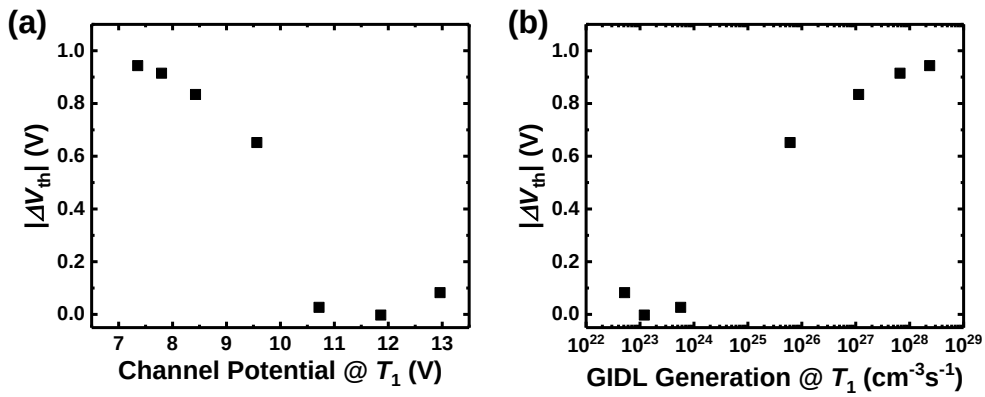

Fig. 2.21. $|\Delta V_{th}|$ depending on simulated (a) channel potential and (b) GIDL generation at T_1

Fig. 2.22 (a) and (b) show channel potential and GIDL generation at T_2 in Fig. 2.17. Compared to the results in Fig. 2.19, channel potential increases and GIDL generation decreases. As the hole generated by GIDL enters the polysilicon channel, the channel potential increases. As the potential of the polysilicon channel increases, the electric field within the channel decreases, and the GIDL generation also decreases. Fig. 2.22 (c) shows the channel potential of the selected WL depending on V_{GIDL} at T_2. The result of Fig. 2.22 (c) is similar to the $|\Delta V_{th}|$ result of Fig. 2.16. When V_{GIDL} is large, channel potential is small at the beginning of the erase pulse, but channel potential increases as holes are supplied for GIDL generation. On the other hand, when V_{GIDL} is small, channel potential is relatively large at the beginning of the erase pulse, but channel potential hardly increases since there is insufficient hole supply. Therefore, $|\Delta V_{th}|$ after erase pulse is large when V_{GIDL} is large.

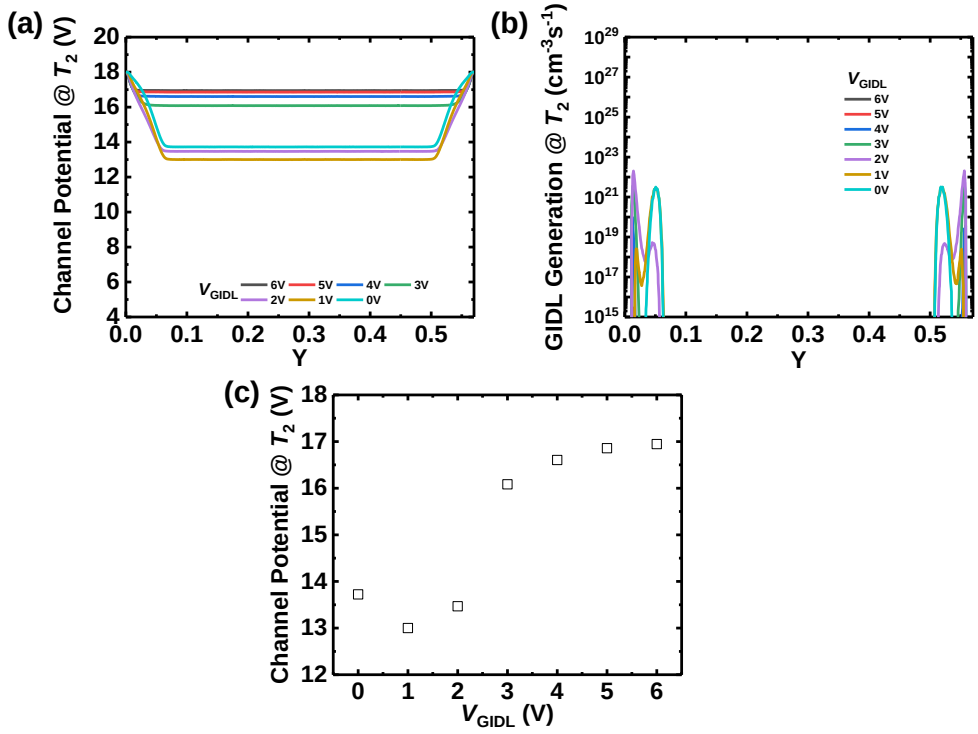

Fig. 2.22. (a) simulated channel potential depending on V_{GIDL} and (b) GIDL generation at T_2 (c) channel potential at selected WL channel depending on V_{GIDL} at T_2

Fig. 2.23 (a) shows $|\Delta V_{th}|$ after erase depending on V_{BL} and V_{SL} when V_{GIDL} is 6 V. Same as the measured result in Fig. 2.8, V_{BL} and V_{SL} have an equal effect on $|\Delta V_{th}|$. Figs. 2.23 (b) and (c) show simulated channel potential and GIDL generation depending on V_{SL} when V_{BL} is 18 V. GIDL generation occurs near BL and SL when V_{DGIDL} and V_{SGIDL} are 6 V and channel potential decreases as V_{SL} decreases. Also, even when V_{BL} and V_{SL} are different, channel potential depending on WL position is negligible. Since channel potential is not affected by WL position even at the moment when erase operation starts, the erase characteristics do not depend on erase pulse width as shown in Fig. 2.9.

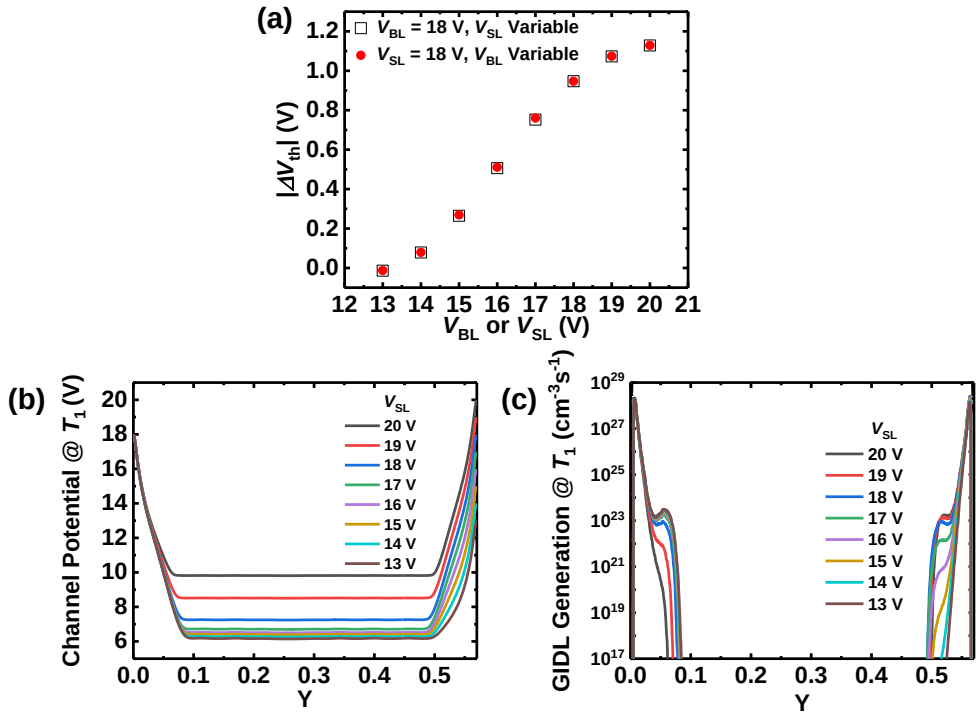

Fig. 2.23. (a) Simulated $|\Delta V_{th}|$ depending on different V_{BL} and V_{SL}, (b) channel potential, and (c) GIDL generation depending on V_{SL} at V_{BL} of 18 V, V_{GIDL} of 6 V

Fig. 2.24 shows simulated and measured $|\Delta V_{th}|$s depending on V_{DGIDL} and V_{SGIDL}. $|\Delta V_{th}|$ from the simulation represents the measurement results well. When large GIDL generation occurs on the SL side with V_{SGIDL} 6 V, $|\Delta V_{th}|$s are about 1V regardless of V_{DGIDL}. On the other hand, when GIDL generation on the SL side is suppressed by V_{SGIDL} 1 V, $|\Delta V_{th}|$ is affected by V_{DGIDL}. From these results, erase inhibition for 1-bit erase is possible for TCAD simulation.

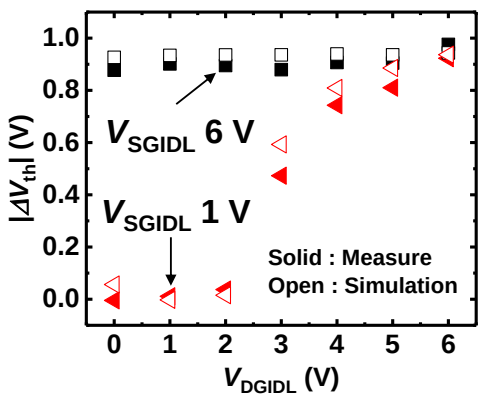

Fig. 2.24. Simulated and measured $|\Delta V_{th}|$ depending on V_{DGIDL} and V_{SGIDL}

Fig. 2.25 shows characteristics of the erase operation using GIDL and negative bias by TCAD simulation. Fig. 2.25 (a) shows the result that $|\Delta V_{th}|$ by erase operation using GIDL and negative bias is smaller than $|\Delta V_{th}|$ by erase operation using only GIDL. Fig. 2.25 (b) shows channel potential results depending on V_{Erase}. When V_{Erase} increases by 1 V, the channel potential increases by 1.45 V. When applying a negative bias to the selected WL, the channel potential and WL potential increase by the amount of the negative bias. However, when increasing V_{Erase}, the channel potential increases more than V_{Erase}. Therefore, erase efficiency using GIDL and negative bias is lower than erase efficiency using only GIDL.

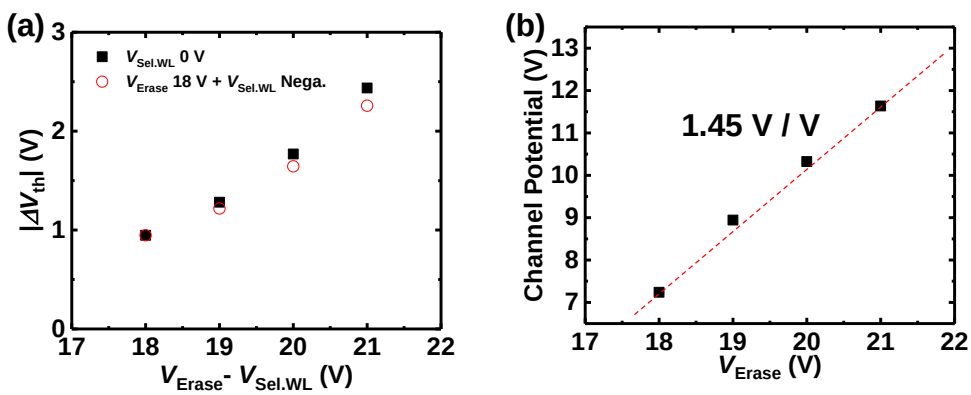

Fig. 2.25. (a) Comparison of $|\Delta V_{th}|$ by erase using GIDL and negative bias and $|\Delta V_{th}|$ by erase operation using only GIDL (b) channel potential depending on V_{Erase}

Since GIDL generation is caused by the electric field between BL/SL and DSL/SSL, GIDL generation is affected by the shape of the plug, doping concentration, or V_{th} of select transistors (DSL, SSL). In the results of Fig. 2.16 and 2.20, when V_{GIDL} is between 2 V to 4 V, $|\Delta V_{th}|$ and GIDL generation are greatly affected by V_{GIDL}. Therefore, when V_{GIDL} is between 2 V to 4 V, the change of erase characteristics depending on DSL V_{th} is analyzed through TCAD simulation. Fig. 2.26 shows the GIDL generation results near DSL depending on DSL V_{th} and V_{DGIDL}. When V_{DGIDL} 6 V, GIDL generation is not affected by DSL V_{th}. On the other hand, when V_{DGIDL} is 3 V, GIDL generation is affected by DSL V_{th}.

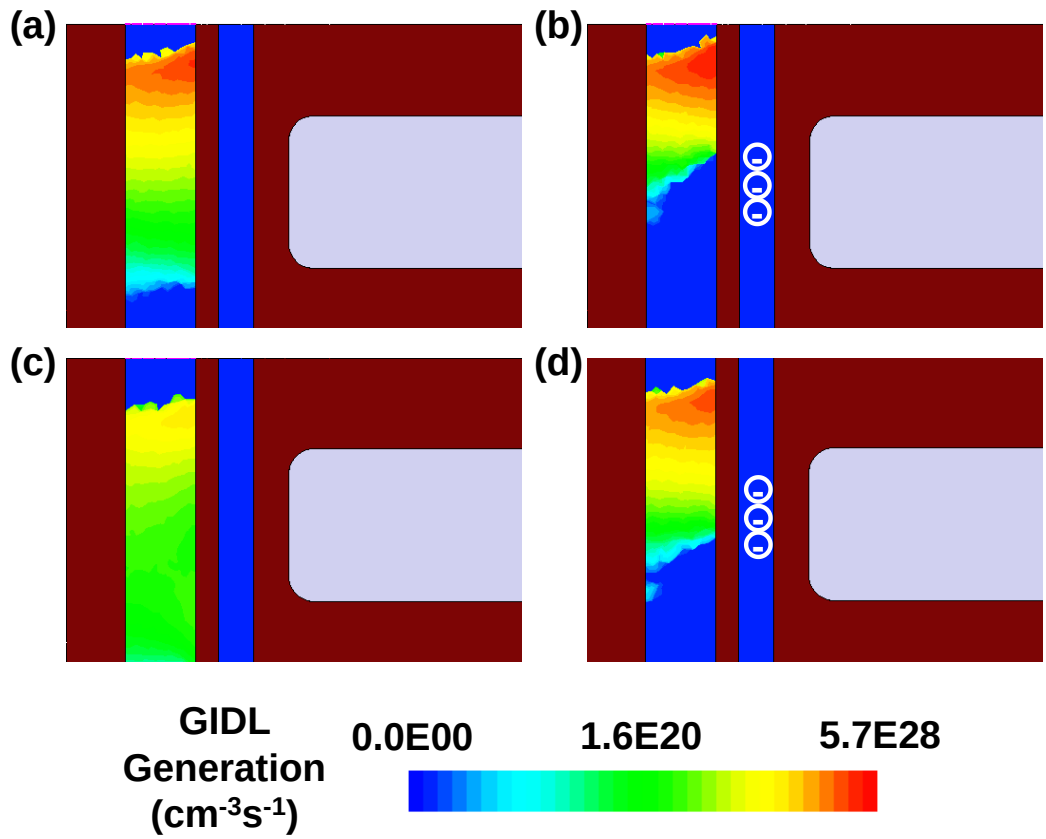

Fig. 2.26. GIDL generation depending on V_{DGIDL} and DSL V_{th} at BL side (a) V_{DGIDL} 6 V, DSL V_{th} 0 V (b) V_{DGIDL} 6 V, DSL V_{th} 3.6 V (c) V_{DGIDL} 3 V, DSL V_{th} 0 V (d) V_{DGIDL} 3 V, DSL V_{th} 3.6 V

Since GIDL generation depends on DSL V_{th}, erase characteristics can also depend on DSL V_{th}. Fig. 2.27 shows simulated V_{th} after erase operation and GIDL generation depending on DSL V_{th}. To minimize the effect of GIDL generation on the SL side, V_{SGIDL} is applied 1 V. When V_{DGIDL} is 6 V, the V_{th}s after erase operation are about -4 V, and the effect of the DSL V_{th} is negligible. On the other hand, when V_{DGIDL} is 3 V, V_{th}s after erase are affected by DSL V_{th} and are varied between -3 V and -4 V. The standard deviation of V_{th} after erase operation is 0.07 V when V_{DGIDL} is 6 V and is 0.34 V when V_{DGIDL} is 3 V. The result of Fig. 2.27 (a) agrees well with the previous study that V_{th} dispersion increases after erase when GIDL generation is insufficient [2]. In the mass-produced semiconductor process, since there are various process variations, sufficient GIDL generation is required for erase operation.

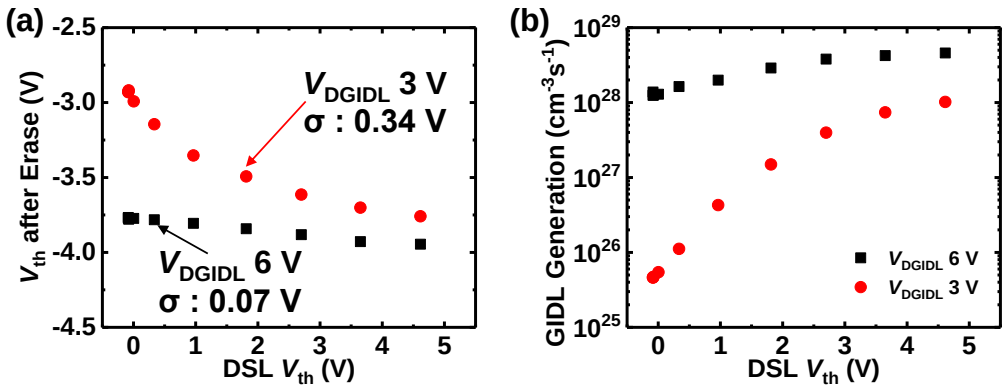

Fig. 2.27. Simulated (a) V_{th} after erase operation and (b) GIDL generation depending on DSL V_{th} and V_{DGIDL}

Chapter 3
Characteristics of 1-bit Erase

3.1 1-bit Erase Condition

Through the erase characteristics of VNAND measured above, 1-bit erase operation is implemented in VNAND. Fig. 3.1 shows the bias condition of the implemented 1-bit erase. Apply high voltage of V_{Erase} (=$V_{Sel.BL}$) to the selected BL. For strings selected by BL and DSL, apply V_{DGIDL} 6 V as $V_{Sel.BL}$ - 6 V to DSL for sufficient GIDL generation. V_{DGIDL} 1 V is applied to the DSL of unselected strings as $V_{Sel.BL}$ - 1 V to suppress GIDL generation. The same voltage as $V_{Sel.BL}$ is applied to SL for erase efficiency. To inhibit GIDL generation on the SL side, V_{SGIDL} 1 V is applied to SSL as $V_{Sel.BL}$ - 1 V. $V_{Sel.BL}$ - 4 V is applied to unselected BL to suppress GIDL generation and reduce erase efficiency. GIDL generation does not occur in the string where unselected BL and unselected DSL are connected, and the erase operation is suppressed with low V_{BL}. 0 V is applied to selected WL and 6 V is applied to the unselected WL. Fig. 3.2 shows the erase pulse diagram for 1-bit erase.

Similar to Fig. 1.4 (erase pulse diagram), different pulse timings are applied to BL and DSL for sufficient GIDL generation. Erase inhibition to minimize GIDL generation is achieved by adjusting the voltage of each terminal. The table summarizes bias conditions of VNAND terminals for 1-bit erase operation.

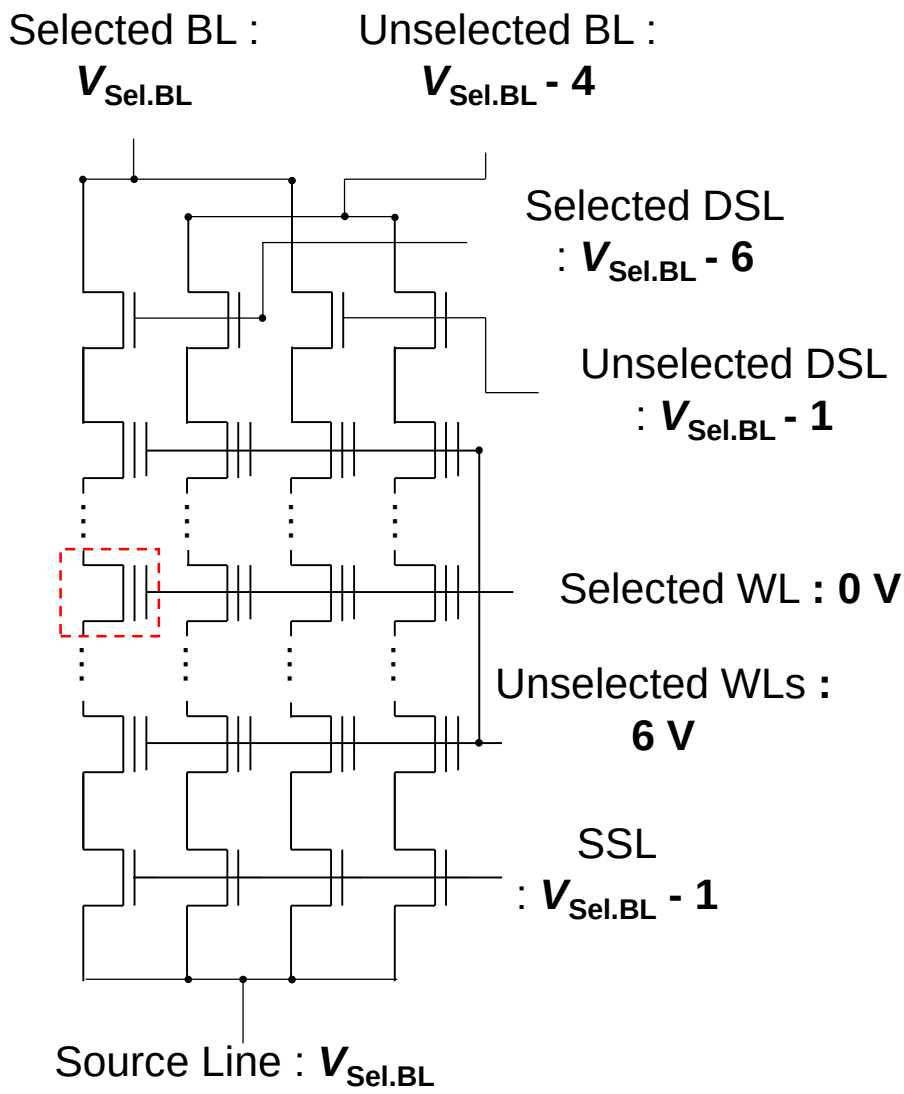

Fig. 3.1. Bias conditions of 1-bit erase operation

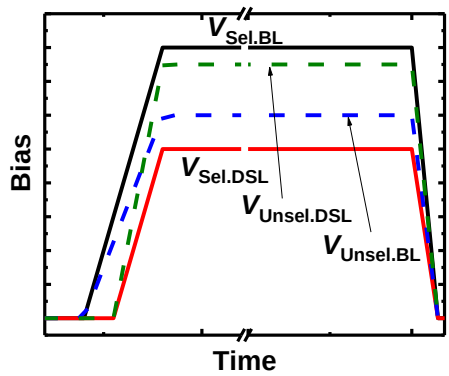

Fig. 3.2. Pulse diagram of 1-bit erase operation

Terminal	Select/Unselect	Bias	Remark
BL	Selected	$V_{sel.BL}$	V_{Erase}
	Unselected	$V_{sel.BL} - 4$	V_{DGIDL} 2 + V_{BL}/V_{SL} Effect
DSL	Selected	$V_{sel.BL} - 6$	V_{DGIDL} 6 (GIDL generation)
	Unselected	$V_{sel.BL} - 1$	V_{DGIDL} 1 (GIDL inhibition)
WL	Selected	0	FN tunneling
	Unselected	6	
SL	Tied in a Block	$V_{sel.BL}$	Erase efficiency (V_{BL}/V_{SL} Effect)
SSL	Tied in a Block	$V_{sel.BL} - 1$	V_{SGIDL} 1

Table 3.1. Bias conditions of VNAND terminals for 1-bit erase operation

3.2 1-bit Erase Characteristics

Fig. 3.3 shows the change of V_{WL}-I_{BL} curves when the 1-bit erase operation is performed after programming the cells of the selected WL. To verify the change in V_{WL}-I_{BL} curve, V_{WL}-I_{BL} curves are compared after the program and after repeating the 1-bit erase operation 50 times. V_{WL}-I_{BL} curve of the selected cell moves to the left after the 1-bit erase operation. On the other hand, V_{WL}-I_{BL} curve of an unselected cell does not move. Fig. 3.4 shows V_{th} and I_{BL} changes of cells while the 1-bit erase operation is repeated. For the unselected cells, the selected BL + unselected DSL, unselected BL + selected DSL, and unselected BL + unselected DSL conditions are applied, respectively. Both V_{th} and I_{BL} of unselected cells are almost unchanged during repeated 50 1-bit erase operations. On the other hand, V_{th} and I_{BL} of the selected cell are changed as the 1-bit erase operation is repeated.

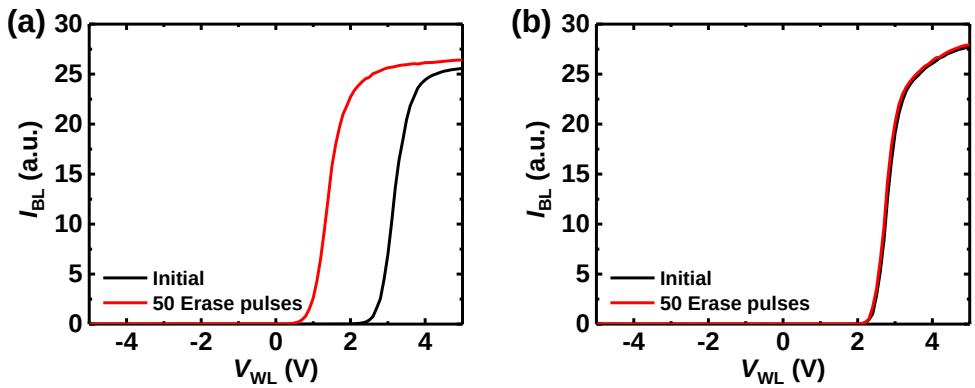

Fig. 3.3. V_{WL}-I_{BL} curves of (a) selected and (b) unselected cell after applying 50 1-bit erase operations

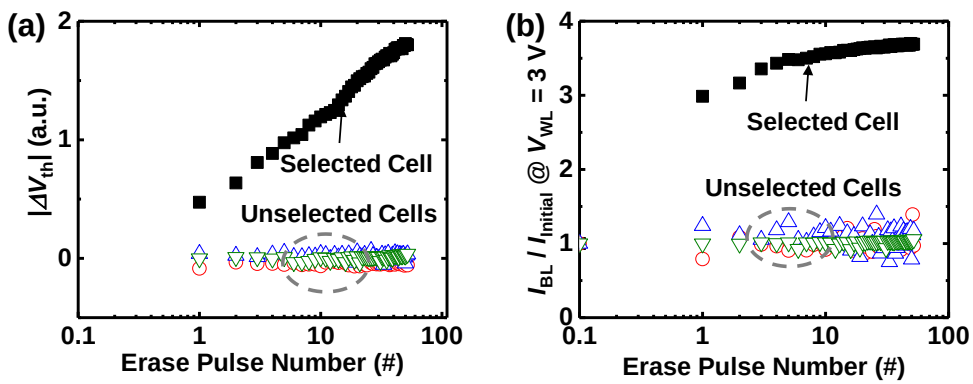

Fig. 3.4. (a) V_{th} and (b) I_{BL} change of cells after applying 50 1-bit erase operations

Fig. 3.5 shows the $|\Delta V_{th}|$ of unselected cells during 1-bit erase operation, disturbance characteristics. To measure disturbance characteristics, cells of adjacent WLs, top and bottom WL are programmed. To verify small $|\Delta V_{th}|$ that can occur due to 1-bit erase operation cells are programmed to 4 V. Also, since $|\Delta V_{th}|$ is very small or the value can change due to variation during measurement, $|\Delta V_{th}|$s are measured while repeating the 1-bit erase operation. Fig. 3.5 (b) shows $|\Delta V_{th}|$s of selected and unselected cells after the 1-bit erase operation. There is only $|\Delta V_{th}|$ of the selected cell and $|\Delta V_{th}|$ of unselected cells are negligible after repeated 1-bit erase operation.

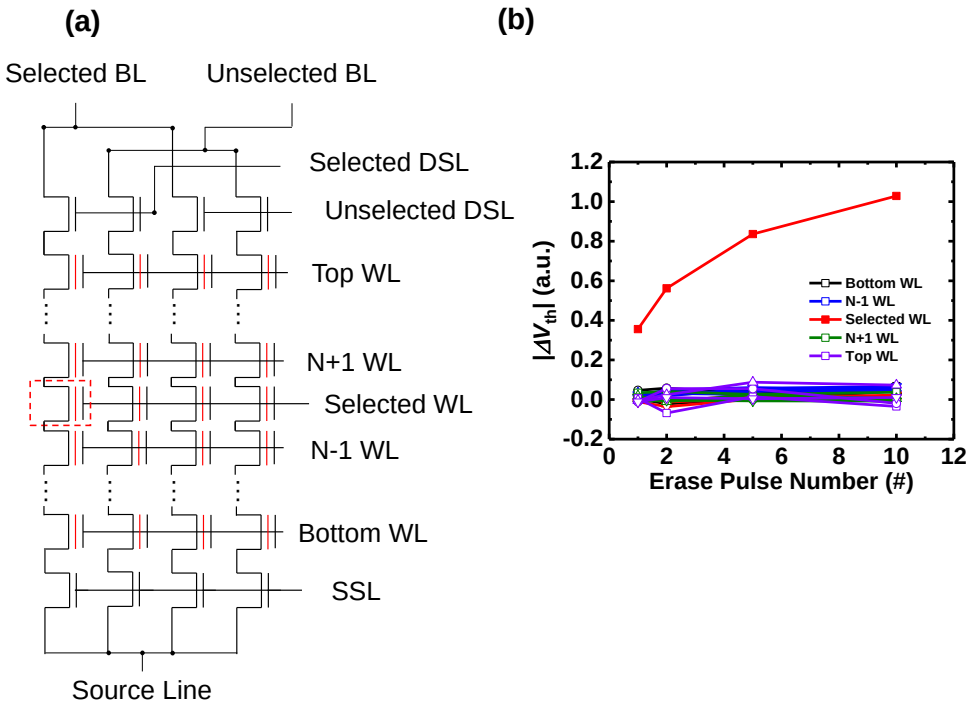

Fig. 3.5. (a) Cell V_{th} conditions to measure disturbance characteristics of 1-bit erase operation (b) $|\Delta V_{th}|$ depending on the number of repeated 1-bit erase operation

Fig. 3.6 shows the disturbance characteristics of the 1-bit erase operation when WL position of the selected cell is top/center/bottom. The plug size of VNAND depends on WL position, and the erase characteristics also depend on WL position [2, 13]. Therefore, the 1-bit erase characteristics may also depend on WL position when the WL position of the selected cell is different. $|\Delta V_{th}|$ of the selected cell is different depending on the WL location. However, $|\Delta V_{th}|$ of unselected cells is negligible regardless of WL position. 1-bit erase operation that changes only the V_{th} of the selected cell in VNAND has been successfully implemented.

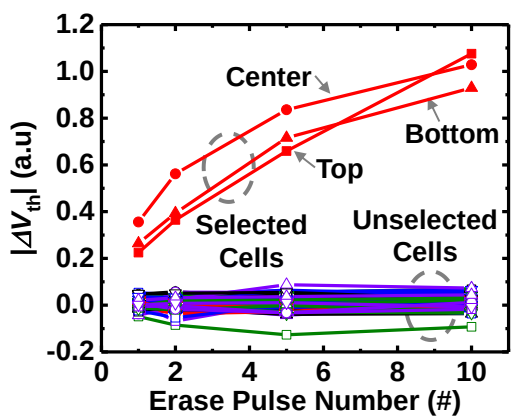

Fig. 3.6. Disturbance characteristics of 1-bit erase operation as a parameter of WL position of the selected cell

3.3 Variation Improvement Results

In the previous chapters 3.1 and 3.2, 1-bit erase operation that changes only the V_{th} and I_{BL} of a specific cell of VNAND was explained. In this chapter, we explain how to adjust the V_{th} and I_{BL} of a cell using 1-bit erase. In a previous study, it has been reported that there are limitations in adjusting V_{th} using only ISPP [4, 8]. Adjusting cell V_{th} by reducing the ISPP step increases the time of program operation. Furthermore, there is a variation that occurs while electrons enter the charge trap layer or floating gate through FN tunneling [4]. Also, it has been reported that larger target I_{BL}, larger I_{BL} variation when adjusting the I_{BL} to the synaptic device of the neuromorphic system [8].

Fig. 3.7 shows the long-term potentiation/depression characteristics of VNAND cells. After programming the cell to an initial state, the I_{BL} of the cell is measured while repeating the erase and program operations with various voltages and pulse widths. At the beginning of long-term potentiation by erase operation, there is a large I_{BL} increase. However, as the erase operation is repeated, the change of I_{BL} decreases. On the other hand, at the beginning of long-term depression by

program operation, there is a large I_{BL} decrease, and as the program operation is repeated, the change of I_{BL} decreases. Through this result, it is difficult to adjust I_{BL} when I_{BL} is large when using only the program operation. On the other hand, the erase operation can adjust well when the target I_{BL} is large, but it is difficult to adjust when the target I_{BL} is small. In both program and erase operations, when the bias and pulse width are reduced, I_{BL} can be accurately adjusted. However, the number of pulses increases exponentially with low bias or short pulse width.

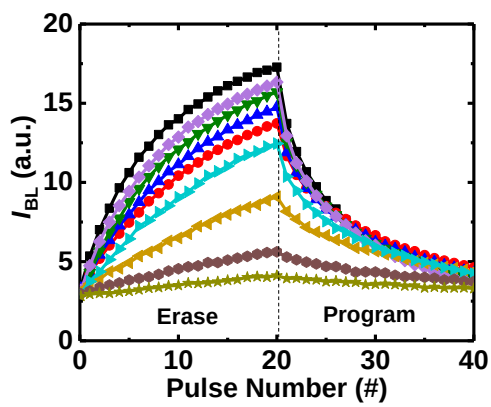

Fig. 3.7. Long-term potentiation/depression characteristics of VNAND cells

Fig. 3.8 shows the results of reducing I_{BL} distribution using a 1-bit erase operation. Target I_{BL} is 10 nA, 30 nA, and 50 nA, respectively. In the case of using only the program operation, the adjusting operation is terminated when I_{BL} becomes smaller than the target I_{BL}. In the case of using program operation and 1-bit erase operation, adjusting operation is terminated when tolerance 1 nA is satisfied. A total of 150 cells are measured, and the same program/erase bias and pulse width are applied. When 1-bit erase operation is not used, the distribution of cell I_{BL} is large. Some I_{BL}s are much smaller than target I_{BL}. As target I_{BL} increases, I_{BL} dispersion increases. On the other hand, when 1-bit erase is used, the I_{BL}s of all cells are within tolerance 1 nA. I_{BL} distribution is not affected by target I_{BL}. Fig. 3.9 shows the standard deviation of the cell I_{BL} results of Fig. 3.8. Without 1-bit erase operation, the standard deviation is 10 % of the target I_{BL}. On the other hand, with 1-bit erase operation, the standard deviation of cell I_{BL} is less than 0.3 nA and is not affected by target I_{BL}. In the case of target I_{BL} 50 nA, the standard deviation is greatly reduced to 1/17 of the case when 1-bit erase is not used.

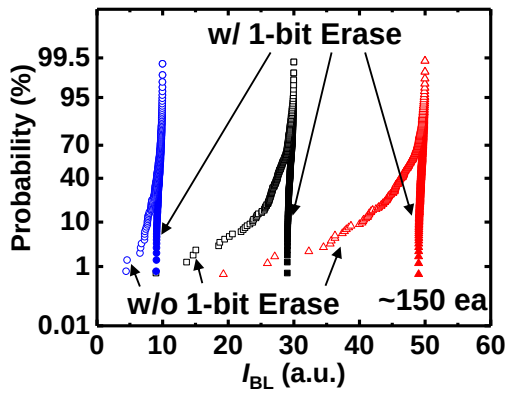

Fig. 3.8. I_{BL} distribution depending on target I_{BL} with and without 1-bit erase operation

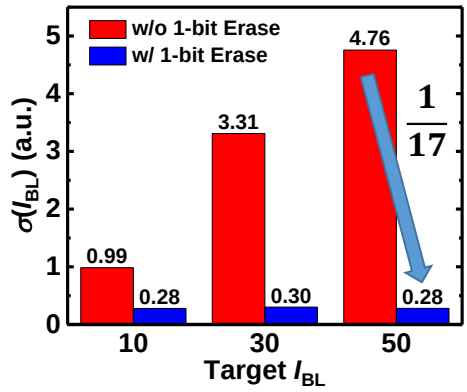

Fig. 3.9. Standard deviation of I_{BL} ($\sigma(I_{BL})$) with and without 1-bit erase operation

Fig. 3.10 shows the effect of WL position when adjusting cell I_{BL} with and without 1-bit erase operation. As WL position goes down, plug size decreases, and cell I_{BL} change by program operation increases. Therefore, when 1-bit erase is not used, the standard deviation of cell I_{BL} distribution increases as the WL position goes down. On the other hand, when 1-bit erase is used, the standard deviation of cell I_{BL} distribution is not affected by WL position.

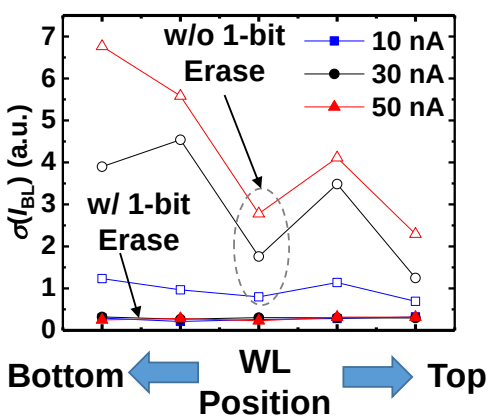

Fig. 3.10. Effect of WL position when adjusting cell I_{BL} with and without 1-bit erase operation

In this chapter, the I_{BL} distribution of cells can be improved in parallel with the program operation by using the 1-bit erase operation. The reason for the improvement in I_{BL} distribution is that the program and erase operations complement each other because the cell I_{BL} change tendencies are different depending on the program and erase operations. In addition, errors due to variations that occur during FN tunneling can be corrected, cell I_{BL} distribution is improved. Finally, WL position effect can be overcome by using a 1-bit erase operation.

Chapter 4

Conclusion

In this work, the 1-bit erase operation that lowers only the V_{th} of a specific cell in VNAND has been proposed. The erase characteristics of VNAND flash memory were measured under various conditions. Erase operation using negative bias has a side effect that erase efficiency decreases and V_{th} of adjacent WL cells increases as electrons enter the Si_3N_4 layer from the gate due to back tunneling. Erase operation/inhibition can be distinguished by applying different V_{GIDL}. V_{GIDL} is separated into V_{DGIDL} on the BL side and V_{SGIDL} on the SL side. By giving V_{DGIDL} differently, GIDL generation can be occurred at the string of selected cell. Hole carriers generated by GIDL near BL/SL side spread across channel of VNAND in less than 100 μs. The measured results were analyzed through TCAD simulation. GIDL generation and channel potential were analyzed, and GIDL generation affects the erase characteristics of VNAND more than channel potential at the beginning of erase pulse. There can be large V_{th} variations after erase operation when GIDL

generation is insufficient. Based on the measured results, the 1-bit erase operation in VNAND was implemented for the first time without structural changes. The implemented 1-bit erase operation changes only V_{th} and I_{BL} of the selected cell but does not change V_{th} and I_{BL} of the unselected cells. The distribution of VNAND flash memory cells was compared with and without using 1-bit erase. When 1-bit erase is used in parallel with program operation, the standard deviation is improved to 1/17 at 50 nA of the target I_{BL}. In addition, by using 1-bit erase, it is possible to overcome the characteristics change depending on WL position that affects cell V_{th} and I_{BL} distribution.

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초 록

낸드 플래시 메모리는 비휘발성 메모리로 높은 집적도를 장점으로 가진다. 낸드 플래시 메모리는 좀 더 높은 집적도를 위해 하나의 셀에 더 많은 비트의 데이터를 저장하거나 채널을 수직으로 세운 적층형 수직 낸드 플래시 기술이 개발되었다. 제한된 쓰기/지우기 구간에 더 많은 비트의 데이터를 저장하기 위해서는 더 좁은 메모리 셀 문턱 전압 산포를 만드는 것이 필요하다. 이를 위해 더 긴 쓰기 시간과 더 강한 오류 수정 코드 (Error Correction Code)가 요구되고 있다. 낸드 플래시 메모리에서 WL 스택의 수를 늘리면서 상위 워드 라인과 하위 워드 라인의 셀 특성 차이를 극복하는 방법이 요구된다. 또한 낸드 플래시 메모리는 높은 공정 성숙도를 가지고 있어 뉴로모픽 컴퓨팅의 시냅틱 디바이스로 큰 장점을 가지고 있다. 시냅틱 디바이스는 뉴럴 네트워크의 가중치를 저장하는 역할로, 낸드 플래시 메모리는 비휘발성 메모리로 긴 수명을 가지고 있어 시냅틱 디바이스에 적합하다. 그러나 기존의 쓰기/지우기 방법으로는 가중치를 나타내는 비트라인 전류를 정확히 맞추기 힘들다.

이 학위 논문에서는 낸드 플래시 메모리의 장점을 이용하면서 단점을 극복하기 위해 낸드 플래시 메모리 셀을 선택적으로 지우는 동작을 제안하고 분석하였다. 적층형 수직 낸드 플래시 메모리 어레이에서 각 단자에 전압을 조정하여 선택한 셀의 지우기 동작과 선택되지 않은 셀의 지우기 억제가 성공적으로 확인되었다. 측정된 결과와 TCAD 시뮬레이션 결과를 통해 DSL/SSL 게이트 전압 조건 의한 전류 누출 (GIDL) 특

성이 지우기 동작에 큰 영향을 주고 있음을 확인하였다. 제안된 1 비트 지우기 동작은 현재의 적층형 수직 낸드 플래시 메모리 어레이의 공정 및 구조를 변경할 필요가 없이 전통적인 쓰기 동작과 병행하여 메모리 셀의 문턱 전압을 바꾸어서 데이터를 수정하거나 문턱 전압 산포를 줄일 수 있다. 1 비트 지우기 동작을 이용하여 워드라인 위치에 따른 메모리 셀의 특성 차이를 극복할 수 있다. 또한 시냅틱 디바이스로써 낸드 플레시 메모리 셀을 이용할 때, 비트라인 전류 산포는 이전의 방법보다 17배 감소시켰다.

주요어 : 적층형 수직 낸드 플래시 메모리, 지우기 동작, 게이트 전압에 의한 전류 누출 (GIDL), 1비트 지우기, 비트라인 전류 (혹은 문턱전압) 분산
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