Master's Thesis

Supply Noise Analysis and Noise, Power-Optimized Capacitor-less LDO Design for Ring Oscillators

링 오실레이터를 위한 캡리스 LDO 의 입력 전압 노이즈 분석과 노이즈, 전력 최적화 설계

by

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Abstract

This thesis presents quantitative analyses of the supply noise of ring oscillators and an effect of a low dropout regulator (LDO), which is widely used to mitigate power supply sensitivity. The phase noise degradation due to supply noise has been perceived as critical. However, no delicate model can calculate the degradation in terms of jitter or phase noise. For this reason, many designers treated the supply noise effect as an unknown factor, which frequently gives rise to a discrepancy between noise levels of pre- and post-silicon. This thesis provides the theoretical foundation explaining how to compromise two effects, supply noise and noise generated from LDO. Furthermore, it gives a guideline to optimize an LDO for the ring oscillator with noise and power consumption constraints. The optimized LDO demonstrates 5.9-nV/√Hz output noise at 1-MHz and consumes only 5-uA quiescent current in a standby state and 0.051-mm^2 die area, including a voltage reference.

Keywords: ring oscillator, low dropout regulator (LDO), impulse sensitivity function (ISF), supply noise, phase noise

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Chapter 1

Introduction

1.1 Motivation

The demand for high-bandwidth digital and communication systems is tremendously increasing. A clock generator is a key part of determining timing-related performances of the systems, and it is crucial to design quality clock generators with predictable performances even in the presence of external noise.

A ring oscillator is a widely used building block in clock generators for its compact size and wide tuning range. However, its jitter and phase noise are susceptible to supply noise which imposes difficulties in the precise prediction of timing-related performances of the systems. Furthermore, due to the supply voltage scaling, as depicted in Fig. 1.1, most of the contemporary ring oscillators adopted single-ended inverter-based topologies [2]-[5], which became extremely susceptible to supply noise.

The most general approach to mitigate the supply noise sensitivity is employing a low dropout regulator (LDO) [6]-[8]. However, while an LDO can improve supply insensitivity, in practice, the LDO output noise due to its device noises (e.g., flicker and thermal noise of MOSFETs) is another critical factor that can degrade the phase noise of a ring oscillator even beyond the noise contribution from the oscillator itself. For this reason, quantitative analyses on supply noise to phase noise conversion and LDO output noise contribution around a ring oscillator are necessary to optimize an LDO in terms of noise.

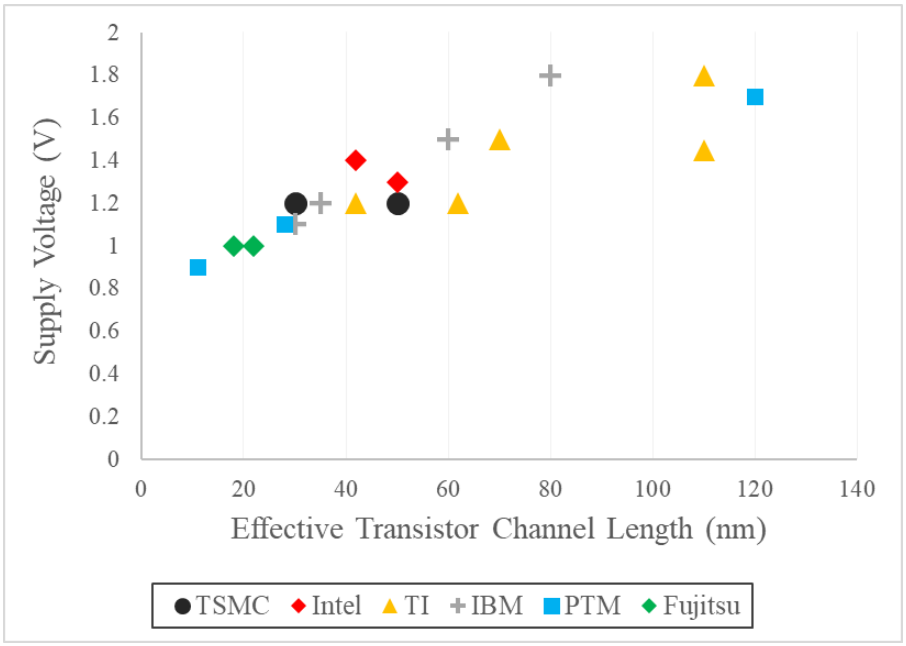

Fig. 1.1 Trend of supply voltage scaling Vs. the effective transistor channel length [1].

This thesis presents an analysis of the effect of power supply and LDO noises on the phase noise of ring oscillators and a design of an LDO for supply regulation, optimizing its noise and power consumption. The optimized LDO demonstrates 5.9-nV/$\sqrt{}$Hz output noise at 1-MHz and consumes only 5-uA quiescent current in a standby state and 0.051-mm^2 die area, including a voltage reference.

1.2 Thesis Organization

This thesis is organized as follows.

In Chapter 2, the theoretical background of the ring oscillator and phase noise is explained. It encompasses the basic operation principle of ring oscillators and their phase noise analysis method using impulse sensitivity function (ISF).

Chapter 3 introduces an analysis of supply noise to phase noise in ring oscillators. The extended theoretical approach using the ISF concept explains how the supply noise is transferred and amplified, exacerbating the jitter and phase noise performances.

Chapter 4 illustrates the effect of LDO output noise in regulated supply ring oscillators. In the general approach, low dropout regulators (LDOs) are employed to suppress the supply noise, and capacitor-less LDOs are preferred. However, even though LDOs may filter the external supply noise, the internal noise is another crucial noise source deteriorating the phase noise of ring oscillators. To investigate the primary design factors to reduce the noise contribution of LDOs, a quantitative model illustrating the contribution of LDO noise sources to the phase noise is presented. In addition, a novel definition of Figure of Merit (FoM) reflecting noise and power optimization performance is proposed.

Chapter 5 presents the noise, power-optimized capacitor-less LDO design for ring oscillators. From the analysis mentioned above, key factors affecting noise performance are deduced, and it is possible to build a systematic design procedure of LDO for ring oscillators.

Chapter 6 shows SPICE and SPECTRE simulation results of LDOs with various optimization levels. An internal voltage reference of LDO is taken into consideration, and the performance of the noise, power-optimized, self-biased LDO is also demonstrated.

Chapter 7 summarizes the proposed works and concludes this thesis.

Chapter 2

Background

2.1 Basic of Ring Oscillator

A ring oscillator is a circuit component comprised of a circular chain of an odd number of inverters (single or differential type.) Fig. 2.1 depicts a simple three-inverter ring oscillator. The operating principle can be explained as follows: First, instability may occur with a trigger to the input node of the auxiliary inverters, and after a finite amount of time, feedback of the trigger coming through the followed inverters arrives to the first node causing oscillation.

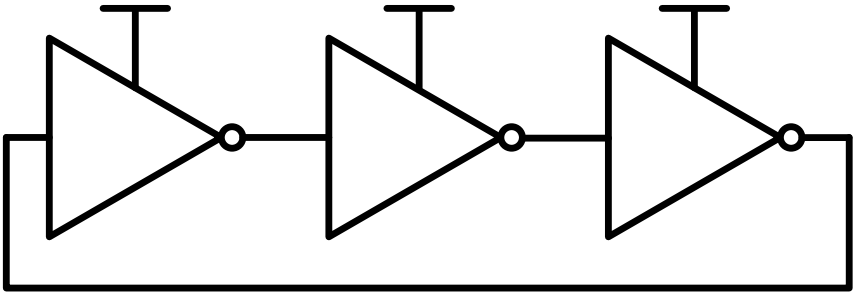

Fig. 2.1 The basic diagram of the ring oscillator.

Each comprising inverter contributes to the delay of the signal around the ring of inverters, and the delay determines oscillation frequency. If t_D represents the time delay for a single inverter, and N indicates the number of inverters in the single-ended ring oscillator, the oscillation frequency is given by:

$$f_{osc} = \frac{1}{2t_D N}. \quad (2.1)$$

Because t_D can be tuned by controlling the inverter voltage, ring oscillators are used as voltage-controlled oscillators (VCOs) in clock generators. Additionally, recent mixed signal systems frequently employ digitally-controlled oscillators (DCOs.) They have digitally controlled resistor (DCR) ladders at the drain nodes of inverters to control the supply voltage, as shown in Fig. 2.2.

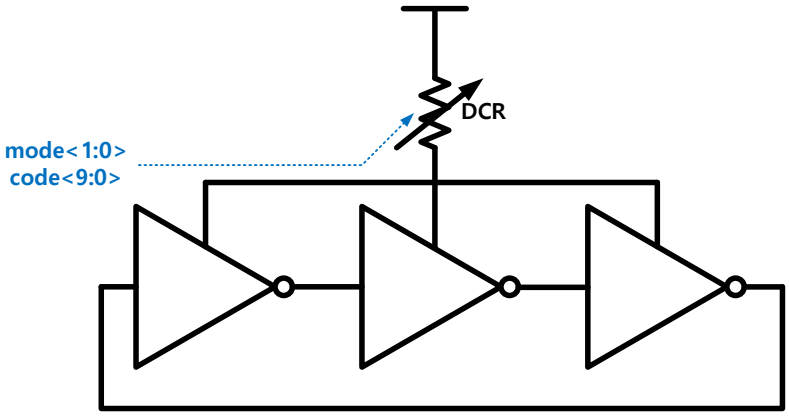

Fig. 2.2 The basic diagram of the digitally controlled ring oscillator.

2.2 Phase Noise in Ring Oscillators

Phase noise is the frequency-domain representation of fluctuations in the phase of a waveform, followed by the concept of jitter, which is the time-domain representation in turn. Today applications (e.g., clock and data recovery (CDR) circuits, frequency synthesizers, and radio frequency (RF) systems) impose more rigorous requirements on the phase noise. Hence analyzing the phase noise and jitter performance of electrical oscillators is essential.

The impulse sensitivity function (ISF), $\Gamma(x)$ [9]-[10] is a delicate mathematical concept illustrating the phase noise generation protocol. The fundamental idea is that the amounts of phase shifts when impulses are injected differ according to the impulse injection timing. For instance, as shown in Fig. 2.3 (a), the phase shift is negligible

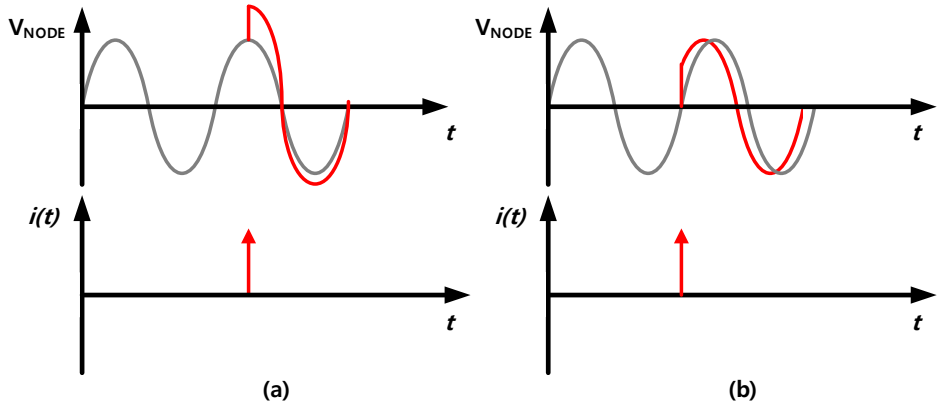

Fig. 2.3 Different phase shift behaviors, (a) and (b) by the impulse injection timing.

when the current impulse occurs at the hill of the oscillating node waveform. On the other hand, as described in Fig. 2.3 (b), when the impulse is injected at the edge of the waveform, there can be a sensitive phase transition. In this sense, the linear-time variant (LTV) ISF, $\Gamma(x)$ can be defined, and as described in Fig. 2.4, this exhibits the edge-sensitive characteristic.

Using ISF, the phase of a practical oscillator, $\phi(t)$ can be written as:

$$\phi(t) = \int d\phi = \int_{-\infty}^{t} \frac{\Gamma(\omega_o \tau)}{q_{max}} i(\tau) d\tau \quad (2.2)$$

where q_{max} is the maximum injected charge and $i(\tau)$ is the injected noise current at the oscillating nodes. For the simplicity, with the assumption that perturbation current $i(t)=I_n\cos[2\pi(nf_o+f_{off})t]$ ($n = 0, 1, 2, \ldots,$) $\phi(t)$ can be calculated by:

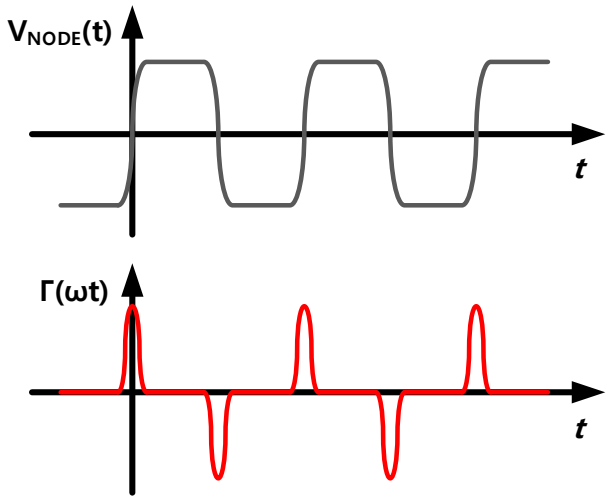

Fig. 2.4 The example waveform and ISF of the typical ring oscillator.

$$\phi(t) \approx \frac{I_n c_n \sin(2\pi f_{off} t)}{4\pi q_{max} f_{off}} \quad (2.3)$$

where,

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n). \quad (2.4)$$

As a result, the single-sideband phase noise at the offset frequency f_{off} is given by:

$$L\{f_{off}\} = L_{thermal} + L_{flicker}$$
$$= \frac{{\Gamma_{rms}}^2}{16\pi^2 {q_{max}}^2} \frac{\overline{{\imath_n}^2}/\Delta f}{{f_{off}}^2} + \frac{{\Gamma_{dc}}^2}{16\pi^2 {q_{max}}^2} \frac{\overline{{\imath_{n,1/f}}^2}/\Delta f}{{f_{off}}^2} \quad (2.5)$$

where,

$$\sum_{n=0}^{\infty} {c_n}^2 = 2{\Gamma_{rms}}^2, \ {c_0}^2 = 2{\Gamma_{dc}}^2 \quad (2.6)$$

and $\overline{\iota_n^2}/\Delta f$ is a (current) white power spectral density (PSD,) and $\overline{\iota_{n,1/f}^2} = \overline{\iota_n^2} \cdot \frac{f_{1/f}}{f_{off}}$ is a flicker noise PSD with a 1/f corner frequency, $f_{1/f}$.

Fig. 2.5 shows that it is possible to approximate $\Gamma(x)$ as a triangular function. With this approximation, Γ_{rms} can be calculated as:

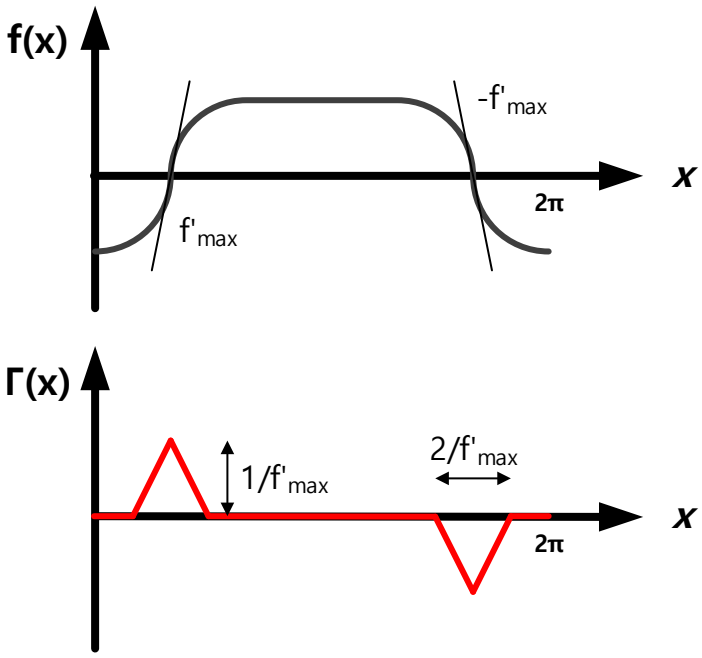

Fig. 2.5 The approximate waveform and ISF for the ring oscillator.

$$\Gamma_{rms}{}^2 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma^2(x)dx = \frac{2}{3\pi}\left(\frac{1}{f'_{max}}\right)^3 \quad (2.7)$$

where f'_{max} is the maximum slope of the waveform depicted in Fig. 2.5.

By using the relationship that $t_D = \eta/f'_{max}$ and $2\pi = 2Nt_D$, illustrated in Fig. 2.6, Γ_{rms} can be expressed as:

$$\Gamma_{rms}{}^2 = \frac{2\pi^2}{3\eta^3}\frac{1}{N^3}. \quad (2.8)$$

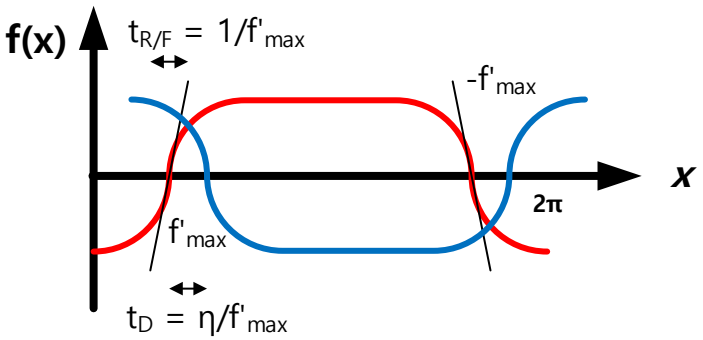

Fig. 2.6 The waveforms of the adjacent oscillation nodes showing the relationship between the rise/fall time and the delay time.

By focusing more on the characteristics of the inverters, it is possible to express the phase noise with the input-referred voltage noise. Fig. 2.7 explains the relationship between voltage and current noises at the common mode bias, V_{CM}. Since the amplification gain $A_0 \approx g_m r_O$, the input-referred noise is given by:

$$\overline{v_{ni}{}^2}/\Delta f = \frac{1}{g_m{}^2}\overline{i_n{}^2}/\Delta f \quad (2.9)$$

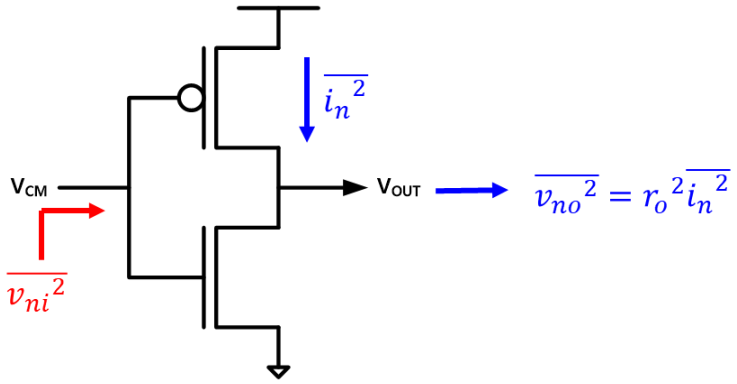

Fig. 2.7 The amplifier-like inverter stage of the ring oscillator at the common mode.

where g_m is the effective transconductance of the transistors.

Finally, by combining the equations (2.5), (2.8), and (2.9), the phase noise in terms of input-referred noise can be calculated as the following:

$$L\{f_{off}\} = \frac{2\pi^2 {g_m}^2/3\eta^3 N^2 \overline{v_{ni}{}^2}/\Delta f}{16\pi^2 {q_{max}}^2 {f_{off}}^2} + \frac{N {g_m}^2 {\Gamma_{dc}}^2 \overline{v_{ni,1/f}{}^2}/\Delta f}{16\pi^2 {q_{max}}^2 {f_{off}}^2}. \quad (2.10)$$

This equation will be used to compare the noise contribution of the ring oscillator and the LDO in the following chapters.

Chapter 3

Supply Noise Transfer Analysis

3.1 Impulse Sensitivity of Supply Voltage

As illustrated in Chapter 2.2, because the amount of phase change due to the current impulse varies according to the injection timing within an oscillation period, the LTV model employing ISF is introduced in [9]-[10]. However, the noise transfer protocol from the supply voltage to the output clock phase exhibits a different aspect.

Fig. 3.1 illustrates the difference in noise contribution protocol for the two cases (a) and (b). The main difference between (a)the phase noise generated itself and (b)the supply noise-induced phase noise comes from the impulse sensitivity of the nodes of interest. The supply voltage change causes the oscillation frequency change, and this change is insensitive to impulse timing.

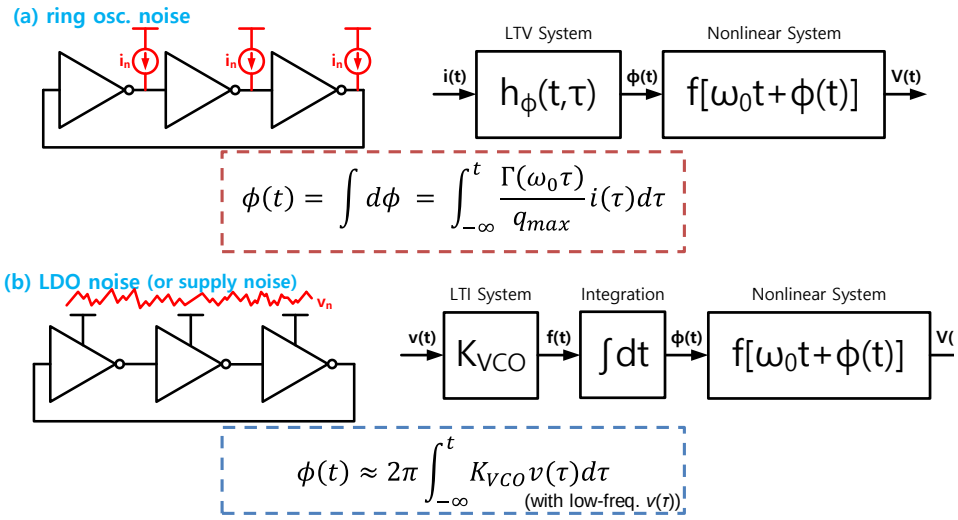

Fig. 3.1 Noise contribution protocols of (a) ring oscillator (internal noise source) and (b) supply noise (external noise source.)

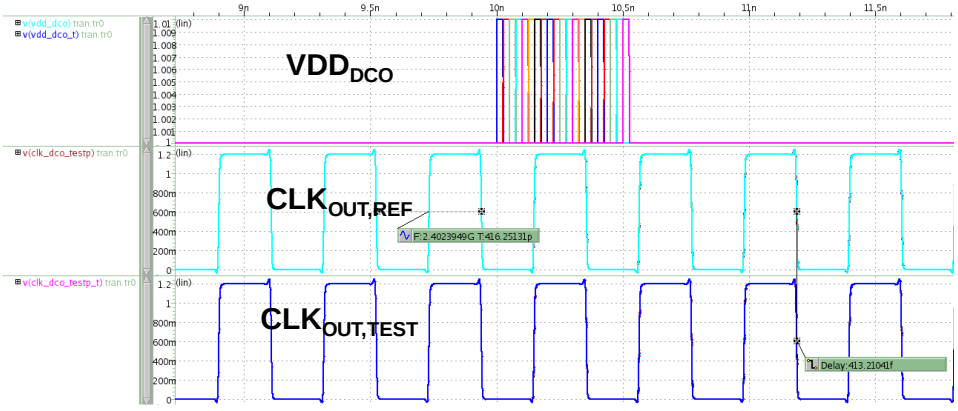

Fig. 3.2 Simulation method of the impulse voltage injection to the supply node.

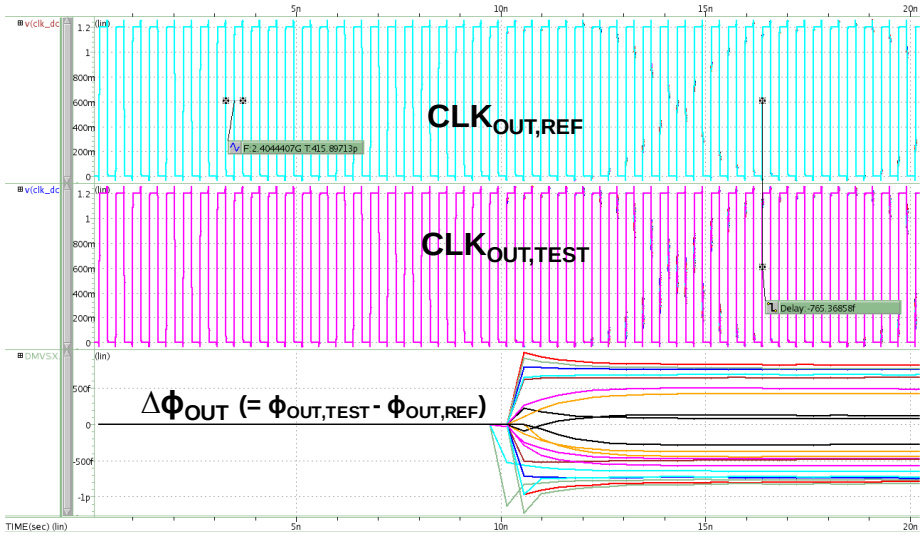

Fig. 3.3 The simulation to measure the amount of the phase shift when the current impulse pair is injected.

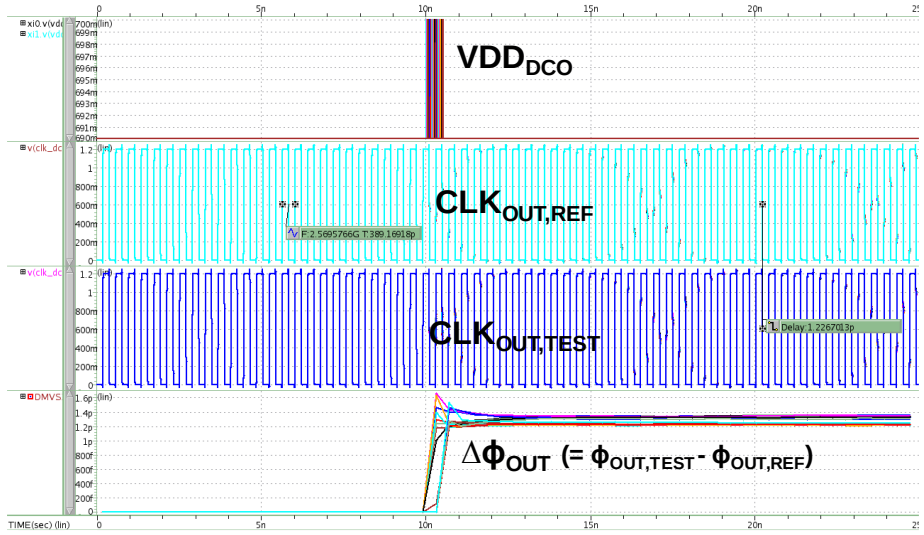

Fig. 3.4 The simulation to measure the amount of the phase shift when the supply voltage impulse is injected.

To verify the impulse sensitivity characteristics, the simulation injecting impulse with different injection timing within an oscillation period is conducted as depicted in Fig. 3.2. The simulation measures the amount of the phase shift when a 25-ps width, 10-mV supply voltage impulse is injected. Fig. 3.3 shows impulse sensitivity with the current impulse pair (+25-μA, -25-μA) at differential nodes. It reconfirms that it is an LTV system sensitive to the impulse injected into the oscillation nodes. Whereas Fig. 3.4 shows the impulse sensitivity result of supply voltage, and regardless of the injection timing, the amounts of the phase shifts are quasi-identical. This result justifies that the linear time-invariant (LTI) model is valid to illustrate the effect of supply noise on phase noise.

3.2 The Effect of Supply Noise on Ring Oscillators

With the result mentioned in Chapter 3.1, the effect of supply noise in ring oscillators can be derived similarly in [9]-[10]. For the perturbation voltage $v(t)=V_n\cos[2\pi(nf_o+f_{off})t]$ $(n = 0, 1, 2, \ldots,)$ $\phi(t)$ is given by:

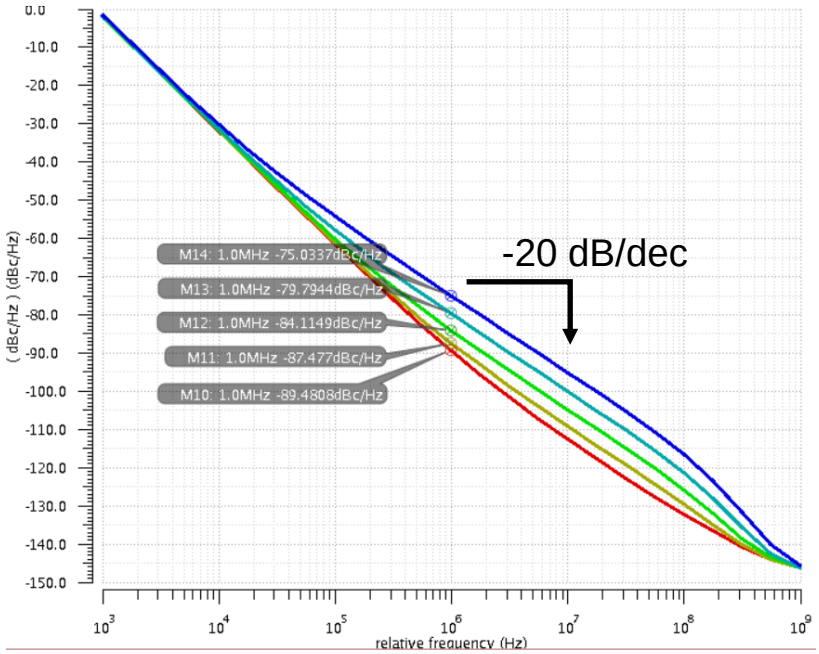

Fig. 3.5 The phase noise plot in the presence of white noises.

$$\phi(t) \approx 2\pi \int_{-\infty}^{t} K_{VCO} v(\tau) d\tau = K_{VCO} V_0 \frac{\sin(2\pi f_{off} t)}{n f_o + f_{off}} \quad (3.1)$$

where K_{VCO} is supply sensitivity (Hz/V.) When $n \geq 1$, $\phi(t)$ is negligibly small since $f_o \gg f_{off}$, and the case with $n = 0$ is only eligible. Thus, the single-sideband phase noise at the offset frequency f_{off} is expressed as:

$$L\{f_{off}\} = \frac{{K_{VCO}}^2}{2} \frac{\overline{v_n^2}/\Delta f}{{f_{off}}^2} \quad (3.2)$$

where $\overline{v_n^2}/\Delta f$ is a supply voltage PSD.

Table I. The simulated and calculated phase noises in the presence of white noises.

Supply noise spectral density (nV/√Hz)	**Calculated phase noise (dBc/Hz)**	Simulated phase noise (dBc/Hz)
0	-90.9	
4.07	**-89.5**	-89.5
7.24	**-87.5**	-87.5
12.9	**-84.1**	-84.1
22.9	**-79.8**	-79.8
40.7	**-75.1**	-75.0

Equation (3.2) is simple enough to calculate the phase noise while the supply voltage PSD is given. To validate equation (3.2), the simulation of ring oscillator phase noise with a white supply noise source is conducted. Fig. 3.5 shows the increased amount of phase noise due to the white supply noise. As shown in Fig. 3.5, it falls 20-dB/dec along with the offset frequency. On the floor of the phase noise value with zero supply noise, phase noises can be calculated according to the injected supply noises using the derived equation (3.2). Finally, comparing the simulated and computed phase noises, as shown in Table I, verifies the strong correlation between the results.

To further analyze the supply noise contribution protocol, it is necessary to recall equation (2.1). Because $q_{max} = It_{R/F}$, where I is a single-stage inverter current, the oscillation frequency can be rewritten as:

$$f_{osc} = \frac{1}{2\eta N q_{max}}. \quad (3.3)$$

With this equation, the supply sensitivity can be calculated as the following:

$$K_{VCO} = \frac{\Delta f}{\Delta V} = \frac{1}{2\eta N q_{max}} \frac{\Delta I}{\Delta V} = \frac{g_m}{2\eta N q_{max}}. \quad (3.4)$$

Therefore, by using the equation (3.2), the phase noise term of the LDO noise portion in the ring oscillator is written as:

$$L\{f_{off}\} = \frac{4\pi^2 {g_m}^2/\eta^2 N^2}{16\pi^2 {q_{max}}^2} \frac{\overline{{v_n}^2}/\Delta f}{{f_{off}}^2}. \quad (3.5)$$

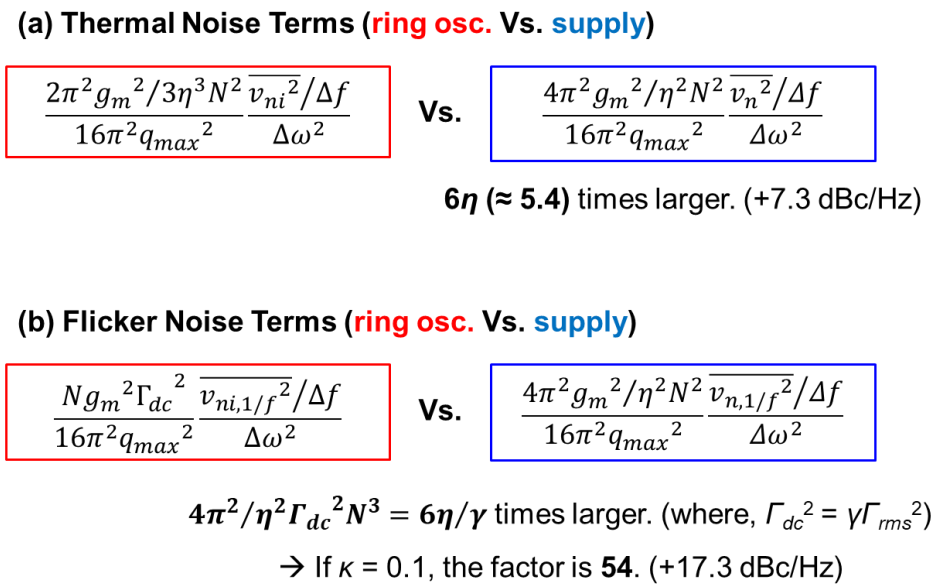

Fig. 3.6 The comparison of the ring oscillator and supply noises in terms of the thermal and flicker noises.

By comparing the two equations (2.10) and (3.5), it can be understood how superior the contribution of the supply noise is compared to that of the internal noise of the ring oscillator. Fig. 3.6 illustrates the comparisons of the thermal noise and flicker noise terms. This shows that it is prone to be degraded by external noise rather than the noise generated internally. For the thermal noise comparison, assuming the same voltage noise level[1], the noise induced from the supply is 6η times larger, resulting in approximately a +7.3 dBc/Hz increase effect in phase noise. When it comes to the

[1] The general circuits are composed of MOSFET transistors and resistive components mostly, and they are the main noise sources of the thermal (or flicker) noise. Hence, for the similar scales of the circuits, the assumption is available for deducing the level of the noise contribution by the comparison.

flicker noise comparison, the contribution of the supply noise is $6\eta/\gamma$ times larger than that of ring oscillator noise, where $\Gamma_{dc}^2 = \gamma\Gamma_{rms}^2$. In practice, γ can be assumed as 0.1, empirically. In this sense, it is more susceptible to flicker noise from the supply rather than the ring oscillator itself, roughly +17.3 dBc/Hz. Therefore, circuit designers should be more careful about the supply noise while designing ring oscillators, especially when they put LDOs or other circuitries at the supply nodes of ring oscillators.

Chapter 4

Effect of LDO Output Noise to Phase Noise of Ring Oscillator

4.1 Necessity of Small-Sized, Capacitor-less LDO

Since contemporary system-on-chip (SoC) designs are comprised of mixtures of analog and digital blocks, supply noises and spurs can be induced externally and internally. On the other hand, because many analog blocks commonly sensitive to supply noise are distributed among intra-chip, small-sized, capacitor-less LDO can be employed to shield the analog blocks from the supply noises, as depicted in Fig. 4.1 [12]-[13]. However, the most noticeable fact is that the LDO is also the main noise

contributor, and the noise level contributed by the LDO higher than that of the ring oscillator itself is occasionally observed.

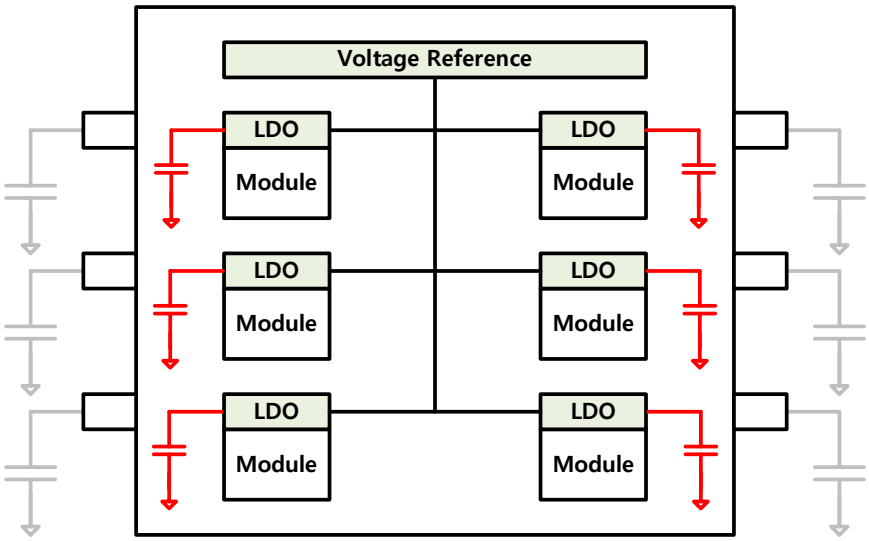

Fig. 4.1 The diagram of distributed, localized capacitor-less LDOs

4.2 Contribution of LDO Internal Noise to Phase Noise of Ring Oscillator

Fig. 4.2 depicts an LDO block diagram comprised of a voltage reference, an error amplifier (EA,) and resistor ladders R_1, R_2, a load capacitor, and a current-sourcing PMOS transistor. Here, the total output noise PSD of the LDO can be written as:

$$N_{OUT}(f) = \left[\left(N_{BGR}(f) + N_{EA}(f)\right)\left(1+\frac{R_1}{R_2}\right)^2 + N_{R2}(f)\left(\frac{R_1}{R_2}\right)^2 + N_{R1}(f)\right] \cdot T_N(f)^2 \quad (4.1)$$

where $T_N(f)$ is a transfer function normalized to $(1+R_1/R_2)$.

To derive an explicit form of the phase noise of the ring oscillator with DCR due to the LDO noise, the Thevenin equivalent model in Fig. 4.3 can be employed. Therefore, the phase noise contributed by the LDO can be calculated as:

$$L\{f_{off}\} = \frac{{K_{VCO}}^2}{2}\frac{\overline{v_n^2}/\Delta f}{{f_{off}}^2} = \frac{1}{2}\left(\frac{R_{eq}}{R_{DCR}+R_{eq}}\right)^2\left(\frac{N_{OUT}(f)}{4kT\gamma/g_m}\right)\frac{kT}{P}\frac{V_{CORE}}{V_{char}}\frac{{f_{osc}}^2}{{f_{off}}^2} \quad (4.2)$$

where g_m is an equivalent transconductance of the MOSFETs in the ring oscillator's inverter chain. Here, the form of the equation (4.2) is similar to that in [10], which is:

$$L\{f_{off}\} = \frac{8}{3\eta}\frac{kT}{P}\frac{V_{CORE}}{V_{char}}\frac{{f_{osc}}^2}{{f_{off}}^2} \quad (4.3)$$

representing the phase noise of the ring oscillator itself, assuming that Γ_{dc} is zero (the flicker noise is negligible, and the white noise is dominant.)

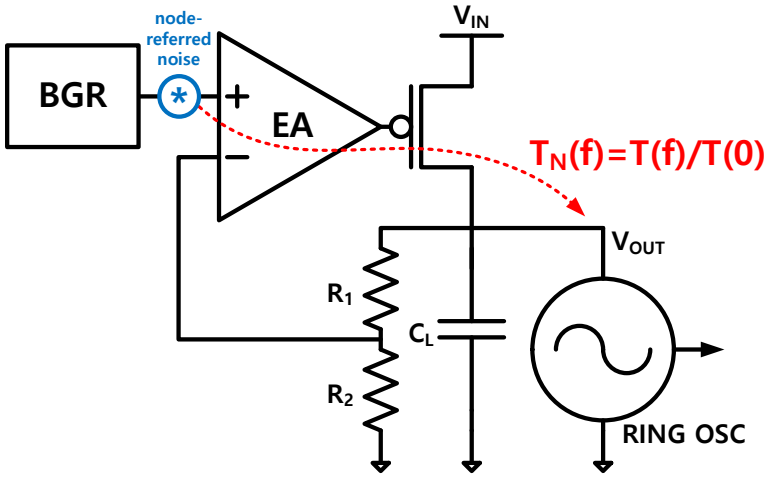

Fig. 4.2 The basic LDO block diagram with noise transfer.

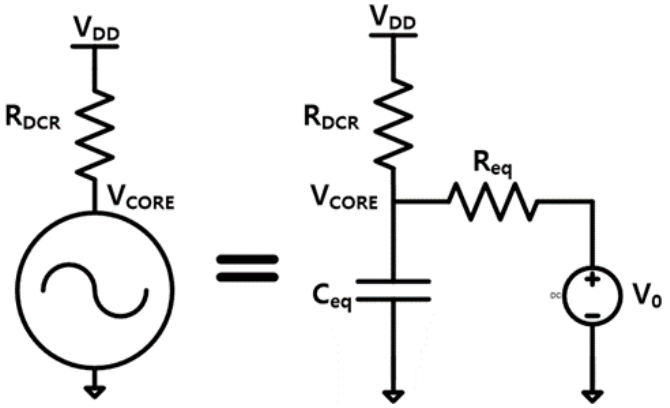

Fig. 4.3 Thevenin equivalent model of the ring oscillator.

By comparing the two equations (4.2) and (4.3), some valuable insights can be taken. First, because the basic form of those two equations is the same, the ratio between N_{OUT} and $4kT\gamma/g_m$, the ring oscillator's device noise, determines the phase noise

contribution. In this sense, the LDO's area and power consumption determining N_{OUT} should be sufficiently large to alleviate the ratio below a certain level. Second, the closer the ratio R_1/R_2 to zero, the noise performance gets better. When it is zero, N_{BGR}+N_{EA} only remains for N_{OUT}. Third, bigger R_{DCR}, the supply noise contribution decreases. However, it should be considered that it can also generate large white noise ($4kTR_{DCR}$.)

4.3 Proposed Figure of Merit

Focusing on the dominant noise source, N_{EA}, the LDO output noise should satisfy the following:

$$N_{OUT} < 16kT\gamma/g_m. \quad (4.4)$$

Here, a new figure of merit can be defined to indicate how well the LDO is optimized, targeting the supply regulation of a ring oscillator and its phase noise. Because $g_m = \sqrt{(2\kappa I)}$, the proposed figure of merit regarding noise performance (FoM_N) can be written as:

$$FoM_N = -10\log N_{OUT}[\mathrm{V}^2/\mathrm{Hz}] - 5\log I[\mathrm{uA}]. \quad (4.5)$$

If you try to enlarge κ to enhance FoM_N, the stability of the LDO may be degraded due to the bandwidth increase. Therefore, reducing the value of FoM_N while keeping the loop stability is a key factor in an LDO optimization process.

Chapter 5

Capacitor-less LDO Design and Optimization for Ring Oscillator

This chapter introduces the LDO design framework to optimize the LDO for regulating the ring oscillator.

Fig. 5.1 is the design framework based on the FoM_N definition. The first optimization step is designing a skeleton LDO with a default structure. Because it is the first step, securing a sufficient stability margin is important. The next step is enlarging the widths of MOSFETs in the EA, maintaining the power consumption constant. Because most designs suffer from the power consumption budget, there is no significant burden in increasing the transistors' sizes. Furthermore, since g_m is proportional to the root of the widths, N_{OUT} decreases. The last step is to increase the power consumption to enhance the noise performance, which is unable to be achieved by the second step due to its loop stability.

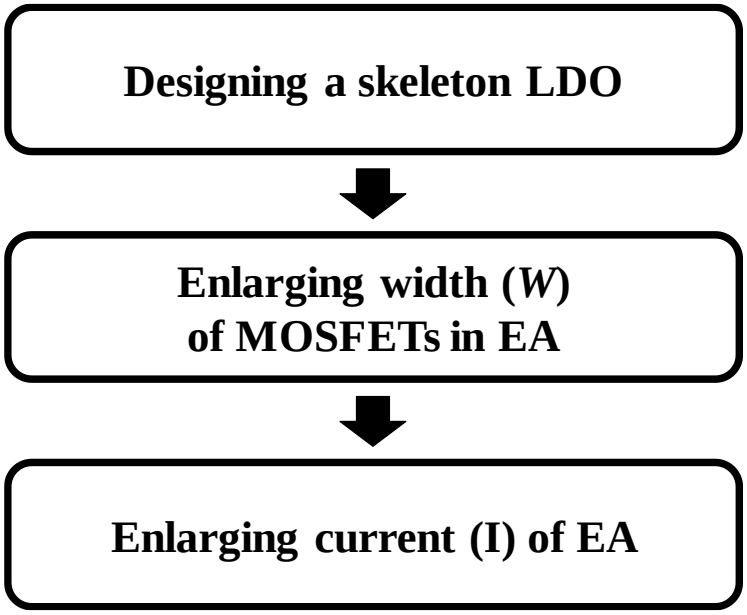

Fig. 5.1 The LDO design framework for the optimization.

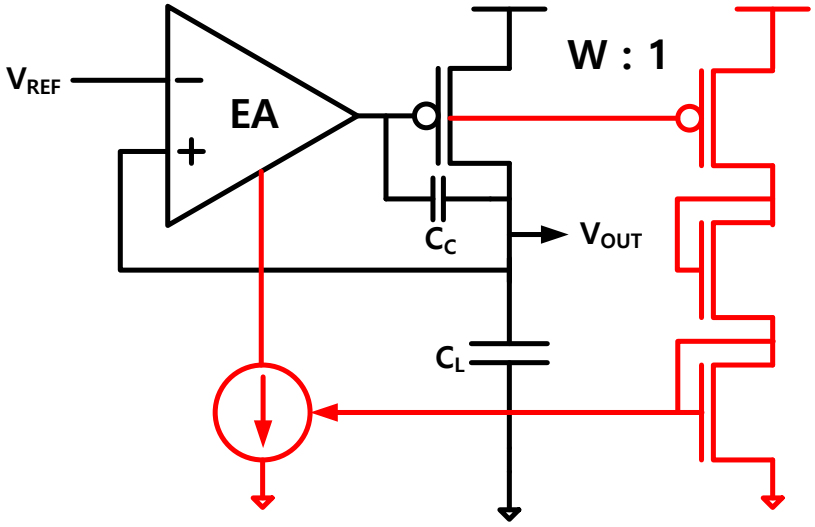

Fig. 5.2 The proposed self-biased LDO architecture.

Furthermore, the self-biased LDO scheme is proposed to avoid the large quiescent power sacrificed to the noise performance. Fig. 5.2 shows the proposed architecture. The current mirror copies and scales the load current and feeds it to the bias of the EA. Finally, it can dynamically scale the power proportional to the load current, saving power consumption and effectively maintaining stability over a wide operating range of the load current.

Chapter 6

Simulation Results

To examine the design framework and compare the optimization steps in section IV, this paper proposes the architecture composed of four LDO blocks representing each optimization step as Fig. 6.1. The LDO1 and LDO2 represent nominal and optimized LDOs, and LDO3 and LDO4 are self-biased LDOs. The difference between LDO3 and LDO4 is the existence of ladder resistors, R1, and R2, which bleed the current significantly. Therefore, LDO4 eliminates the ladder resistors to diminish power consumption and noise level simultaneously.

The proposed architecture has four enable pins to test each LDOs separately. Additionally, the external voltage V_{EXT} can be applied to measure the inherent phase noise generated from the ring oscillator.

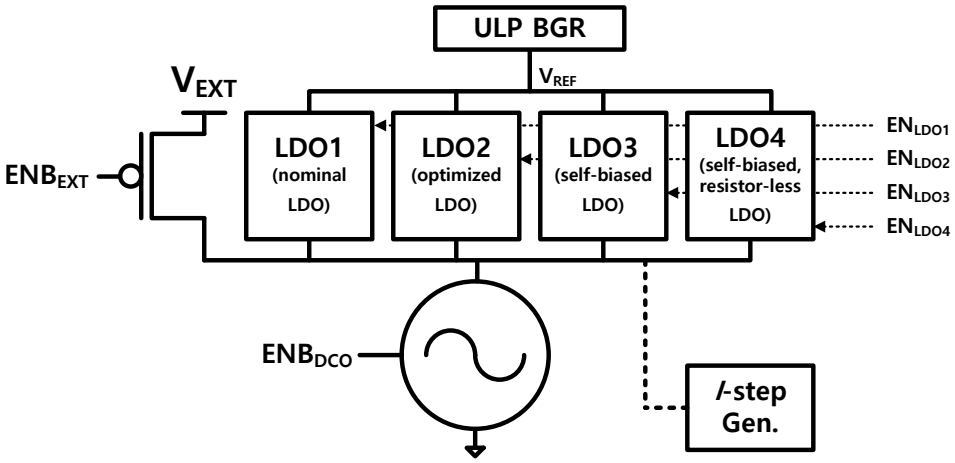

Fig. 6.1 The overall configuration comprised of four LDO test blocks.

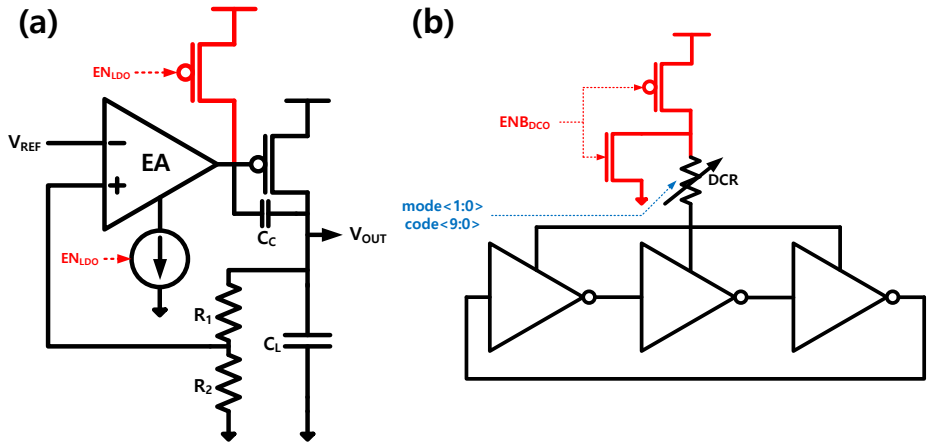

Fig. 6.2 The scheme to switch the (a) LDO and (b) ring oscillator.

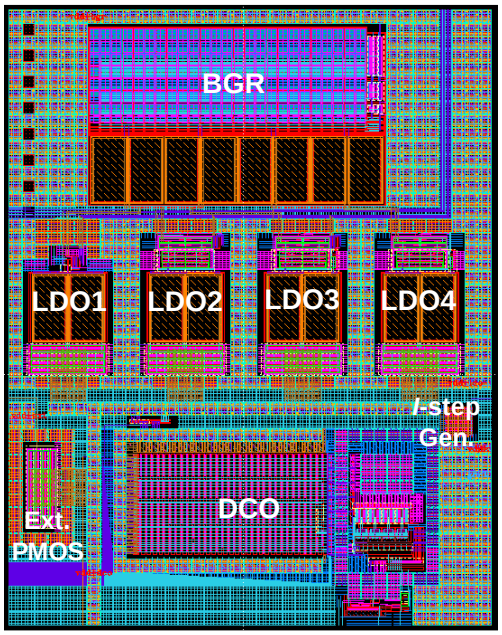

Fig. 6.3 The layout of the proposed architecture.

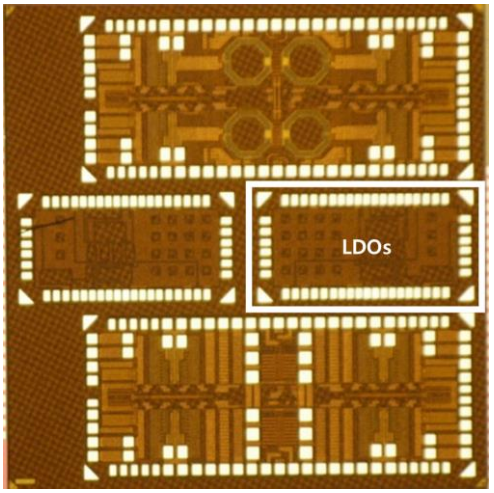

Fig. 6.4 The die photograph of the implemented LDOs.

Because completely turning LDOs on and off is essential, a proper switching method is employed, as depicted in Fig. 6.2. When EN_{LDO} in Fig. 6.2 (a) is high, the current sourcing PMOS is turned off, and at the same time, EA is turned off to avoid unwanted current bleeding. Also, for the measurement of LDO without the ring oscillator, ENB_{LDO} in Fig. 6.2 (b) is applied so that it can completely power off the oscillator by connecting the supply node of the inverter chain to the ground.

The layout of the implementation of the proposed architecture is shown in Fig. 6.3. Also, it is fabricated in a Samsung 65-nm CMOS process, and the die photograph is presented in Fig. 6.4.

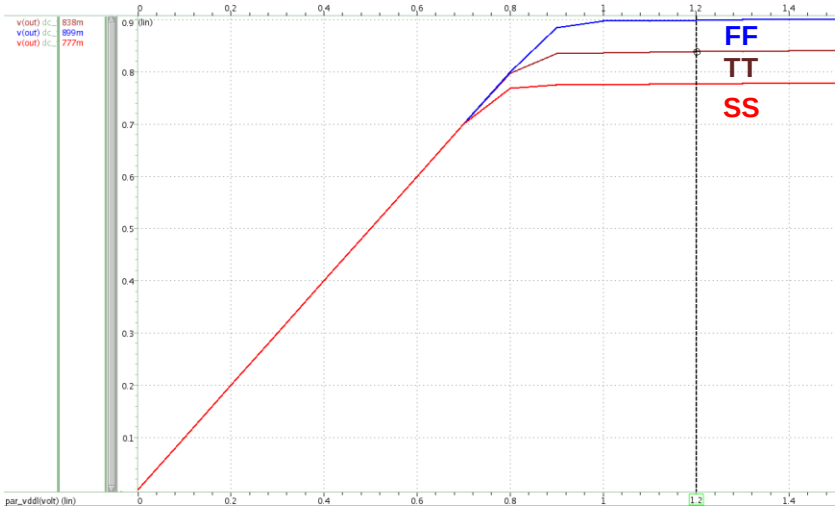

Fig. 6.5 The voltage reference output voltage according to supply voltage at three different process corners (TT, FF, SS.)

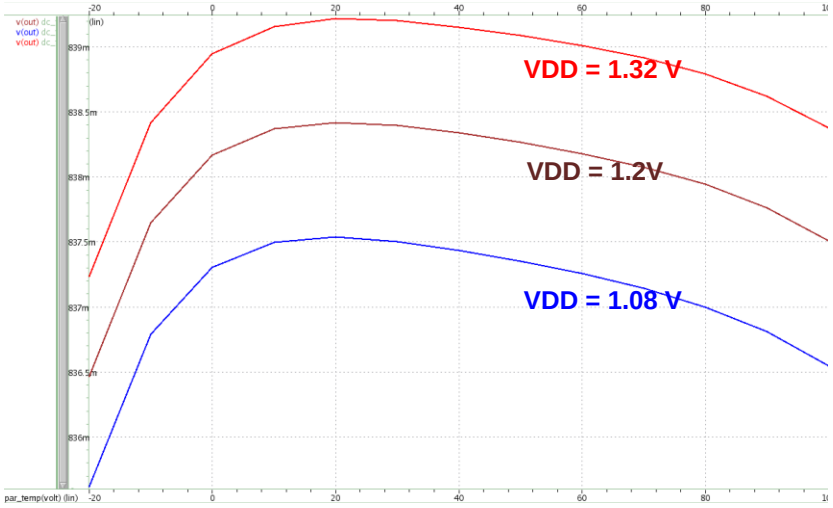

Fig. 6.6 The voltage reference output voltage according to the temperature at three different voltage corners (1.08 V, 1.2 V, 1.32 V).

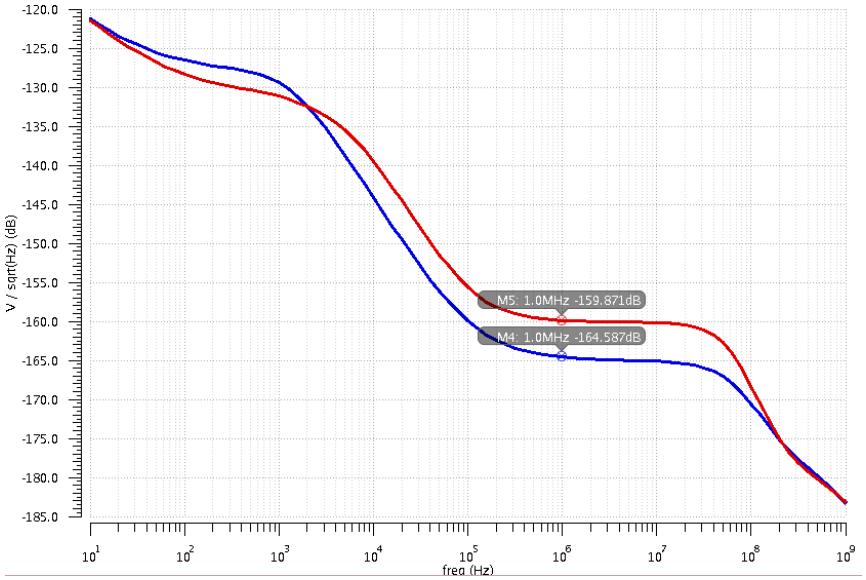

Fig. 6.7 The output noise plot of LDO3 and LDO4.

The voltage reference exploits a stacked version of ultra-low power (ULP) voltage reference in [11] to generate 0.8 or 1.0-V. The insensitivity to process, voltage, and temperature (PVT) variation is requisite for a good voltage reference. Fig. 6.5 and 6.6 are the simulation results of sweeping voltage and temperature at three different conditions. As shown in Fig. 14 and 15, the maximum change in the output voltage due to process variation is 120-mV (15%,) and the full difference due to temperature variation is only 2-mV (<1%.)

The output noise of the voltage reference is also critical since it is directly transferred to the LDO output noise level, significantly affecting the phase noise degradation. The simulated output noise of the voltage reference was only 1.14-nV/√Hz at 1-MHz, which is the frequency of interest.

The implemented voltage reference consumes 0.043-mm^2 die area and 2.4-μA current. However, since the voltage reference output voltage can be shared among multiple LDOs, the area is not a big deal.

The performance comparison between LDO1 and LDO2 is illustrated in Table II. Along with the optimization steps, transistor width optimized LDO (*W*-optimized LDO) and transistor width, current optimized LDO (*W*, *I*-optimized LDO) exhibits better phase noise compared to the nominal one (LDO1.) Also, the consumed areas of LDO1 and LDO2 are 0.0067-mm^2 and 0.0081-mm^2, which are almost the same size. Additionally, considering the ring oscillator size, 0.026-mm^2, and its current consumption, 810-μA, the optimized LDO (LDO2) consumes only 17% die area and 30% power consumption compared to the single ring oscillator.

Table II. The performance comparison between nominal and optimized LDO.

LDO type	DC loop gain (dB)	PSRR @ 1-MHz (dB)	Load regulation (20-ns edge time, 0.1 → 5 / 5 → 0.1 mA) (mV)	Phase noise (w/ ring oscillator) (dBc/Hz)
nominal LDO (LDO1)	28.5	-20	120/140	-79
W-optimized LDO (LDO2)	27.8	-22	170/110	-83
W,I-optimized LDO (LDO2)	**25.6**	**-28**	**105/105**	**-86**

The output noise comparison among the self-biased LDOs, LDO3, and LDO4 is shown in Fig. 6.7. The difference in noise levels is about 5-dB, reflecting that the noise contribution from the ladder resistors is significant.

Finally, the simulation results of LDO3 and LDO4 are illustrated in Table III. Most performance parameters, such as line regulation and load regulation, are almost the same. However, the quiescent current of LDO4 is ten times smaller than LDO3. As a result, the final optimized LDO (LDO4) exhibits 5.9-nV/√Hz output noise at 1-MHz, consuming only 5-uA quiescent current in a standby state and 0.051-mm^2 die area.

Table III. The Performance of LDO3 and LDO4

Parameter	Condition	Specification		Unit
		LDO3	LDO4	
V_{IN}	-	1.2		V
V_{OUT}	-	1.0		V
I_L	Maximum average load current	5		mA
I_Q	Stand-by mode (w/ BGR)	50	5	μA
On-die capacitor	C_{OUT} / C_C / C_{IN}	0 / 5 / 10+10		pF
Line regulation	-	0.034	0.033	V/V
Load regulation	-	3.2	3.2	mV/mA
Load transient	0.1 → 5 / 5 → 0.1 mA (edge time = 20 μs)	100 /100	100 /100	mV
PSRR	@ 1-MHz	-24	-23	dB
Area	LDO only / LDO+BGR	0.0082/0.051	0.0081/0.0052	mm^2

Chapter 7

Conclusion

An analysis of the phase noise degradation due to the supply noise in ring oscillators and the effect of the LDO output noise on the phase noise is presented. The proposed analysis assumes the transfer of supply noise to phase noise as an LTI system, and the obtained similar equation terms of the ring oscillator and LDO noises give meaningful insights. It is revealed that considering g_m, R_1/R_2, and R_{DCR} while designing an LDO is crucial for low-noise design. This thesis presents noise, power-optimized LDO architecture, and its performance with simulation results. This can be applied to distributed, localized LDOs for noise-sensitive analog blocks with the virtue of their small size, low noise, and low power consumption.

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초 록

본 논문에서는 링 오실레이터의 입력 전압 노이즈와 전압 레귤레이터(LDO)의 영향에 대한 정량적인 분석 방법론을 제안하였다. 입력 전압 노이즈에 의한 링 오실레이터의 위상 노이즈(phase noise) 열화는 중요하게 다뤄지고 있지만, 지터(jitter)와 위상 노이즈의 열화 정도를 계산할 수 있는 섬세한 모델이 없었다. 이러한 이유로 많은 회로 설계자들은 입력 전압 노이즈에 대한 영향을 고려하는 데 어려움이 있었고, 실리콘 칩을 만들기 전과 후의 노이즈 레벨 차이(시뮬레이션과 측정 간 결과 차이)가 빈번하게 있었다. 본 논문에서는 입력 전압 노이즈와 전압 레귤레이터가 자체 발생하는 노이즈 사이에서 타협할 수 있는 이론적 기반을 제시하였다. 또한 노이즈와 소모 전력의 제약 하에 전압 레귤레이터를 어떻게 최적화할 수 있는지에 관한 설계 가이드를 함께 제공하였다. 최적화된 전압 레귤레이터 설계는 1-MHz 오프셋에서 5.9-nV/√Hz 의 출력 노이즈를 나타냈고, 오직 5-uA 의 대기 전력을 소모했으며, 레퍼런스 전압 생성기를 포함하여 0.051-mm^2 의 칩 면적을 차지하였다.

주요어 : 링 오실레이터, 전압 레귤레이터, 충격 민감도 함수, 입력 전압 노이즈, 위상 노이즈

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