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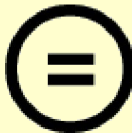

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Ph.D. Dissertation of Materials Science and Engineering

Performance optimization of the TiO_2-based electronic bipolar resistive switching memristor and its neuromorphic computing application

August 2023

Graduate School of Engineering
Seoul National University
Department of Materials Science and Engineering

Xiang Yuan Li

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Adviser: Prof. Cheol Seong Hwang

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Seoul National University
Department of Materials Science and Engineering

Xiang Yuan Li

Confirming the Ph.D. Dissertation written by
Xiang Yuan Li
August 2023

Chair	Sang Bum Kim	(Seal)
Vice Chair	Cheol Seong Hwang	(Seal)
Examiner	Min Hyuk Park	(Seal)
Examiner	Kyung Min Kim	(Seal)
Examiner	Hae Jin Kim	(Seal)

Abstract

In recent decades, there has been significant research activity in resistance random access memory (RRAM) for both one transistor-one resistor and crossbar array configurations. Conventional RRAM devices based on conductive filaments (CFs) suffer from issues such as hard breakdown during electroforming, non-uniformity, and high power consumption. In contrast, electronic bipolar resistance switching (e-BRS) devices, which rely on the trapping and de-trapping of carriers, offer a more favorable alternative. The gradual current switching in e-BRS reduces the likelihood of electrical breakdown, and the absence of an electroforming step is an advantage. Moreover, e-BRS devices exhibit area scalability, making them suitable for integration in crossbar arrays, resulting in reduced power consumption. These devices have also shown potential in flexible memory, security applications, and artificial synapse implementations. However, the endurance and retention performance of many reported e-BRS devices have been unsatisfactory. These issues necessitate the development of suitable methods to prevent oxygen loss and improve device performance.

The Al/TiO_2/Al resistance random access memory (RRAM) showed an area-type electronic bipolar resistive switching (e-BRS)

mechanism, which was mediated by the trapping and detrapping of the carriers at the trap centers. The area-type e-BRS device had area-scalable characteristics and excellent uniformity, which are beneficial for large-scale integrated applications. However, the unsatisfactory endurance and retention performance needed to be improved. In this work, a 1-2nm-thick ZrO_2 thin layer was deposited by the thermal atomic layer deposition on the 25nm-thick sputter-deposited TiO_2 layer to form an $Al/ZrO_2/TiO_2/Al$ memory cell. The thin ZrO_2 layer effectively prevented the active Al top electrode from absorbing oxygen from the TiO_2 resistive switching (RS) layer without significantly affecting the asymmetric energy barrier structure of the device. The suppression of oxygen loss from the TiO_2 RS layer retained the desired trap density of the RS layer even after the extended switching cycle operation. This suppression effect significantly improved the RS performances, such as endurance, uniformity, and retention. The switching endurance was enhanced over two orders of magnitudes (from $<10^3$ to $>10^5$). The ZrO_2 layer also increased the overall resistance values of the memory cell, making it more suitable than the $Al/TiO_2/Al$ structure for high-density applications.

Spiking neural networks (SNN) have attracted considerable interest as a more energy-efficient alternative to deep learning

methodologies. The crucial requirement for artificial synapses in neuromorphic systems lies in their capacity to demonstrate synaptic plasticity, enabling the modulation of synaptic strength through electrical stimulation. Nonvolatile memory devices, such as resistive random access memory, hold promise for emulating artificial synapse functions. Despite the simplicity and flexibility offered by RRAM, many devices suffer from undesired properties due to their reliance on conductive filaments-controlled mechanisms, which exhibit abrupt and stochastic behavior. In contrast, non-filamentary RRAM devices present superior attributes including enhanced uniformity, scalability, and reduced power consumption. However, research on non-filamentary memristors for synaptic applications remains limited. Hence, there is significant potential in exploring and optimizing non-filamentary RRAM as a viable solution for artificial synapses in future studies.

This study presented an Al/ZrO_2/TiO_2/Al (AZTA) memristor based on a non-filamentary mechanism for simulating artificial synapses in spiking neural networks (SNN) for neuromorphic computing. This device feasibly implemented short-term plasticity, long-term plasticity, paired-pulse facilitation, and spike-timing-dependent plasticity through precise modulation of the shapes of pre- and post-synaptic spikes. Additionally, the AZTA device demonstrated high

linear and symmetrical potentiation and depression under identical pulse operation conditions, facilitating multivalued conductance without auxiliary circuits. The trapping and de-trapping of electrons control the synaptic weight at different depth energy levels provided by oxygen vacancy traps. Also, the AZTA memristor showed promising potential for low power consumption and high operating speed due to its area-dependent behavior based on the electronic bipolar resistance switching mechanism. The simulation of the multilayer perceptron with 400 input, 100 hidden, and 10 output neurons using the AZTA synapses can reach 94.9% accuracy of the MNIST dataset.

Keywords: TiO_2-based resistance random access memory, electronic bipolar resistive switching mechanism, ZrO_2 insertion layer, area-dependent behavior, artificial synapses, non-linearity, spiking neural networks, neuromorphic computing

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Chapter 1. Introduction

1.1. Resistance random access memory (RRAM)

Non-volatile memory is a storage technology that is very different from traditional random access memory (RAM), such as DRAM or SRAM, in that it is able to store data in the event of power failure. In the past decade, this type of non-volatile memory device has developed rapidly and is widely used in many fields, such as smart electronic devices (such as mobile phones, computers, in-vehicle systems), encryption technology, artificial intelligence, etc.[1-4] The resistance random access memory has been widely concerned because of its excellent performance, such as fast read and write speed, low power consumption, and compatibility with CMOS technology.[5-9]

Resistive switching was first observed by Hickmott in 1962 in binary oxides, but it was in the early 2000s only when the resistive switching effect caught huge interest triggered by the search for alternative memory technology. The concept of RRAM used for neural networks and logic circuits was first published in Nature by HP in 2008.[10] The paper titled “The Missing Memristor Found” triggered another heat of RRAM development.

Usually, Resistance random access memory consists of a metal-

insulator-metal (MIM) structure, including a top electrode, an intermediate layer as the resistance switching layer, and a bottom electrode.[11] Such a typical MIM-structured RRAM device is schematically shown in Figure 1.1 (a). Under the action of applied voltage, the resistance of the device will be reversibly switched to realize data storage and reading, as shown in Figure 1.1 (b).

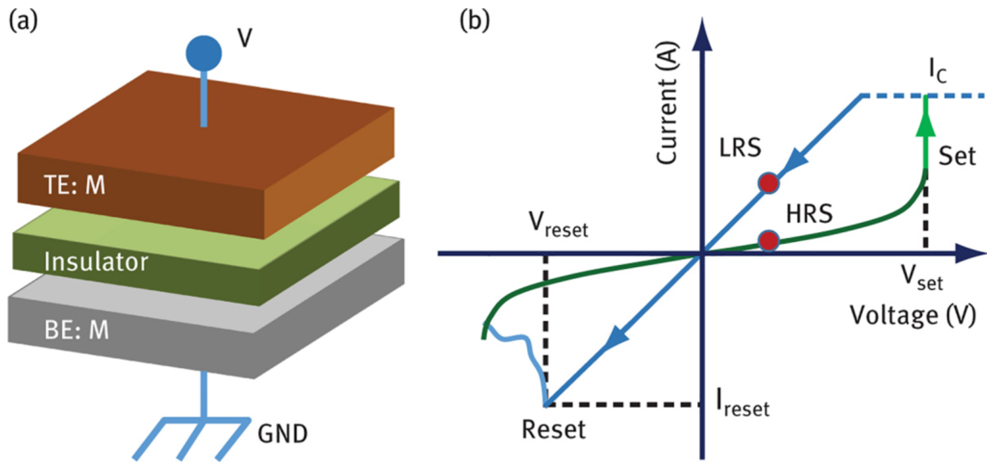

Figure 1.1. (a) Schematic diagram showing typical metal-insulator-metal (MIM) structure of ReRAM with electrical biasing. (b) Schematic illustration of bipolar switching characteristics in ReRAM. For the bipolar switching, "set" and "reset" processes occur at different polarity.[11]

1.2. Two resistance switching mechanisms

At present, the mainstream resistance switching mechanism can be divided into the filamentary type and non-filamentary type, also known as the interface type.

Filamentary-type resistance random access memory devices are controlled by the random formation and rapture of conductive filaments, which are usually composed of oxygen vacancies or active metal ions (such as copper ions, silver ions, etc.), so the resistance transition relies on highly localized conductive filaments, usually tens or tens of nanometers in diameter. There is no doubt that the formation of conductive filaments will inevitably lead to the problem of high power consumption, and the randomly formed conductive filaments also lead to the problem of poor uniformity and low reliability.

In contrast, non-filamentary types of resistance random access memory devices based on oxygen vacancy/ion movement or carrier capture and release control have irreplaceable advantages in some aspects and maybe a better choice. The resistance switching of this type of resistive device occurs over the entire area, so it usually exhibits slow resistance changes, resulting in excellent uniformity, and is not prone to hard breakdown that can cause device failure. In addition, the power consumption of non-filamentary type devices can

be reduced proportionally with the reduction of device size, and this area scalability is particularly beneficial for improving the integration of CBA RRAM. Unfortunately, although non-filamentary resistive devices show many advantages, the reported devices are usually accompanied by poor endurance and retention performance.

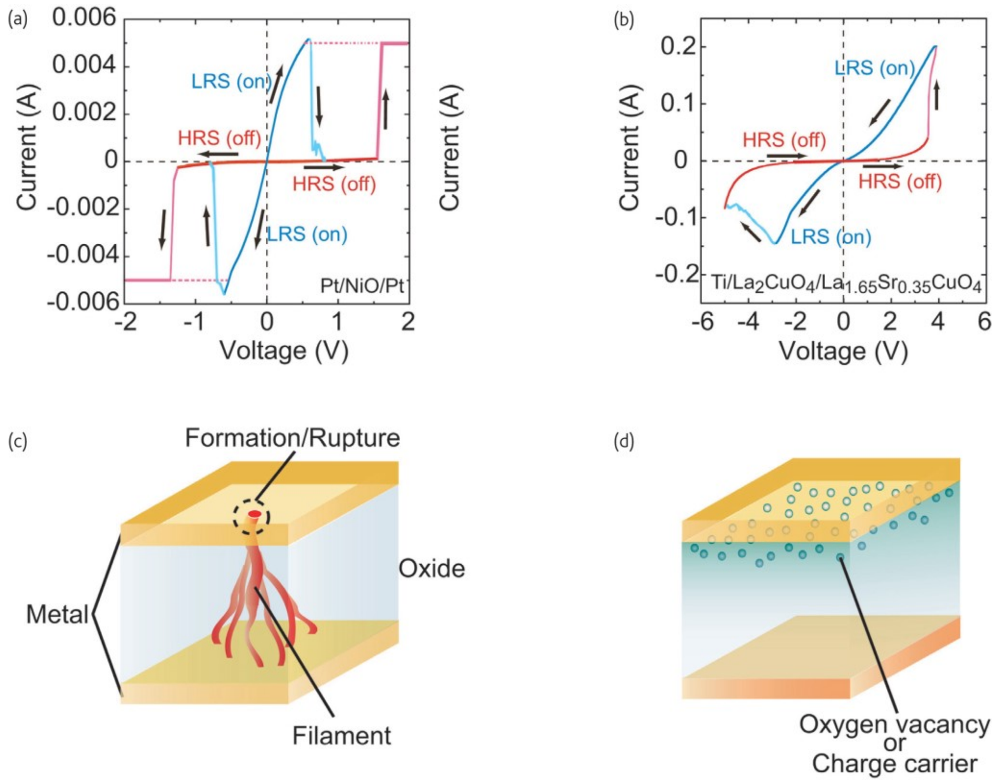

Figure. 1.2. I-V curves for (a) unipolar (nonpolar) switching in a Pt/NiO/Pt cell and (b) bipolar switching in a Ti/La_2CuO_4/$La_{1.65}Sr_{0.35}$ CuO_4 cell. In unipolar switching, the switching direction depends on the amplitude of the applied voltage. Bipolar switching shows directional resistance switching according to the polarity of the applied voltage. Proposed models for resistive switching can be classified according to either (c) a filamentary conducting path, or (d) an interface-type conducting path. (Part (a) courtesy of I. H. Inoue, AIST.)[12]

1.3. Artificial synapses based on nonvolatile memristors for the neural networks

Current neural networks are based on von Neumann architecture, combined with machine learning as a combination of software and hardware components based on complementary metal oxide semiconductor (CMOS) technology. However, the von Neumann computing system requires a central processing unit (CPU) to perform serial operations, its structural design is very inflexible and requires a large number of transistors. Because of this von Neumann bottleneck, the data processing speed of the storage device is limited between the memory and the CPU, forming a storage wall that requires great power consumption and space. Therefore, there is an urgent need for a new neuromorphic computing system with high computing speed, low energy consumption, and small size.

In order to meet this requirement, various memory materials have been studied to simulate the various functions of human brain synapses, as shown in Figure 1.3.[13] A memristor device can function as a single synaptic unit without the need for additional software programming support. The neuromorphic architecture based on a non-volatile memristor is implemented by parallel operation, which has the characteristics of low power consumption, small volume, and

high data processing capacity.

The concept of artificial synapses can be traced back to the 1940s when researchers first began exploring the construction of artificial neural networks. These networks were designed to perform tasks similar to the human brain, and early prototypes employed simple circuits to implement artificial synapses. In recent years, the rapid advancement of technology has allowed researchers to investigate more complex neural networks to achieve more advanced artificial intelligence systems. As a result, artificial synapses have received widespread attention as a key electronic component of these systems, designed to simulate the behavior of biological synapses, which are the connections between neurons in the brain. The primary requirement for artificial synapses that can be used in neuromorphic systems is their ability to exhibit synaptic plasticity, which is the ability to change synaptic strength based on electrical stimulation.[1, 3, 14-16] In addition to synaptic plasticity, other crucial indicators that must be considered include power consumption, scalability, signal-to-noise ratio, operation speed, reliability, non-linearity and so on.[17-21] Currently, there are numerous emerging non-volatile memory devices, including resistive random access memory (RRAM),[22-28] magnetic random access memory (MRAM),[29, 30] phase change memory (PCM),[31, 32] and ferroelectric memory (FRAM),[33-36] that have

been reported to simulate artificial synapses in neuromorphic computing systems. However, few devices can simultaneously fulfill all the necessary requirements for an ideal artificial synapse. Out of these options, metal-oxide RRAM has been widely studied due to its exceptional physical properties, electrical adjustability, and compatibility with traditional complementary metal-oxide-semiconductor (CMOS) integration processes.[37, 38] A schematic diagram of artificial synapses stimulating biological synapses based on ReRAM is shown in Figure 1.4.[13]

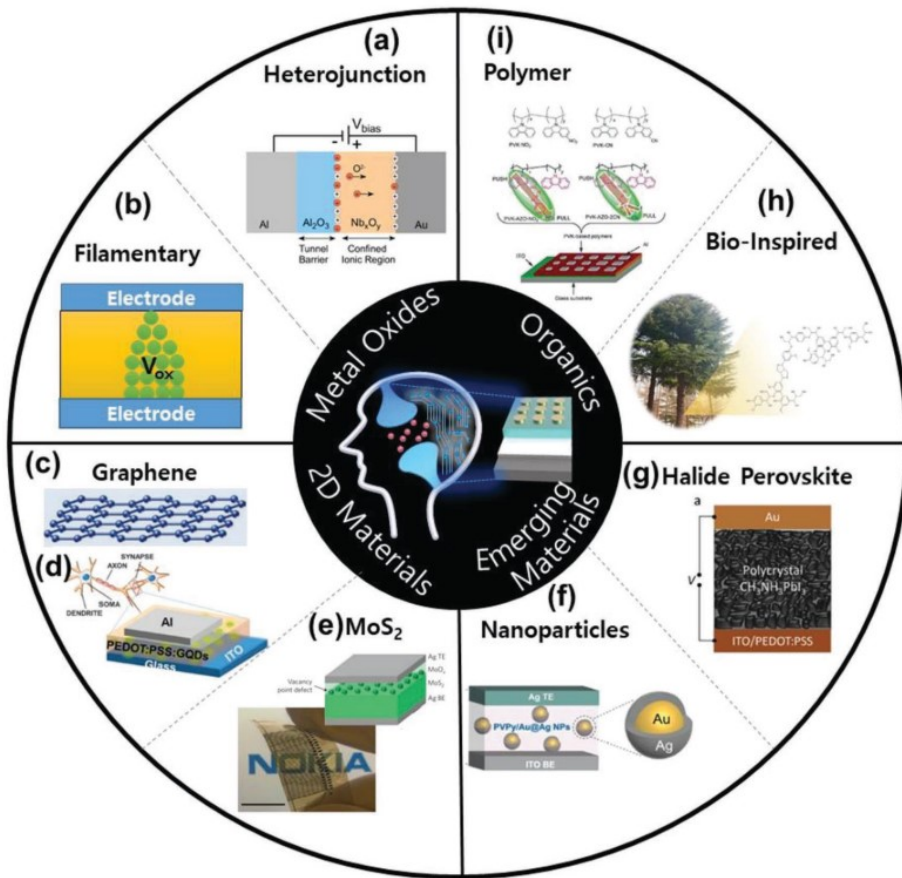

Figure. 1.3. Recent memristive materials applied for artificial synapses: metal oxides, organic materials, 2D materials, and emerging materials.[13]

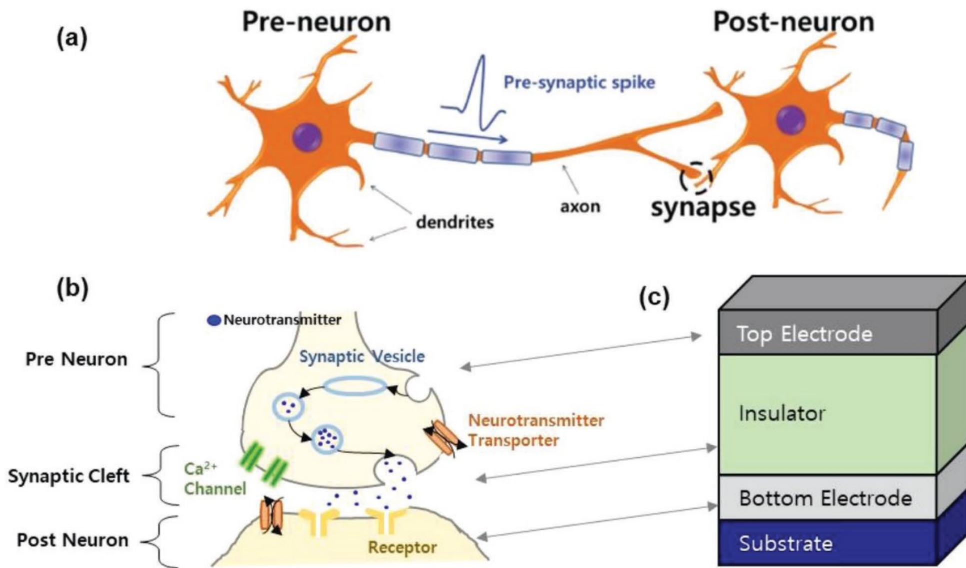

Figure. 1.4. Comparison between biological synapses and artificial synapses. a) Schematic diagram of a preneuron, postneuron, and synapse. Reproduced with permission. b) Schematic diagram of neurotransmission process. c) A general structure of two terminal memristors-based artificial synapses.[13]

1.4. Nonlinearity of the artificial synapses based on RRAM devices

As mentioned in the previous section, an ideal artificial synapse needs to meet a variety of performance indicators, among which non-linearity is a very important one, as shown in Figure 1.5.[17] Under ideal conditions, the device can greatly reduce the design pressure of the peripheral circuit, and it is expected to obtain satisfactory multiple operable states.

Ideal linearity is defined as a state in which changes in conductance update due to a potentiation/depression do not depend on the current conductance state. To obtain the linearity factor of the potentiation (NL_P) and depression (NL_D), the conductance as a function of the normalized pulse number is modeled by:

$$\begin{cases} G_P = K(1 - e^{-NL_P \times P_n}) + G_{min} \\ G_D = G_{max} - K\left(1 - e^{-NL_D(p_{max} - P_n)}\right) \\ K = {G_{max} - G_{min}}/{1 - e^{-NL \times P_{max}}} \end{cases} \qquad (1)$$

, where the G_P and G_D are the conductance value for each potentiation and depression. G_{max} and G_{min} are the maximum and minimum conductance values, respectively. P_n and P_{max} are the normalized pulse number and maximum normalized pulse number (P_{max}=1), respectively. K is the function of NL to fit the G_P and G_D

functions within the range of G_{max}, G_{min}, and P_{max}. When the NL is zero, the conductance update is ideally linear.

Many resistive switching devices have been shown to possess superior potential in achieving synaptic functions for neuromorphic systems.[23-26, 39-41] Memristors based on CFs have received widespread attention due to their exceptional performance as memory devices, which includes low programming voltage, high on/off ratio, and good endurance and retention properties. As a result, filamentary-type RRAM has been extensively studied to simulate artificial synapses and successfully showed various basic features such as short-term and long-term synaptic plasticity, PPF, and STDP. However, the randomly formed and broken filaments result in relatively poor uniformity, and the current of the device cannot be uniformly scaled with device size, leading to high power consumption. Also, the conductance change of synapses based on the filamentary mechanism usually exhibits unsatisfactory non-linearity. In order to achieve near-linear modulation of conductance change to improve synaptic performance, the devices need to apply gradually varying electrical stimuli, such as gradually increasing or decreasing the amplitude or width of the pulse trains, which poses significant challenges in peripheral circuit design.[30, 42-45] Although some researchers have attempted to achieve linearly modulated

conductance by doping, this approach still cannot solve the high power consumption issue associated with such devices.[46] In contrast, RRAM based on a non-filamentary mechanism may represent a better choice for simulating synapses to achieve superior synaptic properties. This is because, unlike filaments that form and break at random, such non-filamentary type memristors participate in electrical conduction throughout the entire electrode area, generally displaying excellent uniformity and good scalability behavior, whereby the area of the device can be scaled to achieve very low power consumption.[7, 21, 47] This unique mechanism makes this device promising to obtain better nonlinearity. However, the synaptic devices based on non-filamentary memristors have been the subject of limited research, and the modulation mechanism of conductance to simulate synaptic behavior still requires further discussion and exploration.[48, 49]

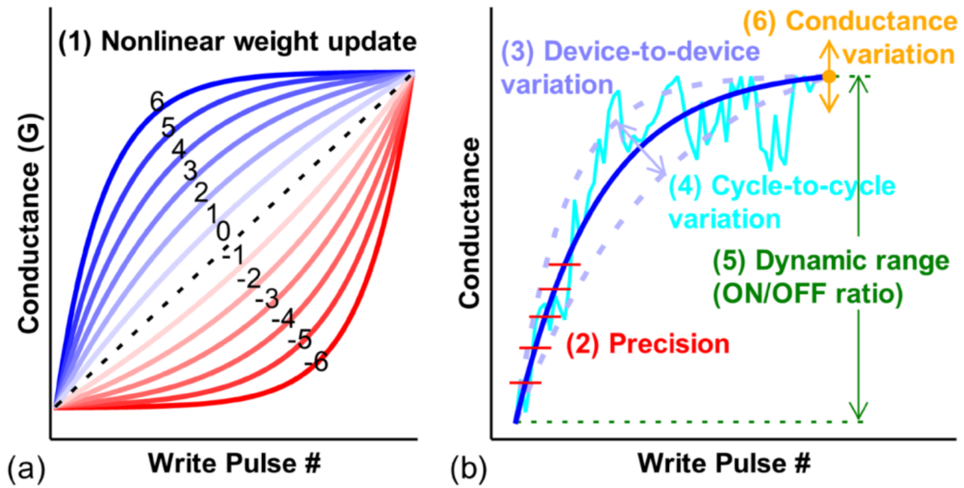

Figure. 1.5. Schematic illustration of non-ideal synaptic device properties modeled in the MLP simulator, including (1) nonlinear weight update (a), (2) weight precision, (3) device-to-device weight update variation, (4) cycle-to-cycle weight update variation, (5) dynamic range (conductance ON/OFF ratio) and (6) conductance variation (b).

1.5. Research scope and objective

The objective of this paper is to investigate the unique electronic bipolar resistive switching mechanism in non-filamentary-type TiO_2-based RRAM. Based on the analysis of its degradation mechanisms, a method is proposed to improve its resistance switching performance by inserting an ultra-thin ZrO_2 layer. Additionally, based on this optimized AZTA RRAM device, the various synaptic characteristics are simulated, exploring its application in neuromorphic computing.

The demand for memory devices is increasing with the development of information technology. Traditional storage devices have some limitations, such as high-power consumption and poor reliability. Therefore, the researchers began to focus on new types of memory devices, including electronic bipolar resistance switching (e-BRS) RRAM, which is controlled by the switching of resistance states through the capture and release of electrons. Compared with other types of memory devices, e-BRS RRAM has the characteristics of low failure risk and no current formation. The study aimed to improve the performance of e-BRS RRAM devices, in particular, to improve their durability and data retention capabilities. In Chapter 2, the method of inserting a protection layer in the resistance switching process is proposed, hoping to prevent the active aluminum electrode

from continuously absorbing oxygen ions, thereby increasing the trap density in the resistance switching layer, and thereby improving the stability and consistency of the device. The main objective of the study was to evaluate the performance improvement after the insertion of ZrO_2 layers at the top interface of the Al/TiO_2/AlO_x/Al RRAM structure. By comparing the Al/TiO_2/AlO_x (ATA) structure with no protective layer inserted, it is expected to observe improved durability, data retention, consistency, and reduced power consumption. At the same time, it is also hoped to verify that the selection of the ZrO_2 layer meets the requirements of the protective layer and does not have a negative impact on the e-BRS mechanism. The resistive conversion process based on the space charge limiting current mechanism will also be discussed in detail. The results of this study will help advance the development of e-BRS RRAM technology and provide a potential solution for the application of high-density memory devices.

With the rapid development of artificial intelligence systems, the third-generation artificial neural morphologic network has been widely studied. Artificial neural networks need to simulate the connections between biological neurons, so artificial synapses, as an important electronic component, have attracted much attention. In order to simulate the performance of brain synapses, artificial

synapses need to have key indicators such as plasticity, low power consumption, scalability, high signal-to-noise ratio, fast operation speed, and reliability. Among many new non-volatile memory devices, metal oxide resistance random access memory (RRAM) has been widely studied due to its excellent physical properties, electrical performance, and compatibility with traditional integrated processes. In Chapter 3, based on the previously developed non-filamentary Al/ZrO_2/TiO_2/Al RRAM device, which has excellent uniformity, no formation operation, and scalability, the ability of the device to simulate artificial synapses is systematically investigated. It also demonstrates excellent synaptic plasticity under more complex biological synaptic functions such as long-term enhancement, long-term inhibition, pulse-pair enhancement, and time-dependent plasticity. By optimizing the pulse stimulation conditions, near-linear long-term enhancement and inhibition changes are achieved. The conductive mechanism that governs the synaptic plasticity of the non-fiber RRAM device, namely the trap-assisted space charge-limiting current mechanism, is also revealed. In addition, due to its area-scalable behavior, non-fiber AZTA synaptic devices show potential for ultra-low power consumption and fast operating speeds. The purpose of this study is to explore and understand the synaptic performance and conduction mechanism of non-fiber Al/ZrO_2/TiO_2/Al

RRAM devices, so as to promote the development of artificial synapses and improve the performance of neural networks.

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Chapter 2. Performance improvement of $Al/TiO_2/Al$ electronic bipolar resistive switching memory via inserting an ultra-thin ZrO_2 layer at the top interface

2.1. Introduction

Over the past decades, the research of resistance switching random access memory (RRAM) with either one transistor-one resistor or crossbar array (CBA) has been very active.[1-13] In both configurations, the resistive switching (RS) is mainly controlled by the formation and rupture of conductive filaments (CFs), which are prone to hard breakdown during electroforming.[14-16] Also, the stochastic nature of the CF generally induced non-uniformity and low-reliability issues. Moreover, the operating current of this type of device is relatively high, which causes relatively high-power consumption. In contrast, the electronic bipolar resistance switching (e-BRS) device, induced by the trapping and de-trapping of the carriers (electrons), could be a better option. This assertion is based on the finding that the gradual current switching makes the catastrophic failure by the electrical breakdown much less probable. This improvement is also supported by the electroforming-free nature of the e-BRS

mechanism. Also, the area-scalable characteristic of the e-BRS device is especially conducive to improving integration for CBA RRAM, that the power consumption will decrease proportionally with the reduction of device size.[17-19] In addition, RRAM based on the e-BRS mechanism has also been found to have potential applications in highly flexible memory devices,[20-23] security applications,[24] and artificial synapse applications.[25-29]

Kim et al. initially suggested the working e-BRS mechanism in the Pt/TiO_2/Pt RRAM cells in 2011.[30] They asserted that the e-BRS performance of the Pt/TiO_2/Pt RRAM, which has to be electroformed first due to the high Schottky barrier between the Pt and TiO_2, was mediated by the electron trapping (low resistance state, LRS) and de-trapping (high resistance state, HRS) at the defect sites (oxygen vacancies, VO) in the TiO_{2-x} region between the Pt electrode and residual CF composed of magnéli phase Ti4O7. They performed a detailed analysis of defect density and the space-charge limited conduction (SCLC) mechanism. They indicated that the asymmetric potential barrier, i.e., high and low Schottky barrier at the Pt/TiO_x and TiO_x/magnéli CF, constituted the fundamental reason for the emergence of the BRS mechanism.

Also, Jeong et al. demonstrated stable e-BRS is closely related to the top and bottom interface domains in metal/amorphous-TiO_2/metal

RRAM devices.[4] They regarded that the top interface with mobile oxygen ions would induce the redox reaction during the set (switching from HRS to LRS) and reset (switching from LRS to HRS) processes. In contrast, the bottom interface played a role as the blocking layer, which prevented the electric breakdown. In 2011, Kim et al. proved the formation of the Al-Ti-O interface layer at the top electrode in the Al/amorphous-TiO_2/Al RRAM structure owing to the strong oxidation power of the Al.[31] They also suggested that the reversible formation and dissociation processes of the Al-Ti-O interface layer by the migration of oxygen ions under an applied bias constituted the RS mechanism.

Then, in 2015, Shao et al. reported Al/TiOx/Al structure e-BRS devices showed outstanding RS performance, such as electroforming-free and area-scalable behavior.[19] An ~5 nm insulating AlO_x layer was naturally formed at the bottom Al electrode interface, which was not the case at the top Al interface. Therefore, this different interface configuration provided the necessary asymmetric potential barrier, in which the electron injection and ejection at the top interface were fluent. In contrast, they were prohibited at the bottom interface. Unfortunately, the switching endurance of such devices was not satisfactory, and the operation current level was generally too high. Detailed electrical and chemical

analysis showed that the top Al/TiO_x interface gradually changed from the quasi-Ohmic contact property to the Schottky-type contact. This change means that the top electrode Al was slowly oxidized to AlO_x due to continuous electrostimulation. At the same time, the top part of the TiO_x RS layer became more oxygen-deficient, which no longer provided effective trap centers. This electrochemical reaction is unnecessary for the e-BRS mechanism to operate efficiently. Therefore, inserting a protective layer at the top electrode interface can be a feasible method to prevent the active Al electrode from continuously absorbing oxygen ions in the resistance layer TiO_2 as the cycle increases, which may improve RS endurance.

Nonetheless, the inserted protective layer must meet the following conditions: 1) The protective layer should not affect the e-BRS mechanism. That is, it should not form a too high potential barrier, thus not affecting the fluent injection and ejection of the electrons. 2) It should not absorb oxygen ions in the TiO_2 layer as efficiently as Al, meaning that the oxidation potential should be close to the TiO_2. 3) The thickness of the protective layer needs to be accurately adjusted, not causing the device operation condition to deviate too much.

To this end, several oxide barrier materials (ZrO_2, HfO_2, Al_2O_3) and different insertion layer thicknesses (1 – 5 nm) were studied, which are grown by thermal atomic layer deposition (ALD). Among them,

the HfO_2 and Al_2O_3 layers were too insulating even at a thickness of 1 nm, interfering adversely with the fluent Ohmic contact property. In contrast, the 1-2 nm thick ZrO_2 layer met the above requirements well.

Therefore, this work evaluated the performance improvement, especially the endurance, and retention, by inserting the ZrO_2 layer at the top interface of the Al/TiO_2/AlO_x (natively formed)/Al RRAM structure. The Al/TiO_2/AlO_x/Al and Al/ZrO_2/TiO_2/AlOx/Al structures are called the "ATA" and "AZTA" samples, respectively. In the AZTA sample, the ultra-thin ZrO_2 layer blocked the undesired reduction TiO_2 layer in contact with the Al top electrode. As a result, the trap density in the TiO_2 resistive layer was maintained robustly even with the increasing number of the switching cycle, demonstrating the electroforming-free behavior, improved endurance to 10^5 times, and optimized uniformity and retention. In addition, the inserted thin ZrO_2 layer also generally decreased the operation current, making the device suitable for high-density array applications.

2.2. Experimental

First, the 100 nm-thick Al bottom electrode film was deposited by the electron beam evaporator (Sorona, SRN-200i) on a 5nm-thick Ta_2O_5 adhesion layer/SiO_2/Si substrate. Next, the samples were transported to the TiO_2 RS layer sputtering chamber via the air atmosphere, so the bottom Al electrode was oxidized to form an ~5nm-thick AlO_x layer. Then, a 35nm-thick TiO_2 film was deposited on this AlO_x/Al/Ta_2O_5/SiO_2/Si substrate by a laboratory-made radio frequency sputter using a Ti_4O_7 target and O_2/Ar reactive gas at room temperature (RF power: 125 W, deposition pressure: 0.015 Torr, oxygen concentration: 20% O_2). For fabricating the AZTA samples, the different thick ZrO_2 layer was then deposited on the TiO_2 layer by the thermal ALD system (Quros, Plus 200) with the 5, 10, and 20 deposition cycles, respectively (precursor: $Zr[N(CH_3)(C_2H_5)]_4$, oxygen source: O_3, deposition temperature: 250 ℃). The growth per cycle for the ZrO_2 film was ~0.13 nm/cycle, so 10 ALD cycles deposited ~1.3nm-thick ZrO_2 layer on the TiO_2 film. Finally, the 100nm-thick Al top electrode was deposited by the electron beam evaporator. The bottom and top Al electrodes were patterned into line shapes with the width of 4, 6, 8, and 10 μm, respectively, via the lift-off process, so the fabricated RRAMs have 16, 36, 64, and 100 μm^2 areas. The fabricated samples were

annealed at 250 ℃ for 60 minutes to stabilize the contact property.

The composition and the film thickness of the TiO_2 and ZrO_2 films were examined by an X-Ray fluorescence analyzer (Thermo Scientific, ARL Quant'X EDXRF) and spectroscopic ellipsometry (Woollam, ESM-300, J. A.), respectively. In addition, the chemical structure of the TiO_2 and ZrO_2 film was examined by X-ray photoelectron spectroscopy (XPS, ThermoFisher Scientific, Sigma Probe).

The current-voltage (I–V) characteristics were measured using a semiconductor parameter analyzer (Hewlett Packard, 4145B) for the direct current (DC) sweep mode. The top electrode was biased, while the bottom electrode was grounded. The semiconductor parameter analyzer (Hewlett Packard, 4155B), a pulse generator (Tektronix, AFG3010C), and an oscilloscope (LeCroy, Wave Surfer 62MXs-B) were used for the pulse switching measurement. All data in this work were tested from the ATA and AZTA samples with an electrode area of $10\times10\ \mu m^2$.

2.3. Results and Discussions

2.3.1. Optimization of the ZrO_2 insertion layer thickness

First, the optimal thickness of the ZrO_2 layer was evaluated by estimating the RS performance of the ATA and ATZA samples with the ZrO_2 ALD cycles of 5, 10, and 20, respectively. Figure 2.1(a) shows the typical I-V characteristics of the samples, which exhibit gradual set and reset switching at the positive and negative biases, respectively, with no involvement of the electroforming step. For these tests, an appropriate compliance current (I_{cc}) of 1 μA was settled to ensure that all traps in the TiO_2 layer could be sufficiently filled with electrons while preventing permanent device degradation. These properties coincide with the previous reports on a similar structure, suggesting that they follow the e-BRS mechanism.[19, 32] Specifically, the fluent electron injection from the top electrode and their trapping within the TiO_2 layer under the negative bias set the device. The de-trapping and trapping of the electrons under the positive bias reset the device.

The initial resistance values of all samples showed no significant difference. Still, the set voltage (V_{set}) and LRS resistance (R_{LRS}) increased with the increasing thickness of the ZrO_2 layer. The V_{set}

and the R_{LRS} are tested at an I_{cc} of 1 μA from 20 cells for statistical accuracy, as shown in Figure 2.1(b), with the different thickness ZrO_2 insertion layer. The ATA sample in Figure 2.1(b) underwent the same annealing process as the AZTA samples (250 ℃, for 1 hour). This step was necessary to make all the samples' initial HRS resistance (R_{HRS}) similar. The long ALD time (40 to 80 min for 5 to 20 cycles) for the AZTA samples rendered the initial R_{HRS} smaller as the ZrO_2 film thickness increased, as shown in Figure 2.2. This abnormal behavior must be due to the structural relaxation of the TiO_2 layer caused by the annealing effect during ALD, which decreased the trap density. Figure 2.1(b) shows that the total R_{LRS}, measured at 0.1 V, increases almost linearly with the ZrO_2 layer thickness, which indicates that the ZrO_2 layer act as a series resistance in the LRS in such a thin thickness range. Therefore, the $|V_{set}|$ also increased almost linearly with the ZrO_2 layer thickness. The slope of the best-linear-fitted graphs indicated the increase rates in the R_{LRS} and $|V_{set}|$ was 3.37×10^8 Ω/nm and 0.66 V/nm, respectively. Figure 2.1(c) shows the cumulative distribution of the R_{HRS} and the R_{LRS} for each sample from the 20 cycles in one cell. The uniformity of the samples was improved as the ZrO_2 layer thickness increased, but the resistance ratio tended to decrease mainly due to the rapid increase of the R_{LRS}. The high non-uniformity of the ATA sample could be

ascribed to the irregular chemical interaction between the top Al electrode and TiO_2 layer, which the adopted ZrO_2 protection layer could suppress. The 5 ALD cycles of ZrO_2 correspond to a physical thickness of 0.65nm, slightly thicker than the one unit-cell thickness of the ZrO_2 (~0.5nm). Therefore, suppressing such side effects by the 0.65nm-thick ZrO_2 layer could be insufficient. Therefore, the data in Figures 2.1 (b) and (c) indicate that the 1.3nm-thick (10 cycles) ZrO_2 layer is the optimum protection layer at the top interface. In the following sections, therefore, the data for the ATA and AZTA samples with the 1.3nm-thick ZrO_2 layer are compared to evaluate the ZrO_2 layer effects.

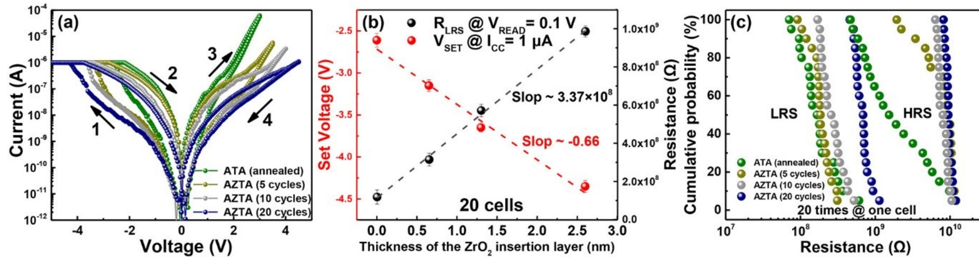

Figure 2.1. The resistance switching characteristics of ATA (annealed) sample and AZTA samples with 5, 10, and 20 deposition cycles of the ZrO_2 film. (a) Typical e-BRS I-V curves with an I_{cc} of 1 μA. (b) RLRS at the read voltage of 0.1 V and VSET at the I_{cc} of 1 μA from 20 memory cells. (c) The cumulative probability graphs of LRS and HRS from the 20 I–V sweeps in a single memory cell.

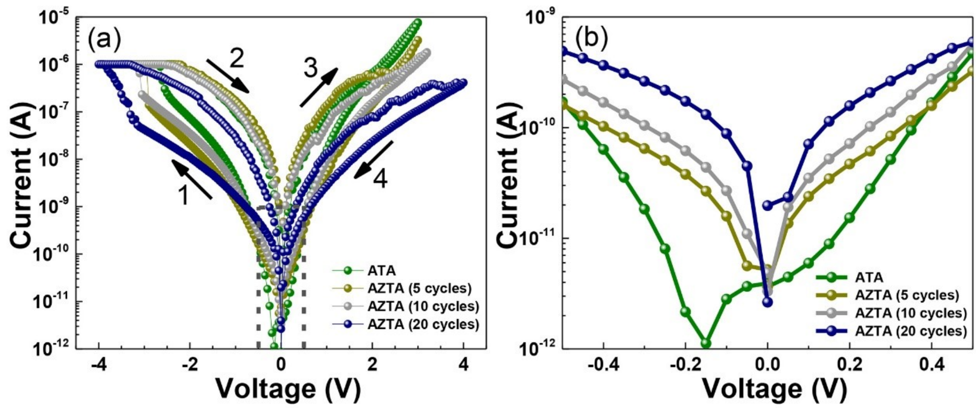

Figure 2.2. (a) Typical e-BRS I-V curves of ATA sample (without annealing), AZTA sample (5 cycles, 40 minutes), AZTA sample (10 cycles, 60 minutes), and AZTA sample (20 cycles, 80 minutes) fabricated by the thermal ALD with the different deposition time. (b) The I-V curves with a smaller range clearly show the degradation of HRS.

2.3.2. The resistance switching performance comparison

Figures 2.3 (a) and (b) showed the typical I-V curves of the ATA and AZTA samples, respectively, measured at room temperature with an I_{cc} of 0.5 μA during the set. Both samples exhibited a gradual set/reset process without the abrupt current jump, which is consistent with the typical electronic type RS characteristics.[19, 30, 33] However, the two samples showed distinctive I-V curves with the increasing number of switching cycles. For the case of the ATA sample, the HRS current (I_{HRS}, read at -0.5V) increases rapidly from 2.1×10^{-2} nA at the first cycle to 1.4×10^{-1} nA at the 10th cycle and then slowly to 4.7×10^{-1} nA at the 100th cycle. The possible reason for such I_{HRS} variation was discussed in the later section, which examined the detailed conduction mechanisms. In contrast, the I_{HRS} of the AZTA sample remained almost unvaried with a value of 3.3 - 7.1 $\times10^{-2}$ nA at the same read voltage during the 100 switching cycles. This improvement could be ascribed to the suppression of the unwanted side effect of the top Al electrode by adopting the reaction barrier ZrO_2 layer. Besides, the $|V_{set}|$ of the AZTA sample increased from ~2.5V for the ATA sample to ~3.2V by the voltage partake effect of the ZrO_2 layer. The electrode area (S)-dependent behavior

of the AZTA sample is shown in Figure 2.4. The R_{HRS} and R_{LRS} showed a slope of ~1 in the log R vs. log S graph, indicating a uniform current flow across the entire electrode area.

Figures 2.5 (a) and (b) showed the endurance performance of two samples from I-V sweeps up to 200 cycles. I_{cc} was set to 0.5 μA, and the resistance value was read at 0.5V for both samples. For the ATA sample, the R_{HRS} rapidly decreased from ~ 1×10^{10} Ω in the first cycle to ~ 1×10^{9} Ω in the 20th cycle, then slowly down to ~ 8×10^{8} Ω in the 100th cycle. The R_{LRS} did not show a notable variation and remained at ~ 8×10^{7} ohms. The resistance ratio decreased from ~ 200 to ~ 10. While the resistance ratio of 10 is not insufficient for a feasible RRAM operation, such a substantial variation adds a burden to the drive circuit.

However, this was not the case in the AZTA sample, as shown in Figure 2.5 (b). The R_{HRS} and R_{LRS} values and their ratio (~ 65) did not show notable variations up to 100 I-V cycles. A similar contrasting trend could be found for the pulse-type switching, which is more relevant to the actual RRAM operation, as shown in Figures 2.5 (c) and (d). The resistance switching characteristics of the AZTA sample in the pulse test mode as shown in Figure 2.6. The resistance changes gradually with the pulse amplitude and length. A similar resistance ratio can be achieved at the pulse conditions with the

increasing pulse amplitude and decreasing pulse length. However, to achieve the best endurance performance in the pulse test, a set pulse with a relatively small pulse amplitude and a long pulse length was chosen to avoid a hard breakdown of the devices. At the same time, a reset pulse with a relatively large pulse amplitude and a long pulse length is chosen to confirm that the trapped electrons are fully detrapped. Finally, the set and reset pulses of -2.5 V/20 ms and 2.7 V/20 ms were selected for the ATA, and -4.0 V/20 ms and 5.0 V/20 ms were for the AZTA sample. For statistical accuracy, three cells per sample were tested. The unusually long pulse (normal RRAM requires < 1 μs) must also be ascribed to the relatively large area of the test cells (100 μm^2). Because the whole electrode region of the device participates in the electrical transportation for e-BRS devices. However, the size of the randomly formed conduct filaments for the filamentary-controlled devices is usually only a few tens of nanometers or even smaller.[14, 34, 35] Therefore, the area-type switching requires sufficient time to supply the required charges, but it also implies that the much smaller area device (ca. 4×10^{-4} μm^2) might require a much shorter switching time (~ 0.1 μs), which can be estimated by the resistance switching characteristics of the AZTA sample with different electrode areas in the pulse test mode, as shown in Figure 2.7. While the ATA sample showed significant decay

of the R_{HRS} and R_{LRS}, even after 1000 cycles, at which the R_{HRS} became even smaller than R_{LRS} of the initial state, AZTA samples showed stable R_{HRS} and R_{LRS} values up to 10^5 switching cycles. This level of stability has not been reported for the TiO_2-based e-BRS RRAMs, demonstrating the superiority of the AZTA sample to the previous works.[19, 22, 36, 37]

The cell-to-cell and cycle-to-cycle uniformity performance of the ATA and AZTA samples are shown in Figures 2.8 (a) and (b), respectively. Both samples showed high device-to-device uniformity, which corroborates the general expectation that the e-BRS type device would have better uniformity than the CF-based ionic RS mechanism device. In contrast, only the AZTA sample exhibited high cycle-to-cycle uniformity in both the R_{HRS} and R_{LRS}.

The retention of the ATA and AZTA samples was measured at room temperature and 85℃ for up to 10^5 s, and the results are shown in Figures 2.9 (a) and (b), respectively. The retention characteristic of the RRAM based on the SCLC mechanism is closely related to the electrons de-trapping from the traps by the influence of thermal noise. Because of the electron trapped configuration in LRS, the R_{LRS} was generally more prone to increase in its value than the R_{HRS}.[19, 22, 25] This was also the case in this work, especially at 85℃, and the tendency was more evident for the ATA sample. The retention

behavior of the HRS for ATA and AZTA sample after different cycling numbers at the temperature of 85℃, as shown in Figure 2.10, further confirm the failure of the device is closely related to the trap depth (E_a). That is, electrons in the trap level closer to the conduction band are more easily to be excited. In addition, the relative resistance ratio in Figure 2.10, normalized to the data at 1 s, decreased by ~ 69 % and ~ 54% for the ATA and AZTA samples, respectively. The improvement could be ascribed to the electron barrier effect of the thin ZrO_2 layer against the carrier detrapping under no bias conditions.

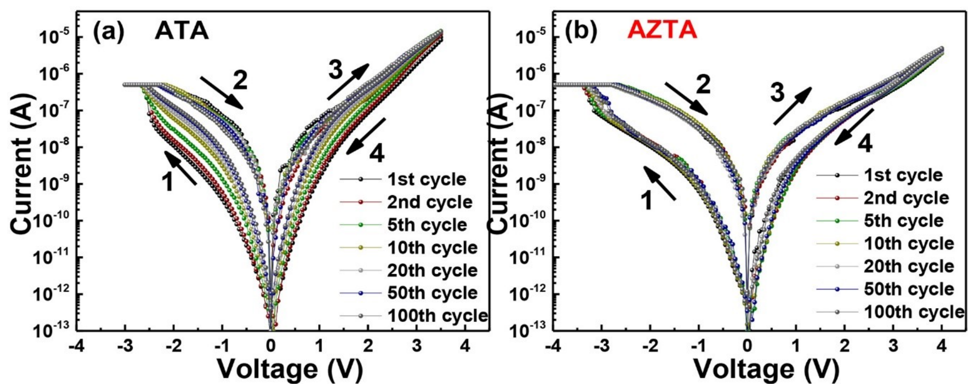

Figure 2.3. Typical e-BRS I-V curves of (a) ATA and (b) AZTA samples at the 1st, 2nd, 5th, 10th, 20th, 50th, and 100th cycles with an Icc of 0.5 μA. The arrows and numbers indicate the switching sequences.

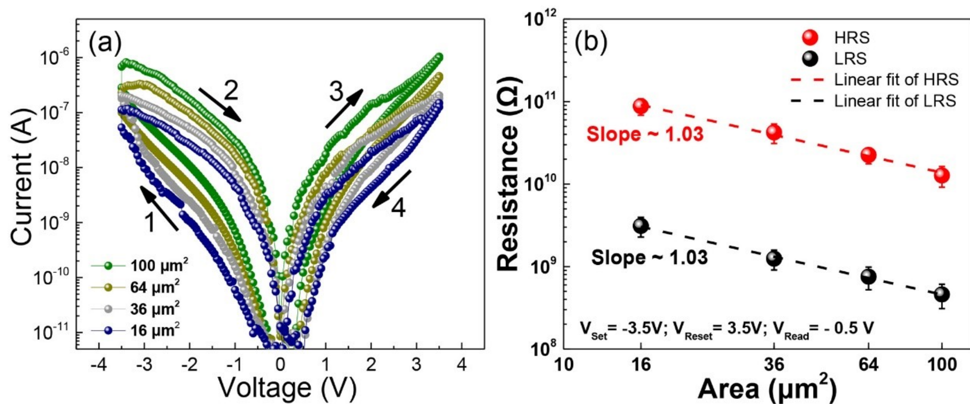

Figure 2.4. The I-V curves of the AZTA sample with the different electrode sizes without the I_{cc}. (b) The electrode area-dependence of LRS and HRS for AZTA sample. Each data point was achieved from 20 cells.

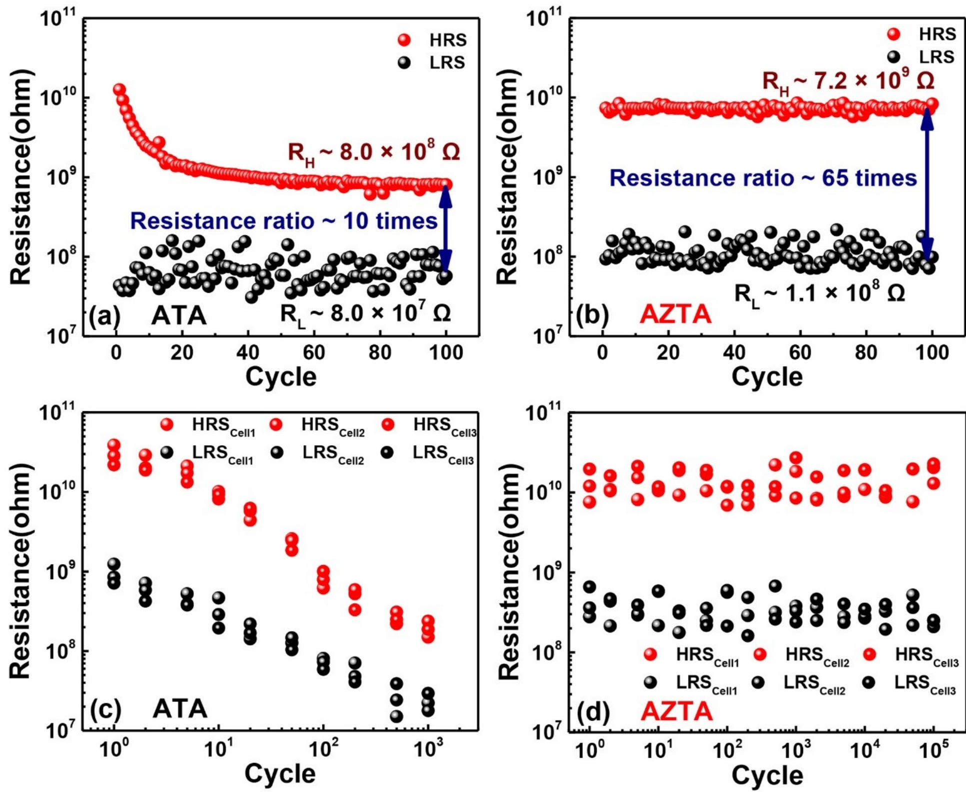

Figure 2.5. The endurance test results from the DC I-V sweeps of (a) ATA and (b) AZTA samples, with an Icc of 0.5 μA. The AC endurance test results of (c) ATA and (d) AZTA samples from the pulse operation mode. The set and reset pulse conditions of the ATA sample (−2.5 V/20 ms and 2.7 V/20 ms), and AZTA sample (−4 V/20 ms and 5 V/20 ms) were tuned to achieve the best test results. The read voltage was 0.5 V.

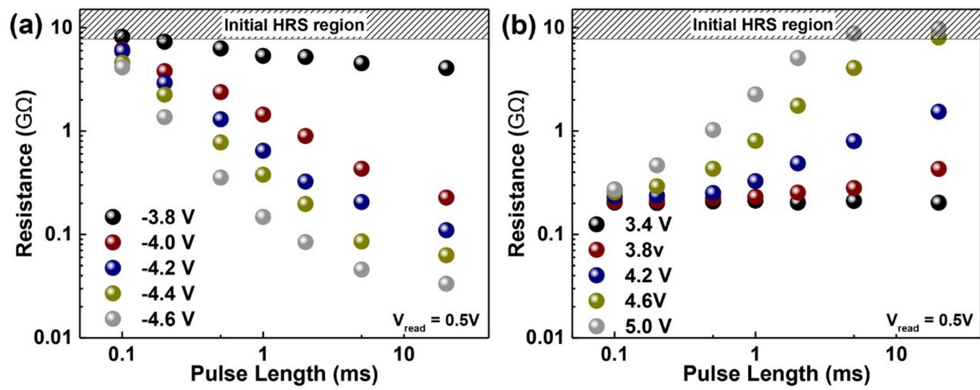

Figure 2.6. The resistance state of the AZTA sample with 100 μm^2 area after applying different (a) set and (b) reset pulse excitations. The initial HRS is ~ 8 GΩ for the set process, and the initial LRS is ~ 0.2 GΩ for the reset process, obtained after applying a −4V/20ms set pulse. The read voltage is 0.5V.

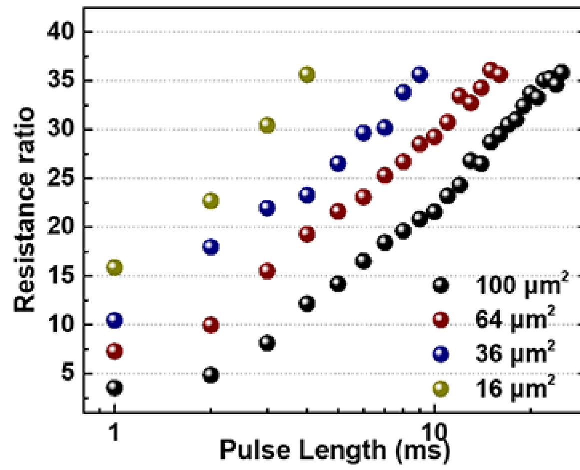

Figure 2.7. The resistance ratio variation of the AZTA samples with different electrode areas after applying set pulses with different pulse lengths when the set pulse amplitude is fixed to -4V.

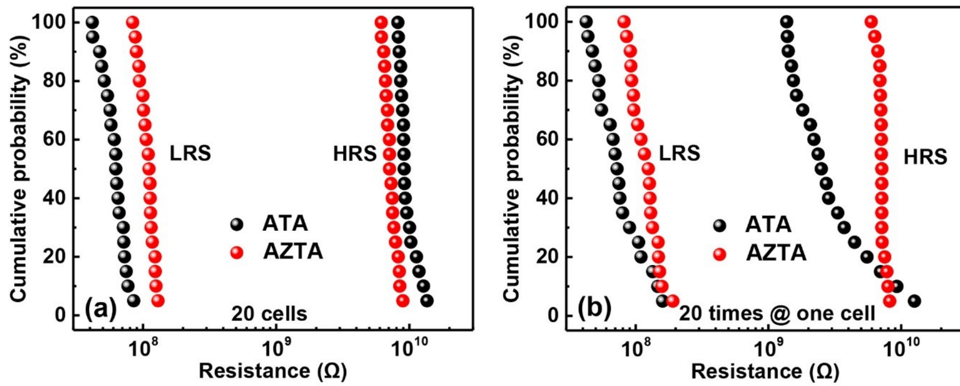

Figure 2.8. The cumulative probability graphs of LRS and HRS for ATA and AZTA samples, respectively. (a) The 20 I-V sweeps from 20 memory cells, and (b) the 20 I-V sweeps from a single memory cell. The Icc is 500nA, and the read voltage is 0.5 V.

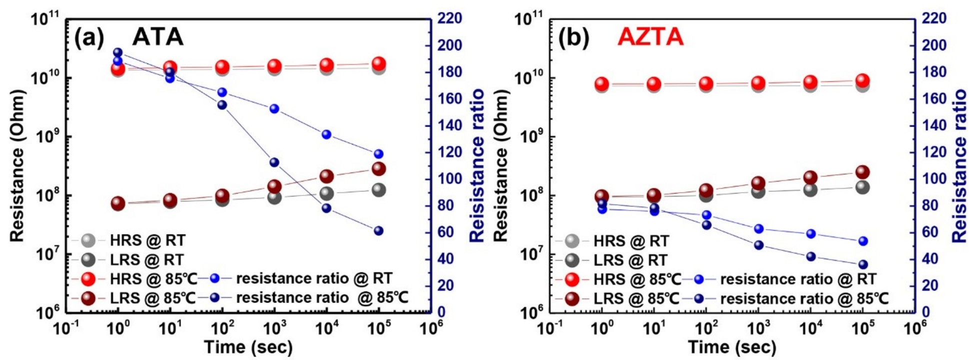

Figure 2.9. The retention characteristics of HRS, LRS, and resistance ratio were measured at room temperature (grey symbols) and 85℃ (color symbols) of (a) ATA and (b) AZTA samples, respectively. The read voltage is 0.5 V.

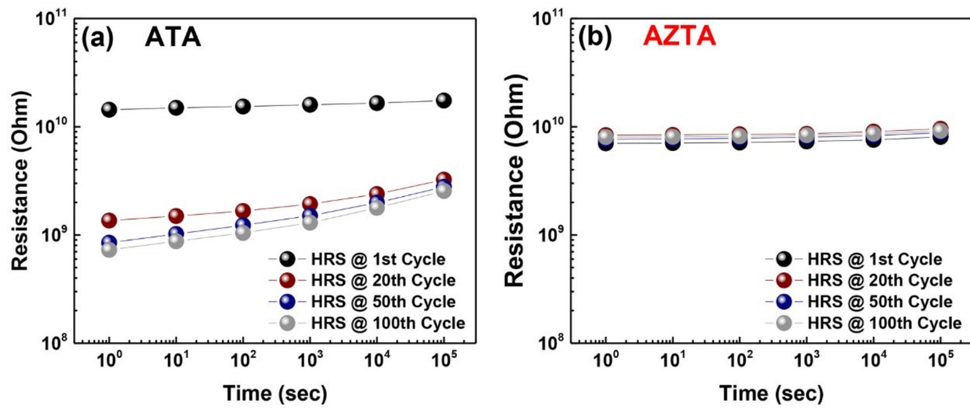

Figure 2.10. The retention behavior of the HRS for (a) ATA and (b) AZTA samples after different cycling numbers at the temperature of 85℃.

2.3.3. The characteristics test and analysis

In this section, the scrutinized chemical properties of the ATA and AZTA by XPS are discussed. The Al top electrode was not deposited for this analysis. The XPS binding energy was calibrated with the C-C binding energy of the adventitious C signal (284.6 eV). Figures 2.11 (a) and (b) showed the XPS Ti 2p and O 1s spectra of the TiO_2 film in the ATA and AZTA samples, respectively. There is no significant shift of the Ti 2p peak position between the two samples, meaning that no significant loss of oxygen has occurred in the TiO_2 film after the deposition of the ZrO_2 film. The weaker peak intensity of the AZTA sample was ascribed to the presence of the 1.3nm-thick ZrO_2 layer on top of the TiO_2 layer. The binding energy difference between the Ti 2p 1/2 (463.7 eV) and Ti 2p 3/2 (457.9 eV) peaks was ~ 5.8eV, indicating that the TiO_2 films are fully oxidized for both samples.[38] The O 1s peak corroborates the Ti 2p spectrum. The 529.4 eV binding energy of the O 1s peak from the ATA and AZTA samples showed no shift and is consistent with the reported value for the Ti–O bonding in TiO_2 (529.7 eV). Also, the 531.3 eV binding energy of another O 1s peak from the AZTA sample is consistent with the Zr–O bonding in ZrO_2 (531.2 eV).[39] These results confirm that the TiO_2 layer of the AZTA sample was almost unaffected by the

deposited ZrO_2 layer and maintained its initial oxidized chemical state. Nonetheless, these XPS data do not necessarily imply that the TiO_2 layer had a defect- (or trap-) free property. Sputtered TiO_2 films usually have a V_O density of 1% or less, which is sufficiently high to induce the e-BRS mechanism but still too low to be detected by XPS. Furthermore, the two peaks of the Zr 3d spectrum of the AZTA sample showed a binding energy difference of 2.4 eV, as shown in Figure 2(c), which corresponds to the Zr^{4+} in ZrO_2, suggesting that the ZrO_2 layer was fully oxidized.[40] Therefore, such a thin, fully oxidized ZrO_2 may play a tunneling barrier role, not the RS layer.

In addition, the cross-section TEM images of the ATA and AZTA sample (10 cycles) were included in Figure 2.12. Both samples show the presence of a ~5nm-thick AlO_x layer at the bottom interface, which provided the necessary asymmetric barrier for the e-BRS mechanism. Also, the high-resolution TEM image shown in Figure 2.12 (f) revealed the presence of an ~2nm-thick ZrO_2 layer at the top interface of the AZTA sample. At the same time, the STEM-EDS mapping confirmed the presence of the different layers according to the suggested device structures, as shown in Figures 2.13 and 2.14, respectively.

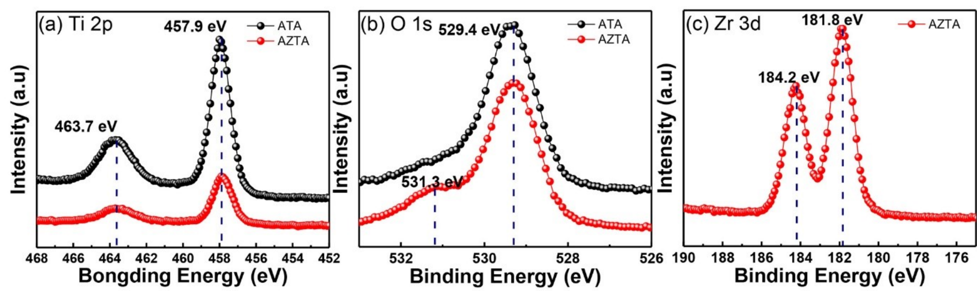

Figure 2.11. The XPS spectra of (a) Ti 2p and (b) O 1s of ATA and AZTA samples, respectively. (c) Zr 3d core level XPS spectrum of AZTA sample.

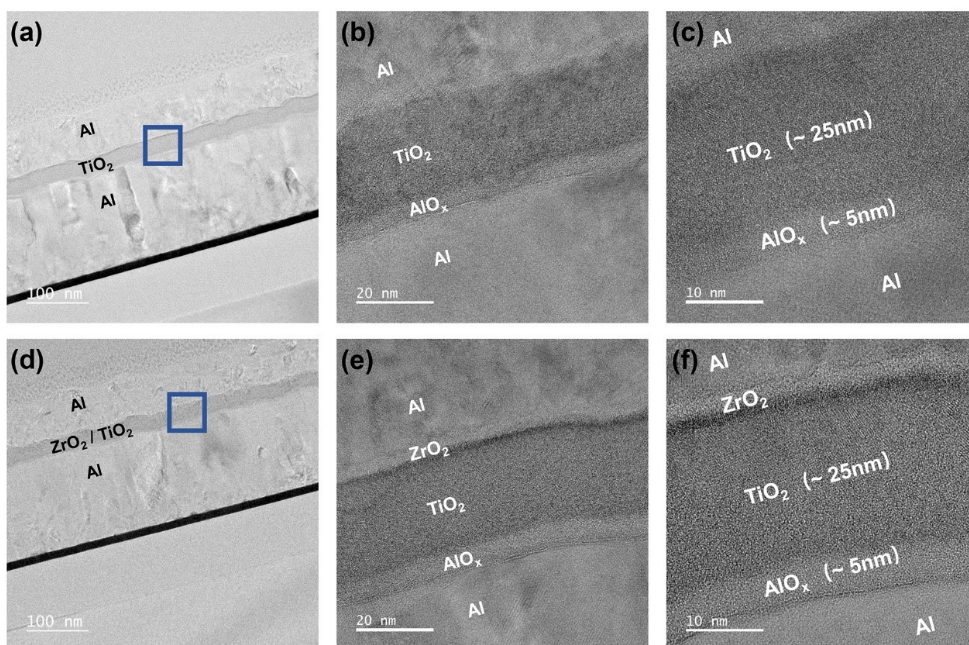

Figure 2.12. (a) – (c) The TEM images with the different magnifications of the ATA sample. (d) – (f) The TEM with the different magnifications of the AZTA sample. HRTEM images correspond to the blue square region in low magnification images.

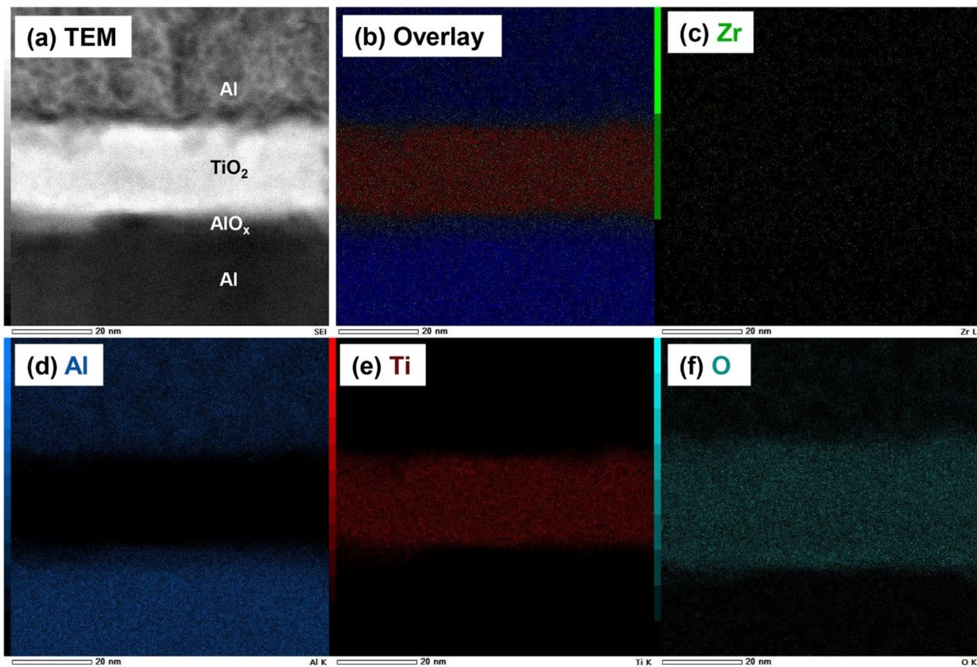

Figure 2.13. STEM-EDS mapping analysis of ATA sample: (a) TEM image of the corresponding area; (b) Overlay of Zr-Al-Ti-O; (c) Zr-L; (d) Al-K; (e) Ti-K; (f) O-K.

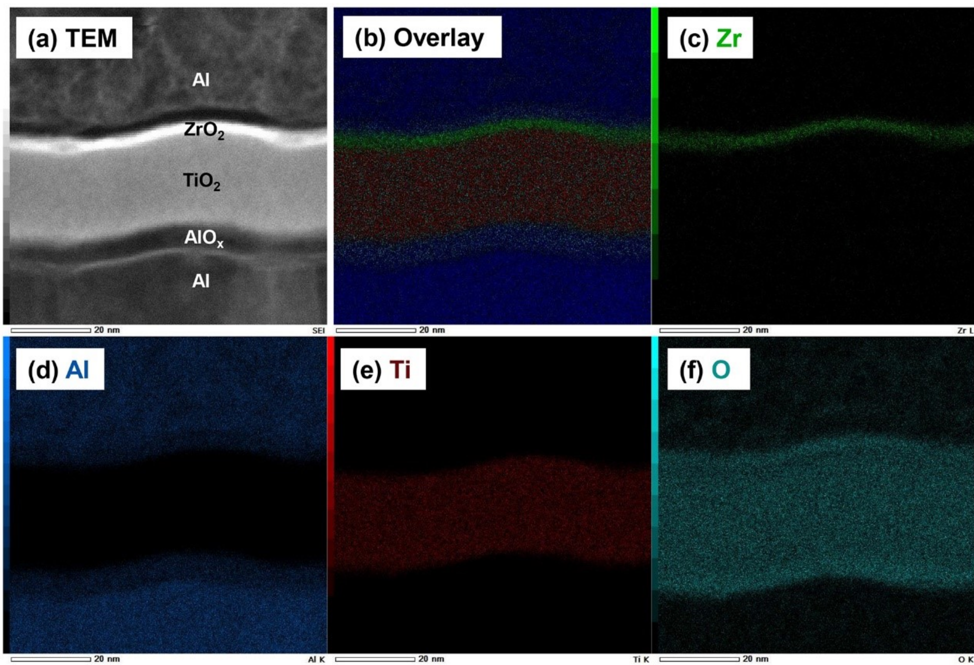

Figure 2.14. STEM-EDS mapping analysis of AZTA sample: (a) TEM image of the corresponding area; (b) Overlay of Zr-Al-Ti-O; (c) Zr-L; (d) Al-K; (e) Ti-K; (f) O-K.

2.3.4. Fitting and analysis of degradation mechanism

Figure 2.15 shows the double-log fitting data of set and reset I-V curves of the ATA and AZTA samples, shown in Figure 2.3, according to the analysis method suggested by Shao et al..[19] Both samples exhibited a reasonable fit to the SCLC mechanism, which is also consistent with previously reported devices with similar structures.[31, 32, 37] For the negative voltage sweep (set process, Figures 2.15 (a) and (b) for the ATA and AZTA samples, respectively), the slope of the absolute-low-voltage region is ~1.1, which can be understood as the Ohmic conduction region of the SCLC mechanism. In this region, thermally generated carriers dominate, and the transport of carriers (electrons) conforms to the hopping mechanism. With the increasing (absolute) voltage, the density of carriers (electrons) injected from the top interface gradually increases, and the SCLC gradually dominates, which is accompanied by the increase in the slope of the fitted graph. Finally, electrons fill all the traps, reaching the trap-filling region, and an abrupt current jump occurs at the trap-filling-limit voltage (V_{TFL}), which corresponds to the set (V_{TFL} ~ V_{set}). It is noted that the transition between these two mechanisms was gradual.

Interestingly, with the increasing number of cycles, the slope of the

ATA sample in the SCLC gradually decreased from 4.6 to 4.0. According to Child's theory of SCLC, the slope of the SCLC region must be 2 when a single trap level exists, but it could be higher when there are exponential distributions of the trap levels for the trap-assisted SCLC model.[30, 37] Therefore, these observed slopes decrease in the indicated region suggested deep traps in the band gap became inactive. Such a variation could be identified as the deep traps being permanently filled with the injected electrons, or the deeper trap centers were annihilated during the electrical cycling. At the same time, the absolute $|V_{TFL}|$ of the ATA sample decreased with the increasing number of cycles, which was also ascribed to the decrease in the effective trap density. As the bottom Al electrode interface involved a naturally formed robust AlO_x film, such an adverse effect should probably occur at the top Al/TiO_2 interface.

In contrast, the slope in the SCLC region and $|V_{TFL}|$ of AZTA samples remain unvaried as the number of cycles increases, which also supports the hypothesis that the inserted ZrO_2 layer effectively prevents the undesired chemical interaction (oxygen migration) at the top interface. As the applied voltage swept back to 0 V, the I-V curves showed a high current flow (set current, I_{set}), indicating that the nonvolatile set switching had occurred. The slope of the two samples in the absolute-high-voltage reign is ~ 2.4, which is a

typical SCLC mechanism. In contrast to the set switching, where the slope was ~ 4.0 – 4.6, all the traps were filled with the electrons in the LRS, so a slope near 2 was obtained. When the applied absolute voltage is reduced, the injected carrier density is lower than the thermally generated carrier density. Then, the Ohmic conduction mechanism dominates again, and the slope drops to ~1.1. The same slope value in the LRS of the two samples indicates that the inserted ZrO_2 film at the top interface did not form a significant Schottky barrier and unaffected the asymmetric barrier structure. This ultra-thin ZrO_2 layer only acts as a series resistance, where electrons are injected into the TiO_2 layer via a tunneling mechanism. Subsequently, for the positive voltage sweep process (reset process, Figures 2.15 (c) and (d) for the ATA and AZTA samples, respectively), a high enough positive bias voltage was applied to release the trapped electrons from the trap centers, recovering the HRS. As for the set process, when decreasing the voltage, the slope in the SCLC region of the ATA decreased from ~ 5.4 to ~ 4.6 with the increasing cycle number, but that of the AZTA sample remained unvaried at ~ 4.7 during the 100 switching cycles. These behaviors in the reset process corroborated the conclusion of the set process of the two types of samples.

The temperature-dependent I-V curves were acquired to clarify the

ATA sample's degradation mechanism further and delineate the positive effects of inserted ZrO_2 film. The I-V curves at the HRS after the first and 100th cycles of the two samples were measured in the temperature range of 303 - 343 K, as shown in Figures 2.16 (a) - (d), which were converted to the Arrhenius-type plots, as shown in Figures 2.16 (e) - (h), respectively. The I-V curves of the two samples showed evident temperature dependency in the absolute-low-voltage region both before and after the cycles. In contrast, the temperature dependency gradually weakened with the increase of the absolute voltage, which was consistent with typical characteristics of the SCLC mechanism. Because the absolute-low-voltage region of the SCLC mechanism conforms to the hopping conduction, the transport of carriers is determined by thermally generated carriers. Therefore, the tunneling rate of electrons between adjacent trap sites can be expressed by the effective diffusion process between them, which can be represented by the Arrhenius-type plots involving the apparent activation energy (E_a).[19, 30] With the increase of the absolute voltage, the injected carriers gradually dominate, which gradually fill the trap from the deep to the shallow level. Therefore, a decreasing E_a should be acquired with the increasing voltage when viewing this effect from the electrons' diffusion, which was indeed the case for both samples. E_a at each

voltage was calculated from the slopes of the best-linear-fit Arrhenius-type plot in Figure 2.16 (e) - (h), and the results are summarized in Figure 2.17.

For both samples at the 1st and 100th cycles, the E_a generally decreases with the increasing absolute voltage, confirming the previous e-BRS behavior.[19, 25, 30] However, the ATA sample showed a significant decrease in the E_a values all over the voltage region, suggesting the gradual annihilation or permanent filling of the deep traps with the increasing cycle number. In contrast, the AZTA sample showed minimal variation in the E_a across the entire test voltage region even after the 100 cycles of switching, again demonstrating stability. It was noted that its initial E_a values were generally lower than those of the ATA sample, but after the 100 cycles, they were even higher due to its invariability. The ZrO_2 ALD process, involving the highly reactive O_3 injection step, might cure the deeper traps in the sputtered TiO_2 layer, rendering the initial E_a relatively smaller.

The initial E_a values of the ATA sample and the AZTA sample, 0.31 eV and 0.27 eV, in this work, are larger than the previously reported E_a values, such as 0.25 eV from Kim et al.,[30] 0.15 eV from Shao et al.,[19] and 0.23 eV from Yan et al.[25] Because these values are intimately related to the distance between the nearby trap sites, the higher value of this work implied lower trap density than in the

previous cases. The most probable origin of these trap sites is V_O. The sputtering process using the Ti_4O_7 target in this work may result in a more stoichiometric composition of the TiO_2 film than in other works, where the metal Ti target was adopted.[19, 25] The higher E_a values resulted in a higher R_{HRS}/R_{LRS}.

Based on the above analysis, the improvement in the electrical performance of the AZTA sample over the ATA sample could be explained using the schematic band diagrams shown in Figure 2.18. The upper panels of Figure 2.18 show the schematic band diagram of the ATA and AZTA samples at the initial (or pristine) state. The middle and lower panels of the same figure show the set and reset processes, respectively, after ca. 100 cycles. At the initial state, the Al top electrode and the TiO_2 constitute a quasi-Ohmic contact, whereas the intervened AlO_x layer at the bottom interface renders the contact Schottky-like. Due to the presence of the traps, the conduction band profile varies as depicted. For the active trap density of 10^{19} cm^{-3} (~ 1% of lattice), the average distance between them is ~ 4.6nm. Therefore, the figure must be taken only qualitatively, not quantitatively precise. The deeper average trap depth (0.31 eV) of the ATA than that of AZTA (0.27 eV) is also displayed.

As shown in the middle panels, the set process coincides with the

trapping of injected electrons from the top Al electrode at the trap sites, while the electron travel to the bottom Al electrode was less efficient due to the presence of the AlO_x barrier layer. The extremely thin ZrO_2 layer in the AZTA sample minimally affects this set operation, given that the applied negative bias voltage was appropriately increased. The reset process moves back the trapped electrons to the top Al electrode. At the same time, the electron injection from the bottom electrode is also minimized by the presence of the AlO_x barrier layer. Also, the thin ZrO_2 layer in the AZTA does not interfere with this operation.

For the case of the ATA sample, the top interface portion of the TiO_2 layer could be reduced by the oxygen loss to the Al top electrode, especially during the reset step. Then, the trap density increases and the potential well depth in that region decreases by more severe overlapping of the potential profiles near the trap centers. Therefore, this region becomes filled with almost free electrons, making it electrically conductive. At the same time, the remaining part of the TiO_2 film closer to the bottom Al electrode also gradually loses oxygen atoms, lowering the trap depth. As a result, the E_a value of the ATA sample decreases from 0.31 eV to 0.15 eV, which accompanies the R_{HRS} and R_{HRS}/R_{LRS} ratio decreases. In contrast, the ZrO_2 layer in the AZTA sample prohibited such an adverse reduction

near the top Al electrode, which could be ascribed to the oxidation potential of ZrO_2. The standard Gibbs free energy of formation at 298K of Al_2O_3, ZrO_2, and TiO_2 is -1582.3, -1042.8, and -888.8 kJ per mole, respectively.[41] The intermediate oxidation potential of ZrO_2 prohibits not only the migration of oxygen from TiO_2 into Al but also retains the oxygen ions of ZrO_2 itself from their reaction toward the AlO_x formation. Therefore, the initial E_a value could be stable during the repeated switching operation, and the endurance could be secured even up to 10^5 cycles.

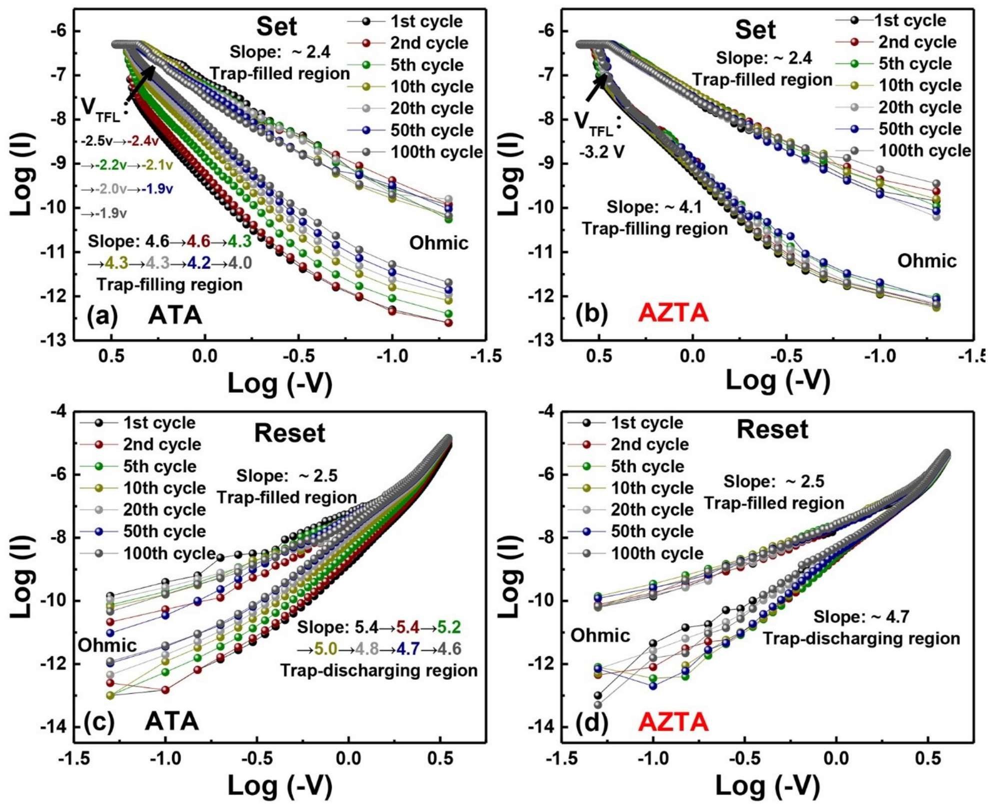

Figure 2.15. Double-log scales and linear fitting of SCLC mechanism for different repetition cycles of (a) set process and (b) reset process for the ATA sample and of (c) set process and reset process for the AZTA samples, respectively.

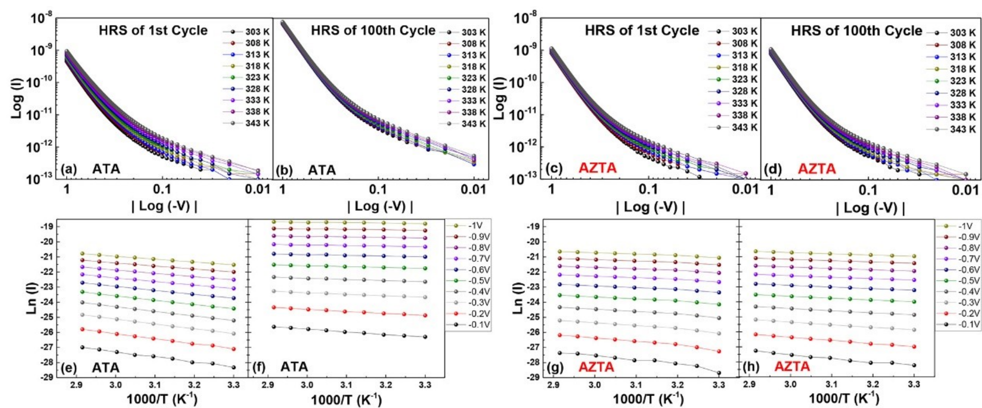

Figure 2.16. (a) - (d) show the temperature dependence characteristics of HRS after the 1st and 100th cycles were measured at the temperature range of 303 K to 343 K of the ATA and AZTA samples, respectively. The Arrhenius-type plots of the (a) - (d) data are shown in (e) - (h) for calculating the activation energy (Ea).

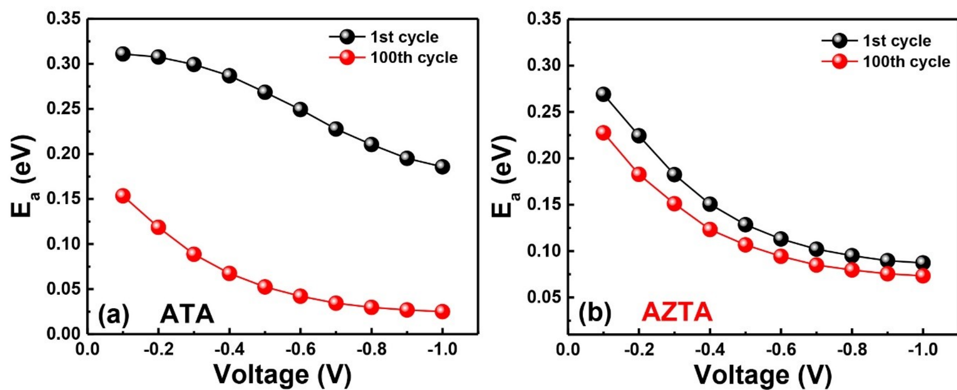

Figure 2.17. The E_a at each voltage for HRS of (a) ATA and (b) AZTA samples, respectively, were calculated from the slopes of the best-linear fitting of figure 2.16 (e) - (h).

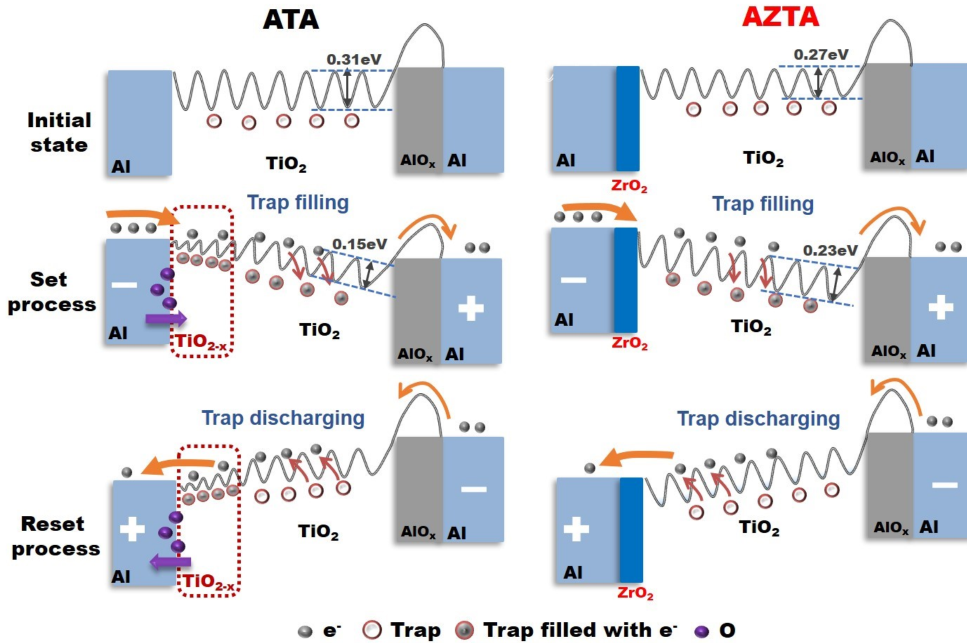

Figure 2.18. The schematic band diagram of ATA and AZTA samples at the initial state (upper panels), set process (middle panels), and reset process (middle panels) after 100 switching cycles. The color code of the subfigures is Al electrode, blue square; AlO_x layer, gray square; ZrO_2 layer, dark blue square; electrons, gray spheres; traps (oxygen vacancies), hollow red spheres; traps filled with electrons (charged oxygen vacancies), hollow red spheres filled with gray; oxygen atoms, violet spheres; direction of current flow, orange arrow; trapping and detrapping of the electrons, red arrow; and direction of oxygen diffusion, violet arrow.

2.4. Summary

In summary, the 1.3nm-thick ZrO_2 insertion layer at the top interface of the Al/TiO_2/Al memristor cell significantly improves its resistive switching (RS) performance. It is worth noting that, in pulse switching tests, the inserted ZrO_2 layer increases the endurance from ~103 cycles to ~105 cycles. This is attributed to the migration of oxygen atoms from the TiO_2 layer to the top Al electrode, which is suppressed by the presence of ZrO_2. The ZrO_2 layer acts as a suitable reaction barrier between TiO_2 and Al due to its intermediate oxygen affinity between Ti and Al. Moreover, in extended switching cycles, the loss of oxygen is minimized. The ultra-thin structure of the ZrO_2 used does not significantly alter the asymmetric barrier distribution in the Al/TiO_2/Al sample, which is essential for the electron-bulk resistive switching mechanism.

Furthermore, in the Al/ZrO_2/TiO_2/Al sample, the retained oxygen concentration in the TiO_2 layer near the top Al electrode ensures stability for electron trapping and enhances data retention over time. On the other hand, compared to previous studies, the higher stoichiometry of the TiO_2 thin film in this research results in deeper trap levels and higher resistance ratios. The addition of the ZrO_2 layer and the higher stoichiometric composition of TiO_2 contribute to a higher resistance value in the storage cell, making Al/ZrO_2/TiO_2/Al

suitable for large-scale array applications.

Additionally, excessively thin (0.65 nm) or thick (2.6 nm) ZrO_2 layers present issues of incomplete blocking or reduced resistance ratio. Therefore, the 1.3nm-thick ZrO_2 layer offers optimal barrier performance, suppressing undesirable chemical reactions between the top Al electrode and the RS TiO_2 layer, while minimizing their adverse effects.

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Chapter 3. Artificial Synapse Based on an $Al/ZrO_2/TiO_2/Al$ Electronic Bipolar Resistance Switching Memristor

3.1. Introduction

Brain-inspired artificial neural networks, such as spiking neural networks (SNN), attract much attention as an alternative to the deep-learning-based back-propagation method, which lacks energy efficiency due to the excessive energy cost of the training steps. The primary requirement for artificial synapses that can be used in neuromorphic systems is their ability to exhibit synaptic plasticity, which is the ability to change synaptic strength (weight) following electrical stimulation.[1-5] Linear increase (potentiation) and decrease (depression) characteristics with the numbers of the selected pulse voltages are necessary to emulate the brain synapses efficiently. Other crucial indicators include power consumption, scalability, signal-to-noise ratio, operation speed, and reliability.[6-10] Several emerging nonvolatile memory devices, including resistive random access memory (RRAM),[11-16] magnetic random access memory,[17, 18] phase change memory,[19, 20] and ferroelectric memory,[21-24] were reported to show the artificial synapse functions. Among these

candidates, metal-oxide RRAM has been widely studied due to its electrical adjustability and compatibility with the conventional complementary metal-oxide-semiconductor (CMOS) integration processes.[25-27] The two-terminal configuration of the RRAM offers flexibility and simplicity in fabricating the synaptic array devices for the neuromorphic systems, compared to devices with three-terminal configurations, such as transistors. [28-31]

However, many RRAM devices have conducting filament (CF)-based switching mechanisms, which generally accompany abrupt and stochastic switching properties due to the random localized formation and rupture of the CFs.[32-34] These properties are undesirable and degrade synaptic functions, such as linear potentiation/depression, paired-pulse facilitation (PPF) and spike-timing-dependent plasticity (STDP).

In contrast, non-filamentary RRAM may represent a better choice for superior synaptic properties. Unlike CF-based RRAMs, such non-filament-controlled memristors participate in electrical conduction throughout the entire electrode area. They generally encompass better uniformity and higher area scalability, whereby the smaller device area induces low power consumption.[10, 35, 36] Nonetheless, the synaptic devices based on non-filamentary memristors have been the subject of limited research.[37, 38]

In the previous chapter, the authors reported a non-filamentary Al/ZrO_2/TiO_2/Al (AZTA) RRAM device that exhibited various promising properties, including excellent uniformity, forming-free characteristics, and area-scalable behavior.[39] These performances were based on the electronic bipolar resistive switching (e-BRS) mechanism. This study further investigated the ability of the AZTA RRAM device to simulate artificial synapses. It demonstrated unprecedentedly linear synaptic plasticity (potentiating and depression) among the two-terminal devices, which allowed for more complex biological synaptic functions such as long-term potentiation, long-term depression, PPF, and STDP under different pulse lengths, amplitudes, and frequency conditions. The electrical conduction mechanism analysis of the AZTA device could scrutinize the origin of such superior synaptic functionalities. The space-charge-limited current (SCLC) mechanism dominates the synaptic behavior, allowing for multilevel or almost analog-type memory states. The notably high online learning capability of multilayer perceptron using the AZTA as the synaptic is also demonstrated using simulations.

3.2. Experimental

First, a 100-nm-thick Al film was deposited onto a Ta_2O_5 (5nm)/SiO_2 (200nm)/Si substrate utilizing an electron beam evaporator (Sorona, SRN-200i), which served as the bottom electrode. The bottom Al layer will swiftly oxidize to form a ~5 nm-thick AlO_x layer at the surface during transfer to the next process chamber through the air atmosphere. Subsequently, using a lab-made sputtering system, a 25-nm-thick TiO_2 film was deposited under the deposition conditions; a Ti_4O_7 target, deposition temperature of 25°C, RF power of 125 W, deposition pressure of 0.015 Torr, O_2/Ar pressure ratio of 1:4, and a deposition duration of 17.3 min. Next, the thermal atomic layer deposition system (Quros, Plus 200) was employed to deposit ~2-nm-thick ZrO_2 layers atop the TiO_2 layer. The deposition conditions were as follows; 10 deposition cycle times, $Zr[N(CH_3)(C2H_5)]_4$ Zr-precursor, O_3 oxygen source, and 250 °C deposition temperature. Finally, a 100 nm-thick Al top electrode was deposited using the same electron beam evaporator. The top and bottom electrodes were patterned by photolithography and lift-off techniques to generate cross-point structured samples of varying electrode areas (4 × 4 μm^2, 6 × 6 μm^2, 8 × 8 μm^2, 10 × 10 μm^2). The TiO_2 and ZrO_2 layers were not patterned to mitigate etching

damage.

The Al top electrode is connected to the bias voltage, while the Al bottom electrode is grounded. Direct current (DC) current-voltage (I-V) characteristics were measured using a semiconductor parameter analyzer (Hewlett Packard, 4145B). For pulse-switching tests, a semiconductor parameter analyzer (Hewlett Packard, 4155B), a pulse generator (Tektronix, AFG3010C), and an oscilloscope (LeCroy, WaveSurfer 62MXs-B) were employed. Due to the extremely high initial resistance (~9×10^{9} Ω @V_{read} = 0.5 V) of the AZTA device with the electrode area of 100 μm^2 and the high input impedance of the oscilloscope of 2 MΩ, the accurate current reading in pulse mode was impossible. Therefore, the device's conductance was measured using the DC sweep mode. A switching box was used to switch between DC and pulse modes. The in-house built test program controls the test interval between switching modes. All data in this work were achieved from the electrode area of 100 μm^2, except for the area-dependent tests.

3.3. Results and Discussions

3.3.1. The gradually changing resistance characteristics

Figure 3.1 shows typical the current-voltage (I-V) characteristics of the AZTA resistance switching memory device at the DC sweep mode. The voltage sweep sequence is set as 0 → -4 V → 0 → 4 V → 0. The set process occurs at the negative bias with a compliance current of 1 μA, and the device is converted from the high resistance state (HRS) to the low resistance state (LRS). Then, a reset process occurs at the positive bias, returning the device to HRS again. The resistance ratio of HRS and LRS is about 500 at the read voltage of 0.5 V. This differentiates the binary state, which can be used to store a logic "0" or "1" for the non-volatile memory applications. However, in order to simulate the function of biological synapses, an analog memristor with multiple resistance states between HRS and LRS is expected, which means the synaptic weights (i.e., resistance or conductance) of the AZTA device can be progressively regulated. This is one of the essential factors for artificial synaptic devices to be applied in artificial neural networks. Figures 3.1 (b) and (c) show the I-V characteristics at the different-voltage DC sweep mode of

the set and reset process, respectively. The sweep voltages are applied following the numerical sequence (1st to 6th for the set; 7th to 12th for the reset). First, a continuous set process is performed with the set stop voltage increasing from -3.7 V to -4.2 V, accompanied by a gradual decrease of the resistance value from HRS to LRS (9.0×10^9 Ω to 5.4×10^7 Ω @V_{read} = -0.5 V). Subsequently, a continuous reset process is performed with the reset stop voltage increasing continuously from 3.9V to 4.4V and the resistance value increasing from LRS to HRS (6.5×10^7 Ω to 7.2×10^9 Ω @V_{read} = 0.5 V). Both processes show gradually changing resistance as the increasing applied voltage. This gradual changing behavior of the resistance at the low voltage sweep range is more clearly shown in the illustrations of Figures 3.1 (b) and (c). In addition, Figures 3.1 (d) and (e) shows the real-time gradual changing behavior of the current at the pulse test mode for the set and reset process, respectively, which also strongly demonstrated that the resistance of the AZTA device could be progressively regulated to achieve multiple states. Also, Figure 3.2 suggests that the gradually changing resistance is substantiated to control by the trap-assisted SCLC mechanism, indicating the AZTA device belongs to a typical non-filamentary type conduction mechanism.[35, 36, 40] Driven by the applied voltage, electrons are captured or released by the traps (most of the oxygen

vacancies and defects) in the TiO_2 layers, and these traps are at different depths of trap energy levels. Therefore, as the electrons gradually fill up the different-depth trap energy levels, multiple resistance states will be obtained.

Importantly, the resistance regulation mode based on the trap-assisted SCLC mechanism will not be easily affected by the previous operation, thus conducive to achieving the precise regulation of the resistance with the same operating conditions in the repeat operation. In contrast, devices controlled by filamentary-type mechanisms usually modulate the resistance by setting different compliance currents or reset stop voltages, closely related to the partial formation or annihilation of CFs.[41-43] After repeated operations, the formation of stronger and larger diameter CFs or multiple CFs will have a continuous impact on subsequent operations. This typically results in a stronger electrical stimulation being required to restore the device's resistance to its initial state. Even sometimes, greater stimulation cannot return the device to the corresponding previous state yet. Therefore, these randomly formed and easily continuously enhanced CFs make it challenging to accurately adjust the resistance in the continuous endurance test.

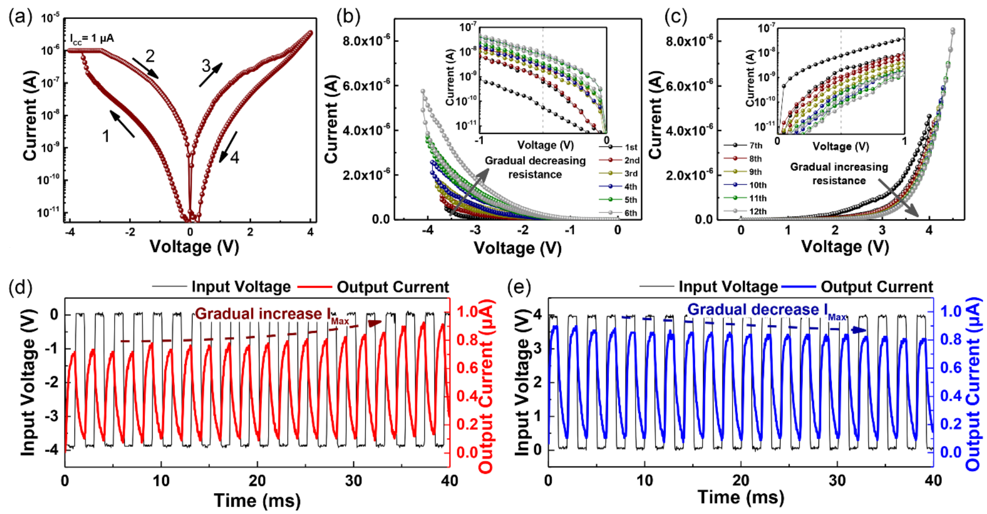

Figure 3.1. (a) Typical I-V curves with an I_{cc} of 1 μA. (b) The set process with gradually decreasing sweep voltage from -3.6 V to -4.1 V. (c) The reset process with gradually increasing sweep voltage from 4.0 V to 4.5 V. The I-V curves in the semi-log scale within the low sweep voltage range are shown in the inset figures. (d) The set and (e) reset process in pulse operation mode with an input voltage of -4 V and 4 V, respectively. The interval and pulse length are both 1 ms.

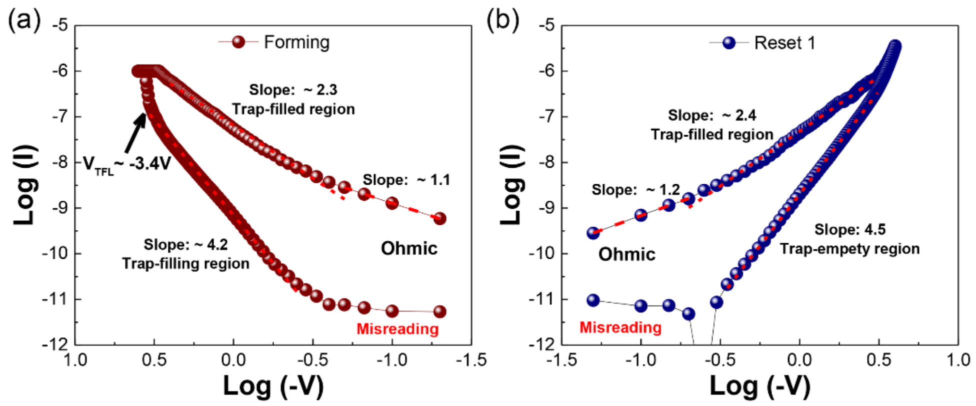

Figure 3.2. The double log fitting of the I−V curves of (a) set process and (b) reset process for AZTA memristor, showing the typical SCLC mechanism. The threshold voltage is approximately −3.4V. The poor linear fitting in the HRS region is due to the current level being close to the detection limit of the equipment.

3.3.2. Evaluation of the artificial synapse performance

Figure 3.3 (a) shows a schematic diagram of the AZTA memristor that simulates the artificial synapse. The charge trapping and detrapping in the TiO_2 resistance switching layer changes the conductance of the AZTA sample, adjusting the synaptic weight, which emulates the human synapse function mediated by the Ca2+ ion channel. The gradual resistance-changing property of the AZTA sample will allow for the fine-tuning of the synaptic weight by changing the pulse amplitude, length, frequency, and number of input pulses. Here, a G_n/G_0 index is introduced to indicate the effect degree of different stimuli on synaptic plasticity (G_0 represents the initial synaptic weight, and G_n represents the synaptic weight after the stimulus). Figure 3.3 (b) suggests the synaptic weight can be effectively modulated by changing the pulse amplitude of the stimulus signal of negative pulses. When the absolute value of applied pulse amplitude was less than 3.4V, synaptic plasticity did not show a noticeable change after applying five consecutive pulses, and the G_n/G_0 remained at 1. However, when the pulse amplitude exceeds 3.4V, the synaptic weight gradually increases with the increase of the pulse numbers, of which the trend is strengthened with the increasing amplitude. For example, after five consecutive

pulses with a pulse amplitude of 4.2 V, the G_n/G_0 index increased to ~20.8. Notably, the pulse amplitude of 3.4 V is consistent with the threshold voltage of the SCLC mechanism, as discussed in the following section. When the applied voltage exceeds the threshold voltage during the DC sweep, all traps in the TiO_2 layer are filled with the injected electrons. The subsequently injected electrons will move into the conduction band, resulting in the trap-filled SCLC mechanism. However, for the pulse operation mode, the electrons may not rapidly fill all the traps at the relatively low pulse length but gradually fill the traps with different energy levels, gradually increasing conductance.

Next, the modulating effects of the pulse length and frequency on the synaptic plasticity of the AZTA device are demonstrated. Figure 3.3 (c) shows synaptic plasticity changes by a single pulse with different pulse lengths. The synaptic weight is enhanced with the increasing pulse length. Notably, the pulse length of the single applied pulse should be long enough to obtain the discernable weight change for the multilevel operation application (more than 500 μs at least for one state). Figure 3.3 (d) shows the influence of the pulse frequency change on synaptic weight. The higher the pulse frequency, the more pronounced the enhancement of synaptic weight. These results indicated that the synaptic plasticity of the AZTA artificial synapses

could be precisely regulated by modulating the parameters of the pulse stimulus, and the transition between short-term and long-term memory behaviors can be achieved.

Based on the above results, suitable pulse conditions were selected to examine the long-term plasticity characteristics of the AZTA artificial synapses, as shown in Figure 3.4. For efficient artificial synapses in neural network computing, the synapse cell should have a nearly linear response over the conductance range, with each pulse changing only a tiny fraction of the overall dynamic range of conductance.[10] For this purpose, the nonlinearity values of the potentiation (NLP) and depression (NLD) are introduced to evaluate the device's performance. The smaller the NLP and NLD, the more linear the conductance change.[44] Figure 3.4 (a) shows the long-term potentiation characteristics of the AZTA synapses, showing the conductance increase with the number of applied pulses under different pulse amplitudes. The conductance increases rapidly at high applied pulse amplitude and reaches a high saturation value. In contrast, the conductance increases slowly at low applied pulse amplitude and reaches a relatively low saturation value. The NLP decreases notably with the decrease of the applied pulse amplitude, which is closely related to the trap-filling rate with electrons. Although the best NLP is obtained at −3.8 V, the conductance ratio is

too low for practical application. Therefore, a pulse amplitude of -4V was selected as the best test condition for long-term potentiation. Here, the conductance ratio is ~20 (initial conductance (G0) and after 50 pulses (G50) are ~ 0.2 nS and 4.5 nS, respectively). The G50 of the potentiation process was selected as the initial state of the subsequent depression test with different pulse amplitudes, as shown in Figure 3.4 (b). The higher the amplitude of the applied pulse, the faster the discharge rate of the trapped electrons in the traps, which leads to a high NLD value. Therefore, similar to the potentiation process, the NLD value of the conductance change is lower at relatively low pulse amplitudes. However, for the too-low pulse amplitudes, some trapped electrons may not be fully de-trapped during the 50 pulses, resulting in the conductance not returning to its initial value. Similar results were verified in the DC sweep test shown in Figure 3.5; to return the conductance to the initial value, the sweep times of the reset process with a low reset voltage must be longer than those of the set process with a high set voltage. Finally, Figure 3.4 (c) shows five consecutive long-term plasticity test results with the optimized conditions of -4.0V/500 μs and 4.2 V/500 μs for potentiation and depression, respectively. The pulse number was set to 30 to eliminate the effect of the conductance saturation region for optimal nonlinearity. Figure 3.4 (d) shows the

average results of these five consecutive cycles, suggesting that the conductance variation of the AZTA synapse is highly linear, with NLP and NLD values of 0.17 and -0.70, respectively. The achieved conductance ratio was ~ 12.0 (G_{min} and G_{max} = 0.28 nS and 3.40 nS). The energy consumption can be calculated by $E_{cons} = V \times I \times t$, where V, I, and t represent the input pulse amplitude (-4 V), the current (0.6 μA), and the pulse length (500 μs), respectively. E_{cons} for one step of the potentiation is ~ 1.2 nJ, much higher than the human synapses (1 - 10 fJ).[38, 45] Nonetheless, because of the area-dependent characteristics of the AZTA device, power consumption is expected to be decreased with the device size scaling. In addition, it is worth noting that this linear variation in conductance is obtained under identical pulse test conditions, a critical merit of this device compared to other reports. The identical pulse condition eliminates the complexity of the control circuit for making non-identical pulse conditions.[18, 46-49]

Moreover, further research was conducted to test the potential for more operable conductance states of the device, as shown in Figure 3.6. When the total input pulse trains are constant (i.e., the input pulse amplitude is -4 V and the total pulse length is 8 ms), the pulse length is equally divided into smaller pulse lengths (500 μs, 200 μs, 80 μs, and 32 μs) with the DC read operation after each pulse. The

number of pulses for these tests is 16, 40, 100 and 250, respectively. As the pulse length decreases and the pulse number increases, the reading conductance fluctuation increases significantly. However, this degradation was not due to the inherent device performance but the test artifacts; the frequent switching of pulse mode and DC reading mode caused a transient response, thus affecting the accuracy of the measurement results. Nevertheless, the linear fitting slope of the conductance to the pulse number decreased, indicating the final conductance also gradually decreased after the same input pulse trains.

However, when inputting the pulse trains without the DC reading steps, even if the pulse length is divided into tiny equal parts, the conductance did not decay, as shown in Figure 3.7. This finding suggests that frequent switching between operating modes affected the memory state of the AZTA device, leading to conductivity attenuation. Notably, similar potentiation and depression characteristics were obtained, even after 1000 pulse tests, as shown in Figure 3.4 (e), which strongly demonstrated the outstanding ability to maintain the linearity for the AZTA synapses.

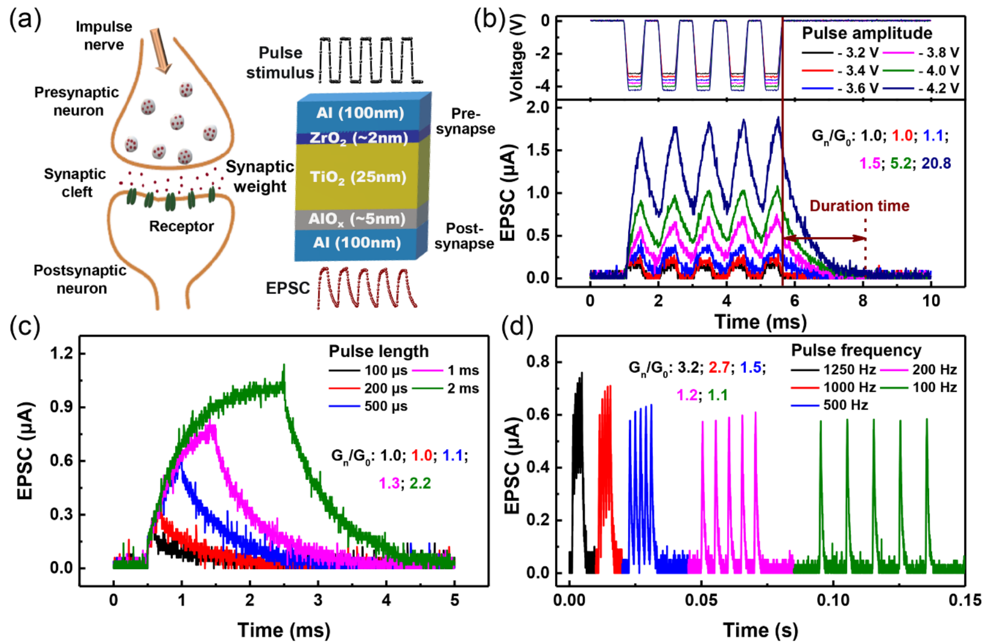

Figure 3.3. (a) Schematic diagram of the AZTA memristor simulating the working mechanism of a biological synapse. Excitatory post-synaptic current (EPSC) under different (b) pulse amplitudes (The pulse length and interval are 500 μs with leading and training times of 100 μs), (c) pulse lengths (The pulse amplitude is −4 V), and (d) pulse frequencies (The pulse amplitude is −4 V and the pulse length is 500 μs), respectively. The leading and training times were not set in the pulse length and frequency tests for better comparison and calculation.

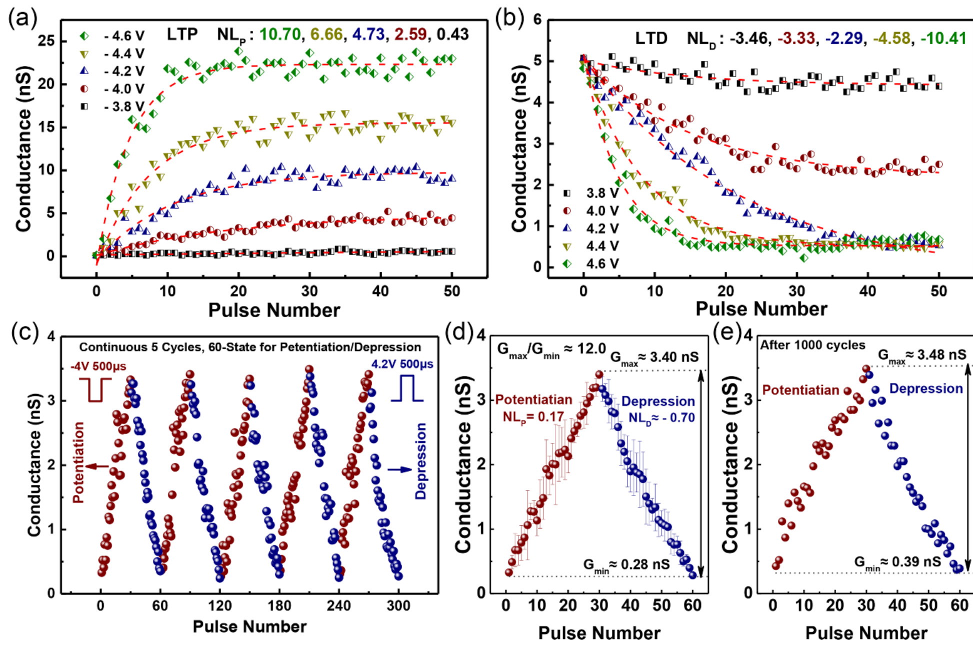

Figure 3.4. (a) Long-term potentiation characteristics under different pulse amplitudes from -3.8 V to -4.6 V. (b) Long-term depression characteristics under different pulse amplitudes from 3.8 V to 4.6 V. (c) Five consecutive long-term plasticity tests with the pulse conditions of -4.0 V/500 μs and 4.2 V/500 μs for potentiation and depression, respectively. (d) The average results of five consecutive cycles with the conductance ratio of 12.0. (e) The potentiation and depression test after 1000 pulse cycles.

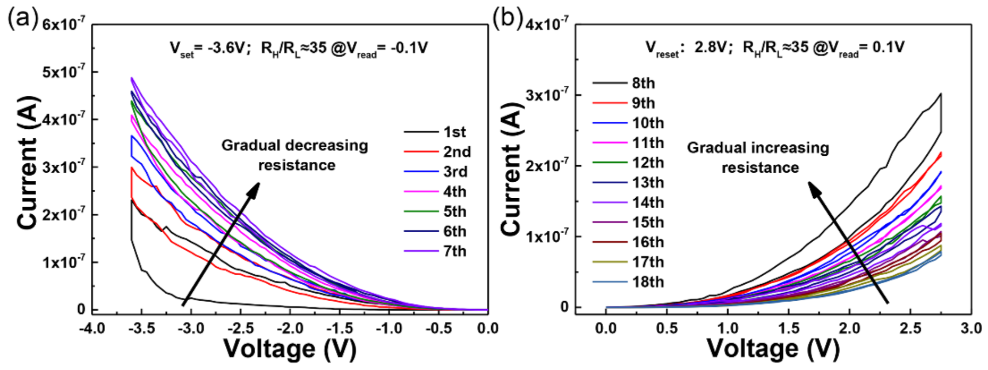

Figure 3.5. The gradual changing I-V characteristics of AZTA memristor at DC sweep mode. (a) The set sweep voltage is set to -3.6V. (b) The reset sweep voltage is set to 2.8V.

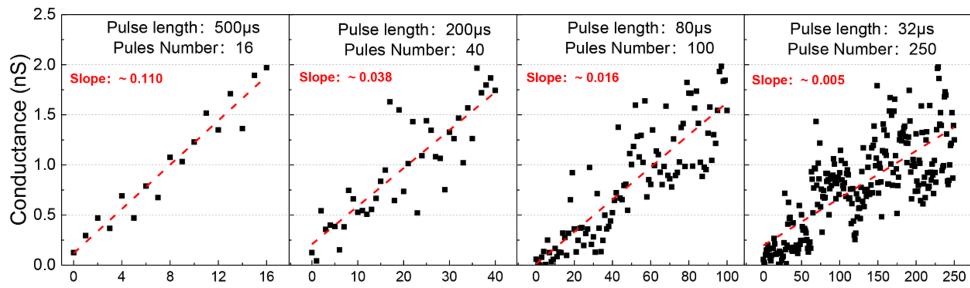

Figure 3.6. The conductance change trend as the different pulse lengths and pulse numbers. The switching box switches between pulse trains and 0.5V DC reading operations with a time interval of 1 second. The red dash line is the best linear fitting for the conductance.

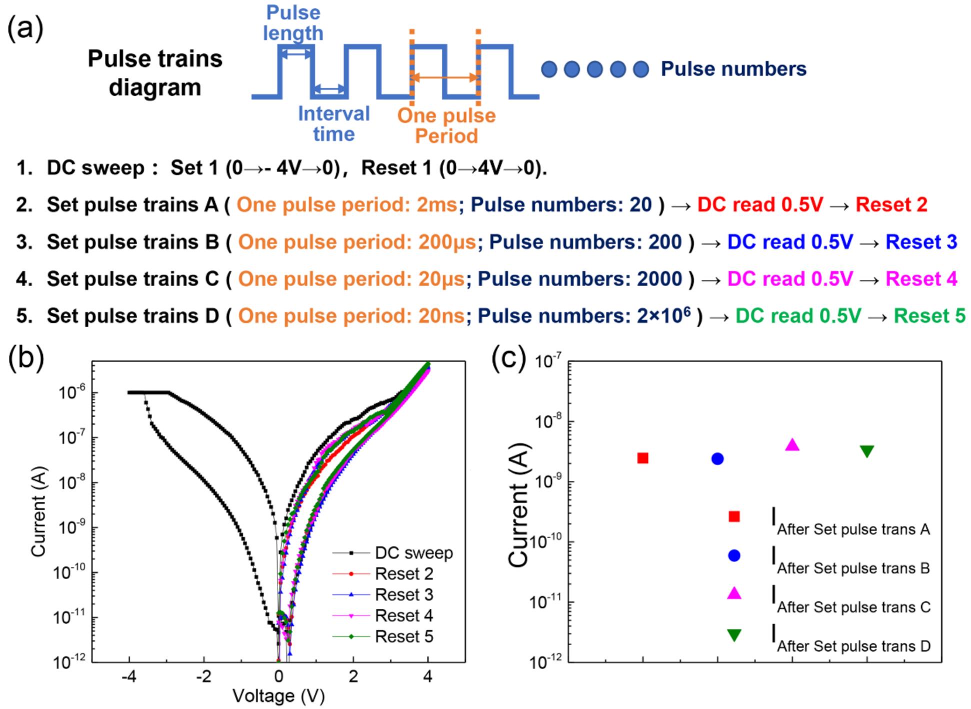

Figure 3.7. (a) The schematic diagram of all pulse trains, while the testing was performed in numerical order from 1 to 5. The total applied pulse length and interval time was equal for all pules trains, both 20ms. (b) I-V curves at DC sweep mode, where the reset sweeps were performed to confirm that the device had returned to its initial state. (c) The read currents after the pulse trains at a read voltage of 0.5 V.

3.3.3. The work mechanism analysis based on the trap-assisted SCLC mechanism

The trap-assisted SCLC mechanism of the AZTA synaptic devices makes a pivotal contribution to this excellent adjustment of the synaptic plasticity. As shown in Figure 3.8 (a), four different states are obtained, named State 1, State 2, State 3, and State 4, respectively, by continuously applying the same pulse trains. Figure 3.8 (b) shows the I-V curves of the four states under a DC sweep operation from 0 to 0.6V. The conductance increase for four states is linear (0.21 nS, 1.32 nS, 2.30 nS, and 3.37 nS, inset figure) at a V_{read} of 0.5 V, corresponding to the data shown in Figure 3.4. Subsequently, the I-V curve in Figure 3.8 (b) is replotted in the double logarithmic scale, as shown in Figure 3.8 (c). In the low voltage range, the fitting slope values of all four states are close to 1, indicating that the electron transport follows the hopping conduction mechanism and the current is mainly dominated by thermally generated carriers. As the sweep voltage increases, the injected carriers gradually become dominant. Thus, the electronic transport mechanism shifts towards the SCLC mechanism and the fitting slope values of four states in the trap-filling region increase. It is worth noting that the slope values in the trap-filling region of State 1 to

State 4 gradually increased (1.6, 1.8, 2.8, and 3.7), indicating that electrons are gradually filled traps from the deep trap level to the shallow trap level. The transition voltage (V_{on}) increases from 0.20 V, 0.24 V, and 0.27 V to 0.31 V for the four states also verified such a trend. The electrons trapped at shallower energy levels can again participate in the electron transport process through recombination and release with thermally generated carriers, thereby increasing the effective lifetime and concentration of thermally generated carriers. Therefore, a higher V_{on} is required to inject more carriers and drive the current transition from the hopping to the SCLC mechanism. Also, through temperature test and linear fitting calculation based on the Arrhenius formula, as shown in Figure 3.9, the activation energy (E_a, the energy level for traps) for four states was obtained from 0 V to 0.6 V, as shown in Figure 3.8 (d). The activation energy of all states decreases as the applied voltage increases, indicating that the electron gradually filled the traps. Subsequently, the best nonlinear fitting of Figure 3.8 (d) was performed to estimate the trap energy levels at zero electric field, which are ~ 0.27 eV, 0.20 eV, 0.15 eV, and 0.12 eV for the States 1, 2, 3, and 4, respectively.

Based on the above results, Figure 3.8 (e) shows a schematic diagram of the potentiation process of the AZTA synaptic device. Under continuous pulse train stimulation, electrons are injected from

the Al/ZrO_2 interface, gradually filling the trap energy levels from deep to shallow. The conductance values corresponding to each state were closely related to the depth of the trap energy level and showed a nearly linear change. In contrast, the trap energy difference of adjacent states gradually decreased. The trap-assisted SCLC current (J) follows the Eq. (1) when a single energy level trap presents:

$$J = \frac{9}{8}\varepsilon\varepsilon_0\mu\theta\left({V^2}/{d^3}\right) \quad (1)$$

, where the θ is ${n_f}/{n_f + n_t}$, n_f, and n_t are the free carrier and trapped carrier density, respectively.[50, 51] At a fixed read voltage, the reading conductance is proportional to θ because the other parameters are constant. When the reading voltage is low, n_t is much greater than n_f, therefore, the reading conductance can be roughly proportional to ${1}/{n_t}$. Also, n_t can be defined with single energy level Et as:

$$n_t = N_t exp\left({-(E_t - E_F)}/{kT}\right) \quad (2)$$

, where N_t, E_F, k, and T are trap density, Fermi energy level, Boltzmann constant, and ambient temperature, respectively. Then, the electrical conductance is approximately proportional to $exp(E_t - E_F)$. Here, the value of E_a in each state is regarded as E_t, and the absolute value of E_F (n-type TiO_2 has several hundred millivolts) is greater than the absolute value of E_t. Then, by plugging in the

activation energies E_a for each of the four states into the exponential relationship, the energy level differences between states 1-2, 2-3, and 3-4 are 0.7 eV, 0.5 eV, and 0.2 eV, resulting in an approximately linear change in the conductance. However, it should be noted that this analysis is based on the assumption that the traps are in a single energy level to help understand this unique potentiation process. The actual situation may be more complex than this simple assumption. The traps in the AZTA synaptic devices will likely exhibit an exponential distribution from deep to shallow level due to the characteristic factor (slopes of the trap-filling region) greater than 2,[52] requiring further research. Moreover, the previous work has confirmed that the trap energy levels of AZTA synaptic devices remained unchanged during the endurance test.[39] This property allows for consistent modulation of synaptic weight after many cycles, meaning similar conductance values can be achieved under the same pulse stimulation.

In addition, the "voltage-time dilemma" in many CF-based RRAM, a trade-off between programming speed (requiring a low energy barrier to facilitate defects motion) and retention (requiring a high energy barrier to prevent defect dispersion), could be overcome with the AZTA sample.[10, 32] First, the retention failure time ($t_{failure}$) of AZTA synaptic devices is related to the trap energy level where the

trapped electrons were located, $t_{failure} \propto Exp\left({E_a}/{kT}\right)$. Figure 3.8 (f) shows the retention characteristics of four states at room temperature for 10^5s. The conductance of all states decreases slightly over time because the trapped electrons are continuously detrapped by thermal noise. As the E_a decreases from State1 to State 4, they become more easily thermally excited and released, resulting in lower retention performance. After 10^5 seconds, the conductance values from State 1 to State 4 were decreased by ~ 2.3%, 14.8%, 19.5%, and 22.2%, respectively. Although the retention performance of the AZTA synaptic device is still not satisfactory compared to filamentary-type RRAM devices, the conductance range used by this device is a portion close to the deep trap level. Therefore, the retention performance as a synaptic device has been optimized somewhat compared to the conductance range used as a digital memory device.

Figure 3.8 (g) shows the trend of synapse weight versus pulse length for different-size AZTA synapse devices. The conductance ratio gradually increases as the pulse length increases for all devices. As the device size decreases, the required pulse length to achieve the same conductance ratio gradually decreases. For example, the required pulse length to achieve the same conductance ratio of 10.8 (gray line) gradually decreases from 10 ms, 6 ms, and 3.5 ms to 1.6

ms for the devices with electrode areas of 100 μm^2, 64 μm^2, 36 μm^2, and 16 μm^2, indicating that the required pulse length is approximately proportional to the device area. This finding means that reducing the device size can effectively increase the operating speed. For example, it is speculated that the AZTA synaptic device with an electrode size of 0.01 μm^2 may require a pulse length of 1μs to achieve a similar conductance ratio. The smaller device area will decrease the output current when the pulse is applied. As a result, power consumption will correspondingly decrease significantly, possibly even below the level of the human brain synapse.

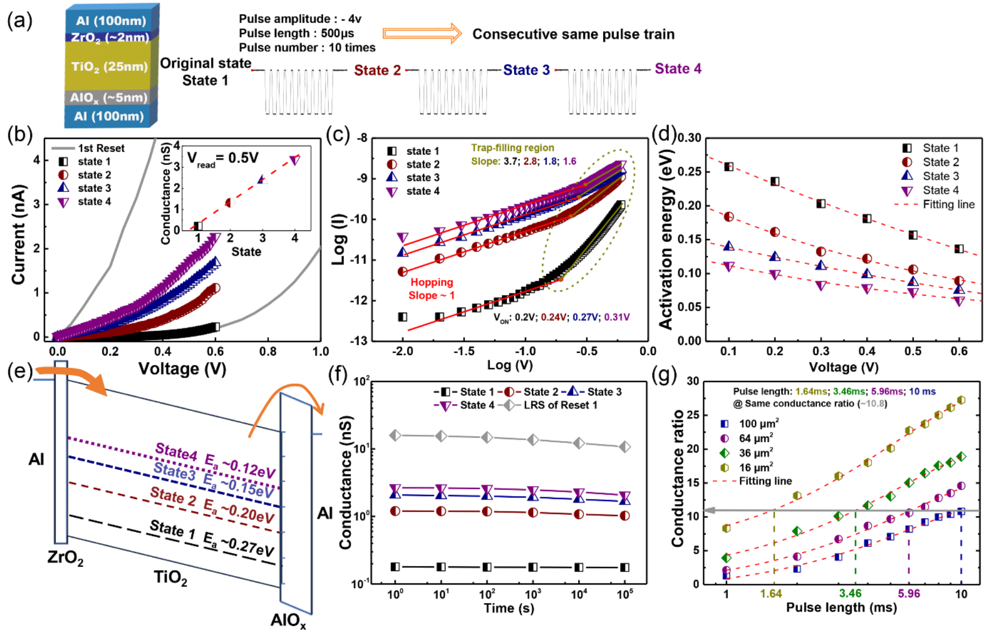

Figure 3.8. (a) Four different conductance states were obtained by continuously applying the same pulse trains. (b) The I-V curves of the four states under a DC sweep mode from 0 to 0.6 V. The conductance of four states at the read voltage of 0.5 V is shown in the inset figure. (c) The double log plot of I-V curves in four states. The red and yellow lines represent the fitting of the hopping and SCLC mechanisms, respectively. The intersection point of the two lines is the transition voltage. (d) The activation energies of four states were obtained from 0 V to 0.6 V by the temperature test and Arrhenius fitting. The red dash line is the best nonlinear fitting of 4 states. (e) Schematic diagram of electronic injection during the potentiation process. Electrons at the top interface are massively injected through the ultra-thin ZrO_2 layer, while their loss at the

bottom interface is minimized due to the high potential barrier of Al2O3. The dash lines of various colors represent trap energy levels at different depths. The number of segments in the dashed lines represents a qualitative comparison of the number of traps. (f) The retention behavior of the four conductance states and the low resistance state (LRS) for the first reset process at room temperature over 105 seconds. (g) The conductance ratio changes of devices with different areas (100 μm^2, 64 μm^2, 36 μm^2, and 16 μm^2) under different pulse lengths from 1 ms to 10 ms. The solid gray line represents the conductance ratio is 10.8. The red dash line is the best nonlinear fitting for each state.

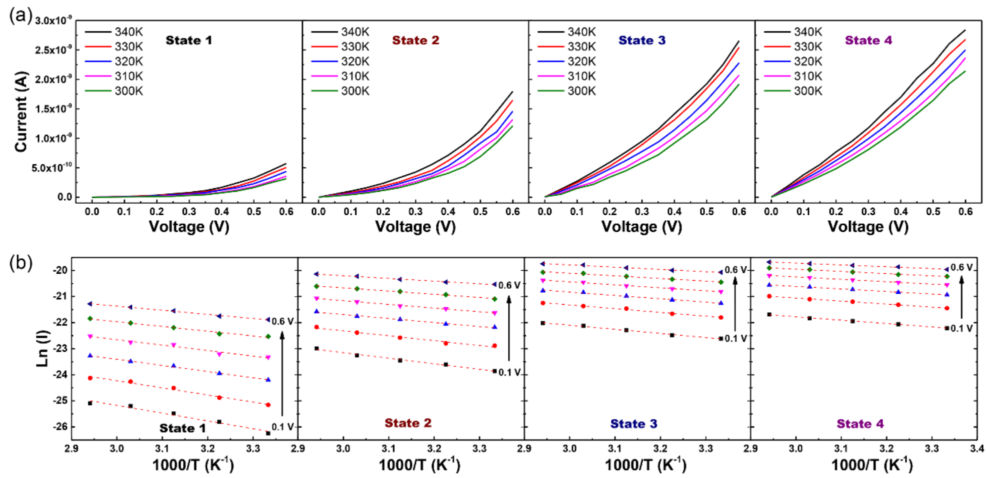

Figure 3.9. (a) The temperature dependence characteristics of the four states at the temperature range of 300 K to 340 K of the AZTA artificial synapse. (b) The Arrhenius-type plots of the temperature test data for calculating the activation energy (E_a) from 0.1 V to 0.6 V.

3.3.4. Neuromorphic computing application

PPF is an essential test for analyzing the short-term plasticity of temporary information in the brain. In SNNs, it can simulate temporal correlation between pre-synaptic neurons, thereby altering the efficiency of synaptic transmission to facilitate information processing and transfer between neurons. Figure 3.10 (a) shows an example of pulse stimulation for AZTA artificial synapse simulating PPF testing. The interval (Δt) between two consecutive pulses regulates this short-term synaptic plasticity. When the second pulse arrives, the current caused by the first pulse does not immediately disappear, increasing the post-synaptic current. The following equation defines the PPF index:

$$PPF\ index = {A_2 - A_1}/{A_1} \times 100\% \tag{3}$$

Figure 3.10 (b) further demonstrates that the results of PPF testing can be well-fitted with a double exponential function for time intervals ranging from 10 μs to 5 ms:

$$PPF\ index = 1 + A_1\, Exp\left(-{\Delta t}/{\tau_1}\right) + A_2\, Exp\left(-{\Delta t}/{\tau_2}\right) \tag{4}$$

, where τ_1 and τ_2 are the time constants of fast and slow relaxations, which are approximately 0.5 ms and 216.4 ms, respectively, comparable to biological synapses and previous reports.[53-55] Three

data points were taken for each time interval sample to improve the accuracy of the fitting results, and the detailed data are shown in Figure 3.11.

Furthermore, the STDP learning strategy is one of the most representative forms of long-term plasticity in SNNs. It is also one of the most common methods of synaptic weight updating. The connection between two neurons depends on the relative timing of pre-synaptic and post-synaptic activations (Δt). If the pre-synaptic spike arrives before the post-synaptic spike, it can result in a long-term potentiation (LTP) effect. Conversely, if the post-synaptic spike arrives before the pre-synaptic spike, it can cause long-term depression (LTD). The following equation can describe the relationship between the change in weight and the time interval:

$$\boldsymbol{\Delta}\omega = \begin{cases} A_+ \, exp\left(-\Delta t/\tau_+\right); if \; \Delta t > 0 \\ A_- \, exp\left(-\Delta t/\tau_-\right); \; if \; \Delta t < 0 \end{cases} \quad (5)$$

The Δω is the change of the synaptic weight, defined by $G_n - G_0/G_0 \times 100\%$. A_+ (A_-) is a scaling factor, and τ_+ (τ_-) is the time constant corresponding to the potentiation and depression of the synaptic connection.[41] For the AZTA synapse device, the pre-synaptic and post-synaptic pulse parameters were set to −4 V/500 μs and 4 V/500 μs, respectively, as shown in Figure 3.10 (c). The modulation of weights by the AZTA synapse based on the STDP

learning rule is shown in Figure 3.10 (d), demonstrating typical antisymmetric Hebbian learning characteristics. By fitting with a single exponential function, $\tau+$ and $\tau-$ were estimated to be approximately 9.3 ms and 10.1 ms, respectively, comparable to the time window of biological synapses in the human brain. These excellent features suggest that this AZTA synaptic device has promising potential for neuromorphic computing applications.

Finally, a fully connected neural network was constructed to evaluate the performance of AZTA synaptic devices, as shown in Figure 3.12 (a). The neural network consists of a 2-layer multilayer perceptron (MLP) with 400 input neurons, 100 hidden neurons, and 10 output neurons for recognizing handwritten digits from the MNIST dataset. The 400 neurons in the input layer correspond to a 20 × 20 MNIST image, while the 10 neurons in the output layer correspond to the 10 classes of digits. During the online learning, the neural network based on AZTA synaptic devices was trained using NeuroSim software with randomly selected images (60,000 images) from the MNIST dataset.[56] Figure 3.12 (b) shows the accuracy evaluation results obtained using the synaptic parameters shown in Figure 3.4. Detailed parameters are summarized in Table 3.1. The results indicate that the final inference accuracy in this artificial neural network (ANN) is closely related to the number of conductance

states of the synaptic device. When utilizing 30 conductance states, the inference accuracy reaches approximately 83.1%, which already surpasses the performances of similar MLPs in several previous reports.[3, 57, 58] Moreover, the potential of AZTA devices for accommodating a higher number of conductance states has been demonstrated. By setting 250 conductance states, the inference accuracy will be significantly enhanced to 94.9%, approaching the accuracy of the software baseline (96% - 97%). These findings suggest the remarkable potential of AZTA devices for achieving excellent performance in neural networks.

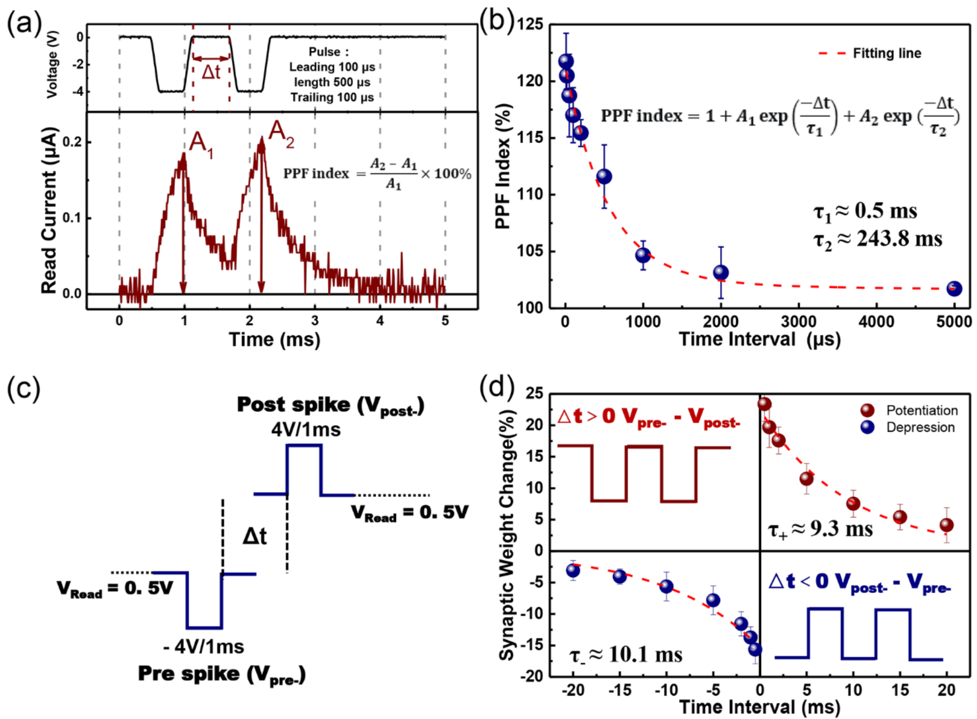

Figure 3.10. (a) Schematic diagram of pulse train stimulation for the PPF test. The pulse train parameter is −4 V/500 μs with the leading and trailing time is 100 μs. (b) PPF index is plotted as a function of the interval time (blue dot ball), extracted from 3 independent tests. The red dash line best fits the data points with a double exponential function. (c) The pre-synaptic and post-synaptic pulses were set to −4 V/500 μs and 4 V/500 μs, respectively. The AZTA synapse was read with a 0.5 V DC voltage before and after the pulse train to determine changes in synaptic weight. (d) The asymmetric STDP behavior of the AZTA artificial synapse. Synaptic weight changes are

plotted as a function of the interval between the pre-synaptic and post-synaptic pulses. The red dashed line best fits the data points with an exponential function.

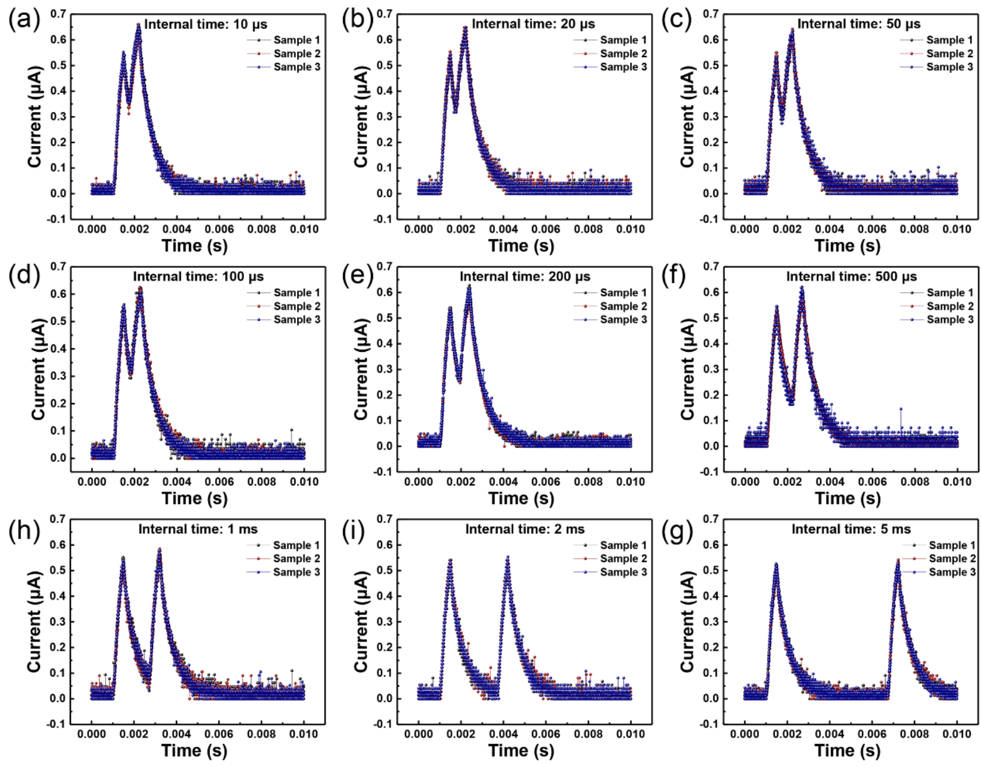

Figure 3.11. EPSC characteristics at different interval times for the PPF test.

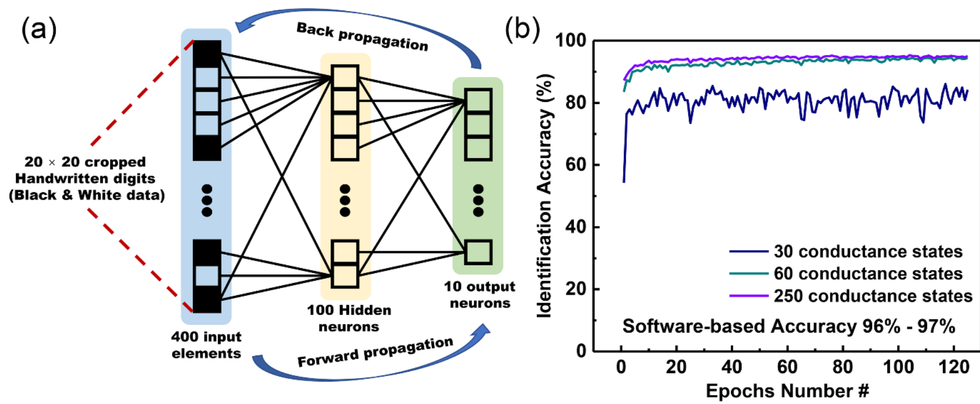

Figure 3.12. (a) Schematic diagram of MLP neural network based on the AZTA synaptic devices. (b) Identification accuracy under different conductance states.

Table 3.1. Online learning accuracy results and detailed simulation parameters in NeuroSim software.

<table>
<tr><th>Potentiation pulse</th><th>Depression pulse</th><th>G_{max} (nS)</th><th>G_{min} (nS)</th><th>Conductance Ratio</th><th>Nonlinearity (P/D)</th></tr>
<tr><td>-4V/500μs</td><td>4.2V/500μs</td><td>3.3965</td><td>0.2830</td><td>12.0</td><td>0.17/-0.70</td></tr>
<tr><th>Average/maximum standard deviation of the potentiation process (nS)</th><th>Average/maximum standard deviation of the depression process (nS)</th><th colspan="2">Conductance states (P/D)</th><th colspan="2">Online learning accuracy
(Average of the last 10 epochs)</th></tr>
<tr><td rowspan="3">0.2638/0.6197</td><td rowspan="3">0.2559/0.5166</td><td colspan="2">30</td><td colspan="2">83.10%</td></tr>
<tr><td colspan="2">60</td><td colspan="2">94.20%</td></tr>
<tr><td colspan="2">250</td><td colspan="2">94.90%</td></tr>
</table>

3.4. Summary

In summary, the non-filamentary and e-BRS AZTA memristor has excellent potential for simulating artificial synapses in neuromorphic computing. By controlling the amplitude, length, and frequency of applied pulses, the weight of the synapse can be precisely regulated. As a result, the AZTA synapse exhibited highly linear and symmetric potentiation/depression with a conductance ratio of ~12 under identical pulse trains. Furthermore, the synaptic weight variation remained consistent with the initial trend even after 1000 pulse cycles. These excellent synaptic characteristics are attributed to the trap-assisted space charge-limited conduction mechanism of e-BRS resistive switching devices. The conductance modulation is controlled by the trapping and detrapping electrons of traps. The conductive transport properties of this mechanism are also discussed in detail.

Moreover, this unique conduction mechanism avoids the voltage-time problem in many CF-based RRAMs. Therefore, it exhibits tremendous potential in low-power consumption and high-speed operation. PPF and STDP tests have also been successfully performed, indicating that the device is expected to be integrated into spiking neural networks. The 2-layer multilayer perceptron with 400 input, 100 hidden, and 10 output neurons using the AZTA

synapses can reach a remarkable accuracy of 94.9% for MNIST dataset recognition, despite the limited number of synapses (4 x 10^5).

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Chapter 4. Conclusion

In the past few decades, there has been increasing research activity on resistance random access memory. Compared to traditional RRAM devices based on conducting wires, electronic bipolar resistive switch devices have many advantages, such as the low risk of electrical breakdown, no electroforming step, high scalability, and low power consumption. In this study, we propose to insert a ZrO_2 layer at the top electrode interface to optimize the resistance switching performance of the device and thus form an Al/ZrO_2/TiO_2/Al structure based on a non-filamentary type mechanism RRAM device, which can also simulate various artificial synaptic functions in the spiking neural network, and demonstrate good synaptic performance.

The Al/TiO_2/Al resistance random access memory showed an area-type electronic bipolar resistive switching mechanism, which was mediated by the trapping and de-trapping of the carriers at the trap centers. The area-type e-BRS device had area-scalable characteristics and excellent uniformity, which are beneficial for large-scale integrated applications. However, the unsatisfactory endurance and retention performance needed to be improved. In the first part of this work, a 1-2nm-thick ZrO_2 thin layer was deposited

by the thermal atomic layer deposition on the 25nm-thick sputter-deposited TiO_2 layer to form an $Al/ZrO_2/TiO_2/Al$ memory cell. The thin ZrO2 layer effectively prevented the active Al top electrode from absorbing oxygen from the TiO_2 resistive switching (RS) layer without significantly affecting the asymmetric energy barrier structure of the device. The suppression of oxygen loss from the TiO_2 RS layer retained the desired trap density of the RS layer even after the extended switching cycle operation. This suppression effect significantly improved the RS performances, such as endurance, uniformity, and retention. The switching endurance was enhanced over two orders of magnitudes (from $<10^3$ to $>10^5$). The ZrO_2 layer also increased the overall resistance values of the memory cell, making it more suitable than the Al/ TiO_2/Al structure for high-density applications.

Furthermore, based on the above optimized e-BRS AZTA memristor with excellent performance, and holds high potential for being used as an artificial synapse in neuromorphic computing applications. Essential synapse functions such as short-term weight, long-term weight, spike-timing dependent weight, paired-pulse facilitation (PPF), and spike-timing-dependent plasticity (STDP) are successfully implemented in this AZTA device by finely modifying the shapes of pre- and post-synapse spikes. Importantly, compared

to traditional filamentary-type memristors, the conductance of this e-BRS AZTA device, controlled by electron trapping and de-trapping, is less influenced by previous operations, making it beneficial for achieving accurate and controllable conductance states with similar non-linearity in repeated endurance tests. Additionally, this AZTA device demonstrates high near-linear and symmetrical potentiation/depression under identical pulse test conditions, effectively reducing the difficulties of external programming and facilitating multivalued conductance without auxiliary circuits. Moreover, due to the area-dependent behavior, the AZTA memristor showed promising potential for low power consumption and high operating speed.

List of publications

1 Journal of Articles (SCI(E))

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deposition. *Journal of Materials Chemistry C* **2022,** *10* (17), 6611-6620.

5. <u>Li, X. Y.</u>; Park, T. G.; Kim, G. S.; Hwang, C. S., Energy-efficient artificial synapse based on an Al/ZrO_2/TiO_2/Al resistance switching memristor with High Linearity. *ACS Appl Mater Interfaces* **2023**, under review.

2 Conference

1. <u>Li, X. Y.</u>; Kim, H. J.; Zhao, J. S.; Hwang, C. S., Improvement in the endurance of bipolar resistance switching Al/TiO_{2-x}/Al memory cell based on electronic mechanism via Al-doping. *The 26th Korean Conference on Semiconductors* **2019**.

Abstract in Korean

TiO_2 기반 전자 양극성 저항 전환 메모리스트의 성능 최적화 및 신경형 컴퓨팅 응용

지난 몇십 년간 저항 스위치 랜덤 액세스 메모리(RRAM)에 대한 연구가 활발히 진행되었습니다. 특히, 하나의 트랜지스터-하나의 저항체 또는 크로스바 어레이(CBA) 구성을 사용한 RRAM 연구가 주목받았습니다. 이러한 구성에서 저항 스위칭은 주로 전도성 필라멘트(CF)의 형성과 파괴에 의해 제어되며, 이는 전기 형성 과정 중 하드 브레이크다운과 같은 문제를 야기합니다. 또한, CF의 확률적 특성으로 인해 비균일성과 신뢰성이 낮아집니다. 이와 대조적으로 전자 양극성 저항 스위칭(e-BRS) 기기는 캐리어(전자)의 포획과 이탈에 의존하며, 전류의 점진적 전환은 전기적 브레이크다운의 가능성을 줄이고, 전기 형성 단계가 없는 장점을 제공합니다. 또한, e-BRS 기기는 크로스바 어레이 통합에 적합한 면적 확장성을 가지며, 이는 전력 소비의 감소와 관련이 있습니다. 이러한 기기는 유연한 메모리, 보안 응용 프로그램 및 인공 시냅스 구현에 잠재력을 보여주고 있습니다. 그러나 많은 기기의 내구성과 보존 성능이 만족스럽지 못하며, 이는 산소 손실을 방지하고 기기 성능을 개선하기 위한 적절한 방법의 개발이 필요함을 의미합니다. $Al/TiO_2/Al$ 저항 랜덤 액세스 메모리(RRAM)는 전자 양극성 저항 스위칭(e-BRS) 메커니즘을 보이며, 캐리어의 포획과 이탈이 함점에서

중재된다는 것을 보여주었습니다. 면적형 e-BRS 기기는 큰 규모의 통합 응용 프로그램에 유리한 면적 확장성과 우수한 균일성을 가지고 있습니다. 그러나 내구성과 보존 성능이 만족스럽지 않았습니다. 이 연구에서는 25nm 두께의 스퍼터 증착 TiO_2 층 위에 열 원자층 증착을 통해 1-2nm 두께의 ZrO_2 얇은 층을 형성하여 Al/ZrO_2/TiO_2/Al 메모리 셀을 제작했습니다. 얇은 ZrO_2 층은 TiO_2 저항 스위칭(RS) 층에서 활성화된 Al 상위 전극이 산소를 흡수하는 것을 효과적으로 방지하였습니다. 이로써 기기의 비대칭 에너지 장벽 구조에 큰 영향을 주지 않으면서도 TiO_2 RS 층의 산소 손실을 억제하였습니다. 이 억제 효과는 확장된 스위칭 주기 동안 RS 층의 원하는 함점 밀도를 유지하게 하였습니다. 이 억제 효과는 내구성, 균일성, 보존력과 같은 RS 성능을 크게 향상시켰습니다. 스위칭 내구성은 10^3 이하에서 10^5 이상으로 향상되었습니다. 또한, ZrO_2 층은 메모리 셀의 총 저항값을 증가시켜 고밀도 응용 프로그램에 더 적합하도록 만들었습니다.

스파이킹 신경망(SNN)은 딥 러닝 방법론에 비해 에너지 효율성이 뛰어난 대안으로 주목받고 있습니다. 뉴로모픽 시스템에서 인공 시냅스의 중요한 요구 사항은 전기적 자극을 통해 시냅스 강도를 변화시킬 수 있는 시냅틱 플라스티시티를 구현할 수 있는 능력입니다. 저전력 소비를 가능케 하는 저변동 메모리 장치인 저항성 랜덤 액세스 메모리(Resistive RAM, RRAM)는 인공 시냅스 기능을 흉내 내는 데 유망한 기술입니다. 그러나 많은 기기가 급격하고 확률적인 특성을 보이는 전도성 필라멘트 기반 스위칭 메커니즘에 의존하기 때문에

원하지 않는 특성을 가지고 있습니다. 이에 반해 비 필라멘트 RRAM 기기는 향상된 균일성, 확장성 및 저전력 소비와 같은 우수한 특성을 보입니다. 그러나 시냅스 응용에 대한 비 필라멘트 메모리스터에 대한 연구는 아직 제한적입니다. 따라서 비 필라멘트 RRAM을 인공 시냅스에 대한 해결책으로 탐구하고 최적화하는 것에 상당한 잠재력이 있습니다.

본 연구에서는 뉴로모픽 컴퓨팅의 스파이킹 신경망(SNN)에서 인공 시냅스를 모방하기 위한 비 필라멘트 메커니즘을 기반으로 한 $Al/ZrO_2/TiO_2/Al$ (AZTA) 메모리스터를 제안했습니다. 이 장치는 프리 시냅스 및 포스트 시냅스 스파이크의 형태를 정밀하게 변조하여 단기적 가소성, 장기적 가소성, 페어드 펄스 증가 및 스파이크 타이밍 종속적 가소성을 구현할 수 있었습니다. 또한, AZTA 장치는 보조 회로 없이 동일한 펄스 동작 조건에서 높은 선형성과 대칭성을 가진 증폭 및 감소를 보여주며, 보조 회로 없이 다중 값 전도도를 가능하게 하였습니다. 전자(전자의 포획 및 이탈)는 산소 공석 함정이 제공하는 서로 다른 깊이 에너지 수준에서 시냅틱 가중치를 제어합니다. 또한, AZTA 메모리스터는 전력 소비가 낮고 작동 속도가 빠른 특성을 가진 면적에 의존적인 동작을 기반으로 하므로 저전력 소비 및 고속 작동에 대한 유망한 잠재력을 보여주었습니다. AZTA 시냅스를 사용하여 400개의 입력, 100개의 히든, 10개의 출력 뉴런을 가진 다층 퍼셉트론으로 MNIST 데이터셋의 94.9% 정확도를 달성할 수 있었습니다.

핵심어: TiO_2 기반 저항성 랜덤 액세스 메모리, 전자 양극성 저항 전환 메커니즘, ZrO_2 삽입층, 영역 의존적인 동작, 인공 시냅스, 비선형성, 스파이킹 신경망, 뉴로모픽 컴퓨팅

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