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**Master's Thesis**

# Design of Near-Threshold Injection-Locked Clock Multiplier

유사문턱전압에서 동작하는

주입 동기 주파수 체배기의 설계

**by**

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**February, 2023**

**Department of Electrical and Computer Engineering**
**College of Engineering**
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# Design of Near-Threshold Injection-Locked Clock Multiplier

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# Design of Near-Threshold
# Injection-Locked Clock Multiplier

by

Jiwon Shin

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# Abstract

The RO-based injection-locked clock multiplier (ILCM) has garnered attention as a solution for power and area-sensitive clock generators due to its compact size and excellent energy efficiency. However, the degradation of reference spur in ILCMs presents a challenge for achieving great performance in low-voltage operations.

In this thesis, a RO-based near-threshold ILCM with an edge-selective error detector (ESED) is proposed. The ESED decouples the effect of pulse distortion, which causes reference spurs in ILCMs, from the frequency tracking path, enabling more accurate frequency tracking. Additionally, the ESED operates at a lower frequency compared to prior art, and employs a shared single detection path, resulting in significant reductions in power and area.

The proposed RO-based near-threshold ILCM is fabricated in a 28nm CMOS process and occupies an area of 0.0097mm². It is measured at supply voltages of 0.4V and 0.5V, and generates output clocks of 300MHz and 1.00GHz, respectively. When the proposed ESED is activated, an integrated jitter of 11.7ps$_{RMS}$ and 2.58ps$_{RMS}$ and a reference spur of -62dBc and -54dBc are obtained, respectively, along with FoMs of -231dB and -239dB.

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# Chapter 1

# Introduction

## 1.1 Motivation

The use of low-voltage ring oscillator (RO)-based phase-locked loops (PLLs) for battery-operated systems is a promising approach due to their compact size and good energy efficiency [1, 2, 3]. However, conventional PLL loop bandwidth is highly susceptible to variation at a low supply voltage, making it difficult to consistently suppress phase noise in the RO. In contrast, the Injection-Locked Clock Multiplier (ILCM), specifically the Multiplying Delay-Locked Loop (MDLL) with constant injection strength of 1, offers a potential solution by achieving a wide phase noise suppression bandwidth consistently. From these advantages, this thesis presents a low-voltage RO-based ILCM employing an Edge-Selective Error Detector (ESED) to improve its jitter performance. The ESED decouples

the effect of pulse distortion, which causes reference spurs in ILCMs [4, 5], from the frequency tracking path, allowing more accurate frequency tracking. Furthermore, the ESED operates at a lower frequency compared to [4, 5], and utilizes a shared single detection path, resulting in significant reductions in power and area.

# 1.2 Thesis Organization

The thesis is organized as follows. Chapter 2 discusses the phase noise characteristics of ILCM and provides a summary of prior art.

Chapter 3 presents the proposed near-threshold ILCM architecture and implementation, analyzes circuit mismatch in near-threshold operation, and details the proposed edge-selective error detector.

Chapter 4 presents the measurement results of the proposed ILCM and verifies its operation. The performance of the ILCM is evaluated in terms of key parameters, including phase noise, integrated jitter, power consumption, reference spur level, and figure of merit (FoM).

Chapter 5 summarizes the thesis and presents the conclusions.

# Chapter 2

# Injection-Locked Clock Multipliers

## 2.1 Phase Noise Analysis for ILCM

ILCM periodically removes the accumulated thermal noise of the oscillator using a clean reference clock, so it has excellent phase noise performance. As such, many studies have been conducted to quantitatively analyze the phase noise of periodically realigned oscillators, and it can be cartegorized into two types. First, there is a method of analyzing a circuit by obtaining a noise transfer function after modeling it with a linear system [6, 7, 8].

Second, there is a method of analyzing the phase noise by modeling the output jitter as a discret-time random process [9, 10]. Since analysis is performed in the discrete-time domain, approximation is unnecessary, and accurate phase noise can be obtained even in a low division ratio. Figure 2.1 is a schematic of the output jitter sequence of ILCM modeled in the second method. Here, we define the

output jitter sequence of ILCM as **x**, and define two main noise sources, injected reference clock jitter and oscillator's accumulated thermal noise as **y** and **z**, respectively. Since **y** and **z** are independent, **x** can be represented as the sum of them. Therefore, the bar graph representing the variance of jitter in the figure has a value of **y** plus **z**. The line shown above the bar graph is an example of a jitter sequence that appears in the time-domain.
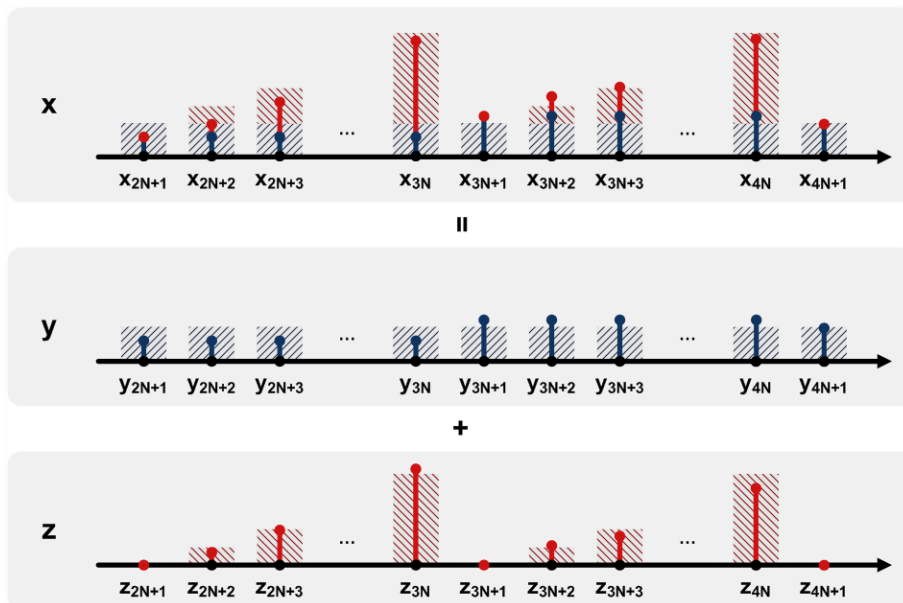


Figure 2.1 Illustration of the output jitter sequence. The bar graph and the lines on the bar represent the variance and the realization, respectively. **x** is output jitter sequence consisting of injected reference noise **y** and oscillator's accumulated noise **z**.

Assuming that **y** and **z** are additive white Gaussian noise, **x** is as follows.

$$\mathbf{x} = \left( y_1 + z_1, \dots, y_1 + \sum_{k=1}^{N} z_k, y_2 + z_{N+1}, \dots y_2 + \sum_{k=N+1}^{2N} z_k, \dots \right).$$

By taking Fourier transform for time-averaged autocorrelation function of **x**, the power spectral density can be obtained as follows.

$$S_{xx}(\omega) = \frac{\sigma_{ref}^2}{2} \sum_{k=0}^{N-1} \frac{1}{N} \cdot \frac{\sin\left(\omega k + \frac{\omega}{2}\right)}{\sin\left(\frac{\omega}{2}\right)} + \frac{\sigma_{osc}^2}{2} \sum_{k=0}^{N-1} \frac{N-1}{N} \cdot \frac{\sin\left(\omega k + \frac{\omega}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}.$$

In this model, $\sigma_{ref}^2$, $\sigma_{osc}^2$ represent the variance of **y** and **z**, respectively. Figure 2.2 is a graph comparing the modeled phase noise for various divide ratio N. The bandwidth of the ILCM is $0.4f_{ref}$, which is higher than conventional PLLs and results in in-band noise that is approximately 8 dB lower. Consequently, it is possible to efficiently reduce the phase noise of the RO.
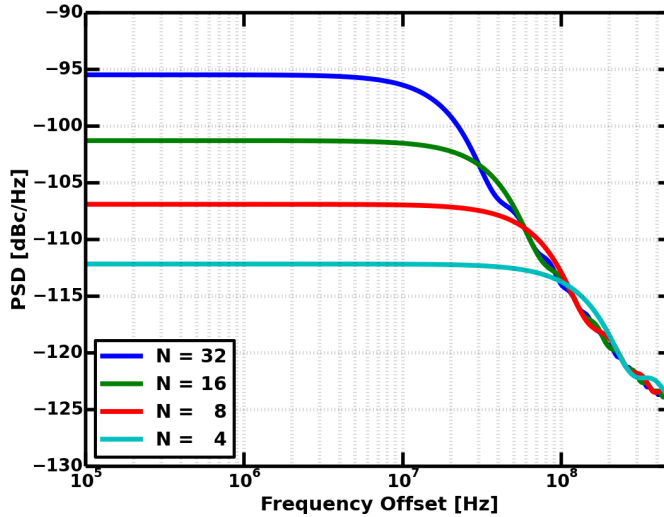


Figure 2.2 Estimated phase noise of an ILCM.

# 2.2 Prior Art

ILCM can effectively suppress the phase noise of the oscillator, but even with a small frequency error, it can generate a high level of reference spur [11, 4]. When there is a frequency error $f_{err}$, high-level frequency distortion is periodically generated by injection. At this time, the distortion index of the reference clock frequency is $2N \cdot |f_{err}/f_{VCO}|$, and a reference spur of $20 \log(N \cdot |f_{err}/f_{VCO}|)$ is generated. To solve this, various calibration loops to minimize frequency error have been proposed.

If the structure of the PLL is used as is, as shown in Figure 2.3 (a), a static phase error occurs, causing the lock to an inaccurate frequency. As can be seen in the timing diagram in Figure 2.3 (b), the two clocks compared in the PD include delays caused by the frequency of $CLK_{DIV}$ and those generated in the injection path. As a result, even though the loop is locked with the two inputs of the PD, $CLK_{DIV}$ and $CLK_{REF}$, aligned, there can still be a frequency error in $CLK_{OUT}$.



**(a)**

**(b)**
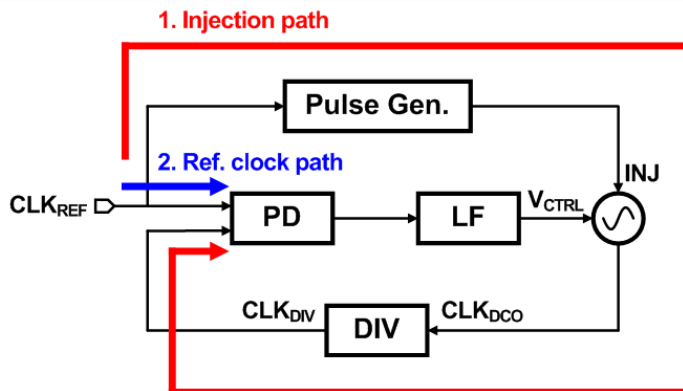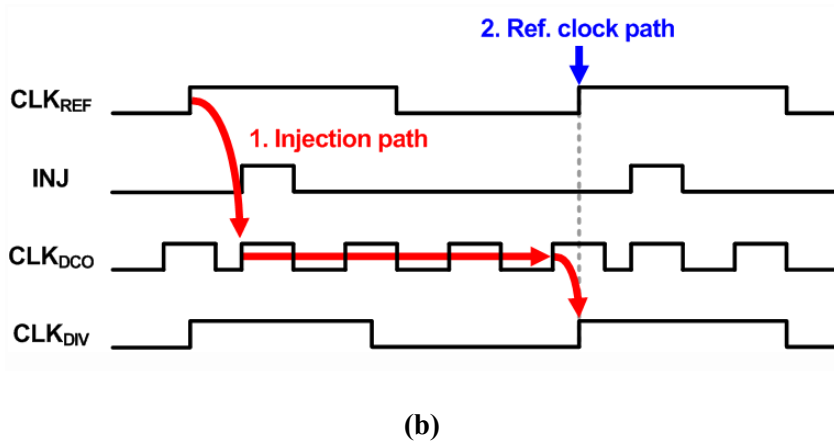
Figure 2.3 (a) Block diagram and (b) timing diagram of ILCM with a PLL-based calibrator.

Several structures have been studied to eliminate static phase error. In [12], the frequency was tracked by using a replica VCO and controlling the frequency of the main VCO with the same control voltage. In [13], the static phase error was suppressed by using a replica delay cell. However, the replica cell is vulnerable to mismatch, limiting the accuracy of frequency tracking. Additionally, power efficiency is compromised due to the power used in the replica cell.
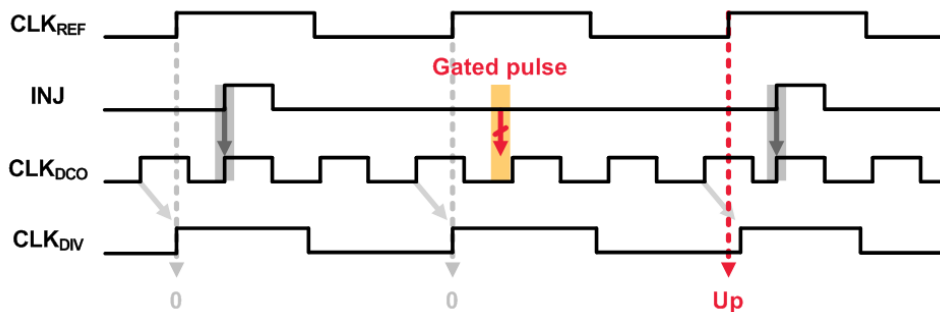


Figure 2.4 Timing diagram of pulse gating technique for detecting phase error.

[11, 14, 15] proposed structures for phase error background calibration. [14, 15] observed the difference between the cases when the injection occurred and when it did not by periodically gating the reference clock, and calibrated the phase error using this information. Figure 2.4 is a timing diagram that tracks phase offset using pulse gating. In the first and second reference clocks, there is a frequency offset, but it can be seen that the PD output is 0 due to the phase error. After the injection is gated in the second reference clock, its effect is reflected in the rising edge of the third $CLK_{DIV}$. Therefore, the PD output can cause an up, and this information can be used to calibrate the phase error.

[11] proposed a continuous frequency tracking technique that detects frequency and phase error by comparing the output clock of ILCM and the clock delayed by two cycles. Figure 2.5 represents the timing diagram of the continuous frequency tracking loop. The frequency error is detected at the edge where injection occurs and the following edge, while the phase error is detected at the remaining edges, making it a way to detect the error without pulse gating.
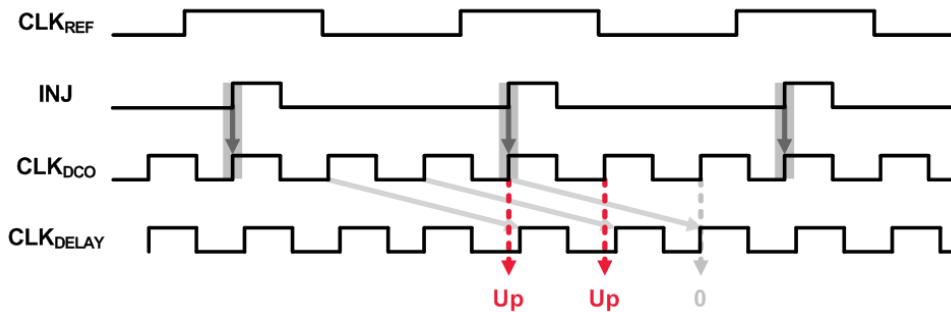


Figure 2.5 Timing diagram of continuous frequency tracking loop.

If the slope of the reference clock changes or there is a mismatch in the injection path, the clock period immediately after the injection will temporarily change. After the frequency and phase errors are removed, nonideality in the injection path has become the main cause of spur performance degradation [4, 16]. Figure 2.6 is the injection path nonideality tracking technique proposed in [4, 16]. In [4], an additional calibration loop was constructed using an edge where the continuous frequency tracking technique was modified to detect the effect of injection path nonideality. In [16], the continuous frequency tracking technique was also used, but it compared different edges to detect the injection path nonideality and reduced the range of the delay line.
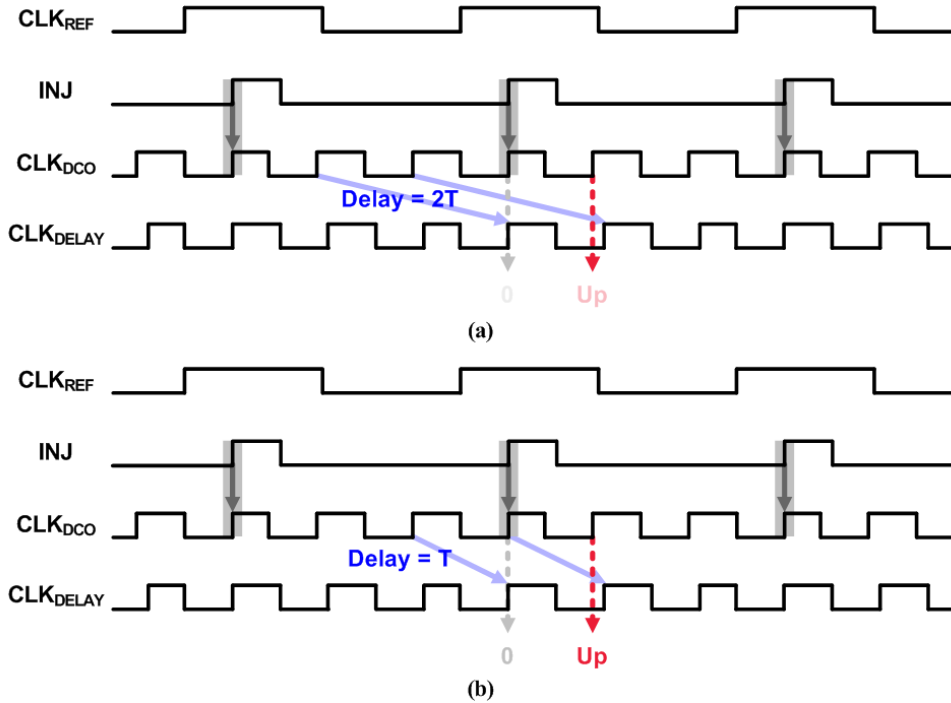
Figure 2.6 Timing diagram of injection path nonideality detection: (a) [4], (b) [16].

# Chapter 3

# Design of Near-Threshold ILCM

## 3.1 Design Considerations

Figure 3.1 compares the advantages and disadvantages of low-voltage opera-
tion and RO-based ILCM. The circuit operating at low voltage can achieve excel-
lent power efficiency as both static power and dynamic power are reduced. How-
ever, due to the increase of the impact from mismatch and degradation of SNR,
[17], consideration of this factor is necessary.

RO-based ILCM is a promising solution for battery-operated systems, given
its small size and improved energy efficiency. Additionally, it offers a wider band-
width than conventional PLLs and is more resistant to PVT variations, allowing
for effective suppression of phase noise in the RO. However, compensation is
necessary to address the high reference spur that occurs in ILCM.
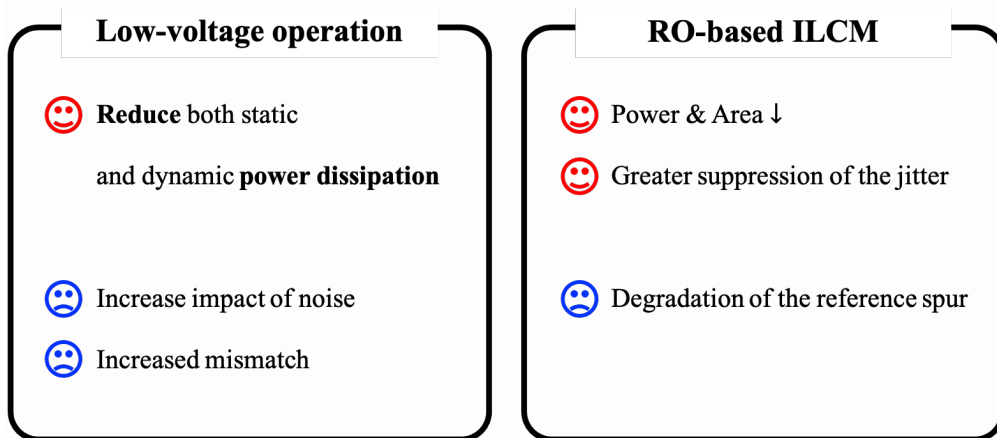
Figure 3.1 Pros and cons of low-voltage operation and ring oscillator-based ILCM.

Designing an RO-based ILCM that operates at low-voltage can effectively compensate for the phase noise characteristics that are degraded at low voltage. However, as the impact of mismatch increases and worsens the reference spur level of the ILCM, it is very important to compensate it.

In this thesis, two design considerations are made. Firstly, the design aims to maximize the advantages of low voltage operation and RO-based ILCM by enhancing power efficiency, reducing area, and improving integrated jitter performance relative to conventional RO-based PLLs. Secondly, a near-threshold voltage architecture is designed to improve reference spur characteristics.

# 3.2 Injection Path Nonideality

Injection path nonideality not only causes reference spurs but also affects other calibration loops, resulting in secondary spur performance degradation. Particularly in the case of ILCMs that operate at low voltages, spur performance is more seriously degraded due to the intensifying nonideality, making analysis and improvement necessary. In this chapter, both the spurs directly generated by the injection path nonideality and the spurs indirectly generated by the conventional frequency tracking loop are analyzed. Moreover, it will be explained how the proposed edge-selective error detector (ESED) solves this problem.

## 3.2.1 Two Modes of Oscillation in ILCM

To analyze the impact of injection path nonideality, the operating state of the oscillator can be classified into two categories: steady-state and distorted state. Figure 3.2 uses a multiplexed ring oscillator (muxed-RO) to demonstrate these two states. The upper figure, steady-state, occurs when injection does not occur for a long time and the operating condition of the oscillator is maintained the same, resulting in a constant steady-state period T. The figure in the middle, distorted state, occurs when the reference clock is injected and the operating condition changes from steady-state, resulting in a distorted period $T-\tau_{ERR}$. As shown in the timing diagram, the muxed-RO operates in the distorted state immediately after injection and gradually converges to the steady-state over time.
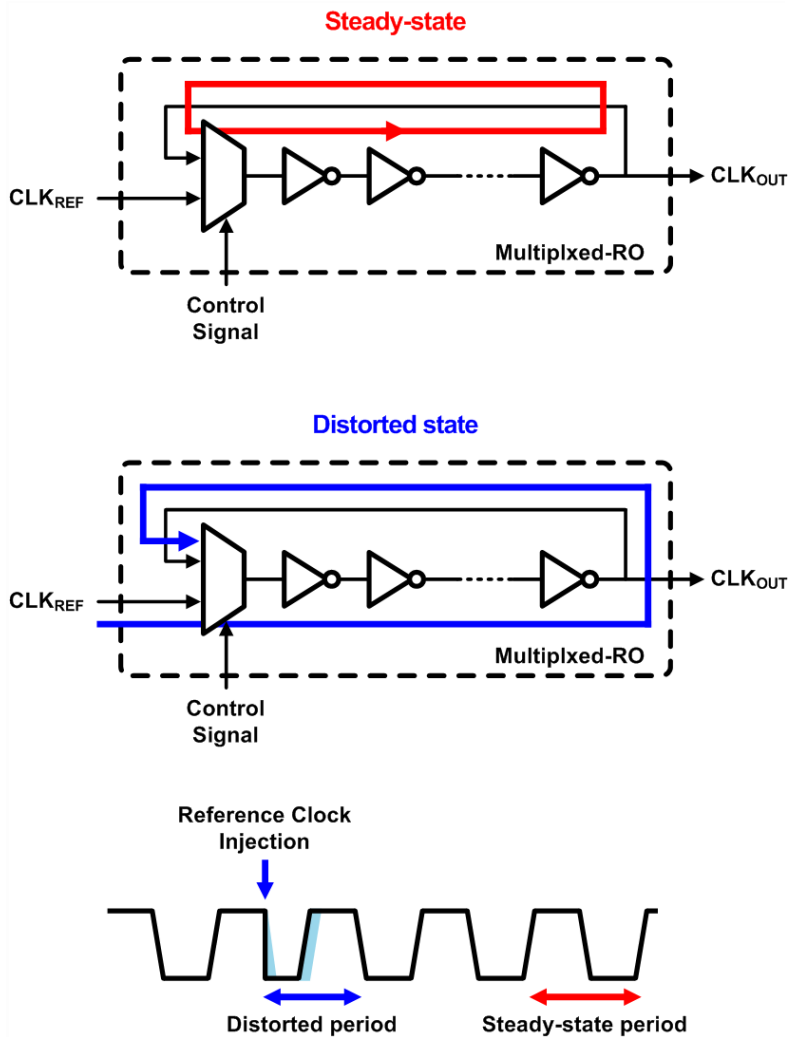
Figure 3.2 Two modes of oscillation in ILCM and corresponding timing diagram.

There are two main causes for the period difference in the steady-state and distorted state. Firstly, there is a mismatch between the two input paths of the mux, and the slope and waveform of $CLK_{REF}$ and $CLK_{OUT}$ are different, resulting in a difference in the driving strength. Secondly, the charging of the mux intrinsic capacitor changes as the control signal transitions from on to off. This results in a change in propagation delay and a subsequent distortion of the period. Both of these causes are influenced by PVT variations, so calibration must be made using a background calibration loop.

## 3.2.2 Impact of Pulse Distortion on Conventional Frequency Tracking Loop

In conventional frequency tracking loop, pulse distortion can negatively impact the accuracy of the frequency tracking. The detailed effect of pulse distortion on the loop is shown in Figure 3.3. In this figure, the period of the oscillator is ideal ($T = T_{REF}/N$), and injection causes a delay of $-\tau_{ERR}$ in the edge immediately following the injection. This delay also affects all subsequent edges, but the next injection occurs after $T_{REF}$, resulting in a period of $T+\tau_{ERR}$ immediately preceding the injection. As a result, the BBPD detects $\tau_{ERR}$, causing inaccurate frequency locking. The timing diagram in Figure 3.3 (c) depicts the locking of the conventional frequency tracking loop under the impact of pulse distortion. The offset of $\tau_{ERR}/N$ in each period of $CLK_{OUT}$ can be seen to result in a zero PD output. Thus, every injection results in deterministic jitter of $\frac{N-1}{N}\tau_{ERR}$ and additional jitter of $\frac{1}{N}\tau_{ERR}$ is generated at each cycle.

To address this issue, ILCMs that calibrate pulse distortion have been proposed in [4] and [5]. However, to achieve accurate frequency tracking, it must be completely calibrated without any residual error. This requires a fine resolution DAC, which is particularly challenging in low-voltage design.
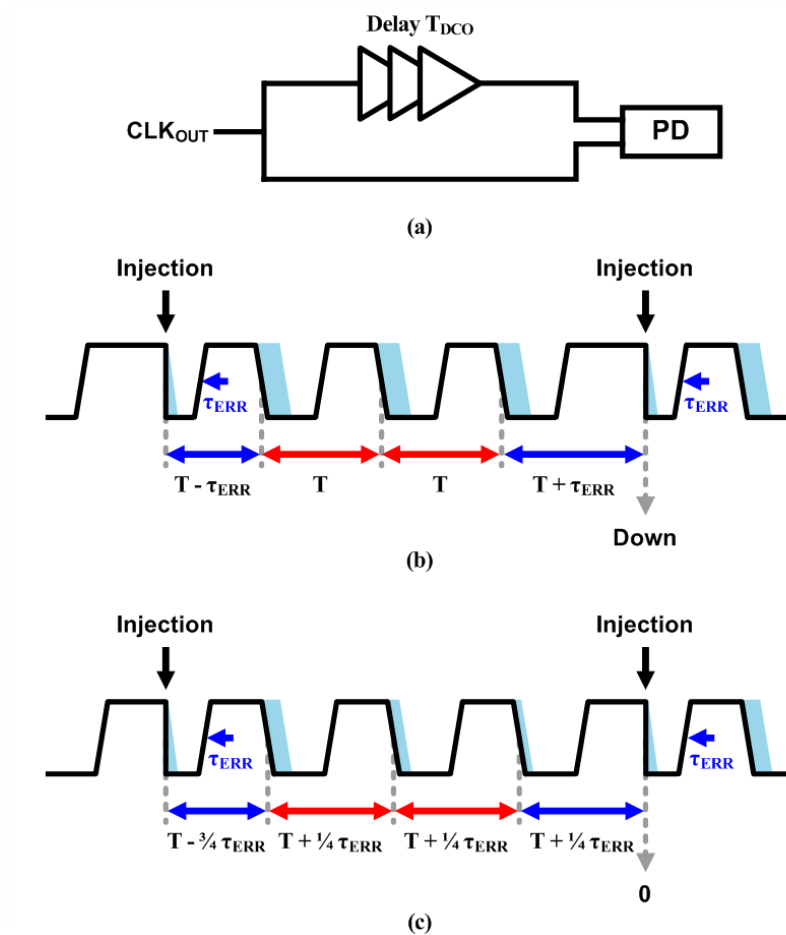


Figure 3.3 The effect of pulse distortion on conventional frequency tracking loop: (a) block diagram of the tracking path, (b) timing diagram with an ideal period, (c) timing diagram illustrating the lock condition of the tracking loop.

### 3.2.3 Proposed Edge-Selective Error Detector

In this chapter, an edge-selective error detector that effectively decouples the impact of pulse distortion on the frequency tracking loop is proposed. This allows for more accurate frequency tracking and makes it possible to achieve low spur levels even with coarse resolution DACs, thereby mitigating the requirements for low-voltage design.
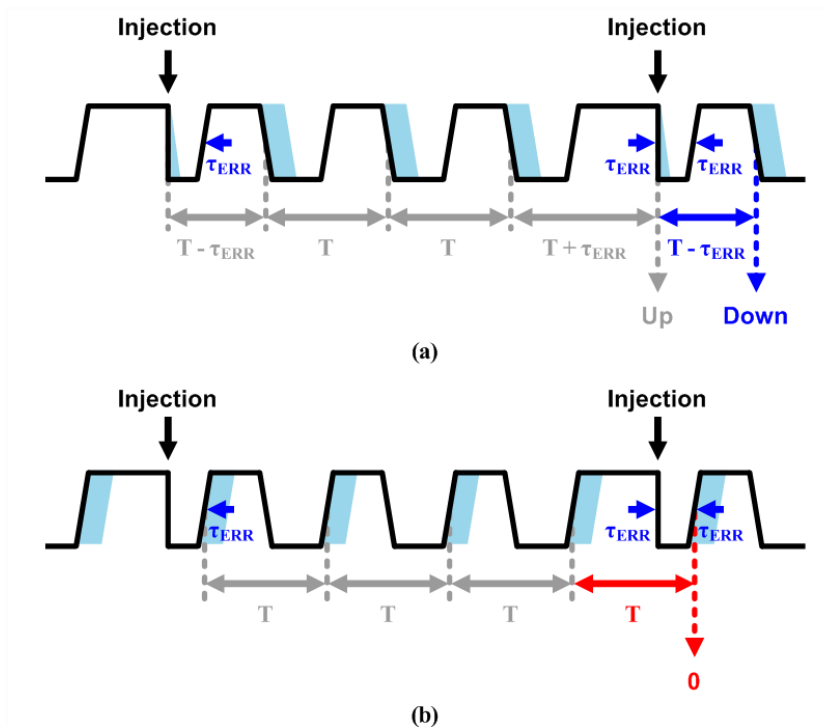


Figure 3.4 Output clock timing diagram with ideal period. (a) period based on falling edges. (b) period based on rising edges.

The ESED tracks frequency errors using rising edges and pulse distortions using falling edges. This technique is based on the observation that the direction of the edges determines the type of error information being conveyed.

The rising edges in a direction opposite to the injected edges are not affected by pulse distortion, thus enabling accurate frequency tracking. As demonstrated in Figure 3.5(a), the rising edge preceding the injected edge experiences a delay of $-\tau_{ERR}$ due to distortion. However, the rising edge following the injection also experiences the same delay. As a result, the effect of pulse distortion is canceled out, enabling accurate frequency tracking using the rising edges before and after the injection. In contrast, the ESED detects pulse distortion by reversing the direction of the edge. As shown in Figure 3.5(b), the period after injection is always $T-\tau_{ERR}$. Thus, the distortion can be detected by comparing the delay between the falling edges immediately following the injection and the average clock period T.

It is important to note that for the proposed ESED to function effectively, it is necessary for the pulse distortion to affect only the edge immediately following the injection. To ensure this requirement, a 9-stage oscillator including multiplexing stage has been designed. This oscillator restores the steady-state period before subsequent edges occur.

# 3.3 Proposed ILCM Architecture
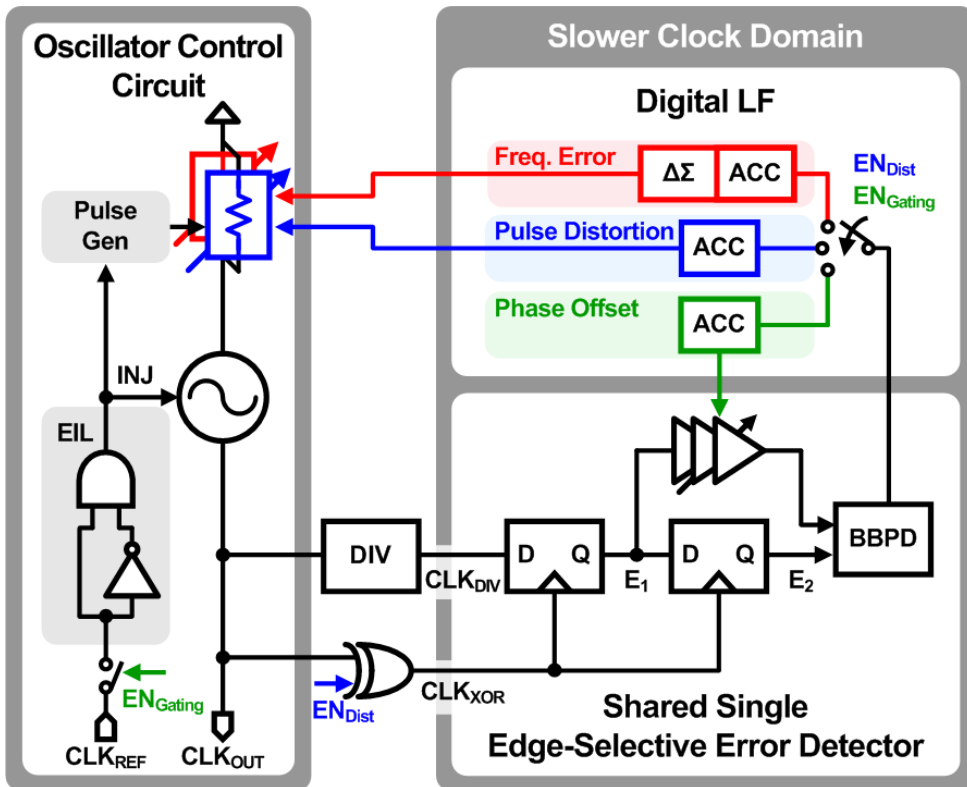


Figure 3.5 Overall block diagram of proposed near-threshold ILCM.

Figure 3.6 shows the block diagram of the proposed ILCM in this thesis. The architecture can be cartegorized into three main parts: the oscillator control circuit, the shared single edge-selective error detector, and the digital loop filter. It is noteworthy that despite the presence of three calibration loops in the ILCM, a single shared error detector is employed. Furthermore, the ESED operates at a

slower frequency compared to prior art [4-5]. These result in several advantages including a reduced operating speed (N times slower), a DCDL with a 1/2 narrow delay range compared to [4], and fewer DCDLs and PDs with 1/3 and half the operating speed of [5].

The oscillator control circuit consists of a digitally controlled oscillator (DCO), an edge injection logic (EIL), and a pulse generator. The EIL generates the signals for injecting a reference clock by detecting the $CLK_{REF}$. Once the signals are generated, the pulse generator produces a pulse that enables the DCO's pulse distortion calibration path. Additionally, an $EN_{Gating}$ signal is used to control whether to inject the $CLK_{REF}$ into the DCO by disabling the path from $CLK_{REF}$ to EIL.

The error detection circuit consists of a divider, edge detector, digitally controlled delay line (DCDL), and phase detector (PD). The divider receives the $CLK_{OUT}$ and outputs the divided clock signal, $CLK_{DIV}$. The edge detector selects the required edges to implement the proposed ESED, and outputs the result. The selection of edges is controlled by an XOR gate placed at the front end of the edge detector, with the digital block sending out the $EN_{Dist}$ signal to control the XOR gate. The DCDL and PD detect the difference between the two outputs of the edge detector, and send the result on to the digital loop filter.

The digital loop filter regulates the frequency and pulse distortion calibration DACs of the DCO, as well as the DAC of the DCDL. Additionally, it generates signals for controlling the type of error to be detected.

## 3.3.1 Frequency and Phase Error Calibration Loop
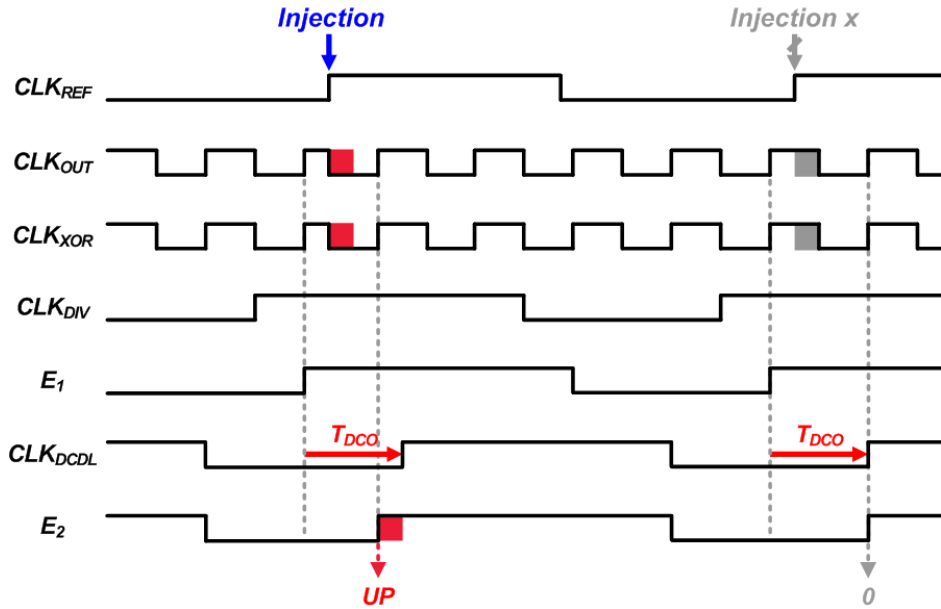


Figure 3.6 Timing diagram of frequency and phase error calibration loop.

The ESED tracks frequency errors by observing the rising edges that occur before and after the injection. The ILCM proposed in this thisis controls the signals to accurately capture these edges as depicted in the timing diagram in Figure 3.7. The $CLK_{OUT}$ is divided by the divide ratio N using the divider, which results in the $CLK_{DIV}$ becoming $V_{DD}$ at the falling edge of $CLK_{OUT}$ just prior to the injection. The direction of the $CLK_{OUT}$ transition is processed by the XOR gate, which is controlled by the $EN_{Dist}$ signal, and the resulting signal is referred to as $CLK_{XOR}$. Finally, the edge detector receives the $CLK_{DIV}$ and $CLK_{XOR}$ signals.

When the frequency and phase error tracking is executed, the $EN_{Dist}$ signal is set to $V_{SS}$ to maintain the direction of $CLK_{OUT}$'s transition. This enables the edge detector to capture the rising edges of $CLK_{OUT}$. The rising edges that occur after the transition of $CLK_{DIV}$ are then output as $E_1$ and $E_2$, respectively. To align the clocks, the DCDL delays $E_1$ by $T_{DCO}$, which represents one period of $CLK_{OUT}$. Finally, the PD compares the two signals.

The timing diagram in Figure 3.7 represents the case where the DCO frequency is slower compared to the target frequency. As a result of the frequency error, the rising edge preceding the injection occurs later than its ideal position and the delay between the rising edges before and after the injection becomes shorter than $T_{DCO}$. In this case, the PD output UP to increase the frequency. On the other hand, when the DCO frequency exceeds the target frequency, the delay between the two rising edges becomes longer than $T_{DCO}$, causing the PD output DN and lowering the frequency of the DCO.

To fix the DCDL delay to $T_{DCO}$, the proposed ILCM uses a pulse gating method that skips the injection. As shown in the right timing diagram of Figure 3.7, when the injection is gated, two edges operating in the steady-state of DCO are output by the edge detector. The delay between these two edges is $T_{DCO}$, thus the DCDL delay can be calibrated by checking if delayed $E_1$ and $E_2$ are aligned.

## 3.3.2 Pulse Distortion Calibration Loop
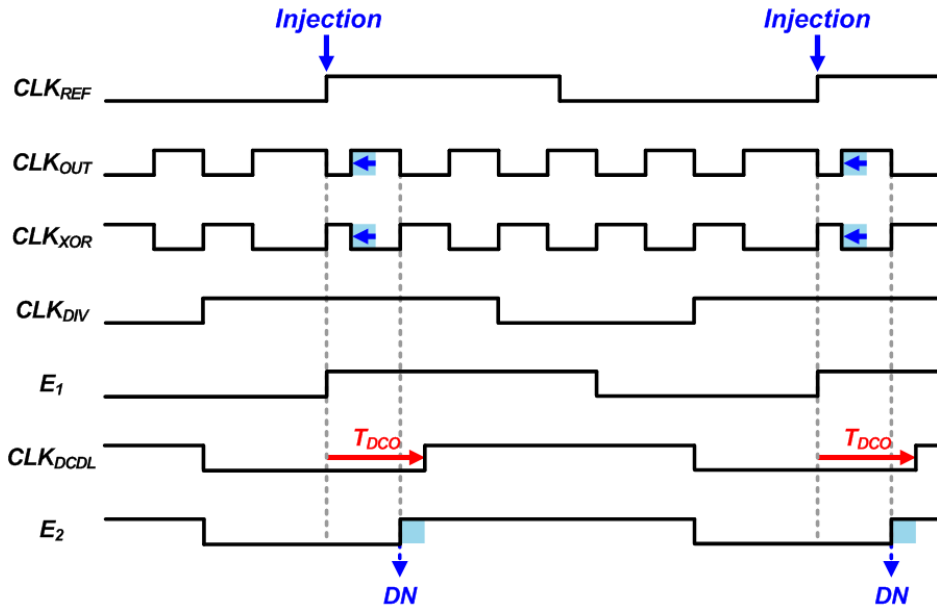


Figure 3.7 Timing diagram of pulse distortion calibration loop.

In the proposed ESED, falling edges after the injection are used to detect pulse distortion. By setting $EN_{Dist}$ to $V_{DD}$ to capture these edges, the XOR gate output is produced as the transition direction-reversed $CLK_{OUT}$. The falling edges of $CLK_{OUT}$ are then captured by the edge detector and output as $E_1$ and $E_2$, respectively. DCDL delays $E_1$ by $T_{DCO}$, and PD compares the delayed $E_1$ with $E_2$. As shown in Figure 3.8, if $\tau_{ERR}<0$, DN is output as the PD output to make the period after the injection longer, while in the opposite case, UP is output to make the period shorter.

The pulse distortion calibration loop shares the error detector with the frequency and phase offset calibration loop, enabling the minimization of mismatches in the detection path. As demonstrated in the results of post-layout simulation in Figure 3.9, the difference in delay when the $EN_{Dist}$ signal is $V_{SS}$ or $V_{DD}$ is less than 60 fs in all three corners (TT, FF, SS), which is considered negligible.
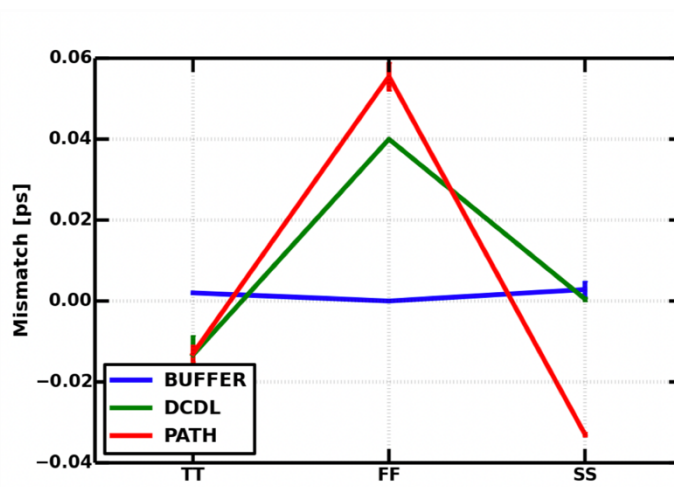


Figure 3.8 Path mismatch between rising edge triggered error-detection and falling edge triggered error-detection.

# 3.4 Circuit Implementation

In this chapter, the implementation details of the key components of the architecture, including the digitally controlled oscillator (DCO), divider, edge detector, and pulse generator, are discussed. The digitally controlled delay line (DCDL), phase detector (PD), and edge-injection logic (EIL) is designed with structures similar to those in [17] for DCDL and PD, and [4] for slope controller.

## 3.4.1 Digitally Controlled Oscillator (DCO)

The DCO consists of a core that performs clock multiplication and reference clock injection, and a frequency control and pulse distortion calibration DACs. The schematic of the DCO is shown in Figure 3.10 and is comprised of a mux and a seven-stage inverter chain. The SEL signal controls the mux, enabling the CLK$_{REF}$ input path when active and the internal clock input path when inactive.
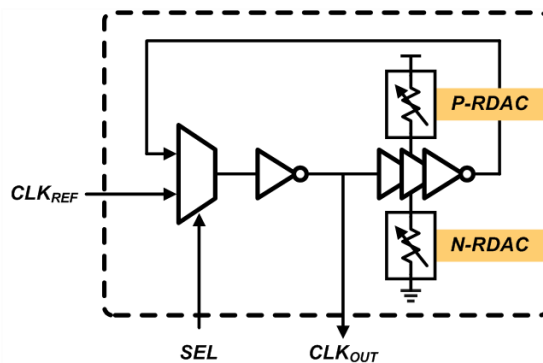


Figure 3.9 Implementation of digitally controlled ring oscillator.

In low-voltage operation, the input voltage in the inactive direction affects the delay of the mux. To minimize this effect, a pre-mux stage is designed to fix the mux input voltage of the inactive path to $V_{DD}$. Figure 3.11 shows the schematic and timing diagram of the mux composed of the pre-mux stage and the mux stage. When the injection is inactive, the mux input REF' on the injection path is maintained at $V_{DD}$. On the other hand, when SEL is activated, the mux input RO' on the RO clock path is maintained at $V_{DD}$. As a result, when a transition occurs on the enabled path, the opposite input of the mux is fixed at $V_{DD}$, and the mux delay is maintained. As a result, $CLK_{REF}$ is always injected with a constant delay.
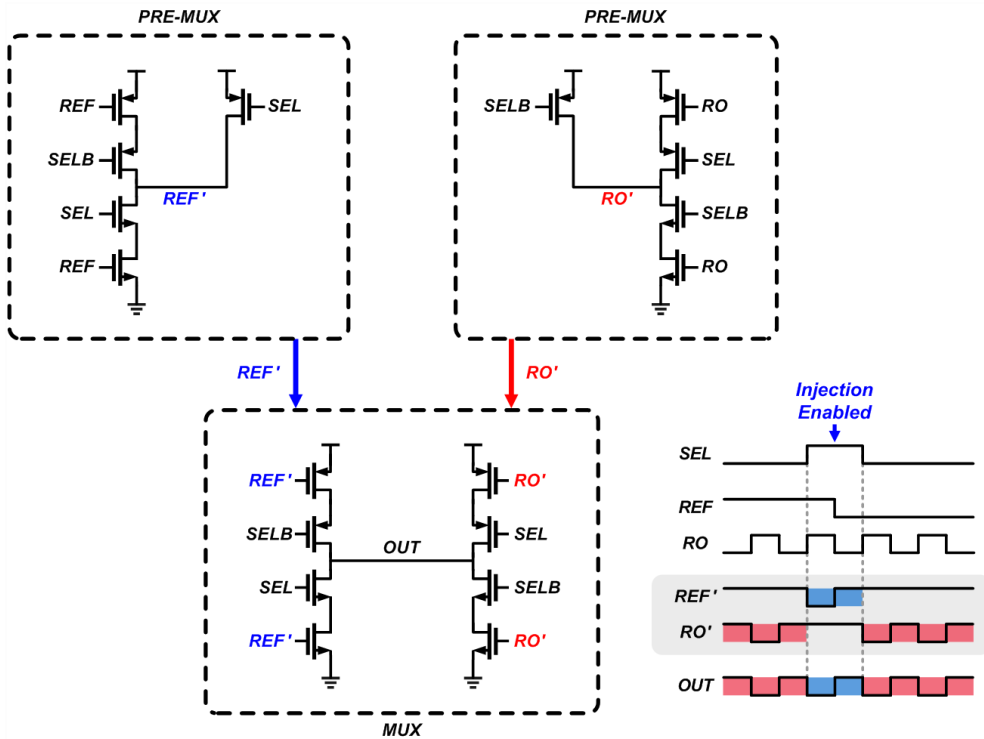


Figure 3.10 Schematic and timing diagram of the pre-mux stage and the mux stage.

The implementation of the DACs for calibrating the frequency and the pulse distortion is shown in Figure 3.12. The frequency is controlled by using a 16-bit coarse DAC and a 128-bit fine DAC, and both the P-RDAC and N-RDAC are used to ensure that the output common mode voltage is equal to $V_{DD}/2$.
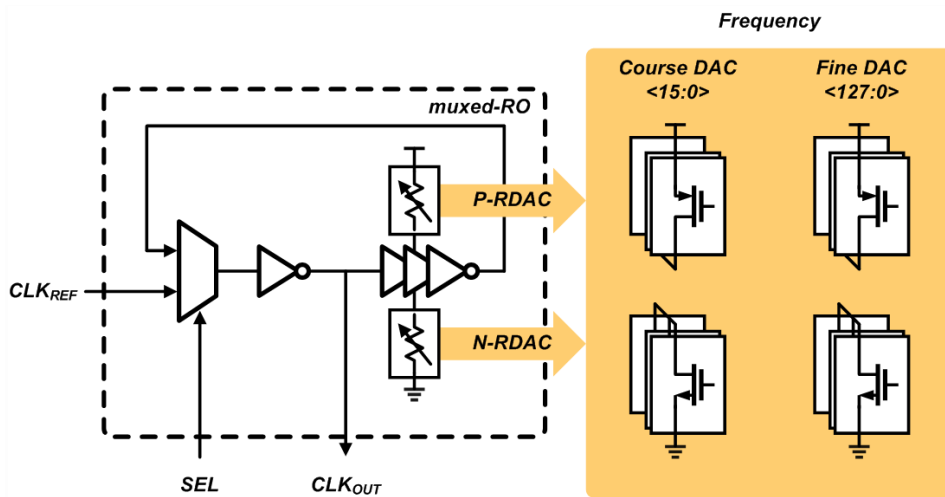


Figure 3.11 Implementation of digital-to-analog converter.

The P-RDAC is employed at the final inverter of the inverter chain to calibrate pulse distortion. Figure 3.13 illustrates the circuit schematic and timing diagram for driving the DAC. It controls the DAC by using two types of signals: a pulse signal that indicates an injection has taken place and the digital code $D_{PERIOD}<23:0>$. The lower 16 bits are controlled using NOR gates, as illustrated in Figure 3.13 (a), while the upper 8 bits are controlled using NAND gates. These gates compensate for $\tau_{ERR}<0$ and $\tau_{ERR}>0$, respectively, and as the value of $D_{PERIOD}$ increases, the period immediately after the injection decreases.

Figures 3.13(b) and 3.13(c) show the timing diagrams of the circuit's operation when digital control code $D_{PERIOD}$ is less than 16 and greater than or equal to 16, respectively. In Figure 3.13(b), the upper 8 bits of the DAC are maintained at $V_{DD}$, while the DAC with $D_{PERIOD}$ equal to 1 in the lower 16 bits is maintained at $V_{SS}$. When $D_{PERIOD}$ is 0 for the lower 16 bits, a pulse signal temporarily increases the period by pulling the DAC to $V_{DD}$. In Figure 3.13(c), the lower 16 bits of the DAC are maintained at $V_{SS}$, and the DAC with $D_{PERIOD}$ equal to 0 in the upper 8 bits is maintained at $V_{DD}$. When $D_{PERIOD}$ is 1 for the upper 8 bits of the DAC, a pulse signal pulls down the DAC to $V_{SS}$, and it is temporarily activated to decrease the period. As a result, when an injection occurs, the period increases the most when $D_{PERIOD}$ is 0 and decreases the most at 23.



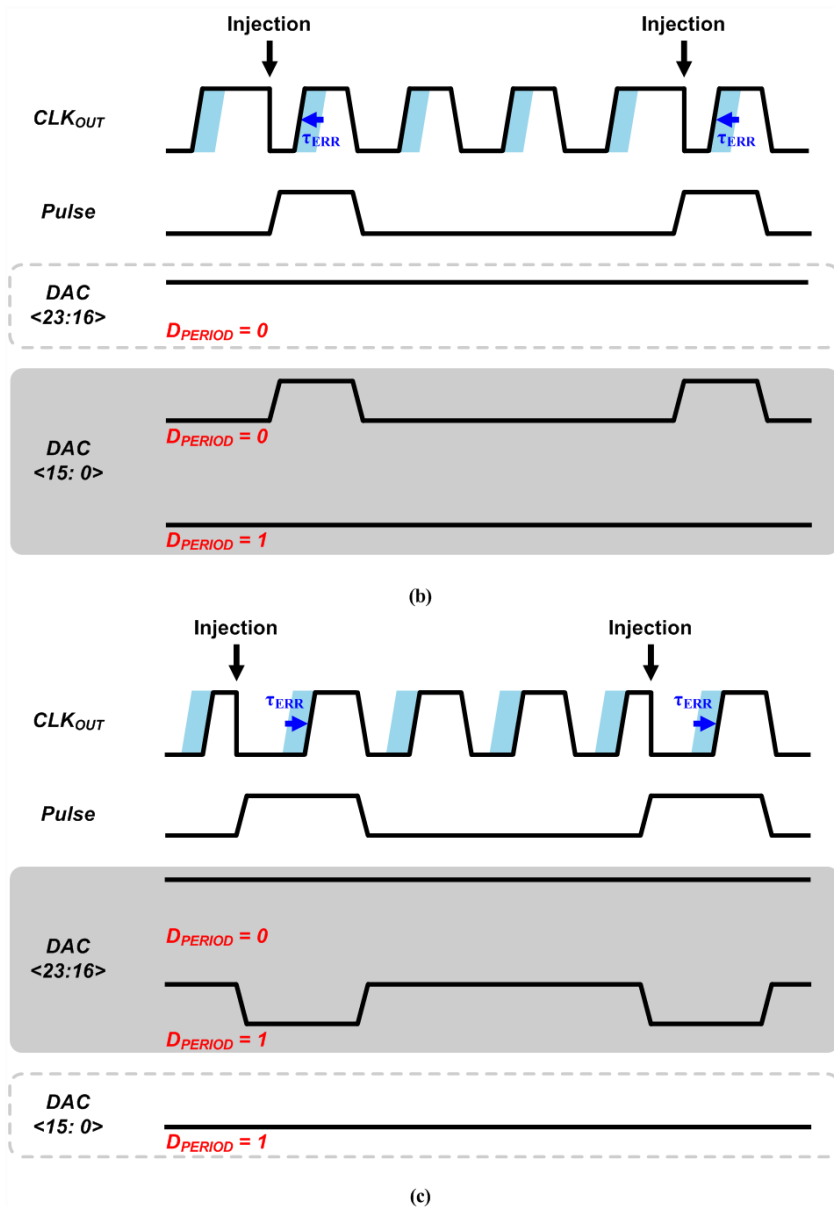| DAC <23:16> | | | | DAC <15: 0> | | |
|---|---|---|---|---|---|---|
| $D_{PERIOD}$ | Pulse | DAC | | $D_{PERIOD}$ | Pulse | DAC |
| 0 | 0 | 0 | | 0 | 0 | 1 |
| 0 | 1 | 1 | | 0 | 1 | 0 |
| 1 | 0 | 0 | | 1 | 0 | 0 |
| 1 | 1 | 0 | | 1 | 1 | 0 |
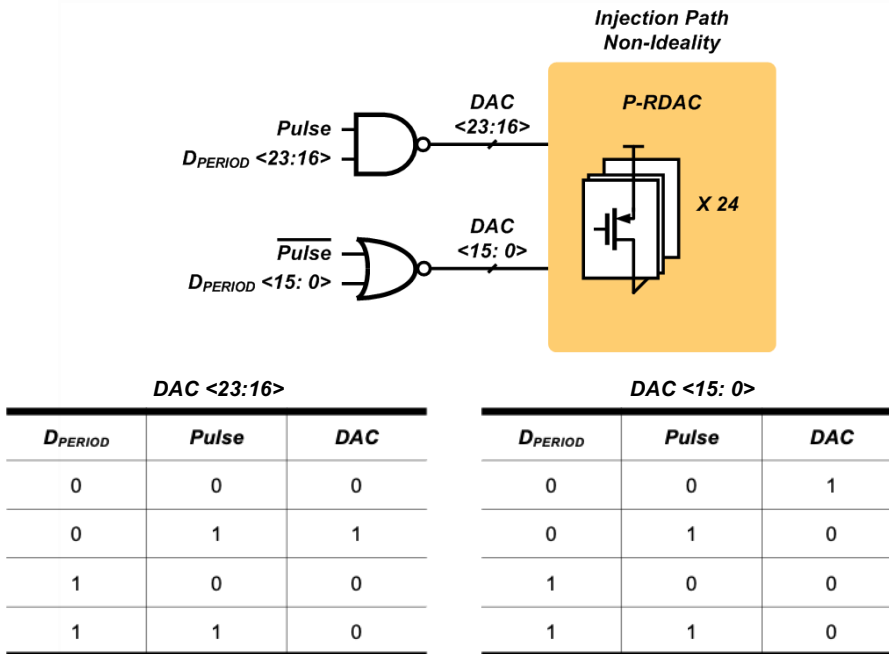
(a)

Figure 3.12 (a) Schematic of the pulse distortion calibration DAC and associated timing diagrams when (b) $D_{PERIOD} < 16$, and (c) $D_{PERIOD} \geq 16$.
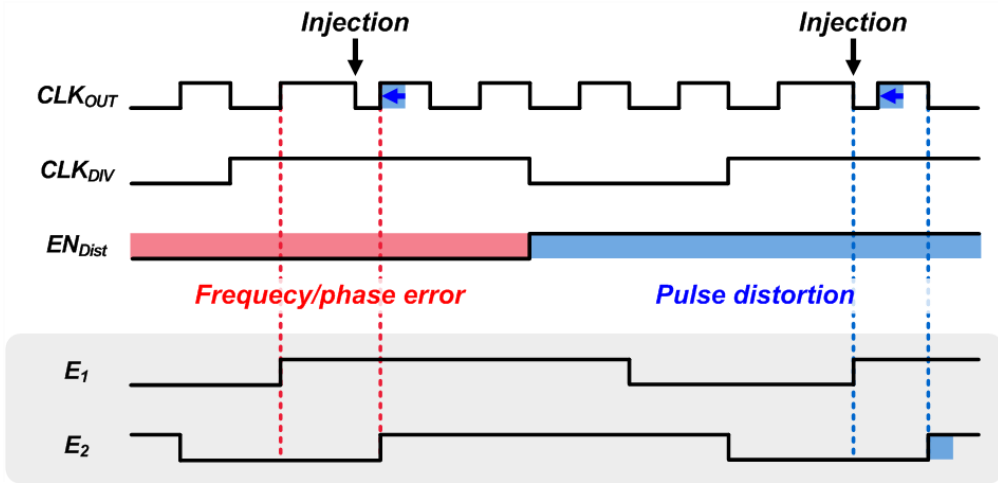
## 3.4.2 Divider and Edge Detector



Figure 3.13 Timing diagram of divider and edge detector.

In order to implement the proposed ESED, a circuit is needed to transmit the accurate edge selected to the inputs of error detector. The divider and the edge detector perform the role of selecting the required edge. Figure 3.14 is a timing diagram that shows how the two circuits operate. First, the output of $CLK_{DIV}$ changes to $V_{DD}$ at the falling edge just one cycle before the injection occurs in $CLK_{OUT}$. The edge detector then selects either the rising edge or the falling edge of $CLK_{OUT}$ after the rising edge of $CLK_{DIV}$ has occurred and outputs it as $E_1$ and $E_2$. It can be seen that when performing frequency and phase error tracking ($EN_{Dist}$: $V_{DD}$), the rising edge is selected, and when performing pulse distortion tracking ($EN_{Dist}$: $V_{SS}$), the falling edge is selected.
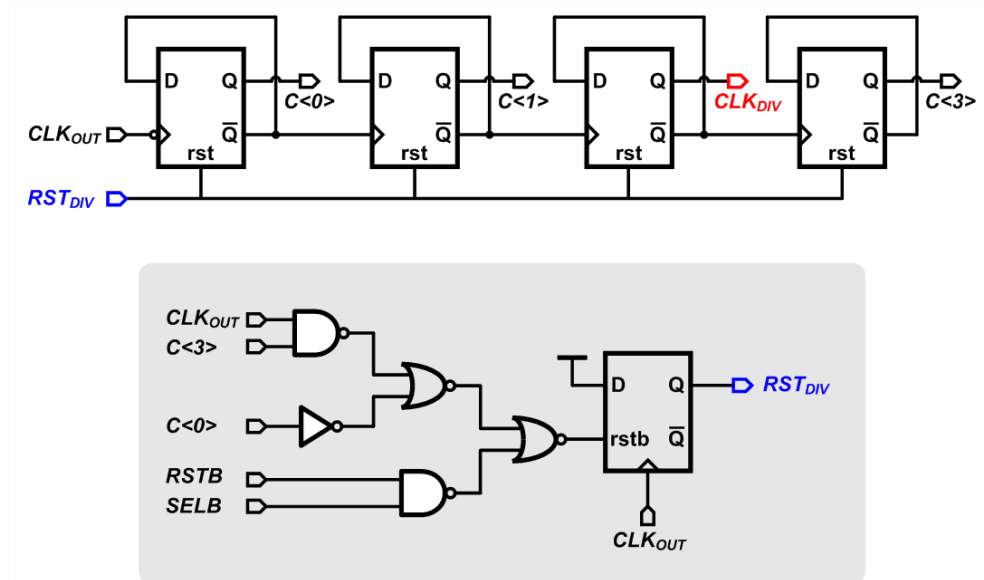
Figure 3.14 Implementation of divider with reset signal generator.

In the design of the divider, it is crucial to ensure that the divider output does not shift even by a single cycle, as this would result in the selection of an incorrect edge and an inaccurate lock. To address this concern, a divider with periodic reset has been designed. Figure 3.15 illustrates the schematic of the divider, which consists of four D flip-flops. The divider divides the $CLK_{OUT}$ and generates the $RST_{DIV}$ signal using the SELB signal, which indicates the injection. By resetting the divider with the $RST_{DIV}$ signal, the timing diagram in Figure 3.14 can be obtained. Additionally, an additional D flip-flop, not shown in Figure 3.15, was used to synchronize $CLK_{DIV}$ with $CLK_{OUT}$.
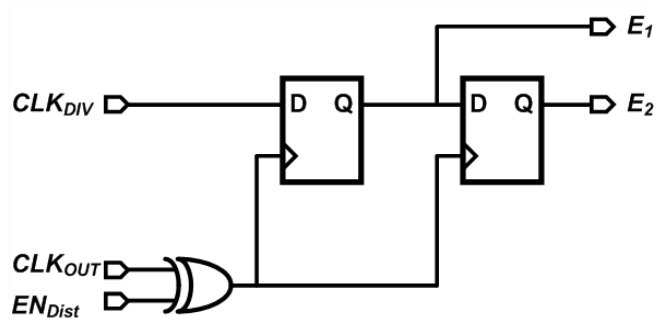
Figure 3.15 Implementation of edge detector.

Figure 3.16 shows the schematic of the edge detector. It converts the rising/falling edges of $CLK_{OUT}$ using an XOR gate and an $EN_{Dist}$ signal. By sampling $CLK_{DIV}$ with the converted clock, the required edge for error-tracking can be selected.

### 3.4.3 Pulse Generator



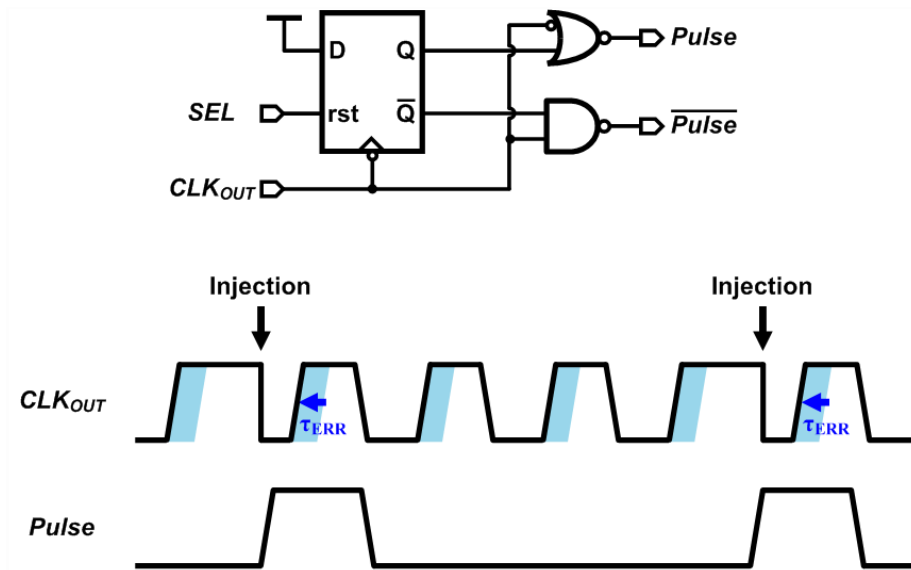Figure 3.16 Schematic and timing diagram of pulse generator.

A signal to indicate the injection is necessary for calibrating the pulse distortion. Figure 3.17 shows the schematic and timing diagram of the pulse generator which generates desired signal. The pulse is generated when the SEL signal, enabling the injection, occurs and is pulled down by the falling edge of $CLK_{OUT}$ after being maintained for one cycle.

# Chapter 4

# Measurement Results

The proposed ILCM is fabricated in a 28nm CMOS process. Figure 4.1 shows a chip micrograph and layout, occupying an active area of 0.0097mm$^2$. The ILCM generates an output clock of 300MHz at 0.4V supply and 1GHz at 0.5V supply, achieving a power efficiency of 184uW/GHz and 171uW/GHz, respectively.
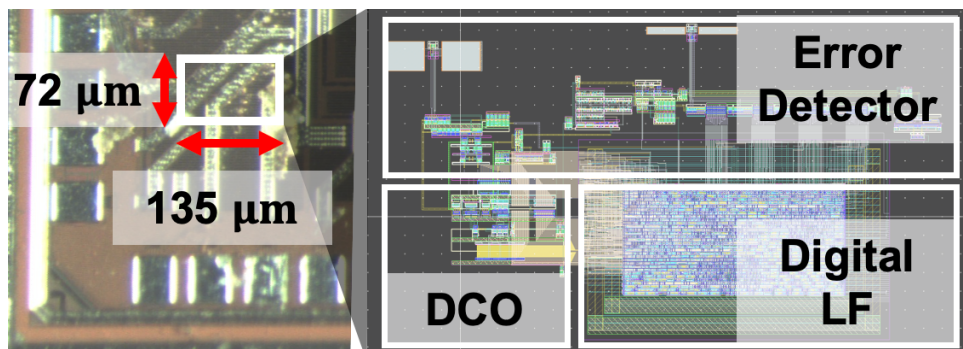


Figure 4.1 Chip micrograph and layout.

Figure 4.2 shows the measurement setup used to measure the chip, including the supply voltage, current bias, I2C signal, reference clock, and the output clock produced by the ILCM. The DC power supply provides 5V voltage and Gnd to the power regulation board, which converts them and delivers to the chip through the LDO. The current bias is generated using a variable resistor and supplied to the chip. The I2C signal, generated at 3.3V by Raspberry Pi, is transmitted to the power regulation board, where it is converted to 0.9V by the level shifter before being delivered to the chip. The reference clock is generated by the BERT and sent to the chip, and the output clock produced by the chip is measured using the UXA Signal Analyzer.
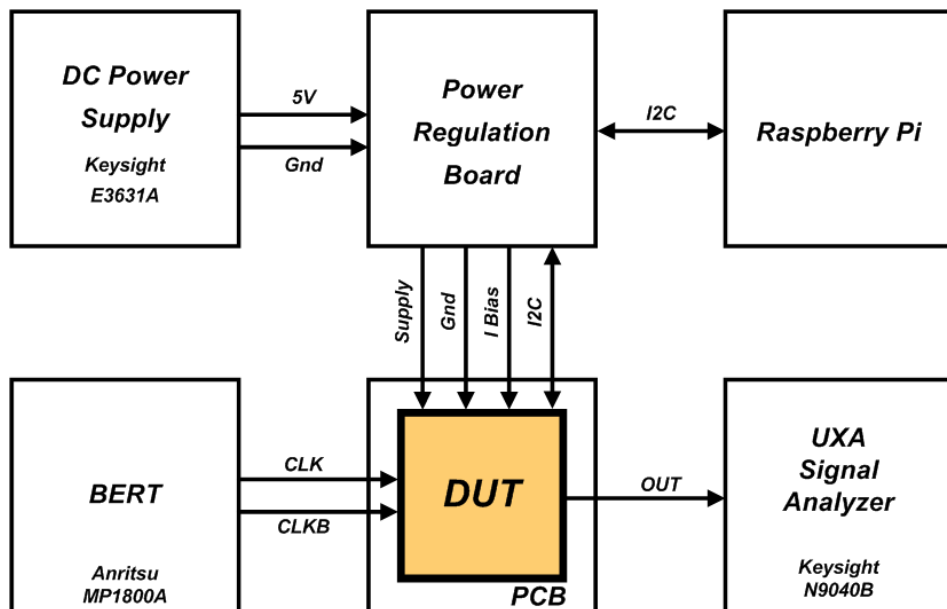


Figure 4.2 Measurement setup.
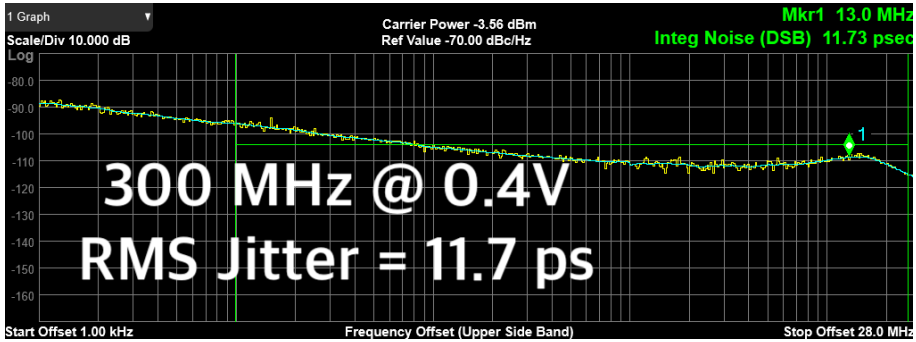
**(a)**
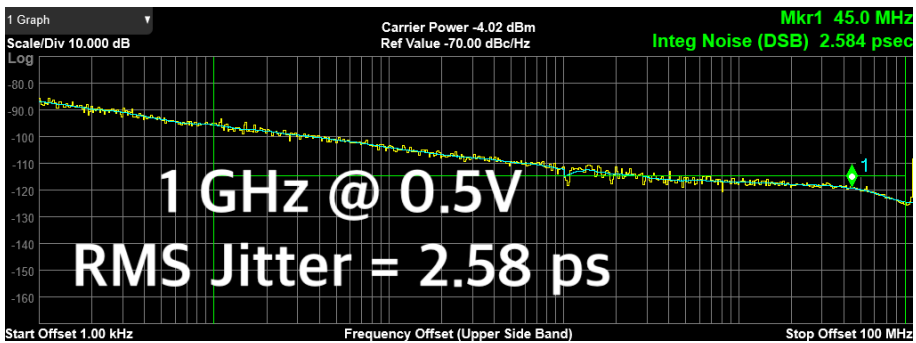


**(b)**

Figure 4.3 Measured phase noise when the proposed ESED is enabled.

(a) 0.4V supply and (b) 0.5V supply.

Figure 4.3 presents the measured phase noise when the proposed ESED is activated. The RO phase noise is effectively suppressed with a wide bandwidth, resulting in excellent RMS jitter performance of 11.7ps$_{RMS}$ and 2.58ps$_{RMS}$ at 0.4V supply and 0.5V supply, respectively.
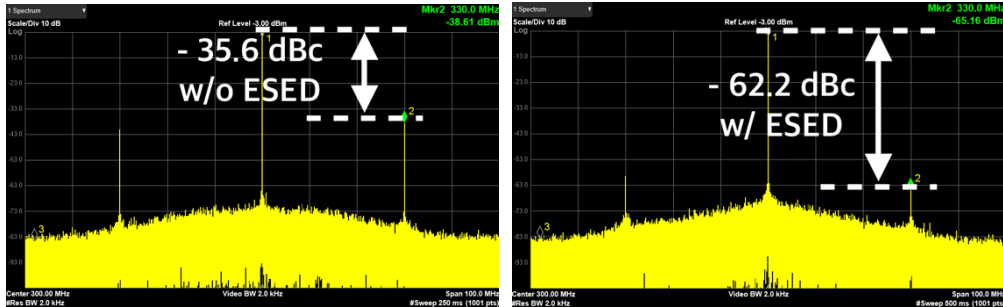
**(a)**
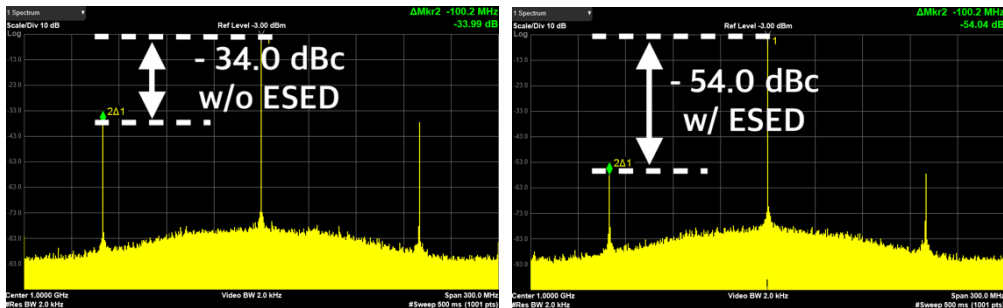


**(b)**

Figure 4.4 Measured spectrum when the proposed ESED is disabled and enabled.

(a) 0.4V supply and (b) 0.5V supply.

Figure 4.4 presents a comparison of the measured output spectrums of the ILCM. The reference spur levels, observed when only injection is active, are -35.6dBc and -34.0dBc at 0.4V supply and 0.5V supply, respectively. Upon activation of the ESED, there is a significant reduction in the reference spur level, reaching -62.2dBc and -54.0dBc
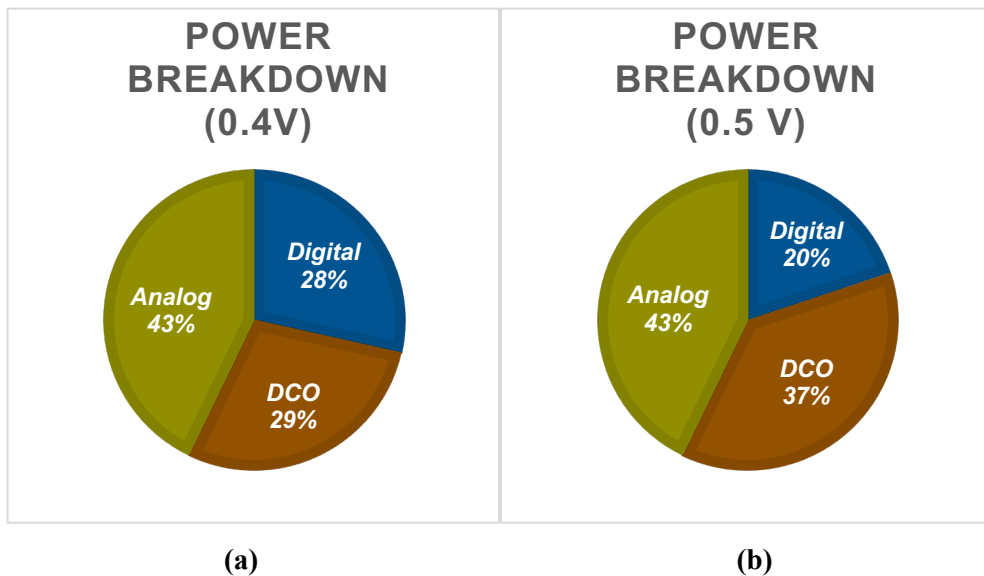
Figure 4.5 Power breakdown. (a) 0.4V supply and (b) 0.5V supply.

Figure 4.5 presents the results of power measurement in each block of the ILCM. The power consumption is measured to be 55.4uW and 171uW at 0.4V and 0.5V supplies, respectively. At the 0.4V supply, the DCO, analog, and digital blocks accounte for 29%, 43%, and 28% of the total power consumption, respectively. Similarly, at the 0.5V supply, these blocks consumes 37%, 43%, and 20% of the total power consumption. The results demonstrate that by operating the ILCM at near-threshold voltage, it can achieve excellent power efficiencies of 184uW/GHz and 171uW/GHz.

Table 4.1 summarizes the performance of the proposed ILCM and compares it with other low-voltage RO-based PLLs. The ILCM has a compact active area of 0.0097mm² and achieves outstanding power efficiency of 184uW/GHz and 171uW/GHz by operating at near-threshold voltage. The proposed ESED results in integrated jitter of 11.7ps$_{RMS}$ and 2.58ps$_{RMS}$ and the best reference spur level at -62dBc and -54dBc, respectively. Additionally, the proposed ILCM attains FoM of -231dB and -239dB. Through these results, the proposed ILCM exhibits superior reference spur performance while retaining comparable active area and power efficiency, and FoM performance.

Table 4.1 Performance Summary and Comparison.

| | This Work | | [1] | [2] | [3] |
|---|---|---|---|---|---|
| Technology | 28-nm | | 40-nm | 7-nm | 14-nm |
| Area (mm$^2$) | 0.0097 | | 0.0087 | 0.012 | 0.021 |
| Supply (V) | 0.4 | 0.5 | 0.4 | 0.65 | 0.6 |
| $f_{OUT}$ (GHz) | 0.3 | 1.0 | 1.6 | 3.0 | 1.6 |
| $f_{REF}$ (MHz) | 30 | 100 | 100 | 200 | 100 |
| Power efficiency (uW/GHz) | 184 | 171 | 106 | 767 | 406 |
| Jitter$_{RMS}$ (ps) | 11.7 | 2.58 | 8.3 | 0.63 | 3.77 |
| Ref. Spur (dBc) | -62.2 | -54.0 | -58.3 | -52.3 | NA |
| FoM (dB) | -231.0 | -239.4 | -229.3 | -240.5 | -230.3 |

# Chapter 5

# Conclusion

In this thesis, I present a RO-based ILCM operating at near-threshold voltage. To improve the reference spur level of the ILCM that becomes more degraded at low-voltage operation, I propose an edge-selective error detector (ESED) that eliminates the correlation between the error detection paths.

The proposed near-threshold ILCM is fabricated using a 28nm CMOS process and occupies a core area of $0.0097mm^2$. It is measured at supply voltages of 0.4V and 0.5V, and generates output clocks of 300MHz and 1.00GHz, respectively. When the proposed ESED is activated, an integrated jitter of $11.7ps_{RMS}$ and $2.58ps_{RMS}$ and a reference spur of -62dBc and -54dBc are obtained, respectively, along with FoMs of -231dB and -239dB. Through this, it is confirmed that the proposed near-threshold ILCM effectively improves the reference spur level while maintaining its small area and low power consumptions.

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# 초 록

RO-based injection-locked clock multiplier (ILCM)은 작은 면적과 우수한 전력 효율로 인하여 배터리로 동작하는 시스템의 요구사항에 부합하는 특성을 갖는다. 그러나, ILCM 에서 발생하는 높은 reference spur 는 저전압에서 우수한 성능을 달성하는데 장애물로 작용하고 있다.

본 논문에서는 이러한 추세에 따라 RO 기반의 near-threshold ILCM 을 설계하였으며, 저전압에서 열화되는 reference spur 성능을 개선하는 새로운 error detection scheme 을 제안하였다. 이를 통해 error-tracking path 사이에 존재하던 correlation 을 제거하였으며, reference spur 를 효과적으로 제거할 수 있도록 설계하였다.

제안된 RO 기반의 near-threshold ILCM 은 28nm CMOS 공정으로 제작되었으며, 0.0097mm$^2$ 의 면적을 차지한다. 0.4V 와 0.5V 에서 측정되었으며, 각각 300MHz 와 1.00GHz 의 클럭을 생성하였다. 제안된 error detector 가 활성화 되었을 때 11.7ps$_{RMS}$ 와 2.58ps$_{RMS}$ 의 integrated jitter 와 -62dBc, -54dBc 의 reference spur 가 발생하였으며, 각각 -231dB, -239dB 의 FoM 을 달성하였다.