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Master's Thesis of Ikcheon Na

Maximizing the High Areal Capacity of All-Solid-State Battery Anode: 100% Silicon

전고체전지 음극의 면적 용량 극대화: 100% 실리콘

February 2023

Graduate School of Natural Science
Seoul National University
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Maximizing the High Areal Capacity of All-Solid-State Battery Anode: 100% Silicon

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Submitting a master's thesis of
Chemistry

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Abstract
Maximizing the High Areal Capacity of All-Solid-State Battery Anode: 100% Silicon

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Recently, all-solid-state batteries (ASSBs) have been actively investigated due to their nonflammability and high energy density. As a negative electrode of ASSB, silicon composite, lithium metal, or anode-free electrode is attracting much attention because of its high energy density. Especially, silicon electrodes have a higher positive working potential and form a more stable interface with the electrolyte than the lithium metal-based electrodes, which certainly has a high risk of detrimental dendrite formation. In addition, silicon is abundant and economical with a theoretical capacity comparable to lithium metal.

The conventional electrode of ASSB consists of active material, conductive agent, binder, and solid electrolyte, which inherently forms a dead volume and interfacial layer prone to side-reactions. Therefore, many researches have been longing for reducing the fraction of solid electrolytes and additives in the composite

electrode in order to maximize the energy density.

Silicon wafers are the ultimate form of additive-free, electrolyte-free, void-free geometry to achieve maximum energy density. To date, attempts to utilize wafers as electrodes have been unsuccessful due to uncontrollable internal stress and cracks, and contact losses. In this work, we developed <110> oriented thin silicon wafer electrodes that could achieve areal capacity of 10 mAh cm^{-2}. Due to the high lithium conductivity of silicon, pure silicon wafers could allow rapid lithium diffusion without the aid of electrolyte incorporation. Moreover, the monolithic nature of the wafer could effectively eliminate undesirable side reactions stemming from particle interfaces within composite electrodes. We discovered that the <110> oriented wafer enables faster lithium diffusion than other oriented wafers, such as <100> and <111>, and enhances cyclability by controlling surface roughness and thickness. The performance including energy and power density could be further improved by optimizing the wafer geometry and surface morphology.

Keywords : All-solid-state battery, silicon electrode, additive-free, electrolyte-free, void-free, high areal capacity

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Chapter 1. Introduction

1-1. Study Background

The recent development of portable devices, electric vehicles, and large-scale energy storage systems has significantly increased the demand for safer and more energy-dense batteries.[1-4] All-solid-state batteries (ASSBs) utilizing sulfide-based electrolytes provide an ideal geometry to attain a higher energy density and improved safety compared with conventional lithium-ion batteries (LIBs) using flammable organic liquid electrolytes.[5-7]

Silicon anodes exhibit a high energy density (3589 mAh g^{-1}) via an alloy reaction, which is 10 times larger than that of graphite anodes (372 mAh g^{-1}).[8] Because silicon is the second most abundant element in the Earth's crust, it is inexpensive and environmentally friendly.[9] Recent developments in metallic lithium anodes demonstrate impressive battery performance owing to their high energy density (3860 mAh g^{-1}); however, they still face the risk of growing lithium dendrites and forming unstable solid electrolyte interfaces originating from the low reduction potential and high reactivity of lithium.[10-13] Moreover, room-temperature operation remains a challenge because the critical current density for reversible lithium metal deposition/depletion is still low.[14]

Therefore, a silicon anode could be an attractive choice as a safer electrode with a high energy density.

1-2. Purpose of Research

In several previous studies, silicon powder composite electrodes were developed as anodes for ASSBs.[15-17] Such silicon powders are generally mixed with electrolyte powders, carbon additives, and polymeric binders forming 3-dimensionally percolated interfaces in composite electrodes. Having large interface areas is not ideal because a detrimental solid-electrolyte-interphase (SEI) grown from the interfaces could decrease the lithium transport and capacity.[18] Because carbon additives are reactive to sulfide electrolytes, silicon powder electrodes with neither carbon species nor electrolytes have been demonstrated recently.[19] However, powder electrodes intrinsically have porous structures with many internal voids, even under a high fabrication pressure, which may impede lithium diffusion.[20,21] This remains a challenge in the fabrication of thick powder electrodes with a high areal capacity. Thus, it is necessary to develop a new electrode design that can achieve a high areal capacity and loading density.

In a battery cell, the areal capacity of the electrode is one of the most important parameters in determining the electrode

performance and achieving a high areal capacity remains a big challenge in ASSBs.[22–25] In this study, we demonstrate that a monolithic, void-free silicon electrode can successfully reach an extremely high areal capacity of 10 mAh cm^{-2}. Thin wafers are attractive model geometries for realizing additive-free, electrolyte-free, and void-free electrodes, and are highly compatible with microfabrication and mass-production infrastructure. Monolithic silicon wafers do not need solid electrolytes or conducting carbon additives inside and can fundamentally suppress parasitic side reactions at interfaces or SEI growth within the electrode. Moreover, monolithically integrated silicon-silicon bonding networks allow facile lithium transport through the thickness direction, utilizing the active materials deeply and enabling a high areal capacity. Specifically, it is challenging to increase the loading density to higher than 1.2 g cm^{-3} for the powder electrode but it is 2.2 g cm^{-3} for the silicon wafer, which is almost twice as high as that of the powder electrode (**Figure 1**). By controlling the surface morphology, we increased the cycle retention up to 87 cycles and successfully operated the full-cell with a Ni-rich NCM cathode.

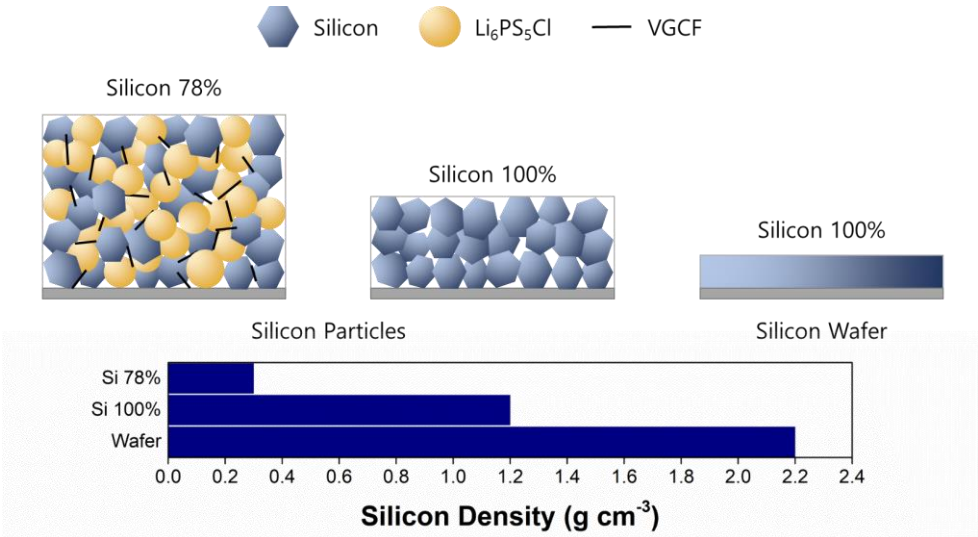

Figure 1. Silicon densities of composite electrode, 100% powder electrode, and wafer electrode (~0.3, 1.2, and 2.2 g cm^{-3}, respectively).

Chapter 2. Experimental Methods

2-2. Electrode Preparation

<100>, <110>, and <111>-oriented silicon wafers were purchased from University wafer Inc. and diced into areas of 0.4 × 0.4 cm^2. The wafer surfaces were cleaned with piranha solution (a solution mixed with sulfuric acid and 30 % hydrogen peroxide in a ratio of 3:1) for 5 h and then cleaned with deionized water. The cleaned <100>, <110>, and <111> wafers were treated with 3 M KOH solution for 24 h at room-temperature to modify their surfaces and thin them. The treated <100>, <110>, and <111> wafers were cleaned with piranha solution and deionized water. The cleaned bare and treated <100>, <110>, and <111> wafers were placed in oxygen plasma to control the composition of the surface. The electrodes were dried at 80 ° C in a convection oven for 3 h to remove water. Pristine $LiNi_{0.8}Co_{0.1}Mn_{0.1}O_2$ (Ni-rich NCM) powder, with a particle size of approximately 10 μm, was purchased from Rov Corp. Commercial Li_6PS_5Cl (LPSCl) with a particle size D50 of approximately 3 μm and polytetrafluoroethylene (PTFE) was obtained from CISOLID Co. and Daikin, respectively. The cathode materials were mixed with a sulfide solid electrolyte, conductive carbon (VGCF), and a binder at a ratio of 80:20:2:0.3 by weight in

an agate mortar until a single flake was formed. A single fake was then fabricated into a freestanding film electrode with the target thickness. All processes were carried out in a dry room (dew point below −55 ° C).

2−3. Cell Assembly

The liquid electrolyte used for the silicon wafer half−cell was 1.0 M $LiPF_6$ with ethylene carbonate (EC) and dimethyl carbonate (DMC) (1:1 v/v %). The CR2032−type coin cell was assembled with a silicon wafer electrode, liquid electrolyte, Celgard 2320 separator, and a Li metal foil counter/reference electrode. A solid−state half−cell was assembled using a silicon wafer electrode, LPSCl, and Li−In foil electrode. The wafer electrode and LPSCl powder were placed in a custom−designed PEEK cell body and cold−pressed at 500 MPa for 2 min. The Li−In alloy electrode, manufactured with lithium metal foil and a thin indium foil with a composition of $Li_{0.5}In$, was attached to the other side of the LPSCl pellet and pressed at 250 MPa for 1 min. A solid−state full−cell was assembled with a composite cathode, LPSCl, and a silicon wafer anode using the same procedures as the half−cell assembly. Instead of the Li−In foil electrode, the cathode composite fabricated in the dry process was attached to the other side of the LPSCl pellet and pressed at 500

MPa for 3 min. The cathode composite used for the full cell was diced to 0.38 × 0.38 cm^2. All the cell assembly processes were carried out in a dry room.

2-4. Electrochemical Analysis

The cycling experiments were conducted using a battery cycler system (WBCS3000L, WonATech, Korea). The solid-state cells were air-tightened and tested under a stack pressure of 28 MPa. All types of cells were rested for 3 h at an open-circuit voltage (OCV) and then cycled with a galvanostatic current density of 0.5 mA cm^{-2}, voltage range of 0.005-1.6 V vs Li/Li^+ for the half-cells or 2-4.3 V for full-cells. The cycling cut-off condition was set to either a voltage or an areal capacity of 10 mAh cm^{-2}. Electrochemical impedance spectroscopy (EIS) measurements of the bare <110> and grooved <110> wafer cells during cycling were carried out using a VSP-300 (BioLogic) and analyzed with EC-Lab software. The cell was cycled up to an areal capacity of 0.5 mAh cm^{-2} followed by 30 min of rest. After the rest period, EIS was performed for the cell with an amplitude of 10 mV in the frequency range of 7 MHz to 100 mHz. The cell continued cycling up to the next targeted areal capacity, and EIS measurements were performed after the rest period. This process was repeated during

the first cycle.

2-5. Characterization

The silicon wafers were disassembled from the solid-state cells within 5 min after the end of the cycle test, and the wafers were carefully delaminated from the solid-state electrolyte layer in a dry room. Scanning electron microscopy (SEM) images and energy-dispersive X-ray spectroscopy (EDS) elemental mapping of the silicon wafers were obtained using field-emission scanning electron microscopy (FE-SEM (MIRA3 XMH, TESCAN)). The loaded SEM samples were placed directly into the chamber and air exposure was minimized. The accelerating voltage was set to 10 kV.

Chapter 3. Results & Discussion

3-1. Silicon Wafers as All-Solid-State Battery Electrodes

Although the monolithic and void-free electrode geometry is ideal for achieving the maximum energy density, the use of a pure silicon wafer as an anode for conventional liquid electrolytes lithium-ion batteries has not been successful. The liquid electrolyte could freely penetrate the electrode through defects or cracks, create fresh solid-electrolyte-interphases, and lead to pulverization because the silicon wafer repeatedly expands and shrinks upon cycling, as shown in **Figure 2**. In ASSBs, the solid electrolyte can densely form 2-dimensional interfaces with the silicon wafer surface, hold the silicon surfaces, and suppress the mechanical failure of silicon during cycling. Because a rigid solid electrolyte cannot penetrate deeply through the silicon electrode, a 2-dimensional interface between the solid electrolyte and silicon wafer could persist, and a detrimental percolated SEI within the electrode does not easily form.

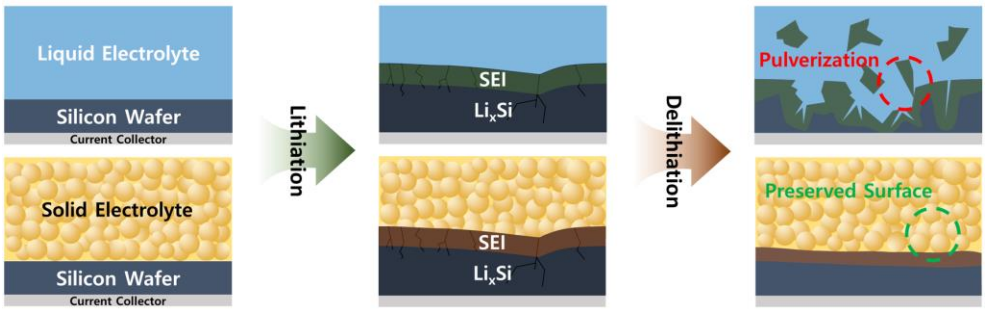

Figure 2. Schematic illustrations of wafers under the liquid electrolyte system and the solid electrolyte system.

Here, we present the battery performance of a bare <100> silicon wafer with 1.0 M $LiPF_6$ in ethylene carbonate (EC) and dimethyl carbonate (DMC) (1:1 v/v %) liquid electrolyte and Li_6PS_5Cl (LPSCl) solid electrolyte as shown in **Figure 3**. It is clear that the silicon wafer lost electrical contact significantly during the first dealloying process in the liquid electrolyte (**Figure 4**) while it efficiently cycled 19 times in the solid electrolyte at current density of 0.5 mA cm^{-2} under cut-off areal capacity of 10 mAh cm^{-2}. This confirms that silicon wafers have a remarkable potential as high-capacity anodes for ASSBs.

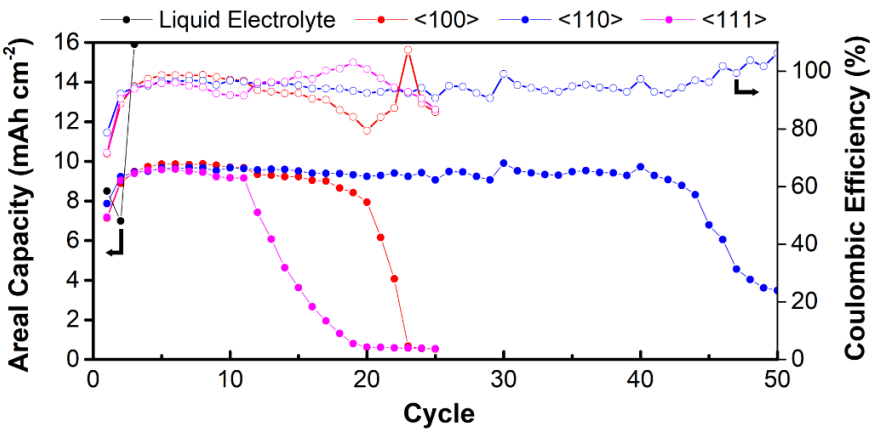

Figure 3. Cycling performance of wafers with the liquid electrolyte and the solid electrolyte at current density of 0.5 mA cm^{-2}.

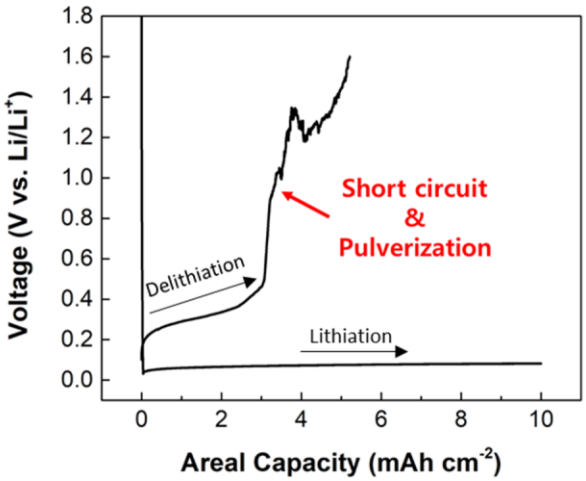

Figure 4. Voltage profile of the first cycle of bare <100> wafer half-cell with 1M $LiPF_6$ in EC/DMC.

3-2. Lithium Diffusion in Different Orientation Wafers

To enhance the compatibility of silicon wafers with solid electrolytes in ASSBs, we evaluated the effect of the crystallographic orientation on lithium diffusion within the electrode. Considering the diamond cubic structure with the Fd$\bar{3}$m space group shown in **Figure 5,** the lattice position displayed along the <110> direction had the largest interstitial spacing and contributed to the fastest lithium diffusion in the <100>, <110>, and <111> directions.[26,27]

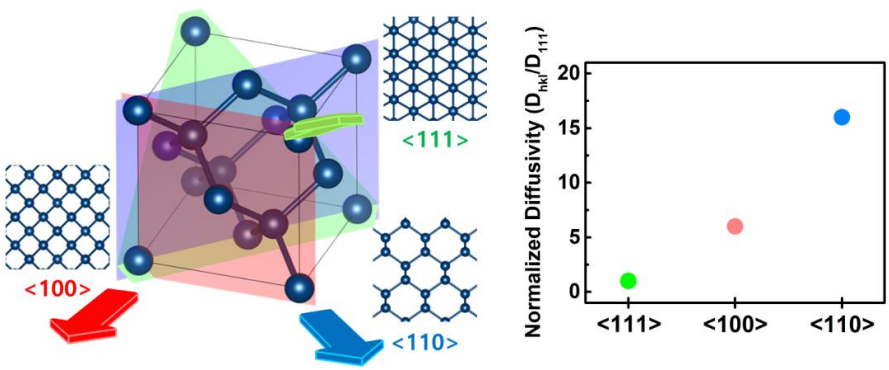

Figure 5. Schematic and normalized lithium diffusivity (D_{hkl}/D_{111}) plot in crystal silicon lattices.[26,27]

Figure 6a-c show the battery performance of the bare <100>, <110>, and <111> wafers tested at a galvanostatic current density of 0.5 mA cm^{-2}. The wafers in this study were used as received from the manufacturers. The thicknesses were 200, 500, and 350

μm for bare <100>, <110>, and <111>, respectively, which we confirm does not play a significant role in the battery performance. They are sufficiently thick to accommodate a high areal energy capacity and alloyed lithium, enabling the evaluation of the intrinsic properties of lithium transport depending on the crystallographic orientation of the wafers. For instance, the cut-off lithiation areal capacity (10 mAh cm^{-2}) still leaves an unreacted silicon substrate underneath and allows cross-sectional scanning electron microscopy (SEM) to visualize the lithiated and unreacted regions by image contrast. **Figure 3 and Figure 6a-f** present the cyclability, voltage profiles, and dQ/dV profiles of each cell at current density of 0.5 mA cm^{-2} under cut-off areal capacity of 10 mAh cm^{-2}. The cell of the bare <110> wafer exhibited the best cyclability of 44 cycles, followed by that of the bare <100> wafer (19 cycles) and bare <111> wafer (11 cycles). The alloyed lithium amounts were constant for all, but the lithium transport depths varied with the wafer orientation. We note that the dQ/dV profile in **Figure 6d-f** during lithiation still diverges and does not have a peak, indicating that the full lithiation capacity has not been reached. The voltage end-points (marked as A in **Figure 6d-f**) in bare <100>, <110>, and <111> are 0.075, 0.082, and 0.057 V, respectively, and could correlate with the effective lithium composition within the active

silicon–lithium alloy regions. **Figure 7a–c** shows that the depths of the lithiated alloys of bare <100>, <110>, and <111> were 80, 160, and 55 μm, respectively. The highest voltage endpoint for bare <110> indicates a low lithium <x> fraction within the Li_xSi alloy and deeper lithium diffusion along the wafer thickness, as characterized by the SEM image in **Figure 7b**. This confirms that lithium diffuses rapidly along the <110> depth direction in the bare <110> wafer. In contrast, point A of the bare <111> wafer is the lowest, indicating the highest lithium <x> fraction within Li_xSi, consistent with the SEM images in **Figure 7c** showing lithium alloys confined near the solid electrolyte interfaces.

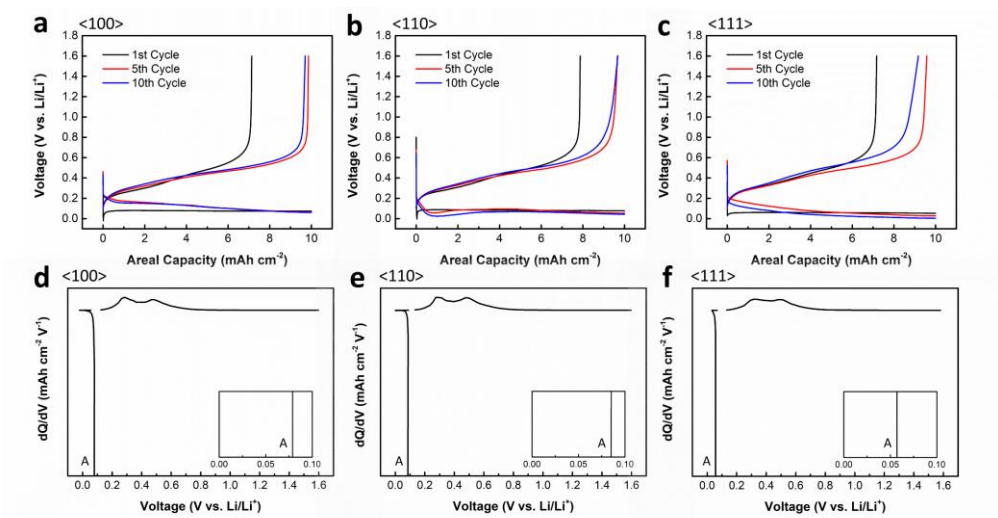

Figure 6. (a–c) Voltage profiles and (d–f) differential capacity plots (inset images are dQ/dV plots in voltage range of 0–0.1 V) of first lithiated bare <100>, <110>, and <111> wafers for ASSBs.

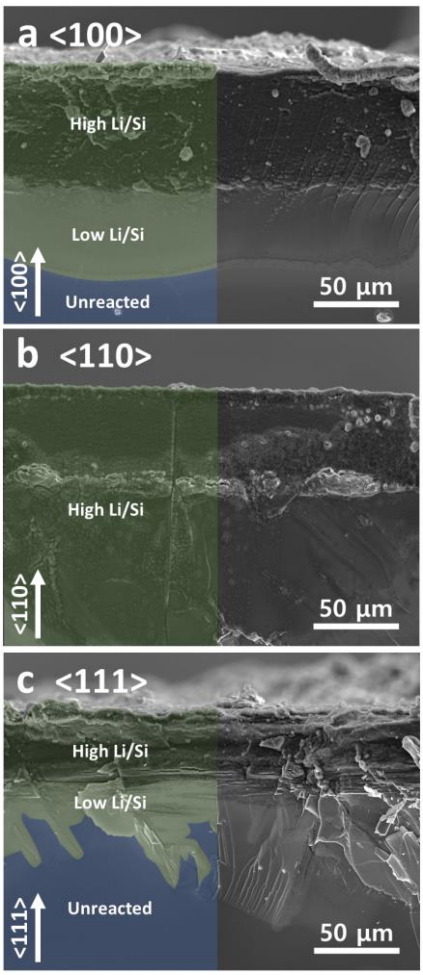

Figure 7. (a–c) cross-sectional SEM images of first lithiated bare <100>, <110>, and <111> wafers for ASSBs.

3-3. Crack Formation on Wafer Electrodes

Lithiation expands the crystalline silicon electrodes significantly along the [110] direction and only slightly along the [100] and [111] directions.[26] **Figure 8a-c** display the preferred expansion directions for each orientation wafer; the <100>, <110>, and <111> wafers have four, two, and six in-plane [110] directions, respectively. The in-plane expansion of the silicon wafer near the interface of the bare <111> wafer was the most severe among the three, followed by the bare <100> and bare <110> wafers. The significant volume expansion along the [110] direction leads to the release of strong compressive stress after lithiation, promoting cracks along the [110] direction. The top-down SEM images of the first lithiated wafer surfaces in **Figure 9a-c** show the cracks generated along the [110] direction, in which rectangularly shaped cracks and triangular/hexagonally shaped cracks were generated for the bare <100> wafer and bare <111> wafer, respectively. In contrast, the bare <110> wafer allows fast lithium diffusion along the <110> thickness direction, effectively suppressing the in-plane expansion while allowing thickness-direction expansion. Thus, cracks rarely form on the electrode surface, maintaining a monolithic electrode structure upon cycling. Cross-sectional SEM images demonstrated that lithium was more evenly distributed along

the thickness, releasing the stress more homogeneously within the electrode in the bare <110> wafers. In contrast, lithium is highly concentrated near the surface of the bare <111> wafer, which is consistent with the dQ/dV plot and could lead to a high local stress at the interface. Thus, the <110> orientation is the optimal choice as a crystalline wafer anode in ASSBs.

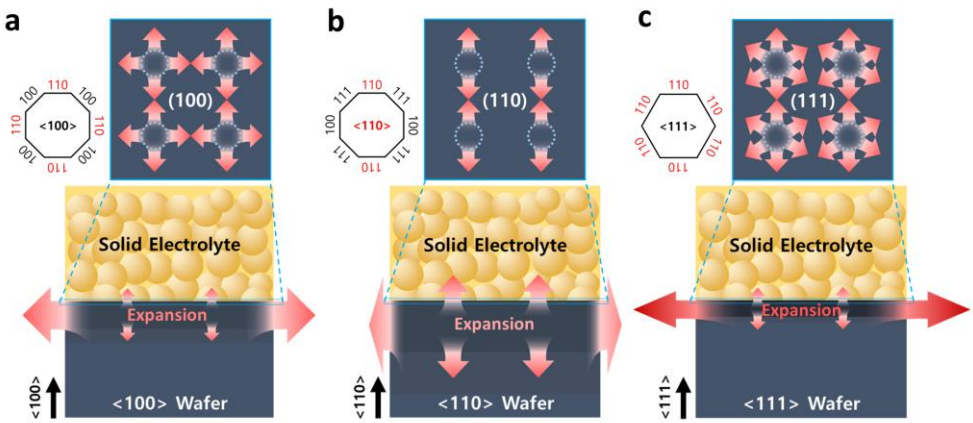

Figure 8. Cracks evolved along [110] direction due to anisotropic volume expansion of wafers. (a–c) Schematic of plane and side views showing major expansion directions along [110] for each wafer.

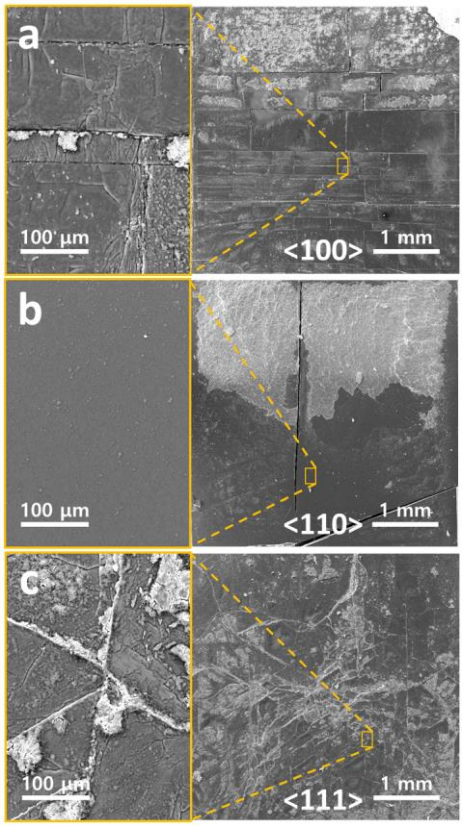

Figure 9. (a–c) Top–down SEM images of first lithiated bare <100>, <110>, and <111> wafer surfaces.

Although the <110> orientation would be more ideal than the others, homogeneously utilizing the entire electrode surface is critical and remains challenging. In practice, it may be difficult to realize a conformal interface between the solid electrolyte and flat electrode surfaces, and faster interfacial domains lead to the lithiation of the current hotspots. The interfaces that initiate lithiation at the beginning of charging expand vertically and push the solid electrolyte along the <110> direction, making the fast

interface more densely contacted. However, this widens the gap between the slow and inactive interfaces, delaminating certain electrode surfaces from the electrolyte (**Figure 10a**). The SEM image shown in **Figure 11a** illustrates the unreacted area left on the bare <110> wafer surface after the first lithiation. These unreacted areas could not be found for bare <111> wafers because lithium tends to diffuse laterally (in-plane direction) along the interface, increasing the active interfacial regions (**Figure 10b**). **Figure 7c and 9c** confirm that the entire surface was active and lithiated.

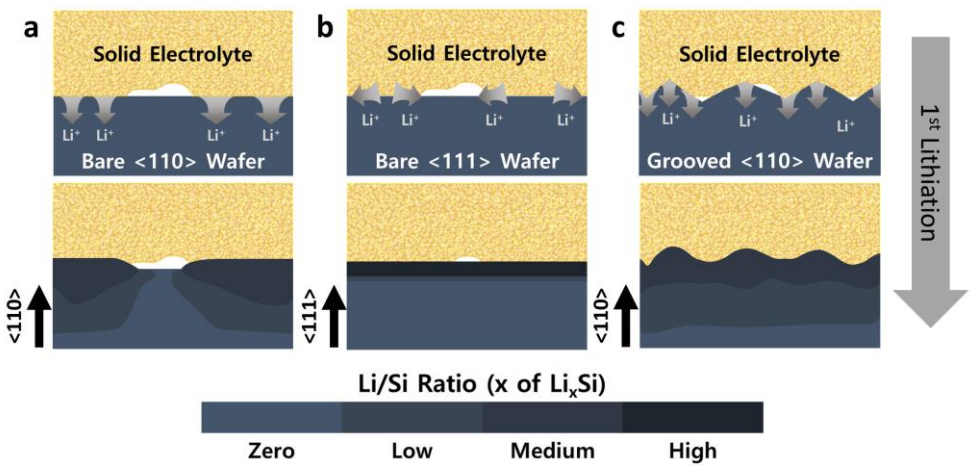

Figure 10. Surface treated <110> wafer. (a-c) Schematic of lithiation at uneven interfaces between solid electrolyte and the wafer.

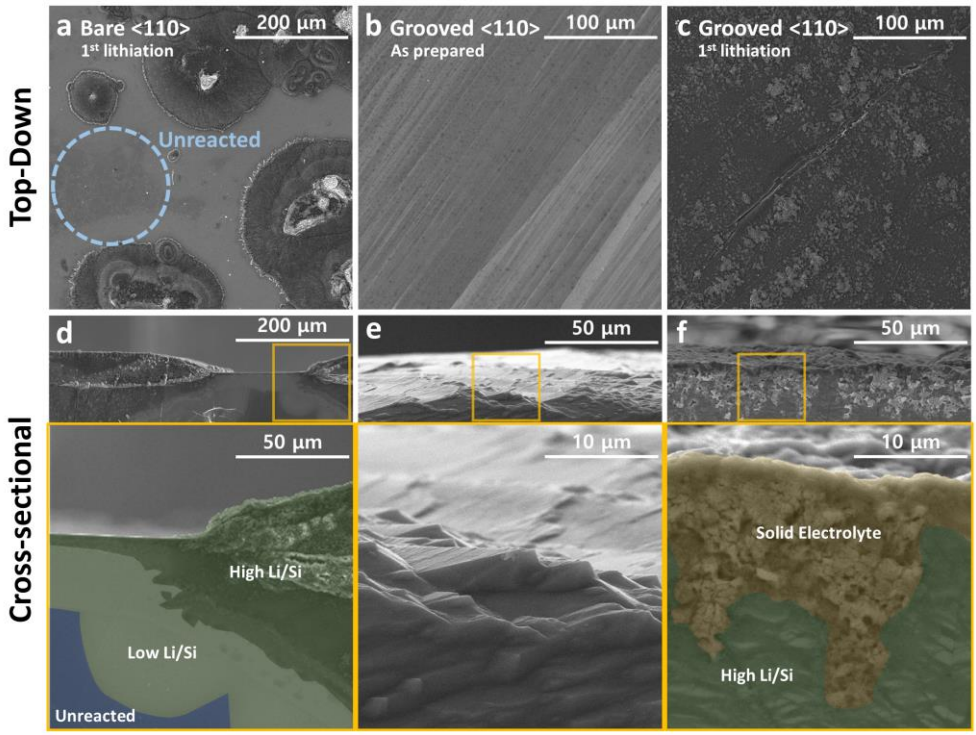

Figure 11. (a–f) Top–down and cross–sectional SEM images of first lithiated bare <110>, pristine grooved <110>, and first lithiated grooved <110> wafers.

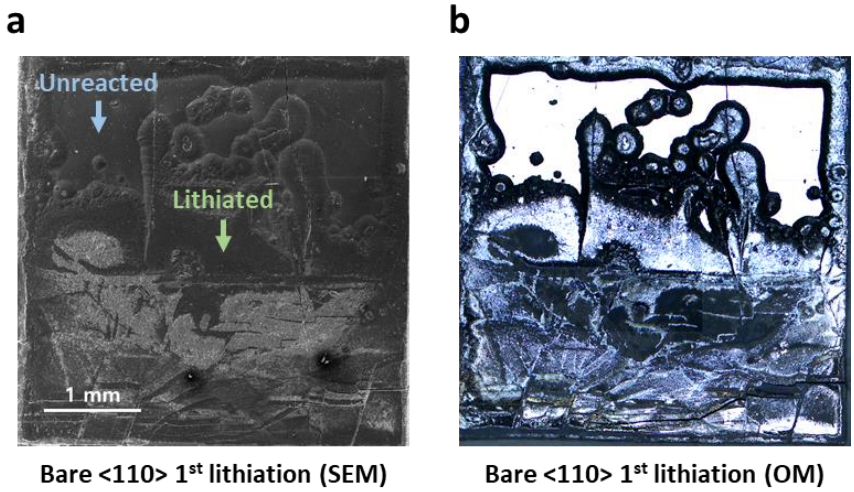

Figure 12. (a) Scanning electron microscopy (SEM) image and (b) optical microscopy (OM) image of the top-down view of the first lithiated bare <110> wafer. The unreacted area at the surface is the shiny polished area in the OM image.

3-4. Surface Treatment of Wafer Electrodes

To improve the contact between the electrolyte and electrode and increase electrode utilization, we etched bare <110> wafers with KOH to create a groove structure on the surface at room temperature for 24 h, which also decreased the wafer thickness. **Figure 11b and e** show that the main peaks of the grooves are decorated with many minor peaks, and the major peak-to-peak distance and amplitude are approximately 10 and 5 μm, respectively. The groove on the silicon surface could effectively penetrate the sulfide electrolyte layers, which have sufficient ductility under the cell fabrication pressure (~500 MPa). The grooved interfaces effectively increased the interfacial area for facile lithiation, and silicon peaks penetrating the solid electrolyte could efficiently distribute the lithiation current homogeneously across the entire silicon wafer (**Figure 10c**). Moreover, we note that silicon groves could strongly bind the sulfide electrolyte, and the SEM plan and side-view images of the electrode after the first lithiation show that the surfaces are entirely covered by the sulfide electrolyte after disassembling the cell (**Figure 11c and f**). This is contrary to the bare <110> wafer, which exhibits delaminated and clean surfaces with no sulfide electrolyte after cell disassembly.

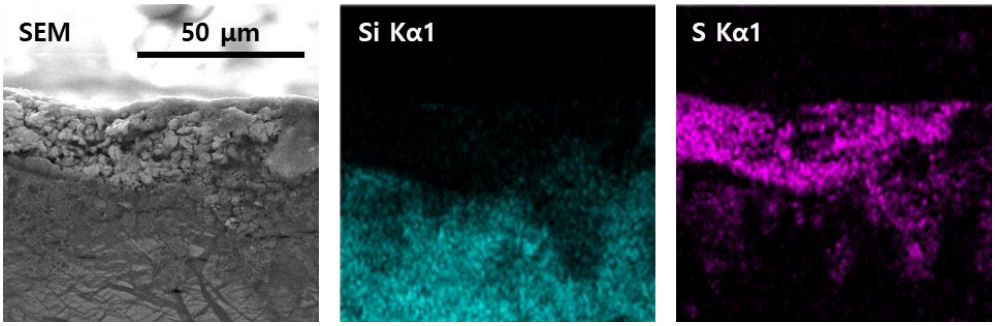

Figure 13. Cross-sectional SEM-EDS mapping of the first lithiated grooved <110> wafer.

Galvanostatic cycling of the grooved <110> wafer was performed at 0.5 mA cm^{-2}. The voltage profile in **Figure 14** shows a lower overpotential and remains more stable compared with that of the bare <110> wafer owing to the stable interface. We characterized the contact resistance via electrochemical impedance spectroscopy (EIS) and found that the grooved <110> wafer showed significantly lower and more consistent contact resistance during lithiation than the bare <110> wafer. The high resistance that decreases at the beginning of the cycle for the bare <110> wafer indicates that the poorly contacted interface between the electrode and electrolyte is densely packed via the depth-direction expansion of the electrode upon lithiation. The consistently low contact resistance of the grooved <110> wafer indicates that the grooved surfaces could effectively penetrate the solid electrolyte during cell

fabrication and maintain the integrity of the contact interfaces during cycling (Figure 16).

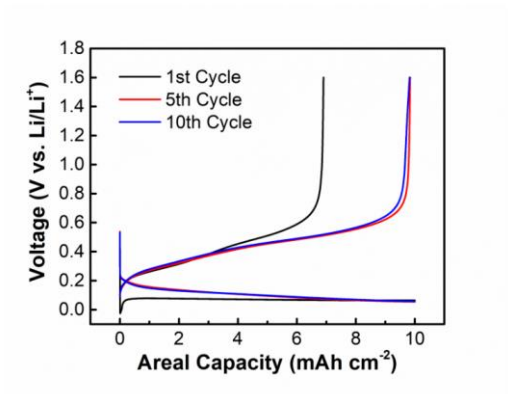

Figure 14. Voltage profile of the grooved <110> wafer half-cell.

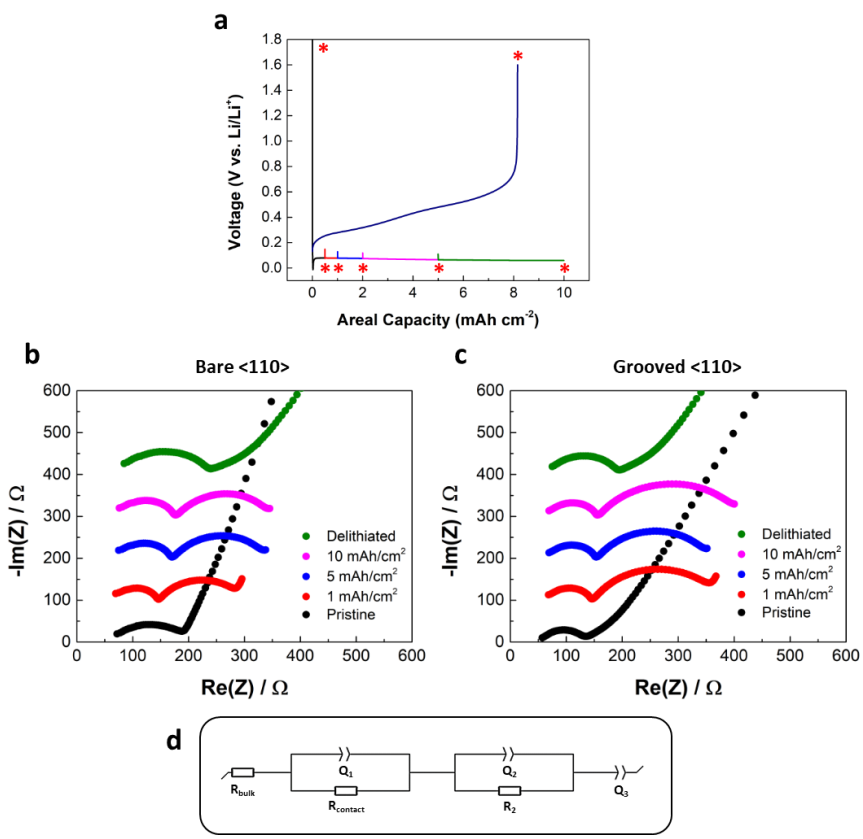

Figure 15. (a) Voltage profile of the <110> wafer. Marked points

are the areal capacities where the EIS measurements were conducted. (b and c) Nyquist plots of bare and grooved <110> during the first cycle. (d) The equivalent circuit used for fitting.

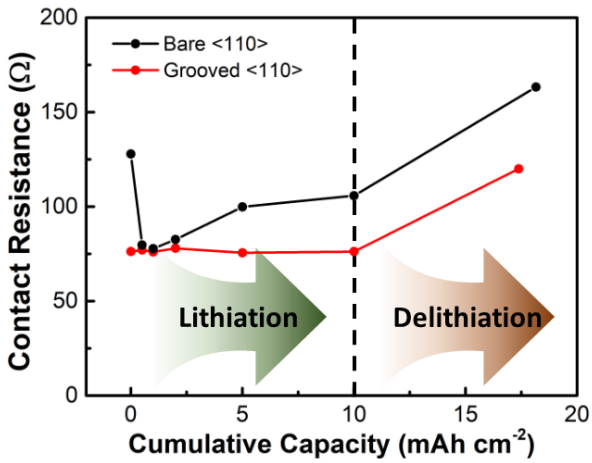

Figure 16. Contact resistance calculated by fitting the Nyquist plots (**Figure 15**) during the first cycle of grooved <110> wafer half cell.

The grooved <110> wafer shows a remarkable cycle life and stably achieves an areal capacity of 10 mAh cm^{-2} at a current density of 0.5 mA cm^{-2} at room temperature (**Figure 17**). The grooved wafers became significantly thinner (220 μm) after KOH etching, indicating that the material cost could be further reduced. Additionally, the thinned wafer could effectively limit lithium diffusion along the thickness direction and efficiently allow lithium to be extracted reversibly during delithiation. Further thinning and

optimizing the wafer thickness can extend the coulombic efficiency and cycle life.

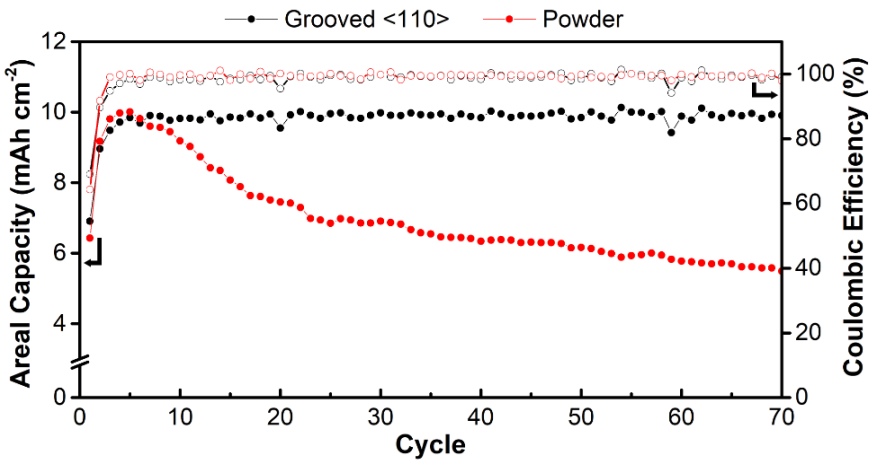

Figure 17. Cycling performance of the grooved <110> wafer and powder electrode half cell.

In contrast, achieving a high areal capacity of as much as 10 mAh cm^{-2} for the conventional silicon powder electrode is not straightforward at room temperature. We attempted to fabricate a thick silicon powder anode and our optimized maximum loading density of the silicon powder anode was 8.3 mg cm^{-2} at best (the theoretical areal capacity is 29.8 mA/cm2). Our thick powder electrode demonstrated an areal capacity of 10 mAh cm^{-2} at the beginning of the cycle, which decreased to 5–6 mAh cm^{-2} after 70 cycles. It remains challenging for silicon powder electrodes to

eliminate voids and pores under an acceptable fabrication pressure of 500 MPa. Thus, they significantly retard lithium transport and decrease the energy density. Conventionally developed powder or nanoparticle-based composite electrodes mixed with solid electrolyte particles or thin-film electrodes for ASSBs show difficulty in achieving a high areal capacity of 10 mAh cm^{-2} at room temperature. To the best of our knowledge, our grooved <110> wafers showed the highest areal capacity at room temperature among the reported silicon anodes developed for ASSB half-cells. (Figure 18).[15,16,28-33]

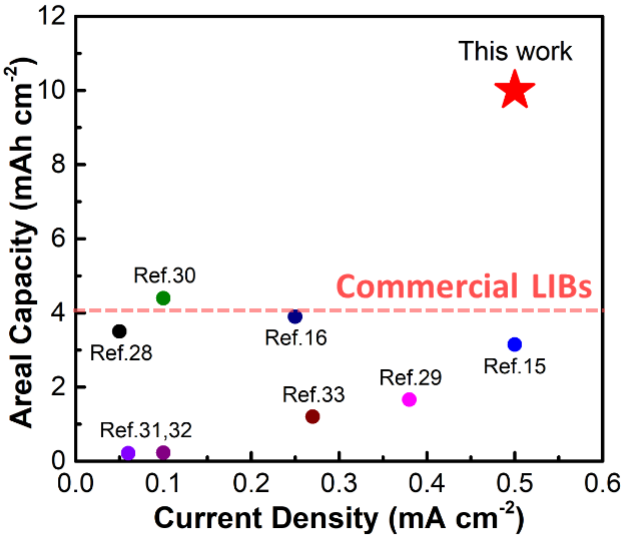

Figure 18. Performance comparison of the grooved <110> wafer half-cell with previously reported ASSB silicon electrode half-cells.[15,16,28-33]

The other <100> and <111> wafers were treated with KOH. Their battery cycle lives were 73 cycles and 10 cycles, respectively, and they could not outperform the grooved <110> wafer, as expected. **Figure 19** shows the cycle retention of all silicon wafers until the delithiation capacity reached 8 mAh cm^{-2}. It is widely known that KOH cannot effectively groove <111> wafers, but only considers it. We attribute the poor cycle retention of KOH-etched <111> wafers to poor lithium diffusion along <111> direction and ineffective surface treatment.

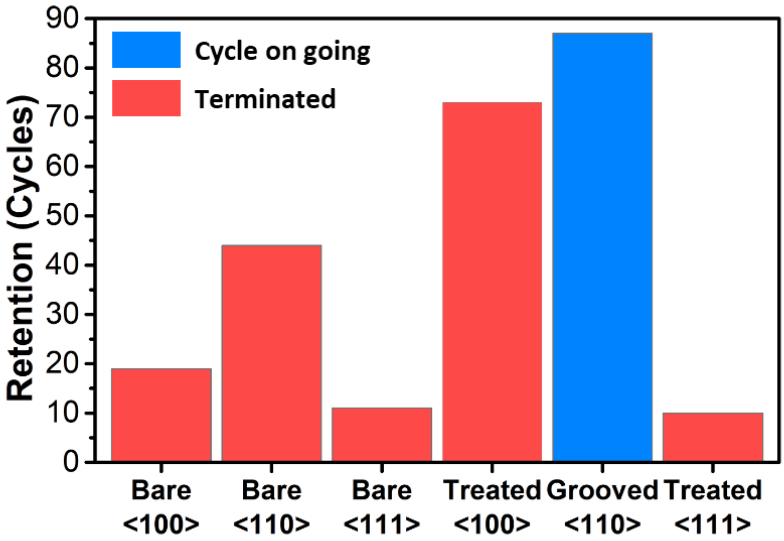

Figure 19. Cycle retentions of bare and treated <100>, <110>, and <111> wafers.

We further demonstrated that our grooved <110> wafer is highly compatible with a Ni-rich NCM cathode and achieved an areal capacity of 8.8 mAh cm^{-2} at 60 ° C, as shown in **Figure 20.** The current density and the voltage ranges are 0.5 mA cm^{-2} and 2-4.3 V, respectively. To match the high areal capacity of the anode, we attempted to develop a high-loading NCM cathode with a thickness of 380 μm, which is beyond the scope of this study. To stably utilize a thick cathode, we operated the full-cell at an elevated temperature, which could run stably and report a discharge capacity of 8.8 mAh cm^{-2}. This indicates that silicon wafers are promising anode candidates for high-areal-capacity ASSB full-cells.

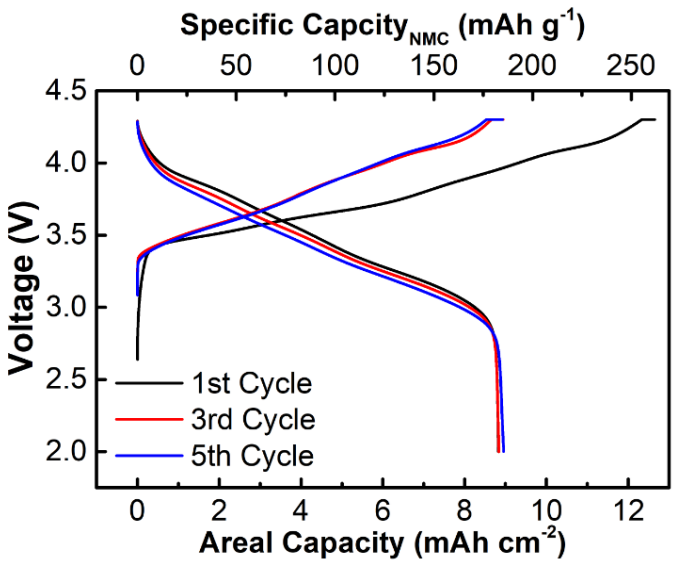

Figure 20. Voltage profile of the full-cell at current density of 0.5

mA cm^{-2} in voltage range of 2−4.3 V.

We highlight that silicon wafer electrodes are intrinsically beneficial for high areal capacity and serve as a model platform for ultrahigh energy density ASSBs. Wafer electrodes are compatible with MEMS technologies and can be microfabricated to improve lithium diffusion and release more internal stress. Moreover, thinning, doping, or amorphizing the wafers could further optimize the battery performance.

Chapter 4. Conclusion

In this study, we successfully demonstrated that a void-free monolithic pure silicon electrode could achieve an areal capacity as high as 10 mAh cm^{-2} in a half-cell at room temperature and 8.8 mAh cm^{-2} in a full cell at 60 ° C. The monolithic silicon structure allowed fast lithium transport across the electrode thickness, and surface modification enhanced the interfacial stability and cycle retention. Our results clearly showed that silicon wafers, which have been largely overlooked in liquid-electrolyte batteries, have great potential as next-generation electrodes for ASSBs. Combined with modern microfabrication technologies, the surface, thickness, crystallinity, defects, etc. can be sophisticatedly engineered to deliver a superior energy density, rate capability, and lifetime. Our results on monolithic Si anodes open a new avenue for next-generation high-energy ASSBs.

Bibliography

(1) Masias, A.; Marcicki, J.; Paxton, W. A. Opportunities and Challenges of Lithium Ion Batteries in Automotive Applications. *ACS Energy Lett.* 2021, *6* (2), 621–630. https://doi.org/10.1021/acsenergylett.0c02584.

(2) Bradley, D. Building Better Batteries. *Educ. Chem.* 2010, *47* (4), 124–125.

(3) Meesala, Y.; Jena, A.; Chang, H.; Liu, R. S. Recent Advancements in Li–Ion Conductors for All–Solid–State Li–Ion Batteries. *ACS Energy Lett.* 2017, *2* (12), 2734–2751. https://doi.org/10.1021/acsenergylett.7b00849.

(4) Wang, J.; Kim, H.; Hyun, H.; Jo, S.; Han, J.; Ko, D. H.; Seo, S.; Kim, J.; Kong, H.; Lim, J. Probing and Resolving the Heterogeneous Degradation of Nickel–Rich Layered Oxide Cathodes across Multi–Length Scales. *Small Methods* 2020, *4* (10), 1–30. https://doi.org/10.1002/smtd.202000551.

(5) Schwietert, T. K.; Arszelewska, V. A.; Wang, C.; Yu, C.; Vasileiadis, A.; de Klerk, N. J. J.; Hageman, J.; Hupfer, T.; Kerkamm, I.; Xu, Y.; van der Maas, E.; Kelder, E. M.; Ganapathy, S.; Wagemaker, M. Clarifying the Relationship between Redox Activity and Electrochemical Stability in Solid Electrolytes. *Nat. Mater.* 2020, *19* (4), 428–435. https://doi.org/10.1038/s41563–019–0576–0.

(6) Wang, M. J.; Carmona, E.; Gupta, A.; Albertus, P.; Sakamoto, J. Enabling "Lithium-Free" Manufacturing of Pure Lithium Metal Solid-State Batteries through in Situ Plating. *Nat. Commun.* 2020, *11* (1), 1-9. https://doi.org/10.1038/s41467-020-19004-4.

(7) Yoon, K.; Kim, H.; Han, S.; Chan, T. S.; Ko, K. H.; Jo, S.; Park, J.; Kim, S.; Lee, S.; Noh, J.; Kim, W.; Lim, J.; Kang, K. Detrimental Effect of High-Temperature Storage on Sulfide-Based All-Solid-State Batteries. *Appl. Phys. Rev.* 2022, *9* (3). https://doi.org/10.1063/5.0088838.

(8) Han, J.; Jo, S.; Na, I.; Oh, S. M.; Jeon, Y. M.; Park, J. G.; Koo, B.; Hyun, H.; Seo, S.; Lee, D.; Kim, H.; Kim, J.; Lim, J. C.; Lim, J. Homogenizing Silicon Domains in SiOx Anode during Cycling and Enhancing Battery Performance via Magnesium Doping. *ACS Appl. Mater. Interfaces* 2021, *13* (44), 52202-52214. https://doi.org/10.1021/acsami.1c14121.

(9) Franco Gonzalez, A.; Yang, N. H.; Liu, R. S. Silicon Anode Design for Lithium-Ion Batteries: Progress and Perspectives. *J. Phys. Chem. C* 2017, *121* (50), 27775-27787. https://doi.org/10.1021/acs.jpcc.7b07793.

(10) Moon, J.; Kim, D. O.; Bekaert, L.; Song, M.; Chung, J.; Lee, D.; Hubin, A.; Lim, J. Non-Fluorinated Non-Solvating Cosolvent Enabling Superior Performance of Lithium Metal Negative Electrode Battery.

Nat. Commun. 2022, *13* (1). https://doi.org/10.1038/s41467-022-32192-5.

(11) Lee, Y. G.; Fujiki, S.; Jung, C.; Suzuki, N.; Yashiro, N.; Omoda, R.; Ko, D. S.; Shiratsuchi, T.; Sugimoto, T.; Ryu, S.; Ku, J. H.; Watanabe, T.; Park, Y.; Aihara, Y.; Im, D.; Han, I. T. High-Energy Long-Cycling All-Solid-State Lithium Metal Batteries Enabled by Silver-Carbon Composite Anodes. *Nat. Energy* 2020, *5* (4), 299-308. https://doi.org/10.1038/s41560-020-0575-z.

(12) Xu, R.; Yue, J.; Liu, S.; Tu, J.; Han, F.; Liu, P.; Wang, C. Cathode-Supported All-Solid-State Lithium-Sulfur Batteries with High Cell-Level Energy Density. *ACS Energy Lett.* 2019, *4* (5), 1073-1079. https://doi.org/10.1021/acsenergylett.9b00430.

(13) Krauskopf, T.; Richter, F. H.; Zeier, W. G.; Janek, J. Physicochemical Concepts of the Lithium Metal Anode in Solid-State Batteries. *Chem. Rev.* 2020, *120* (15), 7745-7794. https://doi.org/10.1021/acs.chemrev.0c00431.

(14) Cao, D.; Sun, X.; Li, Q.; Natan, A.; Xiang, P.; Zhu, H. Lithium Dendrite in All-Solid-State Batteries: Growth Mechanisms, Suppression Strategies, and Characterizations. *Matter* 2020, *3* (1), 57-94. https://doi.org/10.1016/j.matt.2020.03.015.

(15) Cao, D.; Sun, X.; Li, Y.; Anderson, A.; Lu, W.; Zhu, H. Long-Cycling Sulfide-Based All-Solid-State Batteries Enabled by

Electrochemo−Mechanically Stable Electrodes. *Adv. Mater.* 2022, *34* (24), 1–15. https://doi.org/10.1002/adma.202200401.

(16) Kim, D. H.; Lee, H. A.; Song, Y. B.; Park, J. W.; Lee, S. M.; Jung, Y. S. Sheet−Type Li6PS5Cl−Infiltrated Si Anodes Fabricated by Solution Process for All−Solid−State Lithium−Ion Batteries. *J. Power Sources* 2019, *426* (January), 143–150. https://doi.org/10.1016/j.jpowsour.2019.04.028.

(17) Okuno, R.; Yamamoto, M.; Kato, A.; Takahashi, M. High Cycle Stability of Nanoporous Si Composites in All−Solid−State Lithium−Ion Batteries. *J. Electrochem. Soc.* 2022, *169* (8), 080502. https://doi.org/10.1149/1945−7111/ac81f6.

(18) Huo, H.; Janek, J. Silicon as Emerging Anode in Solid−State Batteries. *ACS Energy Lett.* 2022, 4005–4016. https://doi.org/10.1021/acsenergylett.2c01950.

(19) Tan, D. H. S.; Chen, Y. T.; Yang, H.; Bao, W.; Sreenarayanan, B.; Doux, J. M.; Li, W.; Lu, B.; Ham, S. Y.; Sayahpour, B.; Scharf, J.; Wu, E. A.; Deysher, G.; Han, H. E.; Hah, H. J.; Jeong, H.; Lee, J. B.; Chen, Z.; Meng, Y. S. Carbon−Free High−Loading Silicon Anodes Enabled by Sulfide Solid Electrolytes. *Science (80−.).* 2021, *373* (6562), 1494–1499. https://doi.org/10.1126/science.abg7217.

(20) Davis, A. L.; Goel, V.; Liao, D. W.; Main, M. N.; Kazyak, E.; Lee, J.; Thornton, K.; Dasgupta, N. P. Rate Limitations in Composite Solid−

State Battery Electrodes: Revealing Heterogeneity with Operando Microscopy. *ACS Energy Lett.* 2021, *6* (8), 2993–3003. https://doi.org/10.1021/acsenergylett.1c01063.

(21) Kim, J. Y.; Park, J.; Lee, M. J.; Kang, S. H.; Shin, D. O.; Oh, J.; Kim, J.; Kim, K. M.; Lee, Y. G.; Lee, Y. M. Diffusion−Dependent Graphite Electrode for All−Solid−State Batteries with Extremely High Energy Density. *ACS Energy Lett.* 2020, *5* (9), 2995–3004. https://doi.org/10.1021/acsenergylett.0c01628.

(22) Zhang, X.; Ju, Z.; Zhu, Y.; Takeuchi, K. J.; Takeuchi, E. S.; Marschilok, A. C.; Yu, G. Multiscale Understanding and Architecture Design of High Energy/Power Lithium−Ion Battery Electrodes. *Adv. Energy Mater.* 2021, *11* (2), 1–20. https://doi.org/10.1002/aenm.202000808.

(23) Chen, C.; Zhang, Y.; Li, Y.; Kuang, Y.; Song, J.; Luo, W.; Wang, Y.; Yao, Y.; Pastel, G.; Xie, J.; Hu, L. Highly Conductive, Lightweight, Low−Tortuosity Carbon Frameworks as Ultrathick 3D Current Collectors. *Adv. Energy Mater.* 2017, *7* (17), 1–8. https://doi.org/10.1002/aenm.201700595.

(24) Kuang, Y.; Chen, C.; Kirsch, D.; Hu, L. Thick Electrode Batteries: Principles, Opportunities, and Challenges. *Adv. Energy Mater.* 2019, *9* (33), 1–19. https://doi.org/10.1002/aenm.201901457.

(25) Patry, G.; Romagny, A.; Martinet, S.; Froelich, D. Cost Modeling of

Lithium−Ion Battery Cells for Automotive Applications. *Energy Sci. Eng.* 2015, *3* (1), 71–82. https://doi.org/10.1002/ese3.47.

(26) Lee, S. W.; McDowell, M. T.; Choi, J. W.; Cui, Y. Anomalous Shape Changes of Silicon Nanopillars by Electrochemical Lithiation. *Nano Lett.* 2011, *11* (7), 3034–3039. https://doi.org/10.1021/nl201787r.

(27) Choi, Y. S.; Park, J. H.; Ahn, J. P.; Lee, J. C. Interfacial Reactions in the Li/Si Diffusion Couples: Origin of Anisotropic Lithiation of Crystalline Si in Li−Si Batteries. *Sci. Rep.* 2017, *7* (1), 1–9. https://doi.org/10.1038/s41598−017−14374−0.

(28) Cangaz, S.; Hippauf, F.; Reuter, F. S.; Doerfler, S.; Abendroth, T.; Althues, H.; Kaskel, S. Enabling High−Energy Solid−State Batteries with Stable Anode Interphase by the Use of Columnar Silicon Anodes. *Adv. Energy Mater.* 2020, *10* (34). https://doi.org/10.1002/aenm.202001320.

(29) Dunlap, N. A.; Kim, S.; Jeong, J. J.; Oh, K. H.; Lee, S. H. Simple and Inexpensive Coal−Tar−Pitch Derived Si−C Anode Composite for All−Solid−State Li−Ion Batteries. *Solid State Ionics* 2018, *324* (June), 207–217. https://doi.org/10.1016/j.ssi.2018.07.013.

(30) Yamamoto, M.; Terauchi, Y.; Sakuda, A.; Takahashi, M. Slurry Mixing for Fabricating Silicon−Composite Electrodes in All−Solid−State Batteries with High Areal Capacity and Cycling Stability. *J. Power Sources* 2018, *402* (July), 506–512.

https://doi.org/10.1016/j.jpowsour.2018.09.070.

(31) Ohta, N.; Kimura, S.; Sakabe, J.; Mitsuishi, K.; Ohnishi, T.; Takada, K. Anode Properties of Si Nanoparticles in All-Solid-State Li Batteries. *ACS Appl. Energy Mater.* 2019, *2* (10), 7005-7008. https://doi.org/10.1021/acsaem.9b01517.

(32) Miyazaki, R.; Ohta, N.; Ohnishi, T.; Takada, K. Anode Properties of Silicon-Rich Amorphous Silicon Suboxide Films in All-Solid-State Lithium Batteries. *J. Power Sources* 2016, *329*, 41-49. https://doi.org/10.1016/j.jpowsour.2016.08.070.

(33) Gu, L.; Han, J.; Chen, M.; Zhou, W.; Wang, X.; Xu, M.; Lin, H.; Liu, H.; Chen, H.; Chen, J.; Zhang, Q.; Han, X. Enabling Robust Structural and Interfacial Stability of Micron-Si Anode toward High-Performance Liquid and Solid-State Lithium-Ion Batteries. *Energy Storage Mater.* 2022, *52* (June), 547-561. https://doi.org/10.1016/j.ensm.2022.08.028.

Abstract in Korean (요약, 국문초록)

전고체전지는 불연성과 높은 에너지 밀도의 특징으로 연구가 활발히 진행되고 있다. 전고체전지 음극으로는 높은 에너지 밀도의 실리콘 복합전극, 리튬 금속 그리고 무음극이 각광받고 있다. 특히, 실리콘 전극은 리튬 메탈 기반의 전극보다 작동 전위가 더 높아, 황화물계 고체전해질과 더 안정적인 계면을 형성하며 리튬 수지상 성장 위험이 더 낮은 장점이 있다. 게다가 실리콘은 리튬 금속과 비슷한 이론 용량을 가지며, 지구 지각에 두 번째로 풍부한 물질이고 경제적이다.

종래의 전고체전지 전극은 활물질, 도전재, 바인더 및 고체전해질로 구성되어 있다. 이러한 복합 전극은 리튬이온의 충방전에 가용되지 않는 데드-볼륨을 형성하거나 구성 물질간 계면층을 많이 형성하여 부반응이 발생하기 쉽다. 따라서 많은 연구자들은 복합 전극 내 고체전해질 및 기타 첨가제의 분율을 감소시키고, 에너지 밀도를 극대화하기 위해 노력하고 있다.

실리콘 웨이퍼는 무첨가제, 무전해질, 무공극의 특징으로, 실리콘 기반 전극의 최대 에너지 밀도 달성이 가능한 궁극적인 형태이다. 현재까지 실리콘 웨이퍼를 리튬이온전지의 전극으로 활용하려는 시도가 있었으나, 제어할 수 없는 내부 응력 및 균열, 그로 인한 전기적 접촉을 잃는 문제로 실패하였다. 본 연구에서는 전고체전지에서 10 mAh cm^{-2}의 면적 용량을 달성할 수 있는 <110> 배향의 표면 처리된 얇은 실리콘 웨이퍼 전극을 개발하였다. 실리콘은 높은 리튬 전도도를 가져, 고체전해질의 도움없이 순수 실리콘 웨이퍼 전극 내부로 리튬 확산이

가능하도록 했다. 게다가 단결정의 웨이퍼 전극은 복합 전극 내의 입자 계면에서 기인하는 부반응을 효과적으로 제거할 수 있었다. <110> 배향 웨이퍼는 <100> 및 <111>과 같은 다른 배향 웨이퍼보다 빠른 리튬 확산이 가능하도록 했으며, 표면의 거칠기와 전극의 두께를 조절하여 사이클 특성을 향상시킬 수 있었다. 더 나아가 실리콘 웨이퍼의 표면과 기하학적 구조, 형태를 최적화하여 에너지 및 출력 밀도를 포함한 성능을 더욱 향상시킬 수 있을 것으로 기대된다.

주요어 : 전고체전지, 실리콘 음극, 무첨가제, 무전해질, 무공극, 고면적용량

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