



Ph.D. Dissertation

Indirectly Heated Phase Change Memory for Neuromorphic Analog Synapse Applications and Characterization of Crystallization Properties

뉴로모픽 아날로그 시냅스 응용 및 결정화 특성 분석을 위한 간접 가열 상변화 메모리

February 2025

Graduate School of Engineering Seoul National University Materials Science and Engineering

Inhyuk Choi

Indirectly Heated Phase Change Memory for Neuromorphic Analog Synapse Applications and Characterization of Crystallization Properties

Advisor: Prof. Sangbum Kim

Submitting a Ph.D. Dissertation of Materials Science and Engineering

November 2024

Graduate School of Engineering Seoul National University Materials Science and Engineering

Inhyuk Choi

Confirming the Ph.D. Dissertation written by Inhyuk Choi

December 2024

Chair	Min Hyuk Park	_(Seal)
Vice Chair	Sangbum Kim	_(Seal)
Examiner	<u>Hyejin Jang</u>	_(Seal)
Examiner	Yongwoo Kwon	_(Seal)
Examiner	Chanyoung Yoo	_(Seal)

Abstract

As artificial intelligence (AI) technology continues to advance, the demand for computing systems capable of processing the rapidly growing volumes of data and computational parameters with high speed and efficiency is steadily increasing. Traditional Von Neumann computing architectures face significant limitations in addressing these needs due to memory bottlenecks arising from the performance gap between logic and memory components. To overcome these challenges, alternative approaches such as storage-class memory (SCM), which bridges the performance gap in the conventional memory hierarchy, and in-memory computing, which enhances computational efficiency by performing operations directly within memory, are being extensively researched. Additionally, neuromorphic computing, which seeks to emulate the highly efficient processing mechanisms of the human brain, has garnered significant attention. In alignment with these developments, there is a growing demand for next-generation memory devices capable of supporting advanced computing paradigms.

Phase-change memory (PCM) stands as the most mature next-generation nonvolatile memory. However, conventional PCM faces limitations in optimizing device performance due to the trade-offs between device characteristics resulting from the integrated program and read path structure. In contrast, indirectly heated phasechange memory (IHPCM), where the program and read paths are electrically separated, allows for independent optimization of each path, thus facilitating the application of various optimization strategies tailored to the specific requirements of different applications. This study analyzed and evaluated the potential applications of IHPCM through the material and structural optimization.

The first section of this research demonstrated, through device simulation, that when IHPCM was applied to SCM, it could escape from the trade-offs between power consumption and operating speed that arose from device scaling in conventional PCM. Furthermore, it addressed the issue of endurance degradation caused by strong electric fields during program operation. Additionally, it was proposed that energy efficiency could be enhanced through the material and structural optimization, as well as the maximization of thermoelectric effects.

The second section highlighted the use of IHPCM as a tool for precise measurement and analysis of the crystallization characteristics and behaviors of phase-change materials under uniform temperature distributions, achieved through structural optimization via device simulations. By combining device fabrication and measurements with crystallization simulations, this section provided an in-depth analysis of electrical property changes and the nucleation and growth processes during crystallization.

In the final section, the utilization of IHPCM as an analog synaptic device for neuromorphic computing was proposed. A one-shot weight transfer scheme using IHPCM was introduced, demonstrating its ability to achieve fast and robust weight transfer under device-to-device and cycle-to-cycle variations. The IHPCM synaptic device was experimentally demonstrated to achieve a vast number of intermediate states through precise thermal control, facilitated by the absence of threshold switching. Furthermore, a circuit design for implementing the one-shot weight transfer scheme with minimal overhead was proposed, emphasizing its potential for efficient integration into neuromorphic hardware implementations. **Keyword :** Phase-change memory, Indirectly-heated phase change memory, Storage class memory, Thermoelectric effects, Crystallization, Neuromorphic computing, Analog synaptic device, Weight transfer

Student Number : 2018-20684

Inhyuk Choi

Table of Contents

Abstract	i
Table of Contents	iv
List of Figures	vii
List of Tables	xvi
List of Abbreviations	xvii

Chapter 1. Introduction1	
1.1. Overview and Issues on Phase-Change Memory 1	
1.2. Objective and Thesis Overview 5	
1.3. Bibliography7	,
Chapter 2. Simulation-based Analysis of IHPCM for Low Program	m
Current and Endurance Enhancement10	1
2.1. Introduction)
2.2. Experintal Methods 14	
2.3. Results and Discussion	
2.3.1 Calibration of the Electrothermal Simulation	
2.3.2 Optimization of the Vertical IHPCM Structure for Low Power	
Consumption20)
2.3.3 Comparison of $I_{RESET} - R_{SET}$ Trend between Conventional PCM	M
and Vertical IHPCM27	,
2.4. Conclusion	

2.5. Bibliography		
Chapter 3. Characterization of Crystallization Properties in Phase-		
Change Material Using IHPCM with Dual Heaters41		
3.1. Introduction		
3.2. Experintal Methods		
3.3. Results and Discussion		
3.3.1 IHPCM Characterization Device with Dual Heaters		
3.3.2 Evaluation of the IHPCM Characterization Device56		
3.3.3 Characterization of Crystallization Properties in Phase-Change		
Materials67		
3.3.4 Analysis of Crystallization Process in Phase-Change Materials		
3.4. Conclusion		
3.5. Bibliography		
Chapter 4. One-Shot Weight Transfer via Analog IHPCM Synapse for		
Efficient and Variation-Robust Neuromorphic Computing90		
4.1. Introduction 90		
4.2. Experintal Methods		
4.3. Results and Discussion		
4.3.1 One-Shot Weight Transfer Using IHPCM Synaptic Device96		
4.3.2 Device Performance of Analog IHPCM Synaptic Device99		
4.3.3 Proposal of One-Shot Weight Transfer Circuit111		
4.4. Conclusion		

4.5. Bibliography	
Chapter 5. Conclusion	
Abstract in Korean	

- Figure 1-1. (a) Temperature change within the PCM device according to the electrical pulse applied during reset, set, and read processes. b) Cross-sectional schematic of mushroom-type (left) and confined-type (right) PCM structures.
- **Figure 2-1.** (a) $I_{PROG} R_{SET}$ curve according to the size reduction of various PCM devices. $I_{PROG} \cdot R_{SET}$ product equations for the conventional (b) confined PCM structure and (c) wall-type PCM structure.
- Figure 2-2. Schematic of vertical IHPCM structure. Heat is generated by the Joule heating of the heater and subsequently transferred to the phase-change material via conduction. The heater and phase-change material are electrically separated by the inner insulator.
- **Figure 2-3.** Schematics of the 2D-axisymmetric confined PCM (left) and vertical IHPCM (right) structures used in the FEM simulation.
- Figure 2-4. (a) Geometry of the PCM device used for the calibration of the electrothermal model, based on previous experimental research.(b) Cell resistance and program current curves from the experimental results in the reference and the simulated results from our electrothermal model.

Figure 2-5. Schematic diagram of the vertical IHPCM structure with a single

heater. The simulation was performed using a 2D axisymmetric geometry.

- Figure 2-6. Cell resistance and reset current curves of (a) W and (b) TaN heaters as a function of the reduction in thermal and electrical conductivities. (c) Changes in reset programming voltage and power with varying thermal conductivity of TaN heater.
- Figure 2-7. (a) Schematic diagram of the vertical IHPCM structure. q_i represents the heat flux at each boundary, and the ratio of heat flux exiting to the PCL $(q_2/(q_0 + q_4))$ needed to be maximized for optimal thermal efficiency. (b) Variation in R_{PCM} (left) as a function of I_{RESET} and heat transfer rate (right) with increasing (b) L_H and (c) L_P .
- Figure 2-8. Normalized R_{SET} and I_{RESET} changes as a function of device scaling for conventional PCM and vertical IHPCM structures, with the radius of the heat-generating materials varying from 10nm to 1nm.
- Figure 2-9. Variation in R_{PCM} as a function of I_{RESET} with changes in the sign and magnitude of the S value, considering (a) only the Seebeck effect and (b) only the Peltier effect in the simulation.
 (c) Temperature distribution based on the difference in the S values of both heaters, with the simulation including only the Peltier effect.

- Figure 2-10. Normalized R_{SET} and I_{RESET} changes as a function of device scaling for conventional PCM and vertical IHPCM structures. Further reduction in I_{RESET} with consistent R_{SET} was demonstrated in the vertical IHPCM by maximizing the TE effects through an increase in the S_o value, with the heater radius (r_H) fixed at 4nm.
- Figure 3-1. Process flow for fabricating the IHPCM characterization device with dual heaters. The buried BH was fabricated using a W damascene process.
- Figure 3-2. (a) Temperature-dependent steady-state nucleation rate (I_{SS}) and growth velocity (v_G) for $Ge_2Sb_2Te_5$ derived from classical nucleation theory. Piecewise control functions for (b) stability and (c) diffusivity terms in the growth model.
- **Figure 3-3.** (a) Top view and (b) side view of the schematic diagram of the IHPCM structure with a single heater. (c) Bird's-eye view and (d) top view of the IHPCM geometry used in the 3D simulation. The temperature distribution, T(x, y, z), within the dashed PCL region was used to evaluate temperature uniformity.
- Figure 3-4. Comparison of the standard deviation (SD) as a function of average temperature (T_{Avg}) within the designated PCL region, with varying (a) W_{Space} , (b) W_{PCL} , and (c) dielectric layers (DL) between the heater lines (DL2) and between the PCL and heater

(DL3).

- Figure 3-5. (a) Side view and (b) temperature distribution along the xdirection on the top surface of the PCL for the IHPCM with a single heater. (c) Side view and (d) temperature distribution along the x-direction on the top surface of the PCL for the IHPCM with dual heaters.
- **Figure 3-6.** Top (left) and side (right) views of the (a) schematic diagram and (b) scanning electron microscope (SEM) image of the IHPCM characterization device with dual heaters. The PCL line was patterned with a width (W_{PCL}) of 3µm and a length (L_{PCL}) of 50µm.
- **Figure 3-7.** Temperature-dependent resistance variation of (a) the TH and (b) BH, measured using four-point probe structures. The TH and BH were fabricated with widths of 1µm and 3µm, respectively, both with a length of 40µm, and their TCR values (α_{TH}, α_{BH}) were extracted. Resistance variations as a function of heater length for (c) the TH and (d) BH, measured using the transfer length method (TLM) structure with a width of 140µm to determine the contact resistance (R_c) of the heaters.
- Figure 3-8. The electrical measurement setup for measuring V_{TH}^{RESET} applied across the TH.
- Figure 3-9. (a) Bird's-eye view of the IHPCM geometry utilized in the 3D simulation. (b) Electrical and thermal boundary conditions

applied to each pad in the simulation.

- Figure 3-10. (a) Simulated temperature distribution along the x-z plane at $V_{BH} = 3V$. T_{PCM} was defined as the average temperature within a designated 3D region of PCL, extending three times the width of the TH, to ensure sufficient coverage of the amorphous volume. (b) Variation of T_{PCM} as a function of the applied V_{BH} .
- Figure 3-11. (a) Electrical measurement setup and (b) pulse conditions used to evaluate the thermal time constant (τ) and heating rate of the IHPCM characterization device. (c) Transient voltage changes across the oscilloscope channels. V_{OSC}^{V1} and V_{OSC}^{V2} represents the voltage divided across the 50 Ω impedance of the oscilloscope in response to V_{Heat} and V_{Read} , respectively.
- Figure 3-12. (a) Electrical measurement setup for characterizing T_C . Change in R_{PCM} as a function of V_{BH} for (b) $Ge_2Sb_2Te_5$ and (c) Sb_2Te_3 at varying heating rates. T_C was defined as the point where the slope of the R_{PCM} change was maximized.
- Figure 3-13. (a) Electrical measurement setup and (b) pulse conditions used for transient measurements to characterize t_c .
- Figure 3-14. Transient voltage changes measured across the oscilloscope channel for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . The t_c was defined as the interval between the application of V_{BH}^{SET} and the point where V_{OSC1}^{CH2} saturated.

- Figure 3-15. Transient voltage changes measured across the oscilloscope channel for $Ge_2Sb_2Te_5$ using (a) a single pulse and (b) multiple pulses, with $V_{BH}^{SET} = 2.82V$ and the total pulse duration kept constant.
- Figure 3-16. (a) Multi-pulse measurement setup for characterizing the t_c as a function of T_{PCM} . (b) Variation of R_{PCM} with respect to the number of read operations. The t_c was determined by the product of the pulse width of V_{BH}^{SET} and the number of pulses needed to reach the set state.
- Figure 3-17. The measured t_c as a function of T_{PCM} for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . The E_a was extracted using the Arrhenius equation.
- Figure 3-18. (a) Simulation flow for the fully coupled 2D simulation. The heat source is extracted from the 3D simulation and applied to the heaters to generate the heat induced by Joule heating effects.
 (b) Time-dependent heat source data utilized in the set process.
 (c) Schematic diagram of the geometry and boundary conditions employed in the 2D simulation.
- **Figure 3-19.** (a) R_{PCM} as a function of T_{PCM} from electrical measurements and fully coupled simulations under a heating rate of 1K/s. (b) The simulated distribution of $\|\overrightarrow{CD}\|_1 (= CD_1 + CD_2 + CD_3)$ as T_{PCM} was increased from 390K to 419K.

- Figure 3-20. (a) Measurement setup for comparing the crystallization behavior under DC sweeps between the SH and IH. Changes in R_{PCM} as a function of V_{PCM} (SH) and V_{BH} (IH) for (b) $Ge_2Sb_2Te_5$ and (c) Sb_2Te_3 .
- Figure 4-1. Process flow for the fabrication of the IHPCM synaptic device.
- Figure 4-2. (a) Top view of the schematic diagram of the IHPCM synapses. (b) Electric pulse timing diagram for the simultaneous program and read operations in OSWT. (c) Transient variation of G_{PCM} during the program process. In the OSWT scheme, the program pulse is terminated once G_{PCM} reaches the G_{Target} .
- Figure 4-3. Top (left) and side (right) views of (a) the schematic diagram and(b) the scanning electron microscope (SEM) image of the IHPCM synaptic device.
- Figure 4-4. Electrical measurement setup used to characterize the device properties of the IHPCM synapse.
- Figure 4-5. (a) Resistance of the heater measured as a function of stage temperature increase using a four-point probe structure. The four-point probe structure was fabricated with a width of 1µm and a length of 40µm. (b) The estimated temperature within the heater as a function of applied power. The measured TCR value (α_H) was used for the estimation.

Figure 4-6. R_{PCM} variations of the IHPCM synaptic device during repeated

reset and set operations for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 .

- Figure 4-7. (a) Top (left) and side (right) views of the SEM image of the IHPCM synaptic device with a buried heater. R_{PCM} variations of the IHPCM synaptic device with the buried heater during repeated reset and set operations for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 .
- Figure 4-8. R_{PCM} (left) and G_{PCM} (right) variations under gradual set operations with varying V_{SET} for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . A decrease in V_{SET} resulted in more linear changes in G_{PCM} and an increased number of intermediate states.
- **Figure 4-9.** The changes in G_{PCM} by the gradual set operation of analog IHPCM synapses for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 .
- **Figure 4-10.** The variations in R_{PCM} over 10 cycles of repeated gradual set operations for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . The IHPCM synaptic device with $Ge_2Sb_2Te_5$ exhibited substantial variation in intermediate states over cycles, attributed to the stochastic nature of nucleation, whereas Sb_2Te_3 demonstrated small variations, as its primary crystallization occurred at the amorphous-crystalline phase boundary.
- Figure 4-11. Circuit diagram of the proposed OSWT circuit, featuring (a) a voltage divider and (b) amplifiers for converting I_{PCM} into an analog voltage prior to the comparator node.

- Figure 4-12. (a) Circuit diagram utilized in the LTspice simulation. (b) Voltage variations at each node over time during OSWT operations. V_{REF} was set to 1V, with V_{PCM} and V_{SET} monitored at the comparator input node and the output node of the analog switch, respectively.
- Figure 4-13. (a) Electrical measurement setup for implementing OSWT operation using the IHPCM synapse and amplifier-based OSWT circuit. (b) The pulse timing diagram of V_{SET} and V_{Read} utilized for OSWT operations.
- Figure 4-14. Transient variation of V_{SET} and V_{PCM} during OSWT operations using an amplifier-based OSWT circuit and the IHPCM synaptic device.

- Table 2-1. Material properties employed in the simulation of both confined

 PCM and vertical IHPCM structures.
- Table 2-2. Thermal and electrical conductivities of both W and TaN heaters

 used in the simulation. It was assumed that both conductivities

 decreased in accordance with the Wiedemann-Franz law.
- Table 2-3. Comparison of the program voltage, current density, and program

 power between confined PCM and vertical IHPCM structures.
- Table 3-1. Material properties utilized in the electrothermal and crystallization models.
- Table 3-2. Thermal boundary resistances at interfaces between materials

 utilized in the electrothermal model.
- **Table 3-3.** Calculated T_{PCM} , standard deviation, and spatial variation based on the T(x,y,z) data within the designated 3D region of PCL.

List of Abbreviations

AI	Artificial Intelligence
BH	Bottom Heater
CD	Crystal Density
СМР	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
DL	Dielectric Layer
DRAM	Dynamic Random-Access Memory
ECRAM	Electrochemical Random-Access Memory
FEM	Finite Element Method
GND	Ground
GPIB	General-Purpose Interface Bus
GST	$Ge_2Sb_2Te_5$
IHPCM	Indirectly Heated Phase-Change Memory
MLC	Multi-Level Cells
OSWT	One-Shot Weight Transfer
PCL	Phase-Change Layer
PCM	Phase-Change Memory
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PR	Photoresist
ReLU	Rectified Linear Unit

RF	Radio Frequency
RIE	Reactive Ion Etching
RRAM	Resistive Random-Access Memory
SCM	Storage-Class Memory
SD	Standard Deviation
SEM	Scanning Electron Microscope
SH	Self-Heating
SPA	Semiconductor Parameter Analyzer
SPICE	Simulation Program with Integrated Circuit Emphasis
TBR	Thermal Boundary Resistance
TCR	Temperature Coefficients of Resistance
TE	Thermoelectric
TH	Top Heater
TLM	Transfer Length Method
VMM	Vector-Matrix Multiplications

Chapter 1. Introduction

1.1. Overview and Issues on Phase-change memory

As artificial intelligence (AI) technology continues to advance, there is an increasing demand for computing systems capable of processing the rapidly growing volumes of data and computational parameters with high speed and efficiency. [1],[2] Traditional von Neumann computing architectures face limitations in meeting these demands due to the memory bottleneck caused by the performance gap between logic and memory components. To address this challenge, research has focused on alternative approaches, such as storage-class memory (SCM), which bridges the performance gap in conventional memory hierarchies, and in-memory computing [3],[4], which enhances computational efficiency by performing operations directly within memory components. Moreover, the innovative approach of neuromorphic computing, which seeks to emulate the highly efficient processing mechanisms of the human brain, has gained substantial attention [5]-[9]. In tandem with these developments, extensive research has been conducted on next-generation memory devices capable of supporting these advanced computing architectures.

Phase-change memory (PCM) is the most mature technology among emerging non-volatile memory devices, and Intel commercialized 3D Xpoint memory composed of phase-change material and selector devices in 2017 for SCM applications [10]. PCM has several advantages such as a large on/off ratio of $10^2-10^3 \times$, high operation speed (tens of nanoseconds), scalability (sub-10nm), high endurance $(10^{10}-10^{12} \text{ cycles})$, and high data retention $(210^{\circ}\text{C}, 10 \text{ years})$ [11], [12]. Electrical pulses are applied to the PCM to induce Joule heating within the phase-change material, causing a reversible transition between the crystalline and amorphous phases to store information [13]. PCM operates in three main processes: reset, set, and read (Figure 1-1 (a)). In the reset process, by applying an electric pulse with a large amplitude and short duration, the temperature in the phase-change material is raised above its melting point (T_{Melt}) owing to the Joule heating effects. Thereafter, the molten phase is rapidly quenched to become a high resistance amorphous phase. During the set process, sufficient Joule heating occurs after threshold switching, where the application of a voltage exceeding the threshold voltage (V_{th}) leads to a rapid increase in electrical conductivity from the initial highresistance amorphous state. By applying an electric pulse with medium amplitude and long duration, the temperature in the phase-change material is increased above the crystallization temperature (T_c) , resulting in a low resistance crystalline phase through the crystallization process. In the read process, an electrical pulse with low amplitude is applied, such that the phase of the material remains unaffected. Chalcogenide materials are used as the phase-change materials, and typically, Ge-Sb-Te alloy along the pseudo-binary line between GeTe and Sb_2Te_3 (for example, $Ge_2Sb_2Te_5$) is used owing to its high switching speed. Representative device structures are mushroom-type with a small-diameter bottom heater and confinedtype with the scaled volume of phase-change material and enhanced thermal efficiency (Figure 1-1 (b)).

In contrast to conventional PCM structures, which induce heating within the phase-change material itself (Self-heating), research has been proposed on indirect heating PCM (IHPCM), which utilizes an external heater to generate heat and induce phase change. Self-heating- and IH-PCM structures differ in both their structure and device operation. A self-heating PCM structure features a two-terminal configuration, where the program and read paths are integrated, whereas an IHPCM structure

consists of a four-terminal configuration, where the heater material that generates heat and the PCM component responsible for the read process is electrically separated. Furthermore, while self-heating PCM requires threshold switching during the SET operation, IHPCM does not necessitate threshold switching, as it does not generate heat within the phase-change material. So far, the IHPCM structure has been proposed as a radio frequency (RF) switch [14]-[17] or characterization tool [18]-[20]. However, its scope of application remains limited, highlighting the need for further evaluations to expand the potential applications of IHPCM devices.



Figure 1-1. (a) Temperature change within the PCM device according to the electrical pulse applied during reset, set, and read processes. b) Cross-sectional schematic of mushroom-type (left) and confined-type (right) PCM structures.

1.2. Objective and Thesis Overview

This thesis focuses on the evaluation and optimization of IHPCM for various applications. IHPCM enables the independent optimization of both the heater and phase-change material components, in terms of structure and material properties, due to its separate program and read paths. Leveraging this advantage, the ways in which IHPCM can be optimized for various applications have been extensively analyzed.

Chapter 2 analyzes optimization strategies for using IHPCM in SCM applications. Conventional PCM devices face issues such as the trade-off between power consumption and operating speed, which arise from device scaling when used in memory-type SCM applications. Moreover, endurance degradation caused by the strong electric fields applied during a program operation is a significant concern. The structural advantages of IHPCM are proposed to substantially mitigate both the trade-off and endurance degradation issues. Furthermore, based on device simulation analysis, it is suggested that the operating efficiency can be improved through the material and structural optimization, as well as the maximization of additional heating via the thermoelectric effect.

Chapter 3 proposes the use of IHPCM as a comprehensive characterization tool for the precise measurement of crystallization characteristics and analysis of crystallization behavior under uniform temperature distributions through structural optimization. The IHPCM structure was optimized through simulations to generate a uniform temperature distribution within the phase-change region and subsequently fabricated. By combining the electrothermal model with electrical measurements, the key crystallization characteristics and behaviors of phase-change materials were precisely characterized. Furthermore, a fully coupled device simulation incorporating a crystallization model was integrated with the measurement results, enabling an in-depth analysis of electrical property changes, as well as the nucleation and growth processes during crystallization.

Chapter 4 assesses the use of IHPCM as an analog synapse device in neuromorphic computing. The IHPCM synapse device is fabricated and demonstrates a large number of intermediate states through precise thermal control, facilitated by the absence of threshold switching. Furthermore, a one-shot weight transfer scheme utilizing the IHPCM synapse is proposed, enabling fast and robust weight transfer under variations. A circuit for the one-shot weight transfer scheme is designed, emphasizing its potential for effective integration into neuromorphic hardware with minimal overhead.

Finally, Chapter 5 presents the conclusion of the thesis.

1.3. Bibliography

[1] X. Xu et al., "Scaling for edge inference of deep neural networks." *Nature Electronics* 1.4 (2018): 216-222.

[2] M. A. Zidan et al., "The future of electronics based on memristive systems." *Nature electronics* 1.1 (2018): 22-29.

[3] A. Sebastian et al., "Memory devices and applications for in-memory computing." *Nature nanotechnology* 15.7 (2020): 529-544.

[4] S. Yu et al., "Compute-in-memory chips for deep learning: Recent trends and prospects." *IEEE circuits and systems magazine* 21.3 (2021): 31-56.

[5] K. Byun et al., "Recent advances in synaptic nonvolatile memory devices and compensating architectural and algorithmic methods toward fully integrated neuromorphic chips." *Advanced Materials Technologies* 8.20 (2023): 2200884.

[6] G. W. Burr et al., "Neuromorphic computing using non-volatile memory." *Advances in Physics: X* 2.1 (2017): 89-124.

[7] S. Yu, "Neuro-inspired computing with emerging nonvolatile memorys." *Proceedings of the IEEE* 106.2 (2018): 260-285.

[8] Q. Wan et al., "Emerging artificial synaptic devices for neuromorphic computing." *Advanced Materials Technologies* 4.4 (2019): 1900037.

[9] J. Zhu et al., "A comprehensive review on emerging artificial neuromorphic devices." *Applied Physics Reviews* 7.1 (2020).

 [10] R. Smith, "Intel Announces Optane Storage Brand For 3D XPoint Products,"
 AnandTech, https://www.anandtech.com/show/9541/ intel-announces-optanestorage-brand-for-3d-xpoint-products.

[11] G. W. Burr et al., "Phase change memory technology." Journal of Vacuum

7

Science & Technology B 28.2 (2010): 223-262.

[12] G. W. Burr et al., "Recent progress in phase-change memory technology." *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 6.2 (2016): 146-162.

[13] H-S. P. Wong et al., "Phase change memory." *Proceedings of the IEEE* 98.12 (2010): 2201-2227.

[14] N. El-Hinnawy et al., "A four-terminal, inline, chalcogenide phase-change RF switch using an independent resistive heater for thermal actuation." *IEEE Electron Device Letters* 34.10 (2013): 1313-1315.

[15] E. Yalon et al., "Energy-efficient indirectly heated phase change RF switch." *IEEE Electron Device Letters* 40.3 (2019): 455-458.

[16] Z. Hou et al., "Low Energy Consumption GeTe Phase-Change Radio Frequency Switch With Direct Heating of Conductive Filament." *IEEE Electron Device Letters* (2023).

[17] H. J. Li et al., "A Novel Phase Change Material RF Switch with 16nm
Technology to Achieve Low Voltage and Low Ron* Coff for mmWave." 2024 IEEE
Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits). IEEE,
2024.

[18] S. Kim et al., "Thermal disturbance and its impact on reliability of phasechange memory studied by the micro-thermal stage." *2010 IEEE International Reliability Physics Symposium*. IEEE, 2010.

[19] R. Jeyasingh et al., "Ultrafast characterization of phase-change material crystallization properties in the melt-quenched amorphous phase." *Nano letters* 14.6 (2014): 3419-3426.

[20] N. Wainstein et al., "Indirectly heated switch as a platform for nanosecond

probing of phase transition properties in chalcogenides." *IEEE Transactions on Electron Devices* 68.3 (2021): 1298-1303.

Chapter 2. Simulation-based Analysis of IHPCM for Low Program Current and Endurance Enhancement

2.1. Introduction

Phase-change memory (PCM) is one of the next-generation memory devices as a storage-class memory that can fill the gap between DRAM and NAND flash memory [1]. It is also used as a synaptic device in neuromorphic computing hardware for more power-efficient operation beyond the existing Von Neumann architecture [2]-[4]. In the reset process of the PCM, a large amount of energy is required to raise the temperature above the melting point of the phase-change material. In general, the power consumption has been reduced by decreasing the contact area between the phase-change material and the bottom electrode material [5], [6], or the volume of the phase-change material [7]. However, increasing thermal resistance through size reduction leads to an increase in electrical resistance, resulting in a trade-off between the reset programming current (I_{Prog}) and set resistance (R_{SET}) as shown in Figure 2-1 (a) [8], [9]. Doping of phase-change materials for reduction of thermal conductivity also decreases electrical conductivity due to the Wiedemann-Franz law, leading to an unavoidable trade-off in conventional PCM structures with integrated programming and reading paths (Figure 2-1 (b), (c)). The increase in R_{SET} due to the trade-off slows down the read speed [10], which must be addressed. In addition, as the PCM cell is repeatedly operated, the gradual movement of constituent atoms induces endurance failure. One of its main driving forces is a high electric field formed in the phase-change material during programming [11]–[14]. Endurance of PCM has been enhanced to $10^9 \sim 10^{12}$ cycles by inhibiting atomic movement by material doping [15], [16], or void-free confined structure [17], [18]. However, the high electric field formed in the PCM structures with integrated paths still causes electromigration and limits the enhancement of endurance property.

Here, we propose a vertically oriented indirectly heated PCM (IHPCM) structure with the electrically separate program and read paths. The proposed structure can reduce the program power without increasing the R_{SET} and slowing down the read speed, which breaks out of the trade-off in the existing structures with the unified program and read paths. Also, we confirm that the thermoelectric (TE) effects can be optimized independently from the choice of phase-change material in the vertical IHPCM structure to further reduce power consumption. Since the high electric field in the program path is decoupled with phase-change material in the read path, we expect that the endurance could be enhanced by inhibiting the electromigration.

A schematic diagram of the structure and operation of the vertical IHPCM structure is shown in Figure. 2-2. In the program (reset or set) process, sufficiently high electrical pulses are applied to the top electrode of the heater to generate heat by Joule heating. At this time, the inner insulator surrounding the heater prevents current from flowing into the phase-change material, unlike the conventional PCM structures. The heat generated by the heater is transferred to the phase-change material through the inner insulator, causing a phase change. During the read process, a small amplitude electrical pulse is applied to the top electrode of the phase-change material to measure the resistance value.



Figure 2-1. (a) $I_{PROG} - R_{SET}$ curve according to the size reduction of various PCM devices. $I_{PROG} \cdot R_{SET}$ product equations for the conventional (b) confined PCM structure and (c) wall-type PCM structure [8].



Figure 2-2. Schematic of vertical IHPCM structure. Heat is generated by the Joule heating of the heater and subsequently transferred to the phase-change material via conduction. The heater and phase-change material are electrically separated by the inner insulator.

2.2. Experimental Methods

The program performance of the vertical IHPCM structure was simulated through COMSOL Multiphysics based on the finite element method (FEM) [19]. The simulation was conducted solely for the reset process, which necessitated the highest power consumption. Since the vertical IHPCM structure exhibits a thermal time constant similar to that of existing PCM structures, we assumed that the portion of the phase-change material above its melting point became an amorphous phase by rapid quenching. The current continuity (1) and heat transport (2) equations with the addition of TE effects are solved in the simulation

$$\nabla \cdot J = -\nabla \cdot (\sigma(\nabla V + S\nabla T)) = 0 \tag{1}$$

$$dC_P \frac{dT}{dt} - \nabla \cdot (\kappa \nabla T) = \frac{J \cdot J}{\sigma} - TJ \cdot \Delta S - TJ \cdot \frac{dS}{dT} \nabla T$$
(2)

$$\Pi = TS \tag{3}$$

$$\mu_T = T \cdot \frac{dS}{dT} \tag{4}$$

where J is the current density, σ is the electrical conductivity, V is the electric potential, S is the Seebeck coefficient, T is the temperature, d is the mass density, C_P is the heat capacity, κ is the thermal conductivity, Π is the Peltier coefficient, μ_T is the Thomson coefficient.

As shown in Figure 2-3, the reset performance of the vertical IHPCM structure was compared with that of the conventional confined PCM structure through simulation. The height and radius of the heater and phase-change material $Ge_2Sb_2Te_5$ (GST) and the total cell size of both structures were set equal. The heater needs to be a material that is stable at high temperatures such as a refractory metal with a high melting point ($T_m > 3000K$). In addition, two heater materials (H_A and H_B) were used to generate additional heat through the TE effects at the
interface in the vertical IHPCM structure. Both heater materials were assumed to have material properties based on tantalum nitride (TaN), which is a quiet resistive conductor, with the only difference being in their Seebeck coefficient (S) values. The electrical interface resistance between the heater and the electrodes was not considered in this study, as this cell was designed to generate most of the heat at the center of the heater, rather than at the interface. The temperature dependence of electrical, thermal conductivities, and S values for GST were included. The material properties used in the simulations are listed in Table. 2-1 [20]–[25]. In the reset process, an electrical pulse with a duration of 100ns, rise/fall times of 25ns, and an amplitude of 3V was applied.



Figure 2-3. Schematics of the 2D-axisymmetric confined PCM (left) and vertical IHPCM (right) structures used in the FEM simulation.

Table 2-1. Material properties employed in the simulation of both confined PCM

 and vertical IHPCM structures.

	$\sigma [S/m]$	$\kappa [W/m \cdot K]$	S [µV/K]
Ge ₂ Sb ₂ Te ₅ (Crystal)	[20]	[21]	0.10989 * (T - 300) + 30
$Ge_2Sb_2Te_5$ (Amorphous)	0.1	0.19	N/A
Heater A ($S_0: 100 \rightarrow 500$)	1.67e5	3.5	S ₀ @ 300K S ₀ - 100 @ 3000K
Heater B ($S_0: 100 \rightarrow 500$)	1.67e5	3.5	$-S_0 @ 300K$ $-S_0 + 100 @ 3000K$
SiO ₂	1e-14	1.38	N/A
TiN	5e5	13	-100

2.3. Results and Discussion

2.3.1 Calibration of the Electrothermal Simulation

To calibrate the accuracy of the electrothermal model, simulations were conducted under conditions analogous to those of a previous experimental study [20], incorporating Joule heating and thermoelectric effects (Figure 2-4 (a)). In our simulation, however, we modified the temperature dependence of the thermal conductivity of GST, as the phonon contribution was overestimated, and additionally included the S value of TiN [21]. As shown in Figure. 2-4 (b), the cell resistance against program current in the reference experiment and our simulation showed good agreement, with minor differences in negative polarity, which could be attributed to undisclosed parameters, such as boundary conditions and the temperature dependence of the electrical conductivity of GST in the reference study.



Figure 2-4. (a) Geometry of the PCM device used for the calibration of the electrothermal model, based on previous experimental research [20]. (b) Cell resistance and program current curves from the experimental results in the reference and the simulated results from our electrothermal model.

2.3.2 Optimization of the Vertical IHPCM Structure for Low Power Consumption

A simulation model incorporating the Joule heating effect was utilized to evaluate optimization strategies from material and structural perspectives for reducing power consumption during the reset operation of vertical IHPCM. The simulations were conducted using a device structure featuring a single heater, as illustrated in Figure 2-5. Tungsten (W) and TaN were chosen as heater materials due to their stability in high-temperature environments as refractory metals. The electrical and thermal conductivities of metals, governed by the abundance of free electrons, are interrelated through the Wiedemann-Franz law, which establishes their proportionality to temperature.

$$\frac{\kappa}{\sigma} = LT \tag{5}$$

Here, L is the Lorenz number, serving as the proportionality constant and maintaining a consistent value across varying temperatures. Similar to the approach used in conventional PCM, reducing the thermal conductivity of the heater (e.g. material doping) increases thermal resistance, which can lead to a reduction in power consumption. For both W and TaN heaters, the current and power required during the reset process were evaluated in response to the reduction in thermal conductivity. It was assumed that the electrical conductivity would also decrease in accordance with the Wiedemann-Franz law (Table 2-2). The Lorenz number for each heater material was calculated based on the known values of electrical and thermal conductivities at room temperature. The simulation results showed that a decrease in both electrical and thermal conductivities for both heaters led to a reduction in the reset current (Figure 2-6 (a), (b)). Additionally, it was observed that due to the

decrease in electrical conductivity, the required voltage gradually increased, while the power decreased until reaching a certain level of thermal and electrical conductivity values (Figure 2-6 (c)). Therefore, it was confirmed that heater materials with sufficiently low electrical and thermal conductivities are preferable for reducing power consumption. Consequently, TaN was selected as the heater material for the subsequent evaluation. Since the heat generated by the heater is conducted to the phase-change layer (PCL) to induce the phase change, using a material with low electrical conductivity but high thermal conductivity for the dielectric layer (DL1) between the heater and the PCL can help reduce power consumption.

To reduce power consumption in vertical IHPCM, structural optimization is also required to maximize the transfer of heat generated by the heater to the PCL. Decreasing the radius or increasing the length of the heater, electrode, and PCL can increase thermal resistance, thereby lowering programming power. Furthermore, minimizing the thickness of the DL1 between the heater and the PCL, as long as electrical coupling does not occur, enhances the heat transfer to the PCL. Moreover, the thermal efficiency can be influenced by the relationship between the lengths of the heater and the PCL, which may substantially affect power consumption. To evaluate this effect, as shown in Figure 2-7 (a), the heat flux at each boundary was analyzed while varying the lengths of the heater (L_H) and the PCL (L_P) , keeping all other dimensions fixed. Increasing the L_H while keeping the L_P constant resulted in a decrease in reset current (I_{RESET}) (Figure 2-7 (b)). This reduction was attributed to the increased thermal resistance of the longer heater, which reduced the heat transfer rate to the heater's electrodes. However, when the L_H exceeded L_P , the rate of I_{RESET} reduction gradually diminished, as more heat was dissipated toward

the PCL's electrode rather than being effectively transferred to the PCL. When L_P was increased while keeping L_H fixed, the proportion of heat flux transferred to the PCL gradually increased, leading to a significant reduction in I_{RESET} until L_P matched L_H (Figure 2-7 (c)). However, once the L_P became longer than L_H , the rate of I_{RESET} reduction decreased, likely because more heat flux was dissipated through the heater's electrodes.



Figure 2-5. Schematic diagram of the vertical IHPCM structure with a single heater. The simulation was performed using a 2D axisymmetric geometry.

Table 2-2. Thermal and electrical conductivities of both W and TaN heaters used in the simulation. It was assumed that both conductivities decreased in accordance with the Wiedemann-Franz law.

Tungsten (W)		Tantalum Nitride (TaN)		
$\kappa [W/m \cdot K]$	$\sigma[S/m]$	$\kappa [W/m \cdot K]$	$\sigma[S/m]$	
173	1.77e7	3.5	1.67e5	
156	1.60e7	3.2	1.53e5	
139	1.42e7	2.9	1.38e5	
122	1.25e7	2.6	1.24e5	
105	1.07e7	2.3	1.10e5	
88	9.00e6	2	9.54e4	
71	7.26e6	1.7	8.11e4	
54	5.52e6	1.4	6.68e4	
37	3.79e6	1.1	5.25e4	
20	2.05e6	0.8	3.82e4	
3	3.07e5	0.5	2.39e4	

 $*L_W = 3.28 \times 10^{-8} [W\Omega K^{-2}], \ L_W = 7.03 \times 10^{-8} [W\Omega K^{-2}]$



Figure 2-6. Cell resistance and reset current curves of (a) W and (b) TaN heaters as a function of the reduction in thermal and electrical conductivities. (c) Changes in reset programming voltage and power with varying thermal conductivity of TaN heater.



Figure 2-7. (a) Schematic diagram of the vertical IHPCM structure. q_i represents the heat flux at each boundary, and the ratio of heat flux exiting to the PCL $(q_2/(q_0 + q_4))$ needed to be maximized for optimal thermal efficiency. (b) Variation in R_{PCM} (left) as a function of I_{RESET} and heat transfer rate (right) with increasing (b) L_H and (c) L_P .

2.3.3 Comparison of $I_{RESET} - R_{SET}$ Trend between Conventional PCM and Vertical IHPCM

By incorporating only the Joule heating effect in the simulation model, we first compared the changes in R_{SET} and I_{RESET} with those observed in conventional PCM structures [8], [9] by reducing the radius of heat-generating materials (Figure 2-8). For conventional PCM structures, I_{RESET} decreased as the radius decreased, but a trade-off occurred, leading to an increase in R_{SET} . However, in the vertical IHPCM structure, R_{SET} remained constant even as the I_{RESET} decreased. On the other hand, since the heat was dissipated during conduction from the heater to the phase-change material, more program power was required for the vertical IHPCM structure compared to the confined PCM structure, which was designed for high thermal efficiency (See Table 2-3) [26]. Therefore, the TE effects were applied as an additional heat source to enhance the energy efficiency of the vertical IHPCM structure.

The TE effects encompass the Seebeck, Peltier, and Thomson effects, all of which are dependent on the S value [27]. In our simulation-based investigation, we sought to determine the optimal conditions for reducing the I_{RESET} by varying the S value $(S_0=100 \text{ to } 500)$. The sign of the S value is an inherent material property that represents the direction of additional current flow relative to the temperature gradient (Seebeck effect). A positive S value results in the generation of additional current in the same direction as the temperature gradient, while a negative S value induces current flow in the opposite direction. As shown in Figure 2-9 (a), the results demonstrated that in the vertical IHPCM structure under positive polarity, maximizing the Seebeck effect by assigning a positive S value to heater A and a negative S value to heater B effectively reduced the I_{RESET} . At the interface of two different materials, additional heating or cooling occurs to compensate for the difference in heat flux due to the disparity in the Peltier coefficient (Equation (3)) of each material (Peltier effect) [28]. In the vertical IHPCM structure, Peltier heating occurred at the interface when the difference in S value ($\Delta S = S_A - S_B$) was positive at positive polarity, resulting in a reduction in I_{RESET} (Figure 2-9 (b) - circle, (c)). Conversely, when ΔS exhibited a negative value, Peltier cooling occurred, leading to an increase in I_{RESET} (Figure 2-9 (b) - triangle, (c)). Moreover, since the S value is temperature-dependent, additional heating or cooling is induced in the material under a temperature gradient (Thomson effect). As the temperature at the interface of the two heaters became the highest due to Joule heating, Thomson heating occurred in each heater when the sign of the Thomson coefficient (Equation (4)) was negative on heater A and positive on heater B under positive polarity. Therefore, in our simulation, the S value was assumed to change linearly with temperature for simplicity, and the conditions for Thomson heating were applied to both heaters (see Table 2-1).

The change in R_{SET} as a function of I_{RESET} reduction was compared using the electrothermal simulation incorporating both the Joule heating effect and the TE effects, as shown in Figure 2-10. In the vertical IHPCM structure with a fixed radius of heaters (r_H =4nm), the S value was set to positive for heater A and negative for heater B, with the difference in values increasing. The results indicated that the I_{RESET} decreased further as the magnitude of the S value increased, while the R_{SET} still remained constant. When S_0 set to 500, the I_{RESET} was reduced by 70% compared to other conventional PCM structures. However, in the confined PCM structure, the reduction in I_{RESET} due to the thermoelectric effects was minimal.

Therefore, it was demonstrated that the TE effects could effectively enhance the energy efficiency of the vertical IHPCM structure.

Simulation analysis showed that resistive conductors with large S values were required as heater materials in the vertical IHPCM structure. Conventional thermoelectric materials have been developed to increase the figure of merit $(ZT = (S^2\sigma/\kappa)T)$, which requires high electrical conductivity to suppress Joule heating [29]–[31]. However, it is challenging to find a material with high ZT since high electrical conductivity results in a low Seebeck coefficient due to their opposite dependence on the carrier concentration. Fortunately, the vertical IHPCM structure requires heaters with a high Seebeck coefficient and relatively low electrical conductivity, making it much easier to find appropriate thermoelectric materials [32].

Innovative materials, such as 2D materials, are currently being explored as effective thermal barriers [33], [34], and can further enhance the energy efficiency of the vertical IHPCM structure. The thermal barrier between the electrodes and the heater can improve energy efficiency in a manner similar to that demonstrated in previous studies [35]–[37]. 2D materials can be engineered to exhibit low thermal conductivity while maintaining high electrical conductivity, achieved by optimizing acoustic mismatch or phonon dispersion mismatch at the interface [38]–[40]. Additionally, thermal boundary resistance (TBR), which arises from the difference in thermal carrier transport between two materials, serves as an effective thermal barrier [41]. A previous study demonstrated that applying a graphene layer, which exhibits a large TBR with phase-change material, helped reduce the I_{RESET} [42]. Therefore, further increases in energy efficiency could be realized by incorporating electrodes or 2D thermal barrier materials that possess a large TBR in relation to the heater.

Independent optimization of the inner and outer insulators can further enhance both the energy efficiency and density of the vertical IHPCM structure. An inner insulator with relatively high thermal conductivity and TBR with the phase-change material and heater is more favorable, as it facilitates more efficient heat transfer to the phase-change material. Conversely, excessive heat transfer to adjacent cells can compromise device reliability and increase the bit cell size [43]. Therefore, an outer insulator with low thermal conductivity and high TBR with the phase-change material is necessary to reduce the overall size of the vertical IHPCM structure.

As PCM cells undergo repeated operations, the gradual movement of constituent atoms leads to endurance failure. Electrostatic forces and wind forces are primary contributors to atomic migration [11]–[14], alongside other driving forces such as thermal and mechanical stress and diffusion [44]–[46]. The simulation results demonstrated that the current density generated in the phase-change material during programming was significantly reduced in the vertical IHPCM structure (Table 2-3). Therefore, since electrical atomic flux is directly proportional to current density [44], the vertical IHPCM structure could exhibit enhanced cyclic endurance compared to conventional PCM structures.



Figure 2-8. Normalized R_{SET} and I_{RESET} changes as a function of device scaling for conventional PCM and vertical IHPCM structures, with the radius of the heat-generating materials varying from 10nm to 1nm.

Table 2-3. Comparison of the program voltage, current density, and program powerbetween confined PCM and vertical IHPCM structures.

$(\Lambda t r - \Lambda n m)$	V _{Program}	J [MA/cm ²]		P _{Program}
	[V]	Heater	GST	$[\mu W]$
Confined	2.02	N/A	1 12-2	164 77
PCM cell	2.73	IN/A	1.1202	104.77
Vertical	1.00	136.2	22.0	220.01
IHPCM cell	1.09	4.5062	20-9	239.01



Figure 2-9. Variation in R_{PCM} as a function of I_{RESET} with changes in the sign and magnitude of the S value, considering (a) only the Seebeck effect and (b) only the Peltier effect in the simulation. (c) Temperature distribution based on the difference in the S values of both heaters, with the simulation including only the Peltier effect.



Figure 2-10. Normalized R_{SET} and I_{RESET} changes as a function of device scaling for conventional PCM and vertical IHPCM structures. Further reduction in I_{RESET} with consistent R_{SET} was demonstrated in the vertical IHPCM by maximizing the TE effects through an increase in the S_0 value, with the heater radius (r_H) fixed at 4nm.

2.4. Conclusion

This study demonstrates that the vertical IHPCM structure, with the separated program and read paths, resolves the trade-off between set resistance and reset current that arises in conventional PCM structures as the device is scaled down. Furthermore, significant improvements in energy efficiency can be achieved through the optimization of material properties, structural design, and maximization of the thermoelectric effects in the vertical IHPCM structure. Previous studies have reported that cyclic endurance improves as the program energy applied to the phase-change material decreases [47], [48]. The simulation results show a significant reduction (>× 10¹⁰) in the current density within the phase-change material during the programming process, suggesting that the vertical IHPCM structure has the potential for enhanced cyclic endurance. These findings underscore the potential of the vertical IHPCM structure as a high-performance, energy-efficient memory device for SCM applications.

2.5. Bibliography

[1] S. W. Fong et al., "Phase-change memory—Towards a storage-class memory." *IEEE Transactions on Electron Devices* 64.11 (2017): 4374-4385.

[2] W. Zhang et al., "Designing crystallization in phase-change materials for universal memory and neuro-inspired computing." *Nature Reviews Materials* 4.3 (2019): 150-168.

[3] G. W. Burr et al., "Neuromorphic computing using non-volatile memory." *Advances in Physics: X* 2.1 (2017): 89-124.

[4] A. Sebastian et al., "Tutorial: Brain-inspired computing using phase-change memory devices." *Journal of Applied Physics* 124.11 (2018).

[5] A. Pirovano et al., "Scaling analysis of phase-change memory technology." *IEEE International Electron Devices Meeting 2003*. IEEE, 2003.

[6] S. Raoux et al., "Phase change materials and phase change memory." *MRS bulletin* 39.8 (2014): 703-710.

 [7] D. H. Im et al., "A unified 7.5 nm dash-type confined cell for high performance PRAM device." 2008 IEEE International Electron Devices Meeting.
 IEEE, 2008.

[8] M. Boniardi et al., "Optimization metrics for phase change memory (PCM) cell architectures." *2014 IEEE International Electron Devices Meeting*. IEEE, 2014.

[9] S. C. Lai et al., "A scalable volume-confined phase change memory using physical vapor deposition." *2013 Symposium on VLSI Technology*. IEEE, 2013.

[10] P. J. Nair et al., "Reducing read latency of phase change memory via early read and turbo read." 2015 IEEE 21st International Symposium on High Performance Computer Architecture (HPCA). IEEE, 2015.

3 6

[11] S. W. Nam et al., "Electric-field-induced mass movement of Ge2Sb2Te5 in bottleneck geometry line structures." *Electrochemical and Solid-State Letters* 12.4 (2009): H155.

[12] C. Kim et al., "Direct evidence of phase separation in Ge2Sb2Te5 in phase change memory devices." *Applied Physics Letters* 94.19 (2009).

[13] T-Y. Yang et al., "Atomic migration in molten and crystalline Ge2Sb2Te5 under high electric field." *Applied Physics Letters* 95.3 (2009).

[14] Y-J. Park et al., "Electrical current-induced gradual failure of crystallineGe2Sb2Te5 for phase-change memory." *Applied Physics Letters* 103.7 (2013).

[15] H. Horii et al., "A novel cell technology using N-doped GeSbTe films for phase change RAM." 2003 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No. 03CH37407). IEEE, 2003.

[16] T-Y. Yang et al., "Influence of dopants on atomic migration and void formation in molten Ge2Sb2Te5 under high-amplitude electrical pulse." *Acta materialia* 60.5 (2012): 2021-2030.

[17] M. B. Sky et al., "Crystalline-as-deposited ALD phase change material confined PCM cell for high density storage class memory." *2015 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2015.

[18] W. Kim et al., "ALD-based confined PCM with a metallic liner toward unlimited endurance." *2016 IEEE International Electron Devices Meeting (IEDM)*.
 IEEE, 2016.

[19] COMSOL Multiphysics, v. 5.5, COMSOL AB, Sweden, 2019.

[20] D-S. Suh et al., "Thermoelectric heating of Ge2Sb2Te5 in phase change memory devices." *Applied Physics Letters* 96.12 (2010).

[21] A. Faraclas et al., "Modeling of thermoelectric effects in phase change

memory cells." IEEE Transactions on Electron Devices 61.2 (2014): 372-378.

[22] A. Faraclas et al., "Modeling of set and reset operations of phase-change memory cells." *IEEE electron device letters* 32.12 (2011): 1737-1739.

[23] J. Y. Wu et al., "A low power phase change memory using thermally confined TaN/TiN bottom electrode." *2011 International Electron Devices Meeting*. IEEE, 2011.

[24] E. Bozorg-Grayeli et al., "High temperature thermal properties of thin tantalum nitride films." *Applied Physics Letters* 99.26 (2011).

[25] J. Bryner et al., "Characterization of Ta and TaN diffusion barriers beneath Cu layers using picosecond ultrasonics." *Ultrasonics* 44 (2006): e1269-e1275.

[26] I. V. Karpov et al., "SET to RESET programming in phase change memories." *IEEE electron device letters* 27.10 (2006): 808-810.

[27] L. D. Landau et al., "Electrodynamics of Continuous Media Butterworth Heinemann." (1984): 88.

[28] Y. G. Gurevich et al., "Physics of thermoelectric cooling." *Semiconductor science and technology* 20.12 (2005): R57.

[29] G. J. Snyder et al., "Complex thermoelectric materials." *Nature materials* 7.2 (2008): 105-114.

[30] J. R. Sootsman et al., "New and old concepts in thermoelectric materials." *Angewandte Chemie International Edition* 48.46 (2009): 8616-8639.

[31] C. Gayner et al., "Recent advances in thermoelectric materials." *Progress in Materials Science* 83 (2016): 330-382.

[32] M. W. Gaultois et al., "Data-driven review of thermoelectric materials:
 performance and resource considerations." *Chemistry of Materials* 25.15 (2013):
 2911-2920.

[33] C. Catalin et al., "Ultralow thermal conductivity in disordered, layeredWSe2 crystals." *Science* 315.5810 (2007): 351-353.

[34] S. Vaziri et al., "Ultrahigh thermal isolation across heterogeneously layered two-dimensional materials." *Science advances* 5.8 (2019): eaax1325.

[35] C. Kim et al., "Fullerene thermal insulation for phase change memory." *Applied Physics Letters* 92.1 (2008).

[36] F. Rao et al., "Programming voltage reduction in phase change memory cells with tungsten trioxide bottom heating layer/electrode." *Nanotechnology* 19.44
(2008): 445706.

[37] S. Song et al., "Performance improvement of phase-change memory cell using AISb 3 Te and atomic layer deposition TiO 2 buffer layer." *Nanoscale research letters* 8 (2013): 1-6.

[38] L-D. Zhao et al., "Ultralow thermal conductivity and high thermoelectric figure of merit in SnSe crystals." *nature* 508.7496 (2014): 373-377.

[39] G. Tan et al., "High thermoelectric performance in electron-doped AgBi3S5 with ultralow thermal conductivity." *Journal of the American Chemical Society* 139.18 (2017): 6467-6473.

[40] Z. Zheng et al., "Rhombohedral to cubic conversion of GeTe via MnTe alloying leads to ultralow thermal conductivity, electronic band convergence, and high thermoelectric performance." *Journal of the American Chemical Society* 140.7 (2018): 2673-2686.

[41] J. P. Reifenberg et al., "The impact of thermal boundary resistance in phasechange memory devices." *IEEE Electron Device Letters* 29.10 (2008): 1112-1114.

[42] C. Ahn et al., "Energy-efficient phase-change memory with graphene as a thermal barrier." *Nano letters* 15.10 (2015): 6809-6814.

[43] U. Russo et al., "Modeling of programming and read performance in phasechange memories—Part II: Program disturb and mixed-scaling approach." *IEEE Transactions on Electron Devices* 55.2 (2008): 515-522.

[44] T-Y. Yang et al., "Driving forces for elemental demixing of GeSbTe in phase-change memory: computational study to design a durable device." *Current Applied Physics* 13.7 (2013): 1426-1432.

[45] G. Novielli et al., "Atomic migration in phase change materials." *2013 IEEE International Electron Devices Meeting*. IEEE, 2013.

[46] P. Yeoh et al., "Thermal-gradient-driven elemental segregation in Ge2Sb2Te5 phase change memory cells." *Applied Physics Letters* 114.16 (2019).

[47] S. Lai, "Current status of the phase change memory and its future." *IEEE International Electron Devices Meeting 2003*. IEEE, 2003.

[48] I. S. Kim et al., "High performance PRAM cell scalable to sub-20nm technology with below 4F2 cell size, extendable to DRAM applications." *2010 Symposium on VLSI Technology*. IEEE, 2010.

Chapter 3. Characterization of Crystallization Properties in Phase-Change Material Using IHPCM with Dual Heaters

3.1. Introduction

Phase-change memory (PCM) is among the most advanced and mature technologies in next-generation non-volatile memory devices, widely employed in diverse applications such as storage-class memory (SCM), embedded memory, and neuromorphic computing [1]-[9]. The device properties required for these applications are predominantly related to the crystallization properties of PCM. For instance, in memory-type SCM, fast crystallization speed is essential to enable high-speed operation close to the main memory such as dynamic random-access memory (DRAM) [3]. In automotive embedded memory applications, devices must operate reliably at high temperatures and exhibit excellent data retention, both of which are closely linked to the crystallization temperature [5]. In neuromorphic computing, the linear and gradual resistance changes required for PCM synaptic devices are directly associated with crystallization behavior [9]. Therefore, a comprehensive understanding and precise characterization of PCM crystallization properties are indispensable for optimizing its performance across a broad range of applications.

Actual device-based characterization methods using external heaters enable the analysis of crystallization properties for the melt-quenched amorphous phase over a broad temperature range (>600K) and short time constants (sub-µs), while considering the influence of interfaces within the actual PCM device [10]-[12], offering significant advantages over traditional thin-film-based methods [13]-[15].

While recent research has proposed nanosecond probing up to temperatures exceeding the melting point of phase-change materials using indirectly heated phase-change switches, the non-uniform temperature distribution within phase-change materials imposes limitations on precise measurements of crystallization properties [12].

In this study, we propose a comprehensive characterization system capable of measuring crystallization properties and analyzing the crystallization process under uniform temperature conditions. The system features an optimized indirectly heated PCM (IHPCM) device, which incorporates a bottom heater to achieve a uniform temperature distribution and a top heater to locally form a melt-quenched amorphous phase within the uniform region. By employing electrical measurements and the electrothermal model of the dual-heater IHPCM characterization device, it accurately characterizes key crystallization properties, including crystallization. Furthermore, nuclei formation and resistance variations during the crystallization process are analyzed through fully coupled simulations that integrate electrothermal and crystallization models.

3.2. Experimental Methods

The IHPCM characterization device with dual heaters was fabricated following the process flow illustrated in Figure 3-1. A 1-µm thick SiO₂ and a 300-nm thick Si_3N_4 layers were sequentially deposited on a Boron-doped p-type Si wafer via chemical vapor deposition (CVD, Applied Materials, Centura 5200) process. To form the buried bottom heater (BH), the Si_3N_4 layer was patterned through photoresist (PR) coating and baking (PR Track V, Tokyo Electron, MARK-7), followed by exposure using a KrF stepper (ASML, PAS 5500) and then dry etched (Applied Materials, eMax DPS). After patterning, the residual PR was sequentially removed via PR ashing within the dry etch equipment. 20-nm thick Ti and TiN layers were deposited sequentially by sputtering (Applied Materials, Endura 5500) to serve as adhesion and barrier layers, respectively. 250-nm thick Tungsten (W) layer was deposited as a BH using CVD and planarized through a chemical mechanical polishing (CMP, EBARA, F-REX200) process. On the planarized surface, a 50-nm thick Si_3N_4 was deposited via CVD as an insulating layer between the BH and the phase-change layer (PCL). Two types of phase-change materials, $Ge_2Sb_2Te_5$ and Sb_2Te_3 , were deposited to a thickness of 100nm via RF sputtering using a magnetron sputtering system (KVS-2000L, Korea Vacuum Tech, Ltd.). The PCL was patterned through photolithography and reactive ion etching (RIE, Oxford instruments, PLASMA PRO 100 COBRA). The Si_3N_4 layer beneath the PCL was patterned using photolithography and RIE (GIGALANE, NeoS-MAXIS 200L) for the pad opening of BH. The pads for the PCL and the BH were fabricated by coating and patterning negative PR (L300 40), followed by the sequential deposition of 10-nm Ti and 100-nm Au layers using E-gun evaporation (SORONA, SRN-200), and

formed through a lift-off process. As an insulator between the PCL and the top heater (TH), a 50-nm thick Si_3N_4 layer was deposited via plasma-enhanced CVD (PECVD, Oxford Instruments, PLASMAPRO SYSTEM100) under 350°C and patterned using photolithography and RIE. As the TH, a 100-nm thick W layer was deposited by RF sputtering using a magnetron sputtering system and patterned by photolithography and RIE. A 100-nm thick Si_3N_4 capping layer was deposited via PECVD under 350°C and patterned using photolithography and RIE. Finally, the Ti/Au pad for the TH was deposited by E-gun evaporation and patterned via the lift-off process. After the deposition of the PCL, all photolithography processes were carried out using positive PR (SS03A9), a spin coater for the PR coating, a hot plate for PR baking, and a maskless patterning system (NANO SYSTEM SOLUTION, DL-1000 HP) for exposure.

The electrical measurements were performed using a probestation (MST800CL, MS Tech). For DC electrical characterization, a semiconductor parameter analyzer (Keysight, B1500A) was utilized, while AC pulse measurements were conducted using a pulse generator (Keysight, Agilent 81110A) and an oscilloscope (Keysight 5GSa/s, Agilent 4GSa/s). A preamplifier (SRS, SR570) was used to amplify the PCM current corresponding to the phase transitions, which was then read through an oscilloscope.

The temperature distribution and crystallization process within PCL were calculated using finite element method (FEM) simulations (COMSOL Multiphysics). The electrothermal model solves the current continuity equation (1) and the heat transport equation (2) to calculate the temperature profile through the Joule heating effect

$$\nabla \cdot J = -\nabla \cdot (\sigma(\nabla V)) = 0 \tag{1}$$

$$dC_P \frac{dT}{dt} - \nabla \cdot (\kappa \nabla T) = \frac{J \cdot J}{\sigma}$$
(2)

where J is the current density, σ is the electrical conductivity, V is the electric potential, d is the mass density, C_P is the heat capacity, T is the temperature, κ is the thermal conductivity [16], [17].

The crystallization model calculates the changes in the crystal density field vector $(\overrightarrow{CD} = \{CD_1, CD_2, CD_3\})$ during phase transitions using a rate equation based on the phase-field model proposed in previous research [18]-[20].

$$\frac{dCD_i}{dt} = Nucleation_i + Growth_i + Amorphization_i$$
(3)

$$Nucleation_{i} = \alpha_{nuc} \times \left(1 - \left\|\overrightarrow{CD}\right\|_{1}\right) \times (rnd_{nuc} < p_{nuc}) \times (rnd_{i})$$
(4)

$$p_{nuc} = I_{ss}(T) \times Vol_{nuc} \times t_{nuc}$$
⁽⁵⁾

$$Growth_{i} = stbl \times \frac{CD_{i}}{\left\|\overline{CD}\right\|_{1}} + \nabla(diff)\nabla CD_{i}$$
(6)

$$stbl = \alpha_{stbl} \times v_G(T) \times pw_{stbl}(\left\| \overrightarrow{CD} \right\|_1)$$
(7)

$$diff = \alpha_{diff} \times v_G(T) \times pw_{diff}(\|\overrightarrow{CD}\|_1)$$
(8)

$$Amorphization_{i} = \alpha_{amorph} \times (T > T_{melt}) \times CD_{i}$$
(9)

The nucleation term (*Nucleation_i*) calculates the stochastic formation of crystal nuclei within the amorphous region. $\alpha_{nuc} = 0.8ns^{-1}$ is a constant, and $\|\vec{CD}\|_1$ is a one norm of the crystal density field vector, which denotes the phase of the material, with a value of 1 indicating the crystalline phase and 0 indicating the amorphous phase. rnd_{nuc} and rnd_i are random functions that generate random values uniformly distributed between 0 and 1 at regular time intervals and at x, y positions. p_{nuc} is the nucleation probability, which consists of the temperature-dependent steady-state nucleation rate ($I_{ss}(T)$), Figure 3-2 (a)), the nucleation site volume (Vol_{nuc}), and the time interval (t_{nuc}) for updating the random function. The growth

term (*Growth_i*) includes a stability term (stbl), which creates stability points for the crystal density (CD) at 0 and 1, and a diffusivity term (diff), which causes the grains to grow outwards. Here, $\alpha_{stbl} = 0.8nm^{-1}$ and $\alpha_{stbl} = 0.2nm$ are constants, $v_G(T)$ is the temperature dependent crystal growth velocity (Figure 3-2 (a)), pw_{stbl} and pw_{diff} are piecewise control functions (Figure 3-2 (b), (c)). The amorphization term (*Amorphization_i*) changes each CD_i to 0 when the temperature exceeds the melting point (T_{melt}), where $\alpha_{amorph} = -1ns^{-1}$ is a constant.

The material properties used in the simulation are listed in Table 3-1 [16], [17], [22-29]. The electrical conductivity as a function of temperature for each heater was determined using the electrical conductivities measured at room temperature and the thermal coefficient of resistance values (α_{BH} , α_{TH}) obtained from fourpoint probe measurements. The temperature-dependent electrical conductivity and thermal conductivity for $Ge_2Sb_2Te_5$ were taken from previous studies [17]. In addition, to account for the limited phonon-phonon and phonon-electron coupling at the interfaces between materials, thermal boundary resistance (TBR) values were applied [30]. For the interfaces between Ti, W, and the dielectric, typical TBR values for metal-insulator interfaces were used [31]. The temperature-dependent TBR value for the $Ge_2Sb_2Te_5$ - insulator interface was taken from previous research [17], while the TBR value for the Sb_2Te_3 - insulator interface was assumed to be the same as that for the GST-insulator interface at room temperature.



Figure 3-1. Process flow for fabricating the IHPCM characterization device with dual heaters. The buried BH was fabricated using a W damascene process.



Figure 3-2. (a) Temperature-dependent steady-state nucleation rate (I_{SS}) and growth velocity (v_G) for $Ge_2Sb_2Te_5$ derived from classical nucleation theory [21]. Piecewise control functions for (b) stability and (c) diffusivity terms in the growth model [20].

	σ [S/m]	$\frac{\kappa}{[W/(m\cdot K)]}$	ρ [kg/m ³]	C_P [J/kg · K]
W (CVD)	$\sigma_{BH}(T)$	178	1 94e4	132 51
W (Sputtering)	$\sigma_{TH}(\mathrm{T})$	170	1.9101	192.91
$Ge_2Sb_2Te_5$	$\sigma_{GST}(\mathrm{T})$ [17]	$\kappa_{GST}(T)$ [17]	6.35e3	202
Sb ₂ Te ₃	5e4	0.35	6.5e3	206
Ti	1.66e6	21.9	4.51e3	140
TiN	5e5	29	5.43e3	784
Аи	4.26e7	315	1.93e4	129
SiO ₂	1e-14	1.38	2.2e3	703
Si ₃ N ₄	1e-12	3	2.5e3	712
Si	100	134.23	2.33e3	703

 Table 3-1. Material properties utilized in the electrothermal and crystallization models.

 $*\sigma_{BH}(T) = 9.13e6/(1 + \alpha_{BH}(T - 298)), \sigma_{TH}(T) = 5e6/(1 + \alpha_{TH}(T - 298))$

 Table 3-2. Thermal boundary resistances at interfaces between materials utilized in

 the electrothermal model.

	Thermal boundary resistance $[m^2K/GW]$
$Ti - Si_3N_4$	20
$Ti - SiO_2$	20
$W - Si_3N_4$	20
$Ge_2Sb_2Te_5 - Si_3N_4$	$TBR_{GST-SiN}(T)$ [17]
$Sb_2Te_3 - Si_3N_4$	2.5
3.3. Results and Discussion

3.3.1. IHPCM Characterization Device with Dual Heaters

A 3D simulation was conducted to optimize the structure and material properties of the IHPCM device with a single heater to achieve a uniform temperature distribution within the PCL. As shown in Figure 3-3 (a), (b), a buried heater structure fabricated using the damascene process was implemented, allowing the PCL to be deposited on a flat surface and ensuring temperature uniformity. A serpentine heater design was adopted to provide uniform heating across a large area, consisting of 6 lines, each with a width (W_{Heater}) of 2µm and a length (L_{Heater}) of 20µm. Temperature uniformity was assessed by comparing the standard deviation (SD) of temperature data within the 3D PCL region outlined by dashed lines in Figure 3-3 (d).

First, the temperature drop between heater lines was found to have a critical impact on temperature uniformity. When the spacing between heater lines (W_{Space}) was varied, smaller W_{Space} values led to reduced SD values at the same average temperature (Figure 3-4 (a)). This was attributed to the increased overlap of thermal profiles generated by individual heater lines as W_{Space} decreased. Although serpentine heaters achieved uniform temperatures over a wide area, temperature drops were inevitable at the edges of the heater region. Therefore, reducing the width of the PCL (W_{PCL}) to be shorter than the length of the heater lines (L_{Heater}) mitigated the impact of these edge effects, thereby improving temperature uniformity, as confirmed in Figure 3-4 (b). The thermal conductivity of the dielectric layers (DL) between the heater lines (DL2) and between the heater and the PCL (DL3) also influenced the temperature distribution. When Si_3N_4 was used for DL2 and DL3, its higher thermal conductivity compared to SiO_2 improved heat diffusion, thereby enhancing temperature uniformity within the PCL (Figure 3-4 (c)). Using dielectric materials with higher thermal conductivity, such as AlN ($\kappa = 100 W/(m \cdot K)$) [32], can further improve temperature uniformity, although this may increase power consumption.

Using the optimized IHPCM device with a single heater, a uniform temperature region within the PCL was generated during the set operation (Figure 3-5 (a), (b)). However, during the reset operation with the same heater, the width of the formed amorphous region was similar to that of the uniform temperature region formed during the set process. As a result, the uniform temperature distribution was not fully guaranteed near the edges of the amorphous region. To address the inherent limitations arising from the use of a single heater, we developed an IHPCM device with dual heaters by incorporating an additional top line heater above the PCL (Figure 3-5 (c)). In this structure, the TH was used for reset operation to create a narrow amorphous region, while the BH was used for the characterization under uniform temperature. Consequently, the proposed IHPCM structure stably positioned the amorphous region within a uniform temperature region, enabling precise characterization of crystallization properties (Figure 3-5 (d)).



Figure 3-3. (a) Top view and (b) side view of the schematic diagram of the IHPCM structure with a single heater. (c) Bird's-eye view and (d) top view of the IHPCM geometry used in the 3D simulation. The temperature distribution, T(x, y, z), within the dashed PCL region was used to evaluate temperature uniformity.



Figure 3-4. Comparison of the standard deviation (SD) as a function of average temperature (T_{Avg}) within the designated PCL region, with varying (a) W_{Space} , (b) W_{PCL} , and (c) dielectric layers (DL) between the heater lines (DL2) and between the PCL and heater (DL3).



Figure 3-5. (a) Side view and (b) temperature distribution along the x-direction on the top surface of the PCL for the IHPCM with a single heater. (c) Side view and (d) temperature distribution along the x-direction on the top surface of the PCL for the IHPCM with dual heaters.

3.3.2. Evaluation of the IHPCM Characterization Device

The IHPCM characterization device with dual heaters was fabricated as shown in Figure 3-6, and electrical measurements and simulations were employed to investigate the characterization device. The temperature dependent resistances of the TH (R_{TH}) and BH (R_{BH}), as well as the applied voltages across the heaters (V_{TH}^{RESET} , V_{BH}^{SET}) during the set and reset operations, are presented as follows

$$R_{TH}(T) = \rho_{TH, Ref} \frac{L_{TH}^{total}}{t_{TH}W_{TH}} \left(1 + \alpha_{TH} \left(T_{TH} - T_{Ref} \right) \right) + 2R_{C}^{TH}$$
(10)

$$R_{BH}(T) = \rho_{BH, Ref} \frac{L_{BH}^{total}}{t_{BH}W_{BH}} \left(1 + \alpha_{BH} (T_{BH} - T_{Ref}) \right) + 2R_C^{BH}$$
(11)

$$V_{TH}^{RESET} = V_{PG}^{Out} \frac{R_{TH}(T)}{R_{TH}(T) + Z_0}$$
(12)

$$V_{BH}^{SET} = V_{PG}^{Out} \frac{R_{BH}(T)}{R_{BH}(T) + Z_0}$$
(13)

where $\rho_{TH,Ref}$ and $\rho_{BH,Ref}$ represent the electrical resistivity of heaters at T_{Ref} , L_{TH}^{total} and L_{BH}^{total} denote the total length of heaters, t_{TH} and t_{BH} denote the thickness of heaters, W_{TH} and W_{BH} denote the width of heaters, α_{TH} and α_{BH} are the temperature coefficients of resistance (TCR) of heaters, T_{TH} and T_{BH} are the temperature of each heater, T_{Ref} is the room temperature, R_C^{TH} and R_C^{BH} denote the contact resistance, V_{PG}^{Out} is the output voltage from the pulse generator, and Z_0 is the impedance of the oscilloscope.

To construct a simulation that matches the experiments of actual devices, the TCR values and contact resistance for each heater were measured. The temperaturedependent resistance changes for TH and BH were measured using a four-point probe structure by increasing the temperature of the hot stage within the probestation, as shown in Figure 3-7 (a), (b), from which the TCR for each heater was determined. Additionally, the contact resistances of the TH and BH were evaluated at room temperature using the transfer length method, as shown in Figure 3-7 (c), (d).

The V_{TH}^{RESET} and V_{BH}^{SET} applied across each heater were determined by the voltage division between the heater resistance and the impedance of the oscilloscope connected to the bottom electrode of the heaters. The actual voltage across the heater was measured by reading the voltage applied to the top electrode of the heater (V_{PG}^{Out}) through the high-impedance channel of the oscilloscope $(V_{OSC}^{CH1}, Z_0 = 1M\Omega)$, which was connected in parallel to the heater, and subtracting the voltage read from the low-impedance channel of the oscilloscope $(V_{OSC}^{CH2}, Z_0 = 50\Omega)$ connected to the bottom electrode of the heater (Figure 3-8). The measured V_{TH}^{RESET} and V_{BH}^{SET} were used in the simulation to calculate the temperature distributions within the IHPCM.

The temperature within the PCL of the IHPCM characterization device was calculated through 3D simulations incorporating the Joule heating effect (Figure 3-9). The temperature-dependent electrical conductivities of the TH and BH were applied using their respective TCR values and electrical conductivities measured at room temperature. Additional material properties and the TBR at material interfaces were adopted from previously reported studies as listed in Table 3-1 and Table 3-2. As illustrated in Figure 3-9 (b), the measured $V_{TH}^{RESET}(t)$ and $V_{BH}^{SET}(t)$ were applied to the top electrodes of the respective heaters, while all other electrodes were grounded. The thermal boundary of the heater and PCL electrodes was maintained at T=298K, while the remaining upper surface of the IHPCM device was subjected to convective heat flux boundary conditions (Heat transfer coefficient, $h = 5W/m^2K$).

The temperature distribution generated by applying a voltage from 0 to 3V to the BH (V_{BH}) was calculated through simulation. The IHPCM device employed consists

of a BH with 6 lines, each with a length (L_{BH}) of 20µm, a width (W_{BH}) of 2µm, and a spacing (W_{Space}) of 0.5µm, and a TH with a length of 30µm (L_{TH}) and a width of 1µm (W_{TH}) . The T_{PCM} was defined as the average temperature over a 3D PCL region three times the width of the TH, ensuring sufficient coverage of the amorphous region (Figure 3-10 (a)). Figure 3-10 (b) showed the variation of T_{PCM} with increasing V_{BH} from 0 to 3V, while Table 3-3 presented the SD and spatial variation corresponding to T_{PCM} by applying V_{BH} up to 5V. The IHPCM device with a dual-heater structure exhibited spatial variations of less than 1% even at temperatures above the melting point, demonstrating its capability to perform precise characterization under a uniform temperature distribution across a broad temperature range.

The thermal time constant (τ) and heating rate of the IHPCM characterization device were evaluated using the electrical measurement setup shown in Figure 3-11 (a). The IHPCM incorporating $Ge_2Sb_2Te_5$ as the phase-change material was used in the measurement. To measure the change of the PCL current (I_{PCL}) as a function of temperature in the crystalline state, a read voltage ($V_{Read} = 0.2V$) with a 30µs pulse width was applied to the PCL. Simultaneously, a heating voltage ($V_{Heat} =$ 6.86V) with a pulse width of 10µs was applied to the BH, with a 10µs delay (Figure 3-11 (b)). V_{Heat} was set to ensure temperatures above the melting point of $Ge_2Sb_2Te_5$ ($T_{Melt} \approx 873K$), and T_{PCM} was extracted through simulation by applying the measured divided voltage across the BH ($V_{BH}^{Heat} = 4.61V$). The change in I_{PCL} was evaluated by analyzing the variation in the voltage distributed to the oscilloscope channel (V_{OSC}^{V2}) serially connected to the bottom electrode of the PCL. The results showed that the I_{PCL} in the initial SET state increased from 71 µA to 107 µA upon the application of V_{Heat} (Figure 3-11 (c)). The initial state of the PCL was the hexagonal close-packed (hcp) phase, which resulted from a phase transition induced during the PECVD process of the Si_3N_4 layer at 350 °C after the PCL deposition. The increase in I_{PCL} was attributed to the melting of the hcp phase with rising temperature above T_{Melt} . The relatively small increase in I_{PCL} was due to the smaller difference in electrical conductivity between the hcp phase and the molten state of the $Ge_2Sb_2Te_5$ compared to that of the face-centered cubic (fcc) phase in the recrystallized state [33]. The thermal time constant of 3.9 µs was extracted, and the resulting heating rate (~ $1.8 \times 10^8 K/s$) was determined using the $T_{PCM} = 995.3K$ (at $V_{BH}^{Heat} = 4.61V$) obtained through simulations. After the V_{Heat} was turned off, amorphization occurred through the melt-quench process, leading to a reduction in I_{PCM} and a subsequent decrease in V_{OSC}^{V2} .



Figure 3-6. Top (left) and side (right) views of the (a) schematic diagram and (b) scanning electron microscope (SEM) image of the IHPCM characterization device with dual heaters. The PCL line was patterned with a width (W_{PCL}) of 3µm and a length (L_{PCL}) of 50µm.



Figure 3-7. Temperature-dependent resistance variation of (a) the TH and (b) BH, measured using four-point probe structures. The TH and BH were fabricated with widths of 1µm and 3µm, respectively, both with a length of 40µm, and their TCR values (α_{TH} , α_{BH}) were extracted. Resistance variations as a function of heater length for (c) the TH and (d) BH, measured using the transfer length method (TLM) structure with a width of 140µm to determine the contact resistance (R_c) of the heaters.



Figure 3-8. The electrical measurement setup for measuring V_{TH}^{RESET} applied across the TH.



Figure 3-9. (a) Bird's-eye view of the IHPCM geometry utilized in the 3D simulation.

(b) Electrical and thermal boundary conditions applied to each pad in the simulation.



 T_{PCM} : Average temperature within 3D domain (dashed)



Figure 3-10. (a) Simulated temperature distribution along the x-z plane at $V_{BH} = 3V$. T_{PCM} was defined as the average temperature within a designated 3D region of PCL, extending three times the width of the TH, to ensure sufficient coverage of the amorphous volume. (b) Variation of T_{PCM} as a function of the applied V_{BH} .

Table 3-3. Calculated T_{PCM} , standard deviation, and spatial variation based on the T(x, y, z) data within the designated 3D region of PCL.

T _{PCM}	500K	606K	704K	808K	917K
Standard Deviation	2.45K	3.78K	5.02K	6.36K	7.79K
Spatial Variation [%]	0.49	0.62	0.71	0.79	0.85



Figure 3-11. (a) Electrical measurement setup and (b) pulse conditions used to evaluate the thermal time constant (τ) and heating rate of the IHPCM characterization device. (c) Transient voltage changes across the oscilloscope channels. V_{OSC}^{V1} and V_{OSC}^{V2} represents the voltage divided across the 50 Ω impedance of the oscilloscope in response to V_{Heat} and V_{Read} , respectively.

3.3.3. Characterization of Crystallization Properties in Phase-Change Materials

The crystallization properties of phase-change materials were evaluated using an IHPCM characterization device with dual heaters. Crystallization temperature (T_c) is intrinsically linked to the SET power and retention characteristics of the PCM, representing a critical material property for the development of phase-change materials in automotive-embedded applications [34], where excellent retention at high temperatures is essential. T_C measurements were performed for the representative phase-change materials, $Ge_2Sb_2Te_5$ and Sb_2Te_3 . The IHPCM devices used for measurements consisted of THs with dimensions $W_{TH} = 1 \mu m$ and $L_{TH} = 30 \mu m$ for both phase-change materials. The BHs comprised 6 lines, each with $L_{BH} = 20\mu m$ and $W_{Space} = 0.5\mu m$, with $W_{BH} = 2\mu m$ for $Ge_2Sb_2Te_5$ and $W_{BH} = 1.5 \mu m$ for Sb_2Te_3 . During the reset process, $V_{TH}^{RESET} = 3.23$ V and 3.47V were applied across the TH of $Ge_2Sb_2Te_5$ and Sb_2Te_3 , respectively, with a pulse width of 1µs and rise and fall times of 2.5 ns. A DC sweep of V_{BH} was performed using a semiconductor parameter analyzer (SPA), while applying $V_{Read} = 0.2V$ to the PCL and monitoring the changes in PCM resistance (R_{PCM}) (Figure 3-12 (a)). The measurements were conducted at various heating rates, achieved by adjusting the duration of each 10mV voltage step of V_{BH} . As shown in Figure 3-12 (b) and (c), T_C was defined as the point where the slope of the R_{PCM} change was maximized. The results showed that the T_c values of $Ge_2Sb_2Te_5$ and Sb_2Te_3 increased with the heating rate, which was attributed to the slower crystallization rate relative to the rate of temperature change below T_C . It was noteworthy that the measured T_C values for the two phase-change materials were

in good agreement with those reported in previous studies ($T_c = 398 \sim 433K$ for $Ge_2Sb_2Te_5$ and $T_c = 363 \sim 383K$ for Sb_2Te_3) under a similar heating rate (0.16K/s) [35],[36], thus verifying the accuracy of the T_{PCM} extracted from the simulation.

The development of phase-change materials with fast crystallization time (t_c) is essential for advanced memory applications, such as SCM and neuromorphic computing, which require high-speed operation, as the t_c is directly linked to the set speed in PCM [3], [37]. The t_c can be measured through transient measurements of the crystallization process, with the electrical setup shown in Figure 3-13. The BHs of the IHPCM devices used for measurements consisted of 6 lines with $L_{BH} =$ $20\mu m$, $W_{BH} = 1\mu m$, and $W_{Space} = 0.5\mu m$ for $Ge_2Sb_2Te_5$, and 8 lines with $L_{BH} = 20\mu m$, $W_{BH} = 2\mu m$, and $W_{Space} = 0.5\mu m$ for Sb_2Te_3 . The THs had dimensions of $W_{TH} = 1\mu m$ and $L_{TH} = 30\mu m$ for both phase-change materials. $V_{Read} = 0.2V$ was applied to the top electrode of the PCL to monitor changes in I_{PCL} during the crystallization process (Figure 3-13 (a)). However, direct measurement of I_{PCL} from the reset state was limited because it lies within the oscilloscope's noise floor. Therefore, a preamplifier (SRS, SR570) was applied to the bottom electrode of the PCL to amplify the current into a voltage signal. A sensitivity of $10\mu A/V$ was used for the preamplifier, and the amplified signal was captured through oscilloscope channel 2 (V_{OSC1}^{CH2}). The pulse conditions of V_{Read} and V_{BH}^{SET} are shown in Figure 3-13 (b), where V_{BH}^{SET} was applied simultaneously with the V_{Read} pulse, with a 10µs delay. The V_{BH}^{SET} applied across the BH was selected to ensure the completion of the crystallization process within the total pulse width, with V_{BH}^{SET} set to 2.82V for $Ge_2Sb_2Te_5$ and 2.92V for Sb_2Te_3 , respectively. As shown in Figure 3-14, both phase-change materials exhibited very low V_{OSC1}^{CH2} values when only V_{Read} was applied in the initial reset state. Upon application of V_{BH}^{SET} , crystallization occurred, causing V_{OSC1}^{CH2} to increase and eventually saturate. When V_{BH}^{SET} was turned off, the influence of temperature-dependent electrical conductivity diminished, resulting in a reduction of V_{OSC1}^{CH2} . The t_c was defined as the duration from the start of V_{BH}^{SET} to the point where V_{OSC1}^{CH2} converged. t_c can also be determined using a multi-pulse method, as thermal pulses induced by the heater exhibit an additive effect [11]. To evaluate this, t_c values for $Ge_2Sb_2Te_5$ were measured under two conditions with the same $V_{BH}^{SET} = 2.82V$: a single 500µs pulse and ten 50μ s pulses, with the total pulse duration kept constant (Figure 3-15). The results showed that the t_c values were identical under both conditions, confirming the additive effect of thermal pulses. Transient measurements using single and multiple pulses enabled the observation of I_{PCL} changes during the crystallization process. In addition to the t_c measurement, this method can be used to analyze differences in the crystallization process based on crystallization behavior, such as nucleation-dominant or growth-dominant crystallization. It can also be applied to the analysis of multi-level programming processes required in applications such as multi-level cells (MLC) for high density memory and analog synapses in neuromorphic computing.

The activation energy (E_a) for crystallization encompasses the energy barriers associated with both the formation and growth of nuclei, which is closely linked to the retention of the PCM. The E_a can be extracted from the t_c measurements as a function of T_{PCM} using the Arrhenius equation

$$t_c = \tau_0 e^{\frac{E_a}{K_B T}} \tag{14}$$

where τ_0 is the pre-exponential factor, K_B is the Boltzmann constant, and T is the temperature. The BHs of the IHPCM devices used for E_a measurements consisted of 6 lines with $L_{BH} = 20 \mu m$ and $W_{Space} = 0.5 \mu m$, with $W_{BH} = 2 \mu m$ for $Ge_2Sb_2Te_5$ and $W_{BH} = 1.5\mu m$ for Sb_2Te_3 . The THs had dimensions of $W_{TH} = 1\mu m$ and $L_{TH} = 30\mu m$ for both phase-change materials. The t_c as a function of T_{PCM} was measured using the multi-pulse measurement setup (Figure 3-16 (a)). In this setup, R_{PCM} was measured by applying $V_{Read} = 0.2V$ to the PCL using a SPA, while V_{BH}^{SET} and pulse width applied across the BH were varied. The set state was defined as the point where the R_{PCM} decreased by more than 500× for $Ge_2Sb_2Te_5$ and 10^{\times} for Sb_2Te_3 from the reset state. The t_c was determined by the product of the pulse width and the number of pulses required to reach the set state, utilizing the additive nature of thermal pulses as shown in Figure 3-16 (b). For reset process, $V_{TH}^{RESET} = 3.23V$ and 3.47V were applied across the TH of $Ge_2Sb_2Te_5$ and Sb_2Te_3 , respectively, with a pulse width of 1µs and rise and fall times of 2.5ns. The measured t_c values as a function of T_{PCM} , along with the extracted E_a for $Ge_2Sb_2Te_5$ and Sb_2Te_3 , are presented in Figure 3-17 (a) and (b). The E_a values for both phase-change materials were in good agreement with those reported in previous studies [38], [39]. Notably, the non-Arrhenius behavior of phase-change materials was observed with increasing T_{PCM} . This behavior was attributed to the fragile nature of phase-change materials, which exist as supercooled liquids in the amorphous phase. Fragile liquids exhibit a sharp change in viscosity related to diffusion within a specific temperature range above the glass transition temperature [3]. The fragile nature of phase-change materials is a key factor that enables PCM to maintain high retention at low temperatures while promoting rapid

crystallization at elevated temperatures. This inherent nature of phase-change materials was well captured using the IHPCM characterization device.



Figure 3-12. (a) Electrical measurement setup for characterizing T_c . Change in R_{PCM} as a function of V_{BH} for (b) $Ge_2Sb_2Te_5$ and (c) Sb_2Te_3 at varying heating rates. T_c was defined as the point where the slope of the R_{PCM} change was maximized.



Figure 3-13. (a) Electrical measurement setup and (b) pulse conditions used for transient measurements to characterize t_c .



Figure 3-14. Transient voltage changes measured across the oscilloscope channel for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . The t_c was defined as the interval between the application of V_{BH}^{SET} and the point where V_{OSC1}^{CH2} saturated.



Figure 3-15. Transient voltage changes measured across the oscilloscope channel for $Ge_2Sb_2Te_5$ using (a) a single pulse and (b) multiple pulses, with $V_{BH}^{SET} =$ 2.82V and the total pulse duration kept constant.



Figure 3-16. (a) Multi-pulse measurement setup for characterizing the t_c as a function of T_{PCM} . (b) Variation of R_{PCM} with respect to the number of read operations. The t_c was determined by the product of the pulse width of V_{BH}^{SET} and the number of pulses needed to reach the set state.



Figure 3-17. The measured t_c as a function of T_{PCM} for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . The E_a was extracted using the Arrhenius equation.

3.3.4. Analysis of Crystallization Process in Phase-Change Materials

Analyzing the microstructural evolution during the crystallization process is essential for characterizing the crystallization behavior of phase-change materials and advancing research in applications that require gradual phase transitions, such as neuromorphic computing. A fully coupled 2D simulation incorporating both electrothermal and crystallization models was employed to investigate the crystallization process by correlating the results with experimental data obtained from the IHPCM characterization device. The R_{PCM} changes as a function of the T_{PCM} , measured to characterize the T_C , were utilized for comparison, and the 2D simulation was constructed according to the simulation flow illustrated in Figure 3-18 (a). Heat generation in the heaters was simulated by extracting heat source data, based on the applied V_{BH}^{SET} and V_{TH}^{RESET} voltages, from the 3D simulation model and applying it to the heaters over time (Figure 3-18 (b)). A $V_{Read} = 0.2V$ was applied to the PCM electrode to calculate the R_{PCM} change, and crystallization simulations were conducted within a designated 2D region corresponding to three times the width of the TH (Figure 3-18 (c)). The material properties used in the simulation were those listed in Table 3-1, and the simulation results were matched with the experimental results for $Ge_2Sb_2Te_5$, measured at a heating rate of 1 K/s(Figure 3-12 (b)), through the fitting of the temperature-dependent electrical and thermal conductivity, as well as the $I_{SS}(T)$ and $v_G(T)$ of $Ge_2Sb_2Te_5$. As shown in Figure 3-19 (a), the R_{PCM} change according to the T_{PCM} was well reproduced through the simulation. The variation in R_{PCM} was analyzed through the changes in the $\|\overrightarrow{CD}\|_1$ as a function of T_{PCM} . The initial decrease in R_{PCM} with the rise in T_{PCM} from room temperature to $T_{PCM} = 400K$ was attributed to the increase in the electrical conductivity of the amorphous state, resulting from the thermal excitation of carriers [40], given that no nucleation occurred due to crystallization at this range, as illustrated in Figure 3-19 (b). As T_{PCM} exceeded 400K, nucleation initiated, followed by both nucleation and growth processes as the T_{PCM} increased. A sharp decrease in R_{PCM} occurred as the grains progressively grew and began to merge (Figure 3-19 (b)). Complete crystallization of the amorphous regions was observed at temperatures exceeding $T_{PCM} = 419$ K. The methodology integrating electrical measurements with the fully coupled simulation model provides a comprehensive and precise analysis of the temperature-dependent electrical property variations, as well as the nucleation and growth processes, making it highly useful for crystallization studies of PCM.

Conventional PCM using self-heating (SH) of phase-change materials requires threshold switching during the set process by applying a voltage above the threshold voltage, thereby increasing the electrical conductivity in the amorphous phase. In contrast, IHPCM generates heat via an external heater, eliminating the need for threshold switching. To assess the influence of threshold switching on the crystallization process, the changes in R_{PCM} were compared by sweeping the DC voltage applied to the PCL and BH of the IHPCM characterization device (Figure 3-20 (a)). For both $Ge_2Sb_2Te_5$ and Sb_2Te_3 the BH of the IHPCM device used for measurements consisted of 6 lines with dimensions of $L_{BH} = 20\mu m$, $W_{BH} =$ $1\mu m$, and $W_{Space} = 0.5\mu m$, while the TH had dimensions of $W_{TH} = 1\mu m$ and $L_{TH} = 30\mu m$. The changes in R_{PCM} according to the crystallization process under both SH and IH are shown in Figure 3-20 (b), (c). For the SH of phasechange materials, R_{PCM} initially decreased gradually as V_{PCM} increased, followed by an abrupt drop once threshold switching occurred. This behavior was attributed to the sharp increase in the electrical conductivity of the amorphous phase upon threshold switching, which led to a rapid rise in T_{PCM} , subsequently triggering the crystallization process at an accelerated rate. In contrast, for IH, the T_{PCM} gradually increased with V_{BH} , as heat was generated by the heater. This resulted in a more gradual decrease in R_{PCM} compared to SH, which was attributed to the slower crystallization rate. Therefore, IHPCM offers the advantage of precisely controlling the T_{PCM} , facilitating the gradual modulation of R_{PCM} and the acquisition of a large number of intermediate states. This suggests that IHPCM holds potential for use as an analog synapse device for neuromorphic computing and in high-density memory applications, where multistate capabilities are required.



Figure 3-18. (a) Simulation flow for the fully coupled 2D simulation. The heat source is extracted from the 3D simulation and applied to the heaters to generate the heat induced by Joule heating effects. (b) Time-dependent heat source data utilized in the set process. (c) Schematic diagram of the geometry and boundary conditions employed in the 2D simulation.



Figure 3-19. (a) R_{PCM} as a function of T_{PCM} from electrical measurements and fully coupled simulations under a heating rate of 1K/s. (b) The simulated distribution of $\|\overrightarrow{CD}\|_1 (= CD_1 + CD_2 + CD_3)$ as T_{PCM} was increased from 390K to 419K.



Figure 3-20. (a) Measurement setup for comparing the crystallization behavior under DC sweeps between the SH and IH. Changes in R_{PCM} as a function of V_{PCM} (SH) and V_{BH} (IH) for (b) $Ge_2Sb_2Te_5$ and (c) Sb_2Te_3 .

3.4. Conclusion

In this study, an optimized IHPCM device with a dual-heater structure is developed to enable a precise analysis of crystallization properties under a uniform temperature distribution. The proposed device maintains spatial temperature variation of less than 0.1%, even at high temperatures near the melting point, and demonstrates stable operation at a high heating rate of $1.8 \times 10^8 K/s$. Comprehensive analyses of key crystallization properties, including crystallization temperature, crystallization time, the activation energy for crystallization, and non-Arrhenius behavior, are conducted through integrated electrical measurements and device simulations. Moreover, the fully coupled simulation incorporating the crystallization model provides in-depth insights into the temperature-induced variations in electrical properties, as well as the processes of nucleation and growth. The optimized IHPCM device, coupled with the comprehensive analytical methodology, provides a robust framework for the precise and systematic assessment of the crystallization characteristics and behaviors of phase-change materials, highlighting its substantial potential to propel PCM research across a wide range of applications.

3.5. Bibliography

 G. W. Burr et al., "Phase change memory technology." Journal of Vacuum Science & Technology B 28.2 (2010): 223-262.

[2] S. W. Fong et al., "Phase-change memory—Towards a storage-class memory." *IEEE Transactions on Electron Devices* 64.11 (2017): 4374-4385.

[3] W. Zhang et al., "Designing crystallization in phase-change materials for universal memory and neuro-inspired computing." *Nature Reviews Materials* 4.3 (2019): 150-168.

[4] F. Arnaud et al., "Truly innovative 28nm FDSOI technology for automotive micro-controller applications embedding 16MB phase change memory." *2018 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2018.

[5] P. Cappelletti et al., "Phase change memory for automotive grade embedded NVM applications." *Journal of Physics D: Applied Physics* 53.19 (2020): 193002.

[6] A. Redaelli et al., "Material and process engineering challenges in Ge-rich
GST for embedded PCM." *Materials Science in Semiconductor Processing* 137
(2022): 106184.

[7] S. Yu, "Neuro-inspired computing with emerging nonvolatile memorys."Proceedings of the IEEE 106.2 (2018): 260-285.

 [8] M. Xu et al., "Recent advances on neuromorphic devices based on chalcogenide phase-change materials." *Advanced Functional Materials* 30.50 (2020): 2003419.

[9] K. Byun et al., "Recent advances in synaptic nonvolatile memory devices and compensating architectural and algorithmic methods toward fully integrated neuromorphic chips." Advanced Materials Technologies 8.20 (2023): 2200884.

8 5

[10] S. Kim et al., "Thermal disturbance and its impact on reliability of phasechange memory studied by the micro-thermal stage." *2010 IEEE International Reliability Physics Symposium*. IEEE, 2010.

[11] R. Jeyasingh et al., "Ultrafast characterization of phase-change material crystallization properties in the melt-quenched amorphous phase." *Nano letters* 14.6 (2014): 3419-3426.

[12] N. Wainstein et al., "Indirectly heated switch as a platform for nanosecond probing of phase transition properties in chalcogenides." *IEEE Transactions on Electron Devices* 68.3 (2021): 1298-1303.

[13] I. Friedrich et al., "Structural transformations of Ge 2 Sb 2 Te 5 films studied by electrical resistance measurements." *Journal of applied physics* 87.9 (2000): 4130-4134.

[14] J. Orava et al., "Characterization of supercooled liquid Ge2Sb2Te5 and its crystallization by ultrafast-heating calorimetry." *Nature materials* 11.4 (2012): 279-283.

[15] I. McGieson et al., "Crystallization kinetics and thermodynamics of an Ag– In–Sb–Te phase change material using complementary in situ microscopic techniques." *Journal of Materials Research* 37.7 (2022): 1281-1295.

[16] A. Faraclas et al., "Modeling of set and reset operations of phase-change memory cells." *IEEE electron device letters* 32.12 (2011): 1737-1739.

[17] A. Faraclas, et al., "Modeling of thermoelectric effects in phase change memory cells." *IEEE Transactions on Electron Devices* 61.2 (2014): 372-378.

[18] Z. Woods et al., "Modeling of phase-change memory: Nucleation, growth, and amorphization dynamics during set and reset: Part I—Effective media approximation." *IEEE Transactions on Electron Devices* 64.11 (2017): 4466-4471.

8 6
[19] Z. Woods et al., "Modeling of phase-change memory: Nucleation, growth, and amorphization dynamics during set and reset: Part II—Discrete grains." *IEEE Transactions on Electron Devices* 64.11 (2017): 4472-4478.

[20] J. Scoggin, "Modeling and finite element simulations of phase change memory materials and devices." (2019).

[21] G. W. Burr et al., "Observation and modeling of polycrystalline grain formation in Ge2Sb2Te5." *Journal of Applied Physics* 111.10 (2012).

[22] J. F. Shackelford and W. Alexander. *CRC materials science and engineering handbook*. CRC press, 2000.

[23] Q. Li et al., "Temperature dependent thermal conductivity and transition mechanism in amorphous and crystalline Sb2Te3 thin films." *Scientific Reports* 7.1 (2017): 13747.

[24] A. Saci et al., "Thermal conductivity measurement of a Sb2Te3 phase change nanowire." *Applied Physics Letters* 104.26 (2014).

[25] N. Arshi et al., "Thickness effect on properties of titanium film deposited by dc magnetron sputtering and electron beam evaporation techniques." *Bulletin of Materials Science* 36 (2013): 807-812.

[26] T. T. T. Ho et al., "Analysis of Intrinsic Variability in Phase-Change Memory Switching Originating from Stochastic Nucleation Using Fully Coupled Electrothermal and Phase-Field Models." *ACS Applied Electronic Materials* 5.1 (2023): 281-290.

[27] M. Gupta et al., "The preparation, properties and applications of silicon nitride thin films deposited by plasma-enhanced chemical vapor deposition." *Thin Solid Films* 204.1 (1991): 77-106.

[28] M. Von Arx et al., "Process-dependent thin-film thermal conductivities for

thermal CMOS MEMS." *Journal of Microelectromechanical systems* 9.1 (2000): 136-145.

[29] M. Asheghi et al., "Thermal conduction in doped single-crystal silicon films." *Journal of applied physics* 91.8 (2002): 5079-5088.

[30] J. P. Reifenberg et al., "The impact of thermal boundary resistance in phasechange memory devices." *IEEE Electron Device Letters* 29.10 (2008): 1112-1114.

[31] E. T. Swartz et al., "Thermal boundary resistance." *Reviews of modern physics* 61.3 (1989): 605.

[32] C. Duquenne et al., "Thermal conductivity of aluminium nitride thin films prepared by reactive magnetron sputtering." *Journal of Physics D: Applied Physics* 45.1 (2011): 015301.

[33] K. Cil et al., "Electrical Resistivity of Liquid Ge 2 Sb 2 Te 5 Based on Thin-Film and Nanoscale Device Measurements." *IEEE transactions on electron devices* 60.1 (2012): 433-437.

[34] F. Arnaud et al., "High density embedded PCM cell in 28nm FDSOI technology for automotive micro-controller applications." *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2020.

[35] N. Bala et al., "Recent advances in doped Ge 2 Sb 2 Te 5 thin film based phase change memories." Materials Advances 4.3 (2023): 747-768.

[36] Y. Yin et al., "Characterization of nitrogen-doped Sb2Te3 films and their application to phase-change memory." *Journal of Applied Physics* 102.6 (2007).

[37] Y. Wang et al., "Scandium doped Ge2Sb2Te5 for high-speed and lowpower-consumption phase change memory." *Applied Physics Letters* 112.13 (2018).

[38] K. Ding et al., "Recipe for ultrafast and persistent phase-change memory materials." *NPG Asia Materials* 12.1 (2020): 63.

[39] P. Zhang et al., "Research on Improved Crystallization Properties and Underlying Mechanism of the Sb2Te3 Phase-Change Thin Film by Inserting Sn15Sb85 Layers." *ACS Applied Materials & Interfaces* (2024).

[40] A. Redaelli and Lekhwani. *Phase Change Memory*. Springer, 2017.

Chapter 4. One-Shot Weight Transfer via Analog IHPCM Synapse for Efficient and Variation-Robust Neuromorphic Computing

4.1. Introduction

As artificial intelligence (AI) and the importance of big data processing intensify, the conventional von Neumann computing architecture faces significant challenges [1], [2]. This architecture retrieves data from memory units through a data bus and executes computations in separate arithmetic units, resulting in a Von Neumann bottleneck caused by performance disparities between memory hierarchy. In AI applications, where large-scale vector-matrix multiplications (VMM) are frequently executed, the repeated memory access inherent in the existing architecture significantly limits both processing performance and energy efficiency. Therefore, novel computing architectures that aim to complement or replace traditional computing systems are being actively investigated.

Among these, neuromorphic computing, which emulates the brain's efficient data processing mechanisms, has emerged as a promising alternative [3], [4]. The human brain, a biological computing system comprising approximately $10^{10}-10^{12}$ neurons and 10^4 synaptic connections per neuron, operates in parallel and communicates via spike signals. This event-driven functionality enables the brain to perform complex cognitive tasks while consuming only 20W of power. Neuromorphic computing seeks to emulate these energy-efficient, parallel processing mechanisms, offering a potential solution to the current computing systems.

The crossbar array of analog resistive processing units, employed as synapses in neuromorphic computing, enables the concurrent storage and computation of synaptic weights, thereby effectively accelerating VMM operations [5]-[7]. By representing synaptic weights as conductance, pre-neuron outputs as voltages or time, and synaptic outputs as currents, VMM can be executed in a parallel manner according to Ohm's law and Kirchhoff's current law. As a result, various resistive switching devices, including phase-change memory (PCM) [8]-[12], ferroelectric devices [13]-[16], resistive random-access memory (RRAM) [17]-[21], and electrochemical random-access memory (ECRAM) [22]-[25], have been investigated for analog synapse applications.

The PCM analog synapse has been widely proposed for neuromorphic hardware implementations due to its numerous advantageous characteristics, including technological maturity, high on/off ratio, excellent data retention, small cell size (4F²), and compatibility with silicon CMOS technology [26]-[28]. However, the abrupt nature of amorphization through the melt-quench process of PCM imposes limitations on the linear and symmetric modulation of conductance, which is essential for the learning process. Research has been conducted to improve the linearity during the reset process by implementing structural changes, such as superlattices [29], and performing rapid operation below the thermal time constant [30]. Moreover, an alternative approach has been proposed where two PCM cells are combined into a single synapse unit using only the crystallization process, which enables linear conductance modulation [8]. Nevertheless, PCM still faces inherent limitations when compared to charge-based synapse devices, which exhibit superior linearity and symmetry for learning tasks. As a result, a hybrid approach has been employed, where learning of synaptic weight is conducted using software or chargebased devices, and the trained weights are subsequently transferred to PCM synaptic arrays with high data retention for inference tasks [31].

The application of PCM analog devices in inference engines requires the fast and precise transfer of learned weights with robustness to variations. The conventional weight mapping approach requires sequential program-and-verify of each synapse due to the integrated program and read paths of typical self-heating based PCM structures, necessitating a significant number of iterations to mitigate device-to-device and cycle-to-cycle variations [32], [33]. However, the repetitive program-and-verify scheme imposes limitations on both power efficiency and speed, while remaining vulnerable to device variations. Moreover, incremental step pulse programming (ISPP), commonly employed to apply varying programming voltages based on the current conductance state, increases the complexity of the peripheral circuitry in neuromorphic hardware implementations.

In this study, we propose a one-shot weight transfer (OSWT) scheme using indirect heating phase-change memory (IHPCM) as an analog synaptic device, enabling fast, precise operation and robustness to variations. An analog IHPCM synapse has been fabricated, achieving linear conductance modulations and demonstrating a vast number of intermediate states through indirect heating, in contrast to self-heating PCM synapses. Furthermore, by leveraging the separate program and read paths of IHPCM, we design an OSWT circuit with minimal circuit overhead, facilitating real-time assessment of PCM conductance variations and enabling weight transfer via a single programming pulse.

4.2. Experimental Methods

The IHPCM synaptic device was fabricated following the process flow as shown in Figure 4-1. A Boron-doped p-type Si wafer with 100-nm thick SiO₂ layer formed by thermal oxidation was prepared for the fabrication. 100-nm thick Tungsten (W) layer was deposited as a heater using via RF sputtering using a magnetron sputtering system (KVS-2000L, Korea Vacuum Tech, Ltd.). The W heater was patterned through photolithography and reactive ion etching (RIE, Oxford instruments, PLASMA PRO 100 COBRA). As an insulator between the heater and the PCL, a 50nm thick Si_3N_4 layer was deposited via plasma-enhanced CVD (PECVD, Oxford Instruments, PLASMAPRO SYSTEM100) under 350°C. Two types of phasechange materials, $Ge_2Sb_2Te_5$ and Sb_2Te_3 , were deposited to a thickness of 100nm via RF sputtering using a magnetron sputtering system (KVS-2000L, Korea Vacuum Tech, Ltd.). The phase-change layer (PCL) was patterned through photolithography and RIE. The Si_3N_4 layer beneath the PCL was patterned using photolithography and RIE (GIGALANE, NeoS-MAXIS 200L) for the pad opening of the W heater. The pads for the PCL and heater were fabricated by coating and patterning negative PR (L300 40), followed by the sequential deposition of 10-nm Ti and 100-nm Au layers using E-gun evaporation (SORONA, SRN-200), and formed through a lift-off process. As a capping layer of PCL, a 100-nm SiO₂ layer was deposited via plasmaenhanced CVD (PECVD, Oxford Instruments, PLASMAPRO SYSTEM100) under 350°C and patterned using photolithography and for pad opening of PCL and heater. All photolithography processes were carried out using positive PR (SS03A9), a spin coater for the PR coating, and a maskless patterning system (NANO SYSTEM SOLUTION, DL-1000 HP) for exposure.

The electrical measurements were performed using a probestation (MST800CL, MS Tech). For DC electrical characterization, a semiconductor parameter analyzer (Keysight, Agilent 4155C) was utilized, while AC pulse measurements were conducted using a pulse generator (Keysight, Agilent 81110A) and an oscilloscope (Agilent MS07104B, 4GSa/s).



Figure 4-1. Process flow for the fabrication of the IHPCM synaptic device.

4.3. Results and Discussion

4.3.1 One-Shot Weight Transfer Using IHPCM Synaptic Device

IHPCM induces phase change in the PCL by applying an electrical pulse to the heater during the program (set or reset) operation, generating localized heat through Joule heating, which is subsequently transferred to the PCL. During the read operation, a sufficiently small read voltage is applied to avoid Joule heating in the PCL region, enabling the measurement of the PCM resistance (R_{PCM}) or conductance (G_{PCM}) (Figure 4-2 (a)). It is noteworthy that the heater and PCL are electrically isolated by an intermediate dielectric layer, which allows simultaneous program and read operations. As illustrated in Figure 4-2 (b), applying both program and read pulses concurrently enables real-time monitoring of G_{PCM} changes during the program process. This approach enables the program operation to be terminated through the peripheral circuitry once G_{PCM} reaches the target synaptic weight (G_{Target}), thereby facilitating one-shot weight transfer (OSWT) using a single programming pulse, as depicted in Figure 4-2 (c).

The OSWT scheme offers several advantages over the conventional repetitive program-and-verify scheme based on self-heating PCM structures. The conventional scheme necessitates multiple program and read cycles to minimize errors during transfer [31], leading to significant time consumption for each weight transfer operation per device [33]. Furthermore, in hardware implementations, the required number of pulse sets introduces complexity in the peripheral circuitry, with these limitations becoming increasingly pronounced as the PCM array size expands. In contrast, the IHPCM-based OSWT operates at the device speed level using only a single pulse, enabling fast weight mapping. Additionally, while the conventional method requires repeated set and reset operations to reach G_{Target} , OSWT achieves the target weight with just a single program operation, thus reducing stress on the PCM device and enhancing its endurance. Lastly, the OSWT scheme demonstrates robust performance against various device variations. PCM devices typically exhibit device-to-device variation arising from variations in the fabrication of the PCM array, cycle-to-cycle variation induced by device degradation and the stochastic nature of crystallization, and threshold voltage (V_{th}) variation due to structural relaxation in the amorphous phase [4], [34]. In IHPCM synaptic devices, phase change is induced through indirect heating during the program operation, thereby eliminating the need for threshold switching. Moreover, as G_{PCM} changes are monitored in real-time during every weight transfer process, the OSWT scheme demonstrates the potential to maintain robust performance against both device-to-device and cycle-to-cycle variations.



Figure 4-2. (a) Top view of the schematic diagram of the IHPCM synapses. (b) Electric pulse timing diagram for the simultaneous program and read operations in OSWT. (c) Transient variation of G_{PCM} during the program process. In the OSWT scheme, the program pulse is terminated once G_{PCM} reaches the G_{Target} .

4.3.2. Device Performance of Analog IHPCM Synaptic Device

IHPCM synaptic devices based on two phase-change materials, $Ge_2Sb_2Te_5$ and Sb_2Te_3 , were successfully fabricated, as depicted in Figure 4-3. The devices incorporated a heater with dimensions of 1µm in width (W_H) and 20µm in length (L_H), with the PCL electrically insulated from the heater by an intermediate Si_3N_4 layer. The width of the PCL (W_{PCL}) ranged from 2 to 10µm, and the PCL pad was formed above the broad PCL region, with an inter-pad distance (L_{PCL}) ranging from 3 to 10µm. A top SiO_2 layer was employed as a capping layer, providing encapsulation and protection for PCL.

The electrical measurement setup used for characterizing the IHPCM synaptic devices is shown in Figure 4-4. Reset and set pulses were generated by a pulse generator and applied to the heater, with the output resistance and load resistance configured at 50 Ω and 100 Ω , respectively. The voltage applied to the heater's top electrode (V_{PG}^{Out}), after passing through the output resistance, was distributed between the heater and the oscilloscope connected to the heater's bottom electrode. The voltage across the heater (V_H) was calculated by subtracting the voltage measured at the heater's bottom electrode (V_{OSC}^{CH1}) from the voltage measured through an oscilloscope connected in parallel to the heater with a $Z_0 = 1M\Omega$ impedance (V_{OSC}^{CH3}). R_{PCM} was measured after each reset or set operation using a semiconductor parameter analyzer (SPA), which applied a read voltage (V_{Read}) to the top electrode of PCL. All measurement instruments were interfaced with a computer through a general-purpose interface bus (GPIB) and controlled using LabVIEW software.

The temperature of the heater (T_H) as a function of the applied power was estimated by leveraging its temperature-dependent resistance as follows

$$R_H(T) = \rho_{H,Ref} \frac{L_H^{total}}{t_H W_H} \left(1 + \alpha_H \left(T_H - T_{Ref} \right) \right) + 2R_C^H \tag{1}$$

where $\rho_{H,Ref}$ represents the electrical resistivity of heater at T_{Ref} , L_H^{total} denotes the total length of heater, t_H denotes the thickness of heater, W_H is the width of heater, α_H is the temperature coefficients of resistance (TCR) of heater, T_{Ref} is the room temperature, R_C^H denotes the contact resistance. The TCR of the W heater $(\alpha_H = 0.0012K^{-1})$ was measured using a four-point probe structure, with the stage temperature in the probestation systematically increased (Figure 4-5 (a)). A DC voltage sweep was applied to the heater utilizing a SPA, enabling the calculation of the T_H as a function of the applied power via Equation (1). Throughout the analysis, R_C^H was assumed to remain constant over the entire temperature range. The measurement results indicated that achieving a temperature of 1000K within the heater requires power consumption of approximately 180 mW (Figure 4-5 (b)).

The cycle endurance of IHPCM synaptic devices was evaluated under repeated reset and set operations. Devices with $W_{PCL} = 2\mu m$ and $L_{PCL} = 10\mu m$ were used for measurements. During the reset process, pulses with a 1µs width and 2.5ns rise and fall times were applied, using V_H^{RESET} values of 5.2V for $Ge_2Sb_2Te_5$ and 5.0V for Sb_2Te_3 . For set operations, pulses with a 1µs width and 500ns rise and fall times were employed, with V_H^{SET} values of 3.0V for $Ge_2Sb_2Te_5$ and 3.2V for Sb_2Te_3 . The results showed that both phase-change materials demonstrated stable operation over 100 cycles, as depicted in Figure 4-6. The endurance of IHPCM devices can be further improved by employing a buried heater structure to deposit the PCL on a flat surface [35]. As shown in Figure 4-7 (a), the IHPCM synaptic devices incorporating a buried heater structure for $Ge_2Sb_2Te_5$ and Sb_2Te_3 phase-change materials were fabricated using the W damascene process outlined in Chapter 3.2. Devices with PCL

dimensions of $W_{PCL} = 3\mu m$ and $L_{PCL} = 50\mu m$, and heater dimensions of $W_H = 0.5\mu m$ with $L_H = 30\mu m$ for $Ge_2Sb_2Te_5$ and $L_H = 20\mu m$ for Sb_2Te_3 , were used for the measurements. During the reset operation, pulses with a width of 1µs and rise/fall times of 2.5ns were applied, with V_H^{RESET} values of 6.5V for $Ge_2Sb_2Te_5$ and 4.2V for Sb_2Te_3 . In the set operation, pulses with rise/fall times of 500ns were employed, with a pulse width of 50µs and V_H^{SET} of 3.9V for $Ge_2Sb_2Te_5$, and a pulse width of 10µs and V_H^{SET} of 2.3V for Sb_2Te_3 . The results showed that both IHPCM devices demonstrated significantly improved endurance on the order of 1×10^3 to 1×10^4 cycles (Figure 4-7 (b), (c)).

Analog synaptic devices exhibiting high precision offer significant advantages in enhancing integration density by enabling the storage of a wide range of weight states per cell. The multistate capability of IHPCM synapses was evaluated under gradual set operations by varying the V_H^{SET} . Identical pulses with rise and fall times of 500ns and durations of 1µs for $Ge_2Sb_2Te_5$ and 2µs for Sb_2Te_3 were applied. The changes in R_{PCM} and G_{PCM} during gradual set operation are presented in Figure 4-8. The results demonstrated that lowering the V_H^{SET} induced more gradual crystallization in both phase-change materials, leading to more linear G_{PCM} changes and an increase in the number of intermediate states. By applying electric pulses with a duration of 1µs and V_H^{SET} values of 2.38V for $Ge_2Sb_2Te_5$ and 2.03V for Sb_2Te_3 , the gradual set operations achieved 2×10^3 states for $Ge_2Sb_2Te_5$ and 1×10^4 states for Sb_2Te_3 , as shown in Figure 4-9. These results demonstrated an unprecedented level of precision, exceeding the highest record of several thousand states reported in prior studies [36], [37]. The remarkable precision of the IHPCM synaptic devices was attributed to the absence of threshold switching, a

phenomenon inherent to conventional self-heating PCM devices that induces abrupt temperature fluctuations within the PCL. Furthermore, the use of an identical pulse scheme simplifies the design of peripheral circuits for neuromorphic hardware implementations.

Since PCM analog synaptic devices implement multistate through partial crystallization, the crystallization behavior of the phase-change material can influence the programming of intermediate states. To investigate this, the variation of intermediate states under repeated gradual set operations was evaluated for $Ge_2Sb_2Te_5$ and Sb_2Te_3 . Gradual set pulses with 500ns rise and fall times and a duration of 1µs were applied 30 times per cycle for 10 cycles, using V_H^{SET} values of 1.9V for $Ge_2Sb_2Te_5$ and 2.1V for Sb_2Te_3 . The results showed that IHPCM synaptic device with $Ge_2Sb_2Te_5$ exhibited significant variation in intermediate states across cycles, whereas Sb_2Te_3 demonstrated minimal variation, as illustrated in Figure 4-10. These differences can be attributed to the distinct crystallization behaviors, which are governed by nucleation-dominated or growth-dominated mechanisms [38], [39]. Ge₂Sb₂Te₅, a representative nucleation-dominant phasechange material [40], [41], underwent crystallization through the formation and growth of numerous nuclei, leading to stochastic variations in intermediate states during cycling. In contrast, Sb_2Te_3 , a growth-dominant phase-change material often employed as a seed layer in superlattice PCM structures [42], [43], underwent crystallization primarily at the amorphous-crystalline phase boundary, thereby ensuring uniform intermediate states even under repeated cycling. Therefore, the results suggested that the crystallization behavior of phase-change materials can significantly impact synaptic properties, underscoring the need for further research.



Figure 4-3. Top (left) and side (right) views of (a) the schematic diagram and (b) the scanning electron microscope (SEM) image of the IHPCM synaptic device.



Figure 4-4. Electrical measurement setup used to characterize the device properties of the IHPCM synapse.



Figure 4-5. (a) Resistance of the heater measured as a function of stage temperature increase using a four-point probe structure. The four-point probe structure was fabricated with a width of 1µm and a length of 40µm. (b) The estimated temperature within the heater as a function of applied power. The measured TCR value (α_H) was used for the estimation.



Figure 4-6. R_{PCM} variations of the IHPCM synaptic device during repeated reset and set operations for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 .



Figure 4-7. (a) Top (left) and side (right) views of the SEM image of the IHPCM synaptic device with a buried heater. R_{PCM} variations of the IHPCM synaptic device with the buried heater during repeated reset and set operations for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 .



Figure 4-8. R_{PCM} (left) and G_{PCM} (right) variations under gradual set operations with varying V_{SET} for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . A decrease in V_{SET} resulted in more linear changes in G_{PCM} and an increased number of intermediate states.



Figure 4-9. The changes in G_{PCM} by the gradual set operation of analog IHPCM synapses for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 .



Figure 4-10. The variations in R_{PCM} over 10 cycles of repeated gradual set operations for (a) $Ge_2Sb_2Te_5$ and (b) Sb_2Te_3 . The IHPCM synaptic device with $Ge_2Sb_2Te_5$ exhibited substantial variation in intermediate states over cycles, attributed to the stochastic nature of nucleation, whereas Sb_2Te_3 demonstrated small variations, as its primary crystallization occurred at the amorphous-crystalline phase boundary.

4.3.3. Proposal of One-Shot Weight Transfer Circuit

A circuit for the OSWT scheme utilizing the IHPCM synaptic device is proposed. The proposed OSWT circuit is divided into two primary functional stages. The first stage converts the read current from the PCM (I_{PCM}) into an analog voltage, which is subsequently processed by the second stage. In the second stage, the analog voltage is compared with a reference voltage (V_{REF}), which represents the voltage value corresponding to G_{Target} . Based on the comparison result, a control signal is generated to turn the programming pulse on or off for the heater within the IHPCM. This circuit design automatically determines whether additional programming is required for PCM, thereby enabling efficient weight transfer in neural network inference systems.

The most straightforward implementation of this circuit is the voltage divider type, where a resistor (R_1) is connected in series between the bottom electrode of the PCM and ground (GND), as illustrated in Figure 4-11 (a). During OSWT operation, the read voltage (V_{READ}) is applied to the top electrode of the PCM, causing a voltage division that follows Equation (2). The resulting voltage (V_{PCM}) is then compared with the designated V_{REF} to regulate the switching of programming pulses. Although this simple circuit design effectively demonstrates the operational functionality of the OSWT circuit, it is subject to several significant limitations. Specifically, the bottom electrode of the PCM is not fixed to the GND level, which makes the OSWT circuit unusable in the inference phase of the network. Additionally, the available range of V_{REF} is constrained by the absence of current amplification, and employing high V_{READ} to extend this range introduces the risk of self-heating in addition to the indirect heating.

$$V_{PCM} = \frac{R_1}{R_{PCM} + R_1} \times V_{READ} \tag{2}$$

To address this issue, a three-stage amplification circuit utilizing operational amplifiers can be employed. This approach is inspired by the previously reported rectified linear unit (ReLU) neuron circuit that utilizes analog input and output signals [44], enabling the amplification of the I_{PCM} while setting the PCM's bottom electrode to GND (virtual ground). As shown in Figure 4-11 (b), the amplifier-based OSWT circuit consists of the three-stage amplified ReLU neuron circuit, along with additional components such as a comparator for V_{REF} comparison and a multiplexer (analog switch) for controlling program operations. The diode connections used in the ReLU neuron circuit, which serve only as rectifiers for reverse read currents, are omitted in the OSWT circuit. In the first stage of the OSWT circuit, the inverting amplifier converts I_{PCM} into a negative voltage. The bottom electrode of the PCM is consistently maintained at GND by the amplifier, and the output voltage of the first stage ($V_{Out,1}$) is defined as follows.

$$V_{Out,1} = -\frac{R_1}{R_{PCM}} \times V_{READ}$$
(3)

The second stage functions as a voltage follower, serving as a buffer that transmits the signal without distortion while minimizing interference between the input and output. The output voltage of the second stage ($V_{Out,2}$) is as follows.

$$V_{Out,2} = V_{Out,1} = -\frac{R_1}{R_{PCM}} \times V_{READ}$$
(4)

The third stage inverts and amplifies $V_{Out,2}$, outputting a positive voltage. The output voltage of the third stage ($V_{Out,3}$) is determined by the ratio of resistors R_2 and R_3 , as expressed in Equation (5).

$$V_{Out,3} = -\frac{R_3}{R_2} \times V_{Out,2} = \frac{R_1 R_3}{R_2 R_{PCM}} \times V_{READ} = \frac{R_1 R_3}{R_2} \times I_{PCM}$$
(5)

As a result, I_{PCM} is amplified by adjusting the ratio of the three resistors R_1 , R_2 , and R_3 . The final output, $V_{Out,3}$, is directly correlated with G_{PCM} and is therefore defined as V_{PCM} . When V_{PCM} reaches the pre-determined V_{REF} within the comparator, the programming pulse is terminated. The relationship between V_{REF} and G_{Target} is described as follows.

$$V_{REF} = \frac{R_1 R_3}{R_2} \times V_{READ} \times G_{Target} \tag{6}$$

The operation of the proposed OSWT circuit was evaluated using LTspice simulation software, leveraging an extensive simulation program with integrated circuit emphasis (SPICE) model library comprising commercially available components (Figure 4-12 (a)). For precise weight transfer, the components within the OSWT circuit must demonstrate high-speed operation with minimal delay. Moreover, the analog switch must operate reliably under the tens of mA of current applied to the heater during the programming process. The LTspice simulations were performed by selecting components from the available library that best meet these requirements. The increase in V_{PCM} during the crystallization process of the PCM was modeled by simplifying it as a gradual rise in V_{READ} , applied to a resistor representing R_{PCM} . As shown in Figure 4-12 (b), the results demonstrated that V_{PCM} increased with an increase in V_{READ} . Once V_{PCM} reached the V_{REF} , the V_{SET} applied to the heater transitioned to GND after a delay of approximately 0.1 µs. This delay can be further reduced by employing high-performance components and onchip integration of the IHPCM and peripheral circuitry within the wafer. Therefore, it was confirmed that the proposed OSWT circuit can successfully monitor the R_{PCM} change during phase transitions and effectively control the programming process.

The implementation of the OSWT scheme, integrating the amplifier-based OSWT

circuit and the IHPCM synaptic device, can be performed using the electrical measurement setup illustrated in Figure 4-13 (a). During the reset process, a pulse generator applies V_{RESET} to the top electrode of the heater in the IHPCM synapse. An additional pulse generator is employed to apply V_{READ} and V_{SET} , with V_{SET} applied sequentially after V_{READ} following a predefined delay, as shown in Figure 4-13 (b). V_{SET} is delivered to the input of the analog switch within the OSWT circuit, and subsequently, based on the signal transmitted from the comparator to the switch device, either V_{SET} or GND is applied to the top electrode of the heater. V_{READ} is applied to the top electrode of the PCL in the IHPCM synapse, while the bottom electrode of the PCL is connected to the input of the first amplifier within the OSWT circuit, enabling the transmission of I_{PCM} . The operation of the OSWT scheme can be monitored by measuring V_{PCM} at the comparator input and V_{SET} at the output of the switch device using an oscilloscope. The impedance of each oscilloscope channel is set to $1M\Omega$ to ensure accurate measurements. The ideal operating behavior of OSWT is shown in Figure 4-14. In the initial region where only the V_{READ} is applied, the PCM remains in the reset state, resulting in a very low V_{PCM} . When V_{SET} is applied, a phase change occurs, causing V_{PCM} to increase. Once the V_{PCM} reaches the designated V_{REF} value, the V_{SET} applied to the heater of the IHPCM synaptic device is turned off, and the final V_{PCM} value stabilizes at V_{REF} .



Figure 4-11. Circuit diagram of the proposed OSWT circuit, featuring (a) a voltage divider and (b) amplifiers for converting I_{PCM} into an analog voltage prior to the comparator node.



Figure 4-12. (a) Circuit diagram utilized in the LTspice simulation. (b) Voltage variations at each node over time during OSWT operations. V_{REF} was set to 1V, with V_{PCM} and V_{SET} monitored at the comparator input node and the output node of the analog switch, respectively.



Figure 4-13. (a) Electrical measurement setup for implementing OSWT operation using the IHPCM synapse and amplifier-based OSWT circuit. (b) The pulse timing diagram of V_{SET} and V_{Read} utilized for OSWT operations.



Figure 4-14. Transient variation of V_{SET} and V_{PCM} during OSWT operations using an amplifier-based OSWT circuit and the IHPCM synaptic device.

4.4. Conclusion

An OSWT scheme is proposed that enables fast and robust weight transfer under variations, utilizing the separate program and read paths of the IHPCM to monitor resistance changes caused by phase transitions in real-time. The IHPCM synaptic device, which eliminates the need for threshold switching during the set process, is experimentally validated to achieve high precision $(1 \times 10^4 \text{ states})$ through precise temperature control. Furthermore, an OSWT circuit is proposed, leveraging the existing ReLU neuron circuit to minimize circuit overhead, which monitors the resistance change during phase transitions and autonomously controls the programming process. The OSWT scheme utilizing the IHPCM synaptic device offers a promising solution, addressing the inherent limitations of conventional PCM-based inference machines at the hardware level, particularly in terms of operational speed and susceptibility to various variations.

4.5. Bibliography

[1] A. Mehonic, and A. J. Kenyon. "Brain-inspired computing needs a master plan." *Nature* 604.7905 (2022): 255-260.

[2] X. Xu et al., "Scaling for edge inference of deep neural networks." *Nature Electronics* 1.4 (2018): 216-222.

[3] D. Kuzum et al., "Synaptic electronics: materials, devices and applications." *Nanotechnology* 24.38 (2013): 382001.

[4] R. Islam et al., "Device and materials requirements for neuromorphic computing." *Journal of Physics D: Applied Physics* 52.11 (2019): 113001.

[5] Q. Xia, and J. J. Yang., "Memristive crossbar arrays for brain-inspired computing." *Nature materials* 18.4 (2019): 309-323.

[6] N. L. Upadhyay et al., "Emerging memory devices for neuromorphic computing." *Advanced Materials Technologies* 4.4 (2019): 1800589.

[7] T. Gokmen, and Y. Vlasov, "Acceleration of deep neural network training with resistive cross-point devices: Design considerations." *Frontiers in neuroscience* 10 (2016): 333.

[8] M. Suri et al., "Phase change memory as synapse for ultra-dense neuromorphic systems: Application to complex visual pattern extraction." *2011 International Electron Devices Meeting*. IEEE, 2011.

[9] D. Kuzum et al., "Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing." *Nano letters* 12.5 (2012): 2179-2186.

[10] K. Ren et al., "Controllable SET process in O-Ti-Sb-Te based phase change memory for synaptic application." *Applied Physics Letters* 112.7 (2018).

 $1 \ 2 \ 0$

[11] S. La Barbera et al., "Narrow Heater Bottom Electrode-Based Phase
 Change Memory as a Bidirectional Artificial Synapse." *Advanced Electronic Materials* 4.9 (2018): 1800223.

 [12] X. Sun et al., "PCM-based analog compute-in-memory: Impact of device non-idealities on inference accuracy." *IEEE Transactions on Electron Devices* 68.11
 (2021): 5585-5591.

[13] M. Jerry et al., "Ferroelectric FET analog synapse for acceleration of deep neural network training." 2017 IEEE international electron devices meeting (IEDM).
 IEEE, 2017.

[14] M. K. Kim, and J-S. Lee. "Ferroelectric analog synaptic transistors." *Nano letters* 19.3 (2019): 2044-2050.

[15] Y. Goh et al., "High performance and self-rectifying hafnia-based ferroelectric tunnel junction for neuromorphic computing and TCAM applications." *2021 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2021.

[16] M. K. Kim et al., "CMOS-compatible compute-in-memory accelerators based on integrated ferroelectric synaptic arrays for convolution neural networks." *Science Advances* 8.14 (2022): eabm8537.

[17] L. Xia et al., "Technological exploration of RRAM crossbar array for matrix-vector multiplication." *Journal of Computer Science and Technology* 31.1 (2016): 3-19.

[18] W. Wu et al., "A methodology to improve linearity of analog RRAM for neuromorphic computing." *2018 IEEE symposium on VLSI technology*. IEEE, 2018.

[19] K. Moon et al., "RRAM-based synapse devices for neuromorphic systems." *Faraday discussions* 213 (2019): 421-451.

[20] P. Yao et al., "Fully hardware-implemented memristor convolutional neural network." *Nature* 577.7792 (2020): 641-646.

[21] Z. Peng et al., "HfO2-based memristor as an artificial synapse for neuromorphic computing with tri-layer HfO2/BiFeO3/HfO2 design." *Advanced Functional Materials* 31.48 (2021): 2107131.

[22] E. J. Fuller et al., "Li-ion synaptic transistor for low power analog computing." *Advanced Materials* 29.SAND-2017-0895J (2016).

[23] R. D. Nikam et al., "Near ideal synaptic functionalities in Li ion synaptic transistor using Li3POxSex electrolyte with high ionic conductivity." *Scientific reports* 9.1 (2019): 18883.

[24] J. Lee et al., "Strategies to improve the synaptic characteristics of oxygenbased electrochemical random-access memory based on material parameters optimization." *ACS Applied Materials & Interfaces* 14.11 (2022): 13450-13457.

[25] H. Kwak et al., "Electrochemical random-access memory: recent advances in materials, devices, and systems towards neuromorphic computing." *Nano Convergence* 11.1 (2024): 9.

[26] G. W. Burr et al., "Recent progress in phase-change memory technology." *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 6.2 (2016): 146-162.

[27] J. Izraelevitz et al., "Basic performance measurements of the intel optane DC persistent memory module." *arXiv preprint arXiv:1903.05714* (2019).

[28] G. W. Burr et al., "Experimental demonstration and tolerancing of a largescale neural network (165 000 synapses) using phase-change memory as the synaptic weight element." *IEEE Transactions on Electron Devices* 62.11 (2015): 3498-3507.

[29] S. Kang et al., "Bidirectional Electric-Induced Conductance Based on
GeTe/Sb2Te3 Interfacial Phase Change Memory for Neuro-Inspired Computing." *Electronics* 10.21 (2021): 2692.

[30] K. Stern et al., "Sub-Nanosecond Pulses Enable Partial Reset for Analog Phase Change Memory." *IEEE Electron Device Letters* 42.9 (2021): 1291-1294.

[31] S. Ambrogio et al., "Equivalent-accuracy accelerated neural-network training using analogue memory." *Nature* 558.7708 (2018): 60-67.

[32] N. Papandreou et al., "Programming algorithms for multilevel phasechange memory." 2011 IEEE International Symposium of Circuits and Systems (ISCAS). IEEE, 2011.

[33] A. Antolini et al., "A readout scheme for PCM-based analog in-memory computing with drift compensation through reference conductance tracking." *IEEE Open Journal of the Solid-State Circuits Society* (2024).

[34] S. Kim et al., "Resistance and threshold switching voltage drift behavior in phase-change memory and their temperature dependence at microsecond time scales studied using a micro-thermal stage." *IEEE Transactions on Electron Devices* 58.3 (2011): 584-592.

[35] R. M. Young et al., "Improvements in GeTe-based phase change RF switches." 2018 IEEE/MTT-S International Microwave Symposium-IMS. IEEE, 2018.

[36] W. Kim et al., "Confined PCM-based analog synaptic devices offering low resistance-drift and 1000 programmable states for deep learning." *2019 Symposium on VLSI Technology*. IEEE, 2019.

[37] M. Rao et al., "Thousands of conductance levels in memristors integrated on CMOS." *Nature* 615.7954 (2023): 823-829.

[38] A. Redaelli, and Lekhwani. Phase Change Memory. Springer, 2017.

[39] W. Zhang et al., "Designing crystallization in phase-change materials for universal memory and neuro-inspired computing." Nature Reviews Materials 4.3 (2019): 150-168.

[40] S. Privitera et al., "Crystal nucleation and growth processes in Ge 2 Sb 2 Te5." Applied physics letters 84.22 (2004): 4448-4450.

[41] M. A. Luong, et al., "Effect of nitrogen doping on the crystallization kinetics of Ge2Sb2Te5." Nanomaterials 11.7 (2021): 1729.

[42] Y. Saito et al., "A two-step process for growth of highly oriented Sb2Te3 using sputtering." AIP Advances 6.4 (2016).

[43] R. E. Simpson, et al., "Interfacial phase-change memory." Nature nanotechnology 6.8 (2011): 501-505.

[44] F. Kiani et al., "A fully hardware-based memristive multilayer neural network." *Science advances* 7.48 (2021): eabj4801.

Chapter 5. Conclusion

In this dissertation, optimization strategies for various applications have been proposed and analyzed by utilizing the distinct program and read path characteristics of the IHPCM structure.

Chapter 2 demonstrates, through device simulation-based analysis, that the separated program and read paths of IHPCM resolve the trade-off between set resistance and reset current, which becomes a significant issue when scaling down the existing PCM devices. Additionally, it is shown that the significant reduction in current density ($>\times 10^{10}$) in the phase-change material during the program can substantially enhance cycle endurance by suppressing electromigration, which is a major driving force of cycle endurance degradation. Furthermore, energy efficiency is further enhanced by optimizing the structure and material properties of IHPCM, as well as the thermoelectric effects of the heater materials.

Chapter 3 proposes an optimized IHPCM device with dual heaters to enable precise characterization of crystallization properties under a uniform temperature distribution. Through device simulation, the limitations of achieving temperature uniformity in the amorphous region when using a single heater are analyzed, and an additional heater is introduced to locally form the amorphous region, thereby ensuring a sufficiently uniform temperature distribution. The optimized IHPCM characterization structure demonstrates a highly uniform temperature distribution, with a variation of less than 0.1%, even at high temperatures near the melting point, while enabling rapid operation with high heating rates ($1.8 \times 10^8 K/s$). By combining electrical measurements and device simulations, a comprehensive characterization of key crystallization properties, such as crystallization temperature,

 $1\ 2\ 5$

crystallization time, the activation energy for crystallization, and non-Arrhenius behavior, is conducted. Furthermore, by utilizing a crystallization model, electrical property changes during crystallization, as well as the processes of nucleation and growth, are analyzed. The integration of electrical measurements and crystallization modeling with the optimized structure provides an analytical framework for the precise and comprehensive investigation of crystallization characteristics required for various applications.

Chapter 4 proposes that when IHPCM is used as a synapse device for inference machines in neuromorphic computing, the newly proposed one-shot weight transfer (OSWT) scheme enables fast and robust weight transfer across various variations. The IHPCM synaptic device demonstrates significantly high precision $(1 \times 10^4$ states) using identical pulses preferred in neuromorphic hardware implementation. The OSWT circuit has been designed and validated through circuit simulations, demonstrating its capability to real-time monitor synaptic weight changes and autonomously regulate program operations. Leveraging the proposed circuit with minimal overhead and the IHPCM synaptic device, the OSWT scheme enables efficient neuromorphic hardware implementation, alleviating the intrinsic limitations of conventional weight transfer and enhancing the performance of the PCM-based inference machine.

This dissertation proposes and analyzes optimization strategies for various applications of IHPCM, taking advantage of its structural characteristics. The research employs a diverse range of methodologies, including material property analysis, device simulations incorporating electrothermal and crystallization models, device fabrication and measurement, as well as circuit demonstration. The comprehensive insights into IHPCM provided by this dissertation not only expand the scope of its applications but also shed light on the analysis and advancement of conventional PCM devices.

Abstract (in Korean)

인공지능(AI) 기술이 점차 고도화됨에 따라, 급증하는 데이터와 계산 매 개변수를 빠르고 효율적으로 처리할 수 있는 컴퓨팅 시스템에 대한 수요 가 증가하고 있다. 기존의 폰 노이만(Von Neumann) 컴퓨팅 아키텍처는 로직과 메모리 구성 요소 간의 성능 격차로 인해 발생하는 메모리 병목 현상으로 이러한 요구를 충족하는 데 한계를 가진다. 이를 해결하기 위 해, 기존 메모리 계층 구조의 성능 격차를 해소하는 스토리지 클래스 메 모리(SCM)와, 저장 메모리에서 연산을 직접 수행하여 계산 효율성을 높 이는 인 메모리 컴퓨팅과 같은 대안적 접근 방식에 대한 연구가 이루어 지고 있다. 또한, 인간 두뇌의 고효율 처리 메커니즘을 모방하는 뉴로모 픽 컴퓨팅도 많은 주목을 받고 있다. 이러한 발전에 맞추어, 첨단 컴퓨팅 방식에 사용될 수 있는 차세대 메모리 소자 개발에 대한 필요성이 커지 고 있다.

상변화 메모리는 현재 가장 기술 성숙도가 높은 차세대 비휘발성 메모 리이다. 그러나, 기존의 상변화 메모리는 통합된 프로그램 및 읽기 경로 구조로 인해 소자 특성 간의 트레이드오프가 존재하기 때문에 소자 성능 최적화에 제한이 따른다. 반면, 프로그램과 읽기 경로가 전기적으로 분리 된 간접 가열 상변화 메모리는 각 경로를 독립적으로 최적화할 수 있어, 응용 분야별 요구 특성에 맞는 다양한 최적화 방안을 적용하기 용이하다. 본 연구에서는 간접 가열 상변화 메모리의 물성 및 구조 최적화를 통하 여 다양한 응용 분야에 대한 활용을 분석하고 평가하였다.

 $1\ 2\ 8$

첫 번째 파트에서는 간접 가열 상변화 메모리를 SCM 분야에 활용할 경우, 기존 상변화 메모리의 미세화 시 발생하는 소비 전력과 동작 속도 간의 트레이드오프 문제와 강한 전기장으로 인한 내구성 저하 문제에서 벗어날 수 있음을 소자 시뮬레이션을 기반으로 분석하였다. 또한, 물질, 구조 최적화 및 열전효과의 극대화를 통하여 에너지 효율을 향상시킬 수 있음을 제안하였다.

두 번째 파트에서는 소자 시뮬레이션을 활용한 구조 최적화를 통해, 간접 가열 상변화 메모리를 균일한 온도 분포 하에서 상변화 물질의 주 요 결정화 특성과 거동을 정밀하게 측정하고 분석할 수 있는 도구로 사 용할 수 있음을 제안하였다. 소자 제작 및 측정과 함께 결정화 시뮬레이 션을 활용하여, 결정화 과정에서 발생하는 전기적 특성 변화와 핵 생성 및 성장 과정을 심도 있게 분석하였다.

마지막 파트에서는 간접 가열 상변화 메모리를 뉴로모픽 컴퓨팅을 위한 아날로그 시냅스 소자로 활용하는 방안이 제안되었다. 간접 가열 상변화 메모리를 활용한 단일 가중치 전송 기법을 사용할 경우 가중치 전송을 빠르고 소자 및 사이클 간 변동성에도 견고하게 동작할 수 있음을 제안하였다. 간접 가열 상변화 시냅스 소자는 임계 전환을 필요로 하지 않기 때문에 정밀한 열 제어를 통해 상당한 수의 중간 상태를 구현할 수 있음을 실험적으로 입증하였다. 이와 더불어, 단일 가중치 전송 기법을 구현할 수 있는 소형화된 회로 설계를 고안하여, 뉴로모픽 하드웨어 구현에 효율적으로 통합될 수 있음을 제안하였다. 주요어: 상변화 메모리, 간접 가열 상변화 메모리, 스토리지 클래스 메모 리, 열전 효과, 결정화, 뉴로모픽 컴퓨팅, 아날로그 시냅스, 가중치 전달

학번: 2018-20684

최 인 혁