Fabrication and electrical characteristics of high-performance ZnO nanorod field-effect transistors

Won Il Park, Jin Suk Kim, and Gyu-Chul Yi[a)]
National CRI Center for Semiconductor Nanorods and Department of Materials Science and Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk 790-784, Korea

M. H. Bae and H.-J. Lee
Department of Physics, POSTECH, Pohang, Gyeongbuk 790-784, Korea

(Received 3 May 2004; accepted 30 September 2004)

We report on fabrication and electrical characteristics of high-mobility field-effect transistors (FETs) using ZnO nanorods. For FET fabrications, single-crystal ZnO nanorods were prepared using catalyst-free metalorganic vapor phase epitaxy. Although typical ZnO nanorod FETs exhibited good electrical characteristics, with a transconductance of ~140 nS and a mobility of 75 $cm^2/V\,s$, the device characteristics were significantly improved by coating a polyimide thin layer on the nanorod surface, exhibiting a large turn-ON/OFF ratio of 10^4-10^5, a high transconductance of 1.9 μS, and high electron mobility above 1000 $cm^2/V\,s$. The role of the polymer coating in the enhancement of the devices is also discussed. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1821648]

ZnO semiconductor nanowires and nanorods are attractive components for nanometer scale electronic and photonic device applications.[1–3] Recently, a wide variety of nanodevices including ultraviolet photodetectors,[4] Schottky diodes,[5] and light-emitting device arrays[6] have been fabricated utilizing ZnO nanorods (nanowires). In particular, a field-effect transistor (FET),[7] one of the most fundamental and important electronic components, has been fabricated using a ZnO nanobelt. However, the ZnO nanobelt FET has exhibited poor transistor characteristics: a low switching current ON/OFF ratio below 100, a transconductance ($g_m = dI_{sd}/dV_g$) of a few nS, and a maximum ON state source-drain current (I_{sd}) of ~10 nA even at a large source-drain voltage (V_{sd}) of 6.5 V. The poor ZnO nanobelt transistor characteristics may result from a high concentration of impurities in ZnO nanobelts, large contact resistance, or surface-mediated effects including chemisorption and carrier scattering or trap processes by surface states.[8–10] Here, we report on high-performance ZnO nanorod FETs fabricated using high-quality single-crystal ZnO nanorods and a polymer-coating method to reduce surface-mediated effects.

ZnO nanorod FETs were fabricated by using high-quality ZnO nanorods and e-beam lithography [Fig. 1(a)]. Single-crystal ZnO nanorods were prepared on Si or sapphire substrates using catalyst-free metalorganic vapor phase epitaxy (MOVPE),[2] and then dispersed on SiO_2/Si. A 250-nm-thick silicon oxide layer was employed as an insulating gate oxide layer on a heavily doped *n*-type silicon substrate. Good ohmic contacts were obtained by coating Au/Ti metal layers only on nanorod ends and annealing at 300 °C for 2 min.[11] As shown in Fig. 1(b), the metal contacts of source-drain electrodes were separated by 2–5 μm using electron-beam lithography and a lift-off method. Electrical characteristics of ZnO nanorod FETs were measured at room temperature in ambient air using an electrometer and a voltage source meter. To explore the surface passivation effect on the electrical properties of devices, ZnO nanorod FETs were also coated with a polyimide, which has frequently been employed to reduce surface effects in a bipolar technology.[12–14] A 2-μm-thick polyimide (*n*-methoxy methylated nylon) was coated using a spinner and then cured at 120 °C for 5 h.

Figure 2(a) shows typical current–voltage ($I_{sd}-V_{sd}$) characteristic curves as a function of gate voltage (V_g) for ZnO nanorod FETs prepared without any intentional surface treatment. As-grown ZnO nanorod FETs exhibited linear and symmetric $I_{sd}-V_{sd}$ curves at different gate voltages (V_g), indicating low resistance of ohmic contacts formed between ZnO and Ti metal layers. In addition, as V_g increases positively (negatively), I_{sd} increases (decreases), indicating that ZnO nanorods are typical *n*-type semiconductors. $I_{sd}-V_g$ curves of ZnO nanorod FETs also show that the devices op-

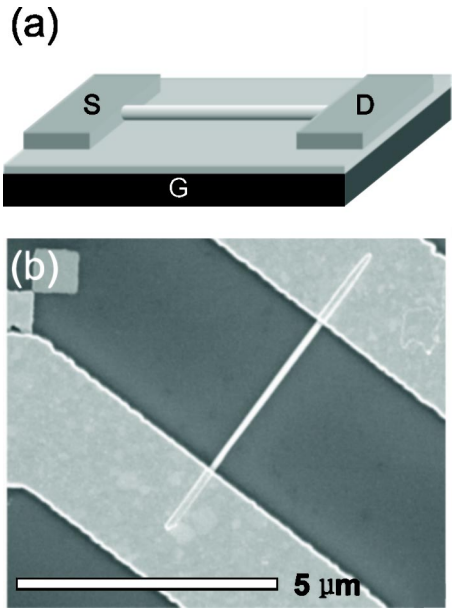

FIG. 1. (a) Schematic side view and (b) field-emission scanning electron microscopy image of a ZnO nanorod FET device. ZnO nanorod FETs with backgate geometry were fabricated on SiO_2/Si by deposition of Au/Ti metal electrodes for source-drain contacts on nanorod ends.

[a)]Author to whom correspondence should be addressed; electronic mail: gcyi@postech.ac.kr

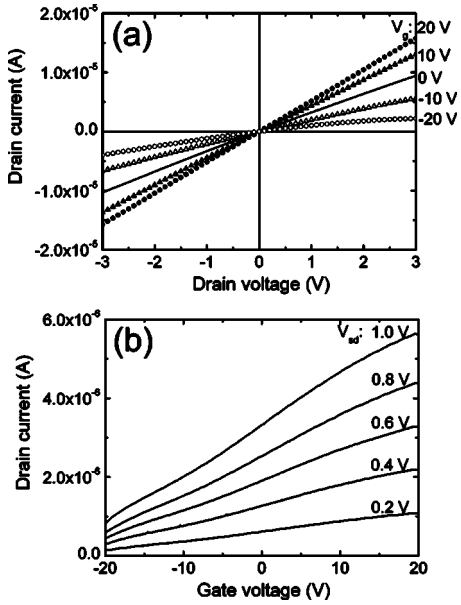

FIG. 2. (a) Typical $I_{sd}-V_{sd}$ characteristic curves as a function of V_g for ZnO nanorod FETs prepared without any intentional surface treatment. The linear and symmetric $I_{sd}-V_{sd}$ curves were obtained under different V_g, indicating the low resistant ohmic contact formation between ZnO and Ti metal layers. (b) $I_{sd}-V_g$ curves of ZnO nanorod FETs show that the devices operate in an *n*-channel depletion mode with g_m of ~140 nS for $V_{sd}=1.0$ V.

erate in a depletion (normally ON) mode and transconductance, g_m is ~140 nS for $V_{sd}=1.0$ V. Assuming that an effective channel width (W) equals a nanorod diameter of 100 nm, normalized transconductance (g_m/W) is estimated to be ~1.4 μS/μm.

It is noted that the normalized transconductance of 1.4 μS/μm for ZnO nanorod FETs is two or three orders of magnitude higher than that (below 5 nS/μm even at large V_{sd} of 6.5 V) for ZnO nanobelt FETs.[7] This may be attributed to high crystallinity and purity of ZnO nanorods prepared using catalyst-free MOVPE. In addition, the reduced contact resistances between nanorods and source-drain electrodes may also affect device characteristics. That is, the previous ZnO nanobelt FETs have been configured by a ZnO nanobelt dispersed on predeposited Au electrodes, yielding high contact resistance. In this research, however, ZnO nanorod FETs were fabricated by evaporating Au/Ti metals on nanorod ends and by thermal annealing. In this device configuration, good ohmic contact resistance for source-drain electrodes was obtained, hence enhancing device performance. Meanwhile, the conductance response to gate bias voltage of ZnO nanorod FETs was still weak, attributed in part to the surface-mediated effects.

The electrical characteristics of ZnO nanorod FETs were significantly improved by coating polyimide on ZnO nanorod surfaces. After the polyimide coating, as shown in Fig. 3, $I_{sd}-V_g$ curves of ZnO nanorod FET exhibit excellent conductance response to V_g: ZnO nanorod FETs were fully turned off even at $V_g=-5$ V and transconductance exhibited the maximum values of 1.9 μS at $V_g=2.3$ V (in case of $V_{sd}=1.0$ V), thirteen times higher than that for as-grown ZnO nanorod FETs before polyimide coating. In addition, the $I_{sd}-V_g$ curve shows drastic decreases of drain current below threshold voltage (V_{th}) and exhibits a large current ON/OFF ratio of 10^4-10^5. A subthreshold swing (S) of ~1.4 V per

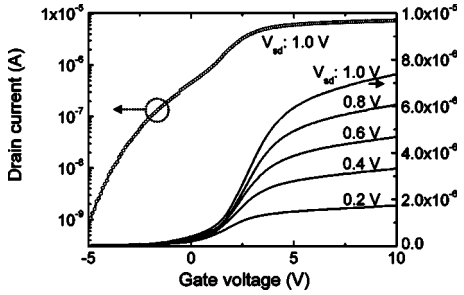

FIG. 3. $I_{sd}-V_g$ curves (solid line) as a function of V_{sd} and log scale plot (open circles) of $I_{sd}-V_g$ ($V_{sd}=1.0$ V) for a ZnO single nanorod FET after polyimide coating on the device. The transistor characteristics of ZnO nanorod FETs were significantly enhanced after polymer coating on ZnO nanorod surfaces.

decade with a maximum ON state current of 7.5 μA was also obtained after polyimide coating.

We further analyzed carrier mobility in ZnO nanorod FETs, an important characteristic of FET. The electron mobility (μ) in ZnO nanorod FETs is calculated by Eq. (1),[15] depending on g_m,

$$\mu = \frac{g_m \times L^2}{C \times V_{sd}}, \tag{1}$$

where C is capacitance given by Eq. (2) for cylinders using an infinite plate model,[16]

$$C = \frac{2\pi\varepsilon_0\varepsilon L}{\ln(2t/r)}. \tag{2}$$

Hence, Eq. (1) can be rearranged as

$$\mu = \frac{g_m \times L^2}{C \times V_{sd}} = \frac{g_m \times L \times \ln(2t/r)}{2\pi\varepsilon_0\varepsilon \times V_{sd}}, \tag{3}$$

where L (5 μm) is the channel length of the nanorod FET, t (250 nm) the thickness of the silicon oxide layer, r (50 nm) the nanorod radius, and ε (3.9) the dielectric constant of silicon.

Figure 4 shows the electron mobility versus V_g plots calculated using Eq. (3). The maximum value of electron mobility of as-grown ZnO nanorod FETs was 75 $cm^2/V\,s$. Although there have been no reports on electron mobility in ZnO nanorod FETs, this value is much higher than that of ZnO-based thin-film transistors (0.01–10 $cm^2/V\,s$).[17] The

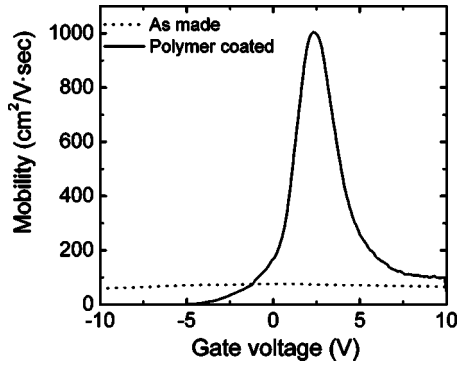

FIG. 4. Electron mobility vs V_g plots of ZnO nanorod FETs before (dotted line) and after polyimide coating (solid line). Mobility was extracted using Eq. (3), and shows the maximum electron-mobility values of 75 and 1000 $cm^2/V\,s$ for as-grown and polyimide-coated ZnO nanorod FETs, respectively.

high carrier mobility of ZnO nanorod FETs results presumably from high crystallinity and low defect concentrations of single-crystal ZnO nanorods due to the catalyst-free growth method employed in this research. Furthermore, the mobility value of nanorod FETs was increased to 1000 $cm^2/V\,s$ by polyimide coating. This value is the highest mobility value among oxide FETs[7,18] and higher than those of any other single-crystal semiconductor nanowire FETs (300 $cm^2/V\,s$ for *p*-type Si nanowire FETs,[19] 600 $cm^2/V\,s$ for *p*-type Ge nanowire FETs,[20] and 150–650 $cm^2/V\,s$ for *n*-type GaN nanowire FETs[21]).

Reproducibility of the polyimide passivation effect on the device performance was also investigated measuring $I-V$ characteristic curves of thirteen different ZnO nanorod FETs before and after the polyimide coating. Before polyimide coating, most of samples showed the relatively weak conductance responses to V_g and they were not fully turned off within applied negative V_g to −20 V. In contrast, the conductance responses to the V_g were significantly enhanced with polyimide coating, and all of the samples were fully turned off in the range of $-15\ V < V_g < -5\ V$. Moreover, the field-effect mobility value of ZnO nanorod FETs was drastically increased from 20–220 $cm^2/V\,s$ with mean value of 75 $cm^2/V\,s$ to 120–3100 $cm^2/V\,s$ with mean value of 680 $cm^2/V\,s$. The highest mobility value of 3100 $cm^2/V\,s$ in ZnO nanorod FETs is even higher than those of the state-of-the-art planar Si MOSFETs (less than 1000 $cm^2/V\,s$) and comparable to well-established single-wall carbon nanotube FETs (1000–20 000 $cm^2/V\,s$).[22,23]

As for the origin of enhanced ZnO nanorod FET characteristics after polymer coating, we make the following suggestions. First, the chemisorption process which decreases transistor gain may be suppressed with polyimide coating. It is well known that there are many chemisorption sites (primarily oxygen vacancy sites) on ZnO nanorod surfaces, where environmental molecules such as oxygen and/or oxygen-containing gaseous species are adsorbed (desorbed) with a negative (positive) charge.[9,10] This chemisorption process may compensate for the conductance response to the applied gate voltage of as-grown ZnO nanorod FETs.[24] However, the polyimide coating blocks the interaction between ZnO nanorod surfaces and molecular species, and may restore the intrinsic transistor gain of ZnO nanorod FETs. Second, modification of ZnO surfaces with polyimide may contribute to passivation of defects which deteriorate transistor characteristics by trapping and scattering carriers.[13,14] Last, the enhanced mobility of polymer-coated nanorod FETs may result from formation of a gate structure surrounded with dielectrics, or low-dimensional electron gas which may be formed by band-bending at the ZnO/polymer interfaces.

In conclusion, we have fabricated high-performance *n*-channel ZnO nanorod FETs. A simple polyimide coating of ZnO nanorod significantly improved FET characteristics, and increased the current on/off ratio from 7 to 10^4–10^5 and also increased transconductance from 140 nS to 1.8 μS. Furthermore, the electron mobility estimated from transconductance exhibits a maximum value of 1000–1200 $cm^2/V\,s$. High-performance nanoscale FETs obtained in this study show the feasibility of semiconductor oxide based nanorods for electronic nanodevice applications. We believe that the simple polymer passivation may be widely used for enhancement of many other nanoscale device characteristics.

This work was supported by the National Creative Research Initiative Project, the National R&D Project for Nano Science and Technology (No. M-0214-00-0115), and the Center for Nanostructured Materials Technology under the 21st Century Frontier R&D Program of the Ministry of Science and Technology. H.-J.L. was supported by the Center for Excellency (Electron Spin Science Center) administered by KOSEF.

[1] M. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, and P. Yang, Science **292**, 1897 (2001).
[2] W. I. Park, D. H. Kim, S. W. Jung, and G.-C. Yi, Appl. Phys. Lett. **80**, 4232 (2002).
[3] W. I. Park, G.-C. Yi, M. Kim, and S. J. Pennycook, Adv. Mater. (Weinheim, Ger.) **15**, 526 (2003).
[4] H. Kind, H. Yan, B. Messer, M. Law, and P. Yang, Adv. Mater. (Weinheim, Ger.) **14**, 158 (2002).
[5] W. I. Park, G.-C. Yi, J.-W. Kim, and S. M. Park, Appl. Phys. Lett. **82**, 4358 (2003).
[6] W. I. Park and G.-C. Yi, Adv. Mater. (Weinheim, Ger.) **16**, 87 (2004).
[7] M. S. Arnold, P. Avouris, Z. W. Pan, and Z. L. Wang, J. Phys. Chem. B **107**, 659 (2003).
[8] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era* (Lattice, Sunset Beach, CA, 1986), Vols. 1, 2, Chap. 8.
[9] M. Liu and H. K. Kim, Appl. Phys. Lett. **84**, 173 (2004).
[10] L. Lagowski, E. S. Sproles, Jr., and H. C. Gatos, J. Appl. Phys. **48**, 3566 (1977).
[11] S. Y. Kim, H. W. Jang, J. K. Kim, C. M. Jeon, W. I. Park, G.-C. Yi, and J.-L. Lee, J. Electron. Mater. **31**, 868 (2002).
[12] T. B. Hook, IEEE Trans. Electron Devices **37**, 1714 (1990).
[13] J. Masum, P. Parmiter, T. J. Hall, and M. Crouch, IEE Proc.-G: Circuits, Devices Syst. **143**, 307 (1996).
[14] Y. Z. Xiong, G.-I. Ng, H. Wang, and J. S. Fu, IEEE Trans. Electron Devices **48**, 2192 (2001).
[15] M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), Chap. 8.
[16] S. Ramo, J. R. Whinnery, and T. V. Duzer, *Fields and Waves in Communication Electronics* (Wiley, New York, 1994), Chap. 4.
[17] H. S. Bae, M. H. Yoon, J. H. Kim, and S. Im, Appl. Phys. Lett. **82**, 733 (2003).
[18] C. Li, D. Zhang, S. Han, X. Liu, T. Tang, and C. Zhou, Adv. Mater. (Weinheim, Ger.) **15**, 143 (2003).
[19] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, Nano Lett. **3**, 149 (2003).
[20] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, Appl. Phys. Lett. **83**, 2432 (2003).
[21] Y. Huang, X. Duan, Y. Cui, and C. M. Lieber, Nano Lett. **2**, 101 (2002).
[22] K. Rim, J. L. Hoyt, and J. F. Gibbons, IEEE Trans. Electron Devices **47**, 1406 (2000).
[23] S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, and P. L. McEuen, Nano Lett. **2**, 869 (2002).
[24] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, IEEE Trans. Electron Devices **48**, 560 (2001).