Analysis of Non-uniform Sampling Effects in Sigma-Delta Modulated Signals

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Abstract—**The effects of non-uniform sampling in the ΣΔ-modulated DAC are discussed in this paper. The non-uniform sampling of the ΣΔ-modulated signals causes in-band noise in the DAC, which will be compared with the harmonic distortions in switched capacitor circuit and the that due to the signal-dependent nonlinearity in the 1-bit DAC. We describe an *error-driven edge selection algorithm* that suppresses the in-band noise and its implementation. We also propose a model of the in-band noise caused by the non-uniform sampling, which predicts the noise reduction of the spectral shaping in the frequency domain quantitatively based upon the transition probability of the modulator output.**

I. INTRODUCTION

THE 1-bit ΣΔ-modulated DACs have been widely used in audio-band applications [1]. The 1-bit oversampling ΣΔ-modulated DAC has significant advantages over the conventional multi-level D/A converter with Nyquist sampling rate since it has only two quantization levels, which inherently eliminates the nonlinearity problem.

The ΣΔ DAC requires an oversampling clock whose nominal frequency is much higher than the required Nyquist sampling rate f_S, typically by the factor of 128 or 256. There are several methods of generating the oversampling clock. The method outlined in Fig. 1(a) generates a clock with the frequency of $2^n \times f_S$ with an analog PLL. This method provides a uniform sampling period, but it is somewhat technology-dependent.

Another method used to alleviate this limitation, as shown in Fig. 1(b), divides an external system clock whose frequency, f_{MCLK}, is much higher than the oversampling frequency of the ΣΔ DAC. However, generally the external system clock is not a multiple of the oversampling frequency of the DAC($2^n \times f_S$) but a multiple of f_S. As shown in Fig. 2, the fractional programmable clock generator(fPCG) can generate a clock of desired frequency by properly mixing two types of pulses of length $P \cdot T_{MCLK}$ and $(P+1) \cdot T_{MCLK}$ if the ratio, D, of the master clock frequency to the oversampling frequency, which is $D(= \frac{f_{MCLK}}{2^n \cdot f_S})$, is in the range of $[P, P+1)$, where $T_{MCLK} = 1/f_{MCLK}$. However, the period of the generated clock is not uniform.

In this paper, we discuss the effects due to **non-uniform sampling** of the ΣΔ-modulated signal. In Section II, we will compare the in-band noise caused by non-uniform sampling in the ΣΔ-modulated signal with (a) that in the SC filter and (b) the in-band noise due to the non-ideal waveforms of the 1-bit DAC. In Section III, we explain an edge-selection algorithm [2], which reduces the in-band noise by selecting edges, based on the time offset. The time offset is defined as the relative time of an edge to the timing of its ideal edge. We will also describe how to compute the time offset, which is required for the efficient implementation of the edge-selection algorithm. Then, we perform an spectral analysis in Section IV. The model adopted in Section IV can quantify the accuracy of the approximation. Finally, concluding remarks follow in Section V.

II. PROBLEM DESCRIPTION

The previous works on the non-uniform sampling are briefly reviewed before describing the non-uniform sampling effects in the

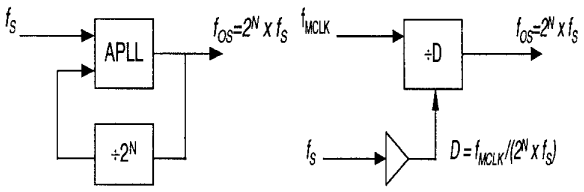

Fig. 1. Two methods that generate an oversampling clock for ΣΔ modulation (a) by using an analog PLL and (b) by dividing an external system clock.

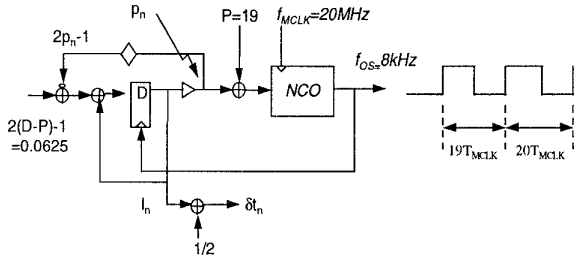

Fig. 2. Block diagram of a fractional programmable clock generator.

ΣΔ-modulated signal. Furthermore, the noise due to signal dependent nonlinearity in 1-bit DAC is also compared with that due to the non-uniform sampling in the ΣΔ modulation.

A. Previous works : Narrow-band signals

An analysis on the effects of non-uniform sampling of the signal in the SC filters was published by P.J.Hurst in [3]. By modeling the non-uniform sampling effect with a phase-modulated sample-hold device, he showed that *unwanted tones* are generated for the sinusoidal inputs. This harmonic distortion resuts from the periodicity in the sampling period sequence of the clock generated by the fractional PCG. The fPCG in Fig. 2 can be interpreted as a first order ΣΔ modulator with a DC input [4]. The fraction part of the desired frequency ratio of an external master clock with frequency f_{MCLK} and the oversampling clock with frequency, f_{OS}, is used as the DC input. It is known that the first and second order ΣΔ modulator with two-level quantization generates the tones , which motivated the use of higher order ΣΔ modulation or dithering techniques to suppress the tones in the PCG [4], [5], [6]. In this paper, however, we do not use the output clock of the fPCG by itself, which lets us use only the first-order conventional PCG. The fPCG is only used to generate an oversampling clock and compute the time offset,δt_n.

If a conventional multi-level oversampling D/A converter is used to convert a digital signal, tones at the normalized frequency of $f_k = \pi k/M$ are produced, where M is the period of the sampling period sequence in the non-uniform oversampling clock [3], [7]. However, the tone generation is true only if the signal is narrow-banded. It is not true for the ΣΔ modulated signal since the noise power of the signal is spread all over the frequency with noise shaping.

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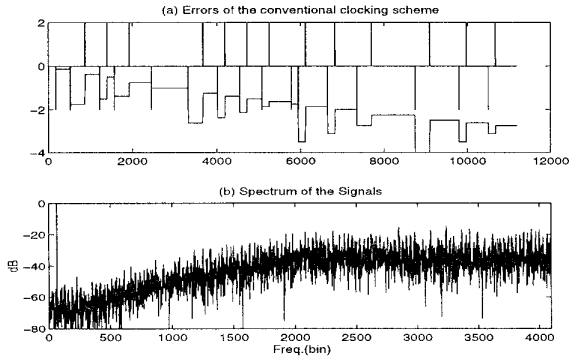

Fig. 3. Trace and spectrum of the errors caused by the non-uniform sampling of the $\Sigma\Delta$-modulated signals with conventional programmable clock generator.

B. Non-uniform sampling in the $\Sigma\Delta$-modulated signal

Think about an example which generates a $\Sigma\Delta$-modulated signal for a sinusoid input with frequency of 2kHz and amplitude of -6dBr. As an oversampling clock, the output of the PCG in Fig. 2 is used, which is a 2nd order $\Sigma\Delta$-DAC easily found in [1]. Assume that the PCG operated at $f_{MCLK} = 20MHz$ and $f_S = 8kHz$. The frequency of the oversampling clock of frequency $128 \times f_S$. This clock can be generated by mixing two pulse streams of width 19 and 20 with the ratio of 15/32 and 17/32, respectively.

The simulation result in Fig. 3(b) shows a noise floor flattened near the base band that greatly reduces the SNDR of the $\Sigma\Delta$-modulated DAC. This spectrum was obtained by applying the FFT to 2^{14} bit-streams of the DAC with a hanning window.

The reason for non-uniform sampling effects is explained with two plots in Fig. 3(a). Fig. 3(a) shows the error caused by the non-uniform sampling clock to the continuous time filter which raises noise floor in the base-band spectrum. These errors will take the values of only $\{+2, 0, -2\}$ because $x_k \in \{+1, -1\}$ for all k. The intervals of the pulse will be that of the time difference between the desired clock and the generated clock, which results in

$$e(t) = \sum_{n=0}^{+\infty} (x_n - x_{n-1})(u(t - nT_{OS} - \Delta t_n) - u(t - nT_{OS})), \quad (1)$$

where $u(\cdot)$ is a unit step function. The sign of this error seems to alternate from -1 to +1 or from +1 to -1 and it is exptected to make its DC error zero. However, the cumulative sum of the errors in Fig, 3(b) shows that the error may not be near zero during a relatively short interval at least. Therefore we can conclude that the error results in the form of the raised in-band noise rather than in the form of tones.

The degradation of the 1-bit DAC and ADC similar to the spectrum in Fig. 3(b) has been found in the early researches on the $\Sigma\Delta$-modulation [1]. Although the 1-bit DAC using the oversampling techniques is superior to the multi-bit DAC in linearity, there still exists the in-band noise due to signal-dependent nonlinearity, which is caused by

- Asymmetry in the beginning and the ending of a transition.
- Unequal pulse width between high pulse and low pulse.
- Asymmetry between a rising transition and falling transition.

as reviewed in [8].

Non-ideality of the waveforms of the quantizer in the $\Sigma\Delta$-modulated ADC and DAC was great concerns. In the works in [9], [10], the effects of the waveform in the $\Sigma\Delta$ ADC were discussed at first while the problem of nonlinearity in the 1-bit high speed DAC was discussed in [8]. The effect of the non-ideal waveform of the quantizer has been minimized with switched capacitor(SC) or switched current(SI) circuit techniques in the ADC and with the differential signal representation and RZ-switching method in single-ended signal representation in the DAC.

Nonetheless, this non-uniform sampling problem in the $\Sigma\Delta$ DAC cannot be directly suppressed with the differential signal representation scheme or the RZ-switching method. It is mainly because the nonlinearity caused by the transition of the output is deterministic in the early problem while that of the non-uniform sampling problem is random.

III. Error-driven Edge Selection for the $\Sigma\Delta$ DAC

As reviewed in the previous section, the performance degradations caused by the non-uniform sampling of the $\Sigma\Delta$-modulated signal cannot be easily suppressed. In this section, we describe an alternative algorithm to suppress the raised noise floor near the base band proposed in [2] and a simple method to compute the time offset for an efficient implementation of the algorithm.

A. Edge-selection Algorithm

First, note that while there is no transition in the signal x_n, the edges of the oversampling clock are insignificant. [1] Therefore, the trace of the errors should be considered only when there is a transition in the signal x_n. Fig. 4 illustrates allowable transitions in the signal x_n, and their corresponding errors for a rising or a falling transition in the signal x_n.

For a rising transition as shown in Fig. 4(a), when the edges of the generated clock do not coincide with that of the desired clock, we can generate an edge earlier or later than the desired edge. If we select a transition earlier than the desired transition, the error contributed to the continuous time filter is positive and its height is +2 because the output of the DAC is either +1 or −1. If we select a transition later than the desired transition, the error is −2. Therefore, the actual amount of the errors integrated over an interval will be proportional to the absolute value of the difference between the non-uniformly sampled data and the uniformly sampled data. A similar result can be drawn for a falling transition.

We will denote the edge generated earlier than the desired oversampling clock with $p_n = 0$ and the retarded one with $p_n = 1$. With this notation, the cumulative error,$\epsilon_1[n]$ during the edge can be updated like the followings :

$$\epsilon_1[n] = \epsilon_1[n-1] + \epsilon_0[n] \quad (2a)$$

$$\epsilon_0[n] = (x_n - x_{n-1}) \cdot (\delta t_n - p_n \cdot T_{MCLK}), \quad (2b)$$

where δt_n is the time offset between the uniform desired edge and the earlier one among the allowed edges.

Based on the properties of the error signal caused by the non-uniform sampling clock, an edge-selection algorithm is proposed in [2], which has the characteristics of the first order noise shaping. Note that we have a **choice to select the sign of the error** for each transition in the $\Sigma\Delta$-modulated signal x_n. For the noise near the base-band to be suppressed, the edge of the signal x_n is properly chosen to reduce $|\epsilon_1[n]|$. Fig. 5 shows the flowchart of this logic to be performed by the selection rule in (3).

$$p_n = \frac{\mathrm{sgn}\{\epsilon_1[n-1] \cdot (x_n - x_{n-1})\} + 1}{2} \quad (3)$$

[1] This statement is only applicable to the NRZ-switching that does not go to the predefined level of the output, which applies to the most of the DAC published.

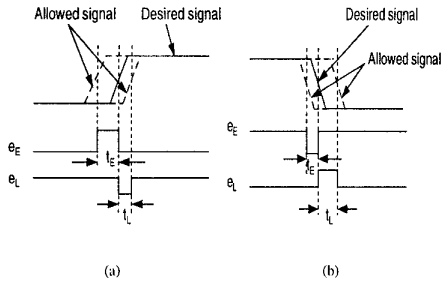

Fig. 4. Allowable transitions in the signal and their corresponding errors for a rising and a falling transition in the signal.

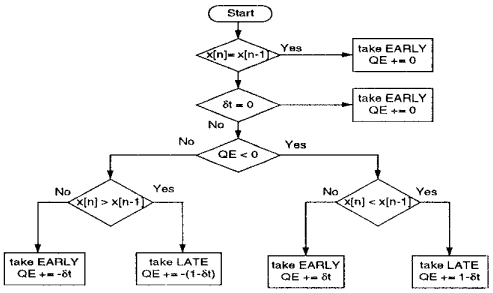

Fig. 5. Flow chart of the edge-selection algorithm which takes either (a) an earlier edge or (b) a later edge.

Fig. 6 shows the simulation results for the $\Sigma\Delta$-modulated signal after realigning the edges with the proposed method in the same condition as that of the Fig. 3. Although the total power of the noise increased with this relaxation in the peak-to-peak jitter, the power spectrum of the noise floor near the base-band decreased significantly by shaping it in the first order as shown in Fig. 6(b). The trace of the cumulative error in the re-aligned $\Sigma\Delta$-modulated signal is shown in Fig. 6(a), which shows a significant improvement in steering the cumulative error to zero. The SNDR of the $\Sigma\Delta$-modulated signal with non-uniform oversampling clock generated with a conventional fPCG and that of its realigned signal with the proposed edge-selection algorithm is summarized in Table I accompanied by that of the uniform sampling. The SNDR of the proposed one is 10dB below that of uniform sampling ,which can be improved by 2nd order noise shaping of the time difference.

Note that the edge-selection is determined with only the signs of

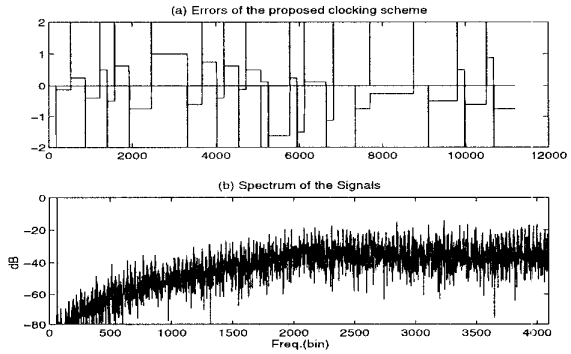

Fig. 6. Trace and spectrum of a $\Sigma\Delta$-modulated signal re-aligned with the proposed edge-selection algorithm.

TABLE I

SNDR OF THE $\Sigma\Delta$-MODULATED SIGNALS : IT IS OBTAINED WITH THE ASSUMPTION OF IDEAL LOW-PASS FILTERING ABOVE 8KHZ.

conventional	proposed	uniform sampling
46.6	66.7	76.7

the cumulative error and the transition of the signal. The size of the circuit to perform this algorithm seems to be reasonably small [2]. However, an efficient computation of the time offset, δt_n is required to make the above algorithm more feasible.

B. Computation of the time offset

The time offset between the desired edge and an edge of the generated clock can be obtained from the clock generator of Fig. 2. Since the output of the quantizer determines the sampling period of the clock produced at that time,p_n, and its input to the $\Sigma\Delta$-modulator is the period of the desired clock,$2(D-P)-1$, the summation of the difference between these two values is the difference between the edge of the desired clock and the generated clock at n-th oversampling clock.

$$\frac{\delta t_n}{T_{MCLK}} = \sum_{k=0}^{n}(D - P - p_k) + p_n \tag{4}$$

Since the fPCG behaves like the first order $\Sigma\Delta$-modulator,

$$2p_k - 1 = 2(D-P) - 1 - (r[k] - r[k-1]) \quad \text{for all } k, \tag{5}$$

$r[k]$ is the quantization error of $(2p_k - 1) - l[k]$. Eq.(5) makes (4) into

$$\begin{aligned}\frac{\delta t_n}{T_{MCLK}} &= -1/2 \cdot \sum_{k=0}^{n}(r[k] - r[k-1]) + p_n \\ &= -r[n]/2 + p_n = \frac{l[n]+1}{2}.\end{aligned} \tag{6}$$

Here, $l[n]$ is the register value of the fPCG and the computation of δt_n is easily obtained by adding the bias of $+1/2$. Consequently the computation of δt_n requires only the addition of $1/2$, which requires a 2-bit full adder for the MSB conversion at most.

IV. Error Analysis

A. Dependency upon the transition probability

The the in-band noise suppressing capability of the edge selection algorithm in [2] depends upon the transition probability of the modulator output. If the $\Sigma\Delta$-modulated output has less transitions, the frequency of correcting the error decreases while the absolute amount of the error also decreases. With the dependency of the error correction upon the transition probability, we can conjecture that the knee frequency of the noise shaping spectrum will decrease because the error is corrected slowly relative to the signal as shown in Fig. 7 by the factor of transition probability, P_t. The simulation results show that the transition probability of the second order $\Sigma\Delta$-modulator is through $1/4$ and $1/3$ or so. This conjecture on the shrinkage of spectrum is confirmed by the simulation results carried out with the following error models.

B. Error models with the time resolution of T_{OS}

To visualize the error in the continuous time domain, we should increase the resolution of the time axis by M. This scale factor

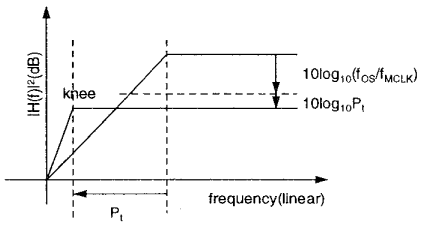

Fig. 7. Dependency of the error spectrum on the transition probability of the modulator output.

is equal to the period of the sampling period sequence M which is variable depending upon the cases. This increase in resolution of the time axis requires a heavy computational complexity in obtaining the spectrum. Therefore, we need a systematic method to approximate the error pulse train with that of the delta function. Each pulse has the area of the error located at that time and is approximated with the corresponding delta function.

The accuracy of this approximation can be written like the followings. We assumed that $\exp(-j2\pi ft)$ is constant during the interval of the integration, which results in the spectrum of the error pulse train as

$$E(f) = \lim_{L\to\infty} \frac{1}{2L\cdot T_{OS}} \int_{-L\cdot T_{OS}}^{+L\cdot T_{OS}} e(t)\cdot e^{-j2\pi ft}dt$$
$$\approx \lim_{L\to\infty} \frac{1}{2L\cdot T_{OS}} \sum_{-L}^{+L} \epsilon_0[n]\cdot \delta t_n \cdot e^{-j2\pi nfT_{OS}} \quad (7)$$

Here, we will take the relative approximation error for each error pulse train. The approximation error caused with this approximation can also be approximated with

$$|\Delta E_n(f)| \approx |\frac{e(nT_{OS})}{T_{OS}}|\cdot|e^{-j2\pi fT_{OS}\cdot n}|\cdot\left|\int_0^{\Delta t[n]} j2\pi f t dt\right|$$
$$= \frac{1}{T_{OS}}\cdot \pi f(\Delta t[n])^2 \quad (8)$$

Also $(\Delta t[n])^2$ is bounded by the period of the external master clock T^2_{MCLK}. The maximum relative error,$|\Delta E_n(f)|/|E_n(f)|$, is also obtained when $\Delta t[n] = T_{MCLK}$ since the time difference error, $E_n(f)$ is $\frac{1}{T_{OS}}\cdot\epsilon_0[n]\cdot e^{-j2\pi fT_{OS}\cdot n}$. Therefore, the maximum relative error can be approximated to

$$\max \frac{|\Delta E_n(f)|}{|E_n(f)|} \approx \frac{\pi f T^2_{MCLK}/T_{OS}}{T_{MCLK}/T_{OS}} = \pi\frac{f}{f_{MCLK}} \quad (9)$$

This approximation is valid in the first order since the duration of the error pulse is relatively short compared with the pulse length of the $\Sigma\Delta$-modulated output. This does not require an increase in the resolution of the time axis to analyze the error terms caused by the non-uniform sampling. Note that the relative error caused by the approximation is proportional to the frequency, which is a good characteristics for increasing the accuracy of the spectrum in the band of interest. In the example used in the simulation, an accuracy of

$$|\Delta E(f)|/|E(f)| \approx \pi \times \frac{40\times 10^3}{20\times 10^6} = 0.6\% \quad (10)$$

is obtained below $f = 40kHz$.

With the proposed power spectrum analysis of the error signals, the spectrum of the pure error terms has been obtained in Fig. 8. This spectrum clearly shows the way of the edge selection algorithm proposed in [2] to suppress the in-band noise efficiently. The comparison of (a) and (c) in Fig. 8 shows the shrinkage of the knee frequency.

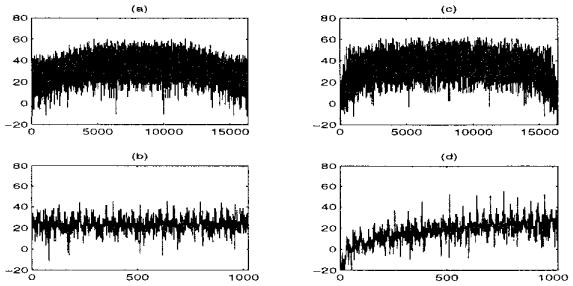

Fig. 8. Comparison of the spectrum of errors. (a)(b) the conventional one (c)(d) the proposed one.

V. Conclusion

In this paper, we have analyzed the effects of non-uniform sampling in the $\Sigma\Delta$-modulated DAC, which raise the in-band noise floor unlike that in the SC-filters. We have also found that this effect cannot be reduced with the conventional methods to eliminate the effects of the non-ideal waveform of the 1-bit DAC.

An error-driven edge selection algorithm that can resolve this non-uniform sampling problem has been described in this paper. We investigated the error model that can explain quite well the error spectrum shaped by the error-driven edge selection algorithm. Especially, it can predict the shrinkage of the knee frequency that depends on the output transition probability. Further studies about the higher order extension of the edge selection algorithm are required to improve its performance.

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