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Cu Electroless Deposition onto Ta Substrates

Application to Create a Seed Layer for Cu Electrodeposition

Chang Hwa Lee,[a,*] Soonsik Hwang,[a] Sang-Chul Kim,[b] and Jae Jeong Kim[a,,z]**

[a]*Research Center for Energy Conversion and Storage, School of Chemical and Biological Engineering, College of Engineering, Seoul National University, San 56-1, Shillim-dong, Kwanak-gu, Seoul 151-742, Korea*
[b]*Dongbu Electronics, Department of Advanced Nano-tech Development, 474-1 Sangwoo-ri, Kamgok-myun, Umsung-kun, Chungbuk 369-852, Korea*

Copper electroless deposition (ELD) was investigated for applications that create a seed layer for Cu electrodeposition. On Pd catalysts formed on the Ta substrates through Sn sensitization–Pd activation, continuous Cu seed layer of 40 nm was electrolessly deposited in a diluted electrolyte. Dilution of the electrolyte enabled the film to make a thin and conformal layer without oxygen incorporation, by which the ELD Cu seed had properties comparable to the physical vapor deposited seed layer regarding surface roughness and resistivity, even after subsequent Cu electrodeposition, and had superior step coverage. Defect-free bottom-up filling by electrodeposition was achieved on these ELD seed layers.
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Copper(Cu) has been used as an interconnect material for ultralarge scale integrated circuits (ULSIs) in place of aluminum-alloys due to its high electrical conductivity and electromigration resistance.[1,2] Among the many deposition methods, electrodeposition (ED) is the most favorable for Cu metallization in terms of the process cost, throughput, and the capability of superfilling.[3,4] In particular, superfilling by the combination of additives in Cu electrodeposition enables the filling of high-aspect-ratio sub-micrometer damascene structures without defects.[5,6] For successful Cu filling by electrodeposition, a Cu seed layer, which is a conductive path for the flow of current on high-resistive barriers such as TiN, Ta, and TaN, is required. Although physical vapor deposition (PVD) has been conventionally used as a Cu seed layer formation method, its discontinuity or nonuniformity produces voids or seams inside the deposits after Cu filling.[7] This is expected to be more serious as the dimension of the feature decreases and aspect ratios increase.

To solve these problems, studies regarding Cu seed layers deposited through chemical vapor deposition (CVD),[8] atomic layer deposition (ALD),[9] and electroless deposition (ELD)[10] have been conducted because of their excellent step coverage. Especially Cu electroless deposition is a promising method for seed repairing or seed layer formation because it has superior conformality and uniformity of the film due to a surface reaction limited deposition,[11,12] as well as it is simple and low-temperature process.

To form a thin and continuous Cu seed layer on the barriers by electroless deposition, the optimization of Pd activation and electroless electrolyte is one of the key processes. First, Pd activation with highly dense and nanosized Pd particles is an indispensable factor because Pd particles affect Cu film by playing a role of nucleation sites for Cu film deposited on them. Although many researchers have studied Pd catalyzing processes of various substrates, it is difficult to activate the Ta-based barrier layer which is verified as having excellent diffusion barrier properties, with small-sized and uniformly distributed Pd catalysts by a displacement reaction because of an agglomeration of Pd particles[13] and damage of the substrate. Thus, vacuum technologies such as ionized cluster beam (ICB)[14] and atomic layer deposition (ALD)[15] can be alternatives to activate the Ta-based substrates. However, for the consistency and simplification of the process, a wet process such as Sn sensitization-Pd activation[13] is recommended because it is possible to activate few nanometers' Pd catalysts uniformly without agglomeration of the particles. Second, two-dimensional growth of the film having stable deposition behavior can be controlled by the optimization of the electrolyte as well as deposition conditions. In the case of an HCHO-based Cu electroless electrolyte which has been traditionally used, some stabilizers and/or surfactants are needed to prevent hydrogen evolution and Cu_2O formation that are intrinsically generated from the reaction. However, they cause an increase in the film resistivity as contaminations.

In this paper, we present electroless Cu seed layers deposited on Ta substrates by the optimized wet activation process and electroless deposition electrolyte. Furthermore, to confirm the applicable possibility of the seed layer for Cu electrodeposition, ELD seeds deposited as the above are compared with PVD seeds in terms of the film properties on both the planar and patterned substrates.

Experimental

The substrates used in the experiments were (100)-oriented p-type Si trench-type patterned wafers with various feature sizes and aspect ratios, and planar wafers covered with Ta (7.5 nm)/TaN (7.5 nm) as a diffusion barrier layer.

Prior to performing Cu electroless deposition onto the Ta substrates, the native oxide Ta_2O_5 was removed in an aqueous solution of HF (50%):HNO_3 (70%):H_2O = 1:1:50 (v/v) for 10 min. Sn sensitization and Pd activation were carried out sequentially in solutions consisting of $SnCl_2$/HCl and $PdCl_2$/HCl, respectively. Immersion times were 2 min and 20 s, respectively.

The electrolyte for fabricating the electrolessly deposited seed layer (ELD seed) was a sevenfold diluted solution of the standard solution which was composed of 0.025 M copper sulfate ($CuSO_4 \cdot 5H_2O$), 0.054 M ethylenediaminetetraacetic acid (EDTA), 2.9 g/L paraformaldehyde $(HCHO)_n$, and 0.49 M KOH. No surfactants or stabilizers were added. The deposition temperature was maintained at 70°C and the thickness of the ELD seed layer was controlled by the deposition time. A PVD seed of 50 nm deposited by dc magnetron sputtering on Ta/TaN/SiO_2/Si substrates was used to compare the properties of the ELD seed layer and the film after Cu electrodeposition.

The base electrolyte used for the subsequent electrodeposition on the PVD and ELD seed was composed of 0.25 M $CuSO_4$, 1 M H_2SO_4 and DI water. Additives used for Cu bottom-up filling were 50 μM bis(3-sulfopropyl)disulfide (SPS), 88 μM polyethylene glycol (PEG, Mw 3400), and 1 mM NaCl. A constant potential of −250 mV was applied by a PAR 263 potentiostat (EG&G Princeton Applied Research Corporation) with respect to a saturated calomel electrode (SCE) at room temperature. An electronic grade Cu bar was used as an anode. After Cu electrodeposition, a heat treatment was performed at 400°C for 30 min under a N_2 atmosphere.

Field-emission scanning electron microscopy (FE-SEM, JEOL 6330F), four-point probe measurements (Chang Min CMT-SR

* Electrochemical Society Student Member.
** Electrochemical Society Active Member.
z E-mail: jjkimm@snu.ac.kr

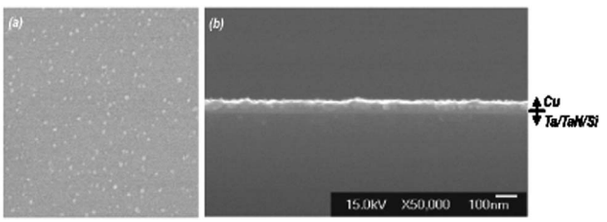

Figure 1. FE-SEMs of (a) Pd particles activated on a Ta substrate after Sn sensitization and (b) electrolessly deposited Cu film on Pd particles activated on a Ta substrate after Sn sensitization. Both images have the same scale.

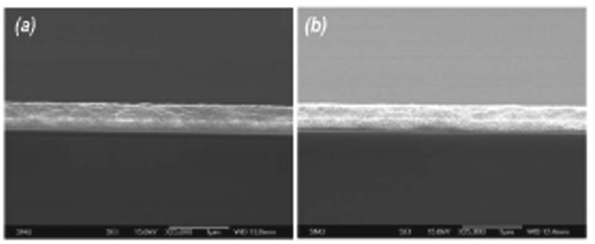

Figure 2. Cross-sectional images of Cu films electrodeposited for 120 s on (a) PVD and (b) ELD seeds.

1000N), atomic force microscopy (AFM, Digital Instruments Dimension 3100), and Auger electron spectroscopy (AES, Perkin-Elmer model 660) were employed to characterize the film properties. Adhesion strength of the film was determined by means of a Scotch tape test.

Results and Discussion

Figure 1a shows Pd particles that were created on a Ta blanket wafer through Sn sensitization and Pd activation. The sizes of the Pd catalysts formed by the wet process were ~5 to 10 nm and the density of the particle was $4.5 \times 10^{10}/\text{cm}^2$, which were smaller size and higher number of particles than those formed on TiN substrates using a one-step Pd activation.[15,16] The two-step Sn sensitization and Pd activation, which reduces Pd ions to metallic Pd by electrons generated from the oxidation of adsorbed Sn^{2+}, does not damage to the substrate as one-step Pd activation which coerce the substrate into oxidizing by F^-. In addition, Sn ions that adsorbed on the substrates lowered the surface energy and provided uniformly distributed sites for Pd ion reduction.[13] Adsorbed Sn ions prevented Pd particles from agglomerating with each other and stabilized the size of the Pd catalyst. The proper size and distribution of the Pd particles is essential to attain a thin and continuous film, because an excessive size or density of the Pd particles leads to high surface roughness and film resistivity.[16]

A cross-sectional image of the Cu film deposited by electroless deposition on the Pd-activated Ta is presented in Fig. 1b. A continuous Cu film of ~40 nm with a smooth surface was acquired. The dilution of the electroless electrolyte promoted two-dimensional growth and inhibited hydrogen gas evolution by decreasing the deposition rate, which resulted in improvements of the adhesion properties, even in the absence of additives such as surfactants or stabilizers which can contribute an increase in the resistivity.

After electrodeposition was carried out on the films with either an electroless deposited seed (ELD seed) or a PVD seed, cross-sectional images of the films were taken and are shown in Fig. 2a and b, respectively. Although there was no distinct difference between the film morphologies, the adhesion properties of the Cu electroplated on the ELD seed against the Ta substrate seemed to be poor compared to that on the PVD seed. In the result of the adhesion test by a Scotch tape, even though the seed layer was very adhesive to the barrier layer, the subsequent electrodeposition deteriorated the adhesion property between the Cu and Ta layer. It is believed that the ELD seed, which has a relatively random texture orientation due to the growth on the Pd catalysts compared to the PVD seed, underwent a higher stress change during thickening because of the applied potential.

Table I summarizes the electrical and physical properties of the different films. Although the ELD seed was thinner than PVD seeds, the film resistivity was 3.46 $\mu\Omega$ cm, which was only about 24% higher than that of the PVD seed. This decreased to less than 10% in 440 nm thick films deposited by Cu electrodeposition on them. Furthermore, through an annealing treatment at 400°C for 30 min, the resistivity was reduced from 2.59 to 2.15 $\mu\Omega$ cm for the Cu electroplated on the ELD seed and the adhesion was improved to be comparable to that of the PVD seed. Annealing at high temperature caused a reduction of the dislocations and grain boundaries by the formation of larger strain free grains, which probably resulted in the observed decrease of the film's resistivity and the increase in the adhesion strength.[17] The surface roughness of the film thickness in the ELD seeds was comparable to the value of the PVD seeds after Cu electroplating.

Generally when HCHO is used as a reducing agent for Cu electroless deposition, undesired Cu_2O, codeposited from the baths containing $Cu(OH)_2$ precipitates, causes a degradation of the electrical properties. Two approaches were taken to reduce the formation of Cu_2O: increasing the deposition temperature and diluting the electrolyte. While the solubility of oxygen or Cu_2O increases at high deposition temperatures,[18] the evolution of hydrogen gas is accelerated by any increases in the deposition temperature due to a fast reaction rate. However, diluting the electrolyte along with elevating the deposition temperature enabled the Cu film to achieve superior adhesion properties and conductivity. Simultaneously diluting the electrolyte lowered the possibility of the formation of a $Cu(OH)_2$ precipitate by positioning the Cu bath in a more homogenous region by reducing the concentration of Cu ions, even though the molar ratio of [EDTA]/[Cu] and [OH]/[Cu] remained the same.[19]

As a result, oxygen was not detected inside the ELD Cu seed layer (Fig. 3a). Additionally, there was no significant difference in the amount of contaminants such as carbon or oxygen between the PVD and ELD seeds even after Cu electrodeposition (Fig. 3b and d).

The ELD seed, which was comparable to the PVD seed regarding the electrical and physical properties of the film, was applied to

Table I. Physical and electrical properties of the films before and after annealing.

Film structures		Thickness (nm)	R_s (m$\Omega/\square$)	Resistivity ($\mu\Omega$ cm)	RMS roughness (nm)	Adhesion tape test
As-deposited	PVD seed	56.08 ± 1.07	499.66 ± 7.80	2.80	1.276	Pass
	ELD seed	39.87 ± 2.38	867.80 ± 5.70	3.46	2.781	Pass
	PVD seed+ED	440.60 ± 4.90	54.16 ± 1.60	2.39	4.864	Pass
	ELD seed+ED	439.22 ± 7.30	59.04 ± 0.92	2.59	5.066	Fail
After annealing	PVD seed+ED	440.60 ± 4.90	42.51 ± 0.78	1.87	—	Pass
	ELD seed+ED	439.22 ± 7.30	48.87 ± 0.40	2.15	—	Pass

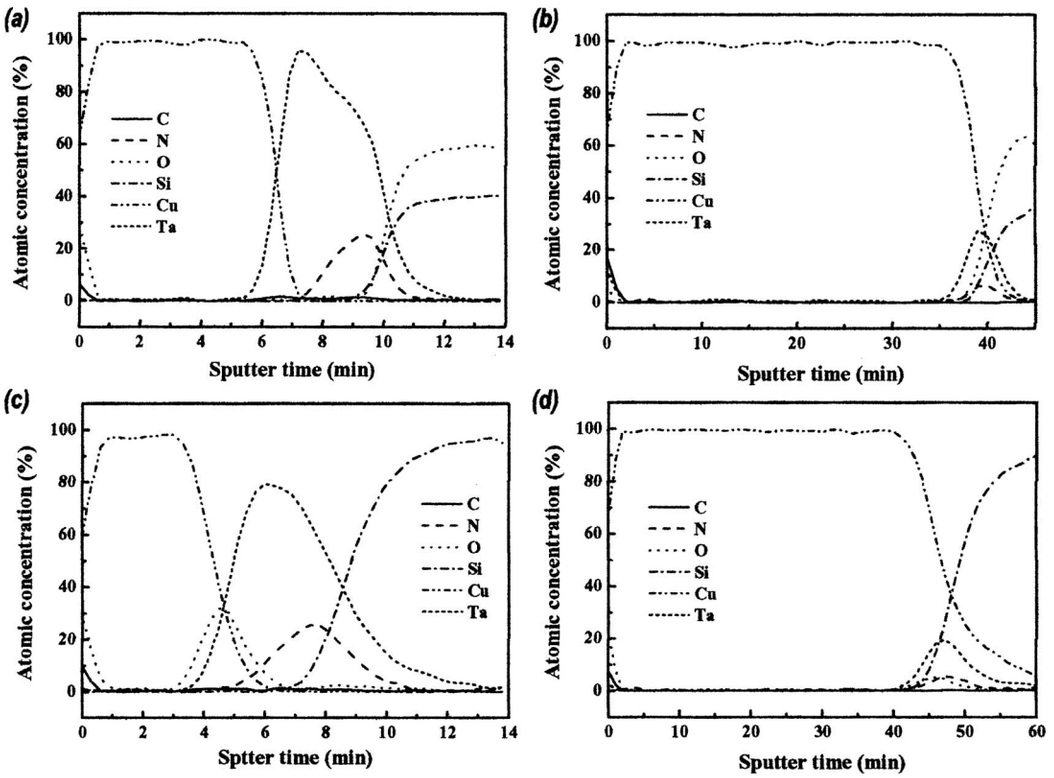

Figure 3. AES depth profiles of (a) Cu ELD seed, (b) electrodeposited Cu on a Cu ELD seed, (c) PVD seed, and (d) electrodeposited Cu on a Cu PVD seed.

the patterned wafer to be compared with the PVD seed, as indicated in Fig. 4. The sidewall step coverage (defined as sidewall thickness/top thickness $\times 100$) and bottom step coverage (defined as bottom thickness/top thickness $\times 100$) were calculated for both the PVD and ELD seeds on the trenches with a width of 0.13 and 0.18 μm and aspect ratios of 2.5 and 2.2. The PVD seeds had 67.6% (0.13 μm) and 72.8% (0.18 μm) sidewall step coverage, and 74.9% (0.13 μm) and 80.2% (0.18 μm) bottom step coverage, respectively. Poor step coverage in the PVD seeds can cause the formation of voids due to the patchy and discontinuous seed layers on the features with high aspect ratios. On the other hand, the ELD seeds exhibited a uniform film thickness of about 38 nm on the trench with 99.7% (0.13 μm) and 97.0% (0.18 μm) sidewall step coverage, and 100% (0.13 and 0.18 μm) bottom step coverage. In addition, we confirmed that a continuous ELD Cu seed of about 20 nm could be deposited in the diluted electroless bath as shown in Fig. 5, which is expected to be applied to the seed layer formation method for below 65 nm of the feature size.

To examine the feasibility of the ELD seeds for electrodeposition, Cu electrodeposition was carried out on the trench patterns covered with ELD seeds, as shown in Fig. 6a-d. The Cu electrodeposition that was performed as a function of time proves that

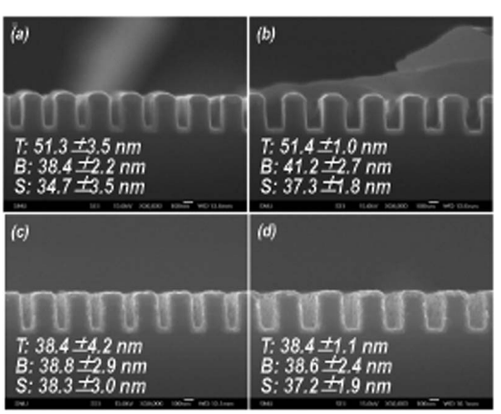

Figure 4. FE-SEMs of damascene structures covered with (a and b) PVD Cu seeds and (c and d) ELD Cu seeds at trench widths of 0.13 (a and c), and 0.18 μm (b and d). (T, B and S means top, bottom, and sidewall thicknesses, respectively).

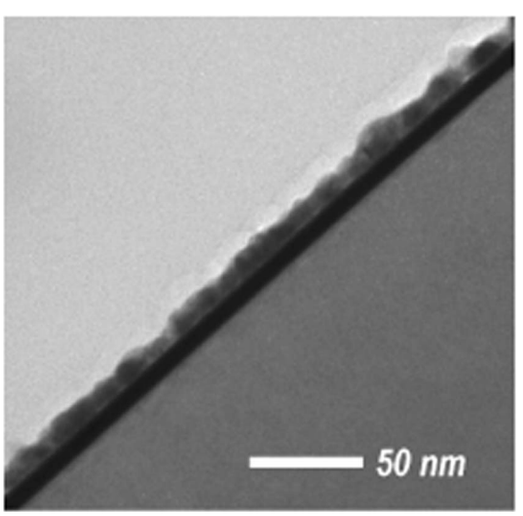

Figure 5. TEM of an electroless Cu seed layer deposited down to 20 nm with the diluted electrolyte.

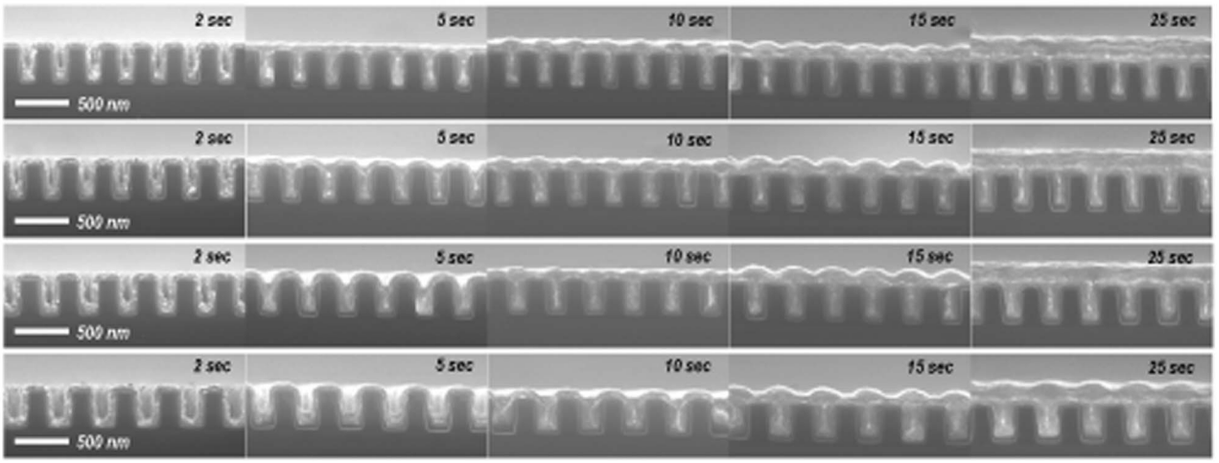

Figure 6. FE-SEMs of the electrodeposited Cu with an elapsed time on various sizes of trench patterns covered with ELD Cu seeds. (a) 0.13, (b) 0.16, (c) 0.18, and (d) 0.21 μm.

bottom-up filling can be successfully achieved even on the ELD seeds by additives combining with SPS, PEG, and Cl^-. The observation of bumps, which are evidence of superfilling without voids or seams, in all different sizes of damascene trench patterns, represents an ample possibility of using the electroless deposition method for seed layer formation in future interconnect processes.

Conclusions

We investigated Cu electroless deposition for application to the seed layer of electrodeposition. The deposition of a seed layer which has superior conformality and thin thickness as well as good film properties was carried out through the two approaches. First, highly dense nanoscale Pd catalysts were formed by a two-step Sn sensitization and Pd activation, which resulted in making completely continuous Cu films below 40 nm. Second, the dilution of the electrolyte and the elevation of the deposition temperature enhanced the film properties with regard to the surface roughness, film resistivity, and adhesion due to stable two-dimensional growth by lowered deposition rate, despite the absence of additives.

Cu ELD seeds showed almost comparable properties to PVD seeds even after subsequent Cu electrodeposition. However, the sidewall and bottom step coverage of the ELD film deposited on the damascene structures were better than PVD seeds, irrespective of the trench width. Even though the adhesion between the Cu film and the barrier layer was worsened by Cu electrodeposition, it was improved overall by an annealing process at 400°C and the resistivity also decreased down to 2.15 μΩ cm. Especially on the damascene structure, the bottom-up filling by Cu electrodeposition was successfully achieved without voids and seams on ELD seed layers formed in various sizes of the trenches. The result of a seed layer deposited down to about 20 nm clearly shows that the ELD seeds can be potentially applied for 65 nm interconnect technologies.

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