A 2 GHz CMOS Double Conversion Downconverter with Robust Image Rejection Performance against the Process and Temperature Variations

Eunseok Song, Soo-Ik Chae and Wonchan Kim
System Design Group, SoEE, Seoul National University
56-1 Shillim-dong, Kwanak-gu, Seoul 151-742, Korea

Abstract
This paper presents a 2 GHz image rejection (IR) down-converter implemented in a 0.65 μm CMOS technology. It maintains high IR ratio against the process and temperature variations if the on-chip passive RC components are relatively matched. The experimental circuit provides an IR ratio of 40.8 dB without any off-chip filtering or tuning, and dissipates 91 mW at 3.3 V.

Introduction
The proliferation of portable communication systems has brought about a great demand for low-cost, low-power, small form-factor transceiver. A method that can satisfy these requirements is to develop a monolithic transceiver using a standard CMOS technology. Although the superheterodyne receiver is popular nowadays, it requires many discrete components to suppress the image. Therefore it is difficult to achieve high integration level with conventional superheterodyne systems.

Recently, double conversion receiver, shown in Fig. 1, is often used to reject the image sufficiently without off-chip element [1]-[3]. It suppresses the image through quadrature modulation. Therefore the IR filter and IF filter that are required in a superheterodyne receiver can be eliminated. Consequently, the receiver can be fully integrated from the LNA to the ADC. However, the IR ratio of the double conversion downconverter is very sensitive to I-Q mismatches. The I-Q mismatches are usually caused by on-chip RC variations used in phase shifters. In this paper we propose a double conversion downconverter whose IR ratio is less sensitive to RC variations.

Image Rejection Downconverter
A. Image Rejection in the Conventional Double Conversion Downconverter
Image rejection in the double conversion downconverter is very sensitive to I-Q mismatches. If the quadrature LO signals are generated from off-chip phase shifters with high accuracy, double conversion downconverter can suppress the image about 40 dB. However, to integrate a receiver fully including a frequency synthesizer, the quadrature LO signals must also be generated from on-chip phase shifters.

Fig. 1. Double conversion receiver. It suppresses the image through quadrature modulation.

Fig. 2 shows an example of how to make quadrature LO1 and LO2 signals generation. I-Q mismatches may occur when RC product deviates from designed value.

Fig. 2 shows an example of how to make quadrature LO1 and LO2 signals using RC-CR phase shifters. The ratio of A1 to A0 and that of B1 to B0 in Fig. 2 vary with the R, C and ω. Because it is difficult to achieve the exact value of on-chip passive components, I-Q amplitude mismatches can arise. However, the ratio of R1 to R2 and that of C1 to C2 rarely deviate from the designed value if two phase shifters are placed closely to each other inside a chip. Therefore, if we assume that the relative accuracy error of the passive components is zero, then the following relationship can be obtained.

\[
\frac{A_0}{A_1} = \frac{B_0}{B_1}
\]
Fig. 3. Conventional double conversion downconverter. Though the on-chip passive elements are relatively matched, IR ratio of BBquadrature-phase is still sensitive to the absolute inaccuracy of passive elements.

Fig. 4. Proposed downconverter. It maintains good IR ratios for both BBin-phase and BBquadrature-phase if the on-chip passive elements are relatively matched.

Considering Eq. (1), a conventional double conversion downconverter is drawn in Fig. 3 with variations of signal amplitude. From Eq. (1), we can describe the BBin-phase signal as follows:

\[
BB_{\text{in-phase}}(t) = v_{RF}(t) \left( A_0 B_1 \sin(\omega_{LO1} t) \cos(\omega_{LO2} t) + A_1 B_0 \cos(\omega_{LO1} t) \sin(\omega_{LO2} t) \right)
\]

\[
= v_{RF}(t) A_0 B_1 \sin(\omega_{LO1} t) \cos(\omega_{LO2} t) + v_{RF}(t) A_1 B_0 \cos(\omega_{LO1} t) \sin(\omega_{LO2} t)
\]

\[
= v_{RF}(t) A_0 B_1 \sin(\omega_{LO1} t + \omega_{LO2}) + A_0 B_1 \cos(\omega_{in} t) \sin(\omega_{out} t)
\]

Here \(\omega_{\text{in}} = \omega_{LO1} + \omega_{LO2}\) and \(\omega_{\text{out}} = \omega_{LO1} - \omega_{LO2} - \omega_{BB}\). After low pass filtering, the signal becomes:

\[
BB_{\text{in-phase}}(t) = -\frac{K_w A_0 B_1}{2} \sin(\omega_{BB} t)
\]

This equation shows that the image signal is eliminated and only the wanted signal is left if Eq. (1) holds. However, it is not true for the BBquadrature-phase in Fig. 3 even though Eq. (1) holds. The BBquadrature-phase signal can be described as:

\[
BB_{\text{quadrature-phase}}(t) = v_{RF}(t) \left( A_1 B_0 \cos(\omega_{LO1} t) \cos(\omega_{LO2} t) - A_0 B_1 \sin(\omega_{LO1} t) \sin(\omega_{LO2} t) \right)
\]

\[
= v_{RF}(t) A_1 B_0 \cos(\omega_{LO1} t) \cos(\omega_{LO2} t) - v_{RF}(t) A_0 B_1 \sin(\omega_{LO1} t) \sin(\omega_{LO2} t)
\]

\[
= v_{RF}(t) A_1 B_0 \cos(\omega_{LO1} t + \omega_{LO2}) + A_0 B_1 \cos(\omega_{in} t) \sin(\omega_{out} t)
\]

\[
= v_{RF}(t) A_1 B_0 \cos(\omega_{LO1} t + \omega_{LO2}) + v_{RF}(t) A_0 B_1 \cos(\omega_{in} t) \sin(\omega_{out} t)
\]

\[
= [K_w \cos(\omega_{in} t) + K_i \cos(\omega_{out} t)] + [A_1 B_0 \cos(\omega_{LO1} t + \omega_{LO2})] + [A_0 B_1 \cos(\omega_{in} t) \sin(\omega_{out} t)]
\]

\[
= [A_1 B_0 \cos(\omega_{LO1} t + \omega_{LO2})] + [A_0 B_1 \cos(\omega_{in} t) \sin(\omega_{out} t)]
\]
Fig. 5. IR ratio vs. R variation. (a) BB\text{in-phase}. (b) BB\text{quadrature-phase}. IR ratio of BB\text{quadrature-phase} in a conventional downconverter is very sensitive to the absolute accuracy error of R.

B. Image Rejection in the Proposed Double Conversion Downconverter

The proposed downconverter is shown in Fig. 4. By introducing two additional phase shifters in the IF signal paths, we can change the connections of B_{\text{cos}w_{LO}} and B_{\text{sin}w_{LO}} in BB\text{quadrature-phase} signal path. Therefore, both equations of BB\text{in-phase} and BB\text{quadrature-phase} are well reduced and no image term appears if Eq. (1) holds.

Consequently, the IR ratio of the proposed downconverter is insensitive to the absolute inaccuracy of RC product in a phase shifter and only depends on the relative matching. Because the relative matching property of on-chip passive components is usually satisfactory [4], [5], the IR performance is robust against the process and temperature variations. However, there is some attenuation because phase shifters are inserted in the signal paths.

Similarly, after low pass filtering, the BB\text{quadrature-phase} signal becomes:

\[ BB_{\text{quad-phase}}(f) = \frac{K_y A_t B_t}{2} \cos \omega_{\text{IF}} f + \frac{K_y (A_t B_t - A_0 B_0)}{4} \cos \omega_{\text{IF}} f \]

The second term in this equation is the image. Consequently, in a conventional double conversion downconverter, either in-phase or quadrature-phase signal is seriously affected by the absolute inaccuracy of passive components caused by process and temperature variations.

Simulation and Experimental Results

The conventional double conversion downconverter in Fig. 3 and the proposed one in Fig. 4 were compared through simulations with SpectreRF. Fig. 5 shows the simulation results of IR ratio vs. R variation, while maintaining the ratio of R_{1} to R_{2} in Fig. 2. From Fig. 5 (b), the IR ratio of a conventional downconverter is below 40 dB when R deviates by more than ±10 % from the designed value (R=1), even though the relative accuracy error is zero. The proposed downconverter, on the other hand, maintains IR ratio above 50 dB though the R deviates up to ±50 %.

The proposed image rejection downconverter was implemented using 0.65 µm CMOS technology. The microphotograph of the IR downconverter is shown in Fig. 6. The active area of the IR downconverter is 3.3 × 1.9 mm². The prototype downconverter was assembled with the testboard using a chip-on-board (COB) packaging technology. Fig. 7 shows the COB test setup. This was done to reduce the effects of parasitic lead inductance of package.

The following measurements have been performed on the realized chip at supply voltage of 3.3 V. The RF signal frequency and power were 2 GHz and -20 dBm, respectively. 1.8 GHz LO, and 204 MHz LO, signals were applied by the external sources and their power levels were 0 dBm. Fig. 8 shows the downconverter output spectrum. In order to distinguish the image from the wanted in the output spectrum, the image was applied at the frequency of 1.602 GHz, though the real image frequency is 1.6 GHz.
Fig. 8. Measured baseband output spectrum. IR ratio of 40.8 dB was obtained.

Fig. 9. Measured IR ratio as a function of RF frequency.

The measured power level of baseband signal was –16 dBm at 4 MHz. The downconverted image appeared at the frequency of 6 MHz. The measured IR ratio was 40.8 dB without any off-chip filtering or tuning. The overall IR ratio required in a receiver is about 60 dB in general. However, IR of 40 dB is sufficient for the downconverter core because the off-chip RF filter prior to the LNA offers IR of 20 dB.

Fig. 9 shows the IR ratio as a function of RF frequency. The measured IR ratio almost maintained above 37 dB as the RF frequency varied in the range of 100 MHz. Channel selection is performed by the LO. Because the frequency of LO is very high, the LO phase shifter is less sensitive to the same amount of frequency variation. In order to reduce the effect of frequency and RC variations more, we used 2nd order polyphase filters [6] rather than 1st order RC-CR phase shifters. The output buffer was designed to drive a 50 Ω load and the total power consumption of the downconverter was 91 mW. The measurement results of the proposed downconverter are summarized in TABLE I.

**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF frequency</td>
<td>2 GHz</td>
</tr>
<tr>
<td>LO1 frequency</td>
<td>1.8 GHz</td>
</tr>
<tr>
<td>IF frequency</td>
<td>200 MHz</td>
</tr>
<tr>
<td>LO2 frequency</td>
<td>204 MHz</td>
</tr>
<tr>
<td>Baseband frequency</td>
<td>4 MHz</td>
</tr>
<tr>
<td>Silicon Technology</td>
<td>0.65 μm CMOS</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>27.7 mW @ 3.3 V</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>4 dB @ 0 dBm LO1, LO2</td>
</tr>
<tr>
<td>IR Ratio</td>
<td>40.8 dB</td>
</tr>
</tbody>
</table>

**Conclusion**

A double conversion downconverter with robust IR performance has been described in this paper. The proposed downconverter maintains high IR ratio against the process and temperature variations if the on-chip passive RC components are relatively matched.

The prototype circuit was implemented using 0.65 μm CMOS technology and it dissipates 91 mW at 3.3 V. The measured IR ratio was 40.8 dB.

**References**


